Memories Data Book

1986–87 Edition

Fujitsu Limited

Fujitsu Microelectronics, Inc.

Fujitsu Mikroelektronik GmbH

Worldwide Suppliers of Communications and Electronics Equipment

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Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications. Consequently, complete information sufficient for construction purposes is not necessarily given.

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Fujitsu Limited

Fujitsu Limited, headquartered near Tokyo, Japan, is Japan's largest supplier of computers and ranks in the top ten companies operating in Japan. Fujitsu is also one of the world's largest suppliers of telecommunications equipment and semiconductor devices.

Established in 1935 as the Communications Division spinoff of Fuji Electric Company Limited, Fujitsu Limited, in 1985, celebrated 50 years of service to the world through the development and manufacture of state-of-the-art products in data processing, telecommunications and semiconductors. Fujitsu operates subsidiaries worldwide in two dozen countries and employs over 70,000 people to generate annual sales in excess of six billion US dollars. (As of March 31, 1985 consolidated base.)

Fujitsu has five plants in key industrial regions in Japan covering all steps of semiconductor production. Five wholly owned Japanese subsidiaries provide additional capacity for production of advanced semiconductor devices. Two additional facilities operate in the U.S. and Europe to help meet the growing worldwide demand for Fujitsu semiconductor products. In all, Fujitsu operations occupy over 1.6 million square meters of manufacturing space worldwide.

Semiconductor Products

In 1985 Fujitsu introduced 1M-bit DRAMs as well as a 256K-bit SRAM, 1M-bit EPROMs and a 1M-bit ROM. A 1M-bit SRAM will be introduced in 1986 or 1987 to further compliment the already available full range of dynamic and static memories in low-power CMOS as well as high-speed NMOS and ECL versions.

Fujitsu offers a full line of 4-bit, 8-bit and 16-bit microprocessors and peripherials to provide designers with a total of 150 products including 90 products in CMOS families, 50 products in NMOS families and 10 products in bipolar peripherals.

Fujitsu's Digital Signal Processor provides designers of telecommunications and speech recognition equipment with the world's fastest digital signal processor. It is also one of the world's largest integrated circuit designed using "standard cell" technology.

Other Fujitsu industry standard products include GaAs FETs, GaAs FET amplifiers, Si MW transistors and light wave semiconductors. Discrete products include a high speed switching power transistor and a Darlington transistor.

Fujitsu's custom product lines include application-specific gate arrays and standard-cell arrays using high-speed Bipolar and ECL technologies and advanced CMOS technologies. Gate arrays ranging in size from 350 to 20,000 gates are available, many with on-chip memory. Standard-cell arrays are available up to 8000 gate equivalents and also include on-chip memory and PLA.

Virtually every major type of electronics equipment on the globe utilizes Fujitsu technology in integrated circuits. Fujitsu's leadership position in worldwide integrated circuit development and manufacturing assures equipment manufacturers that they will always be able to design with the latest in technology utilizing the highest standards of quality and reliability.

Fujitsu Microelectronics, Inc.

Established in 1979, Fujitsu Microelectronics, Inc., headquartered in Santa Clara, California, markets Fujitsu semiconductors through representatives located throughout the U.S. and North America.

The Component Division, Fujitsu Component of America, Inc., markets bubble memories, keyboards, plasma displays, relay switches, hybrid ICs and the newly introduced "IC Card" which incorporates a microprocessor into a credit card.

FMI's San Diego manufacturing facility provides capacity for manufacturing of many high-technology devices for the U.S. and North American market.

Customer support for custom designs is available through Fujtsu's design centers in Santa Clara, Dallas and Boston. Technology Centers offering on-site customer training, CAE design facilities and design assistance are planned for 1986.

Fujitsu Mikroelektronik GmbH (European Sales Center)

Fujitsu Mikroelektronick GmbH (FMG) was established in June, 1980, in Frankfurt, West Germany, and is a totally owned subsidiary of Fujitsu Limited, Tokyo. FMG is the sole representative of the Fujitsu Electronic Device Group in Western Europe. The wide range of IC products, LSI memories and, in particular, gate arrays are noted throughout Western Europe for design excellence and unmatched reliability. Five branch offices to support Fujitsu's semiconductor operations are located in Munich, London, Paris, Stockholm, and Milan.

Fujitsu Microelectronics Ireland, Ltd (European Production Center)

Fujitsu Microelectronics Ireland, Ltd. (FME) was established in 1980 in the suburbs of Dublin as Fujitsu's European Production Center for integrated circuits. FME supplies 64K/256K DRAMs, 64K CMOS/NMOS EPROMs, 256K EPROMs, and other LSI memory products.

Fujitsu Microelectronics, Ltd (European Design Center)

Fujitsu Microelectronics, Ltd., Fujitsu's European VLSI Design Center, opened in October of 1983 in Manchester, England. The Design Center is equipped with a highly-sophisticated CAD system to ensure fast and reliable processing of input data. An experienced staff of engineers is available to assist in all phases of the design process.

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NMOS Dynamic RAMs

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MB81256 1-12
MB81257 1-30
MB81256-W 1-50
MB81257-W 1-66
MB81416 1-84
MB81461 1-102
MB81464 1-129
MB811000 1-148
MB811001 1-161
MB8264A 1-176
MB8264A-W 1-192
MB8265A 1-199
MB8266A 1-219
MB85101A 1-239
MB85103A 1-241
MB85108A 1-243
MB85201 1-245
MB85203 1-263
MB85204 1-282
MB85208 1-299
MB85210 1-318
MB85211 1-337
MB85213 1-354
MB85214 1-367
MB85227 1-379

FUJITSU
MICROELECTRONICS

MB8118-10
MB8118-12

NMOS 16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

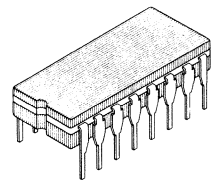
DESCRIPTION

The Fujitsu MB8118 is a fully decoded dynamic NMOS random access memory organized as 16,384 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory peripheral storage and environments where low power dissipation and compact layout are required.

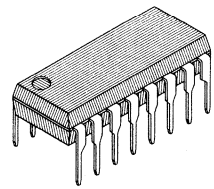
Multiplexed row and column address inputs permit the MB8118 to be housed in a standard 16-pin DIP. Pin outs conform to the JEDEC approved pin out.

The MB8118 is fabricated using silicon-gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs are TTL compatible; the output is three-state TTL.



CERAMIC PACKAGE
DIP-16C-C03

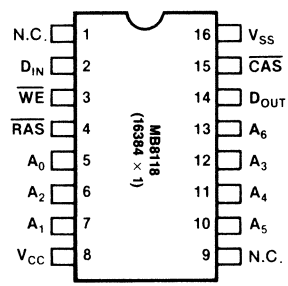


PLASTIC PACKAGE
DIP-16P-M01

FEATURES

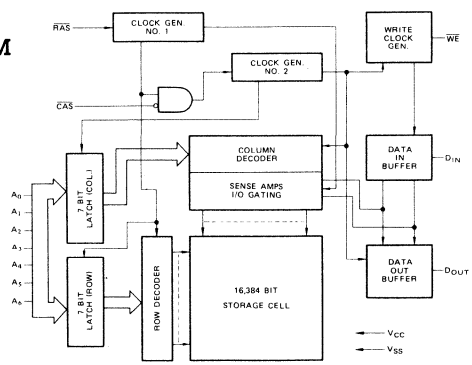
- **16,384 × 1 RAM, 16 pin package**
- **Silicon-gate, Double Poly NMOS, single transistor cell**
- **Address access time:**
  - **100 ns max (MB8118-10)**
  - **120 ns max (MB8118-12)**
- **Cycle time:**
  - **235 ns min (MB8118-10)**
  - **270 ns min (MB8118-12)**
- **Low power:**
  - **182mW max (MB8118-10)**
  - **160mW max (MB8118-12)**
  - **16.5mW max (Standby)**
- **+5V single power supply, ±10% tolerance**
- **On chip substrate bias generator**
- **All inputs TTL compatible, low capacitive load**
- **Three-state TTL compatible output**
- **Hidden refresh capability**
- **Common I/O capability using "Early Write" operation**
- **Output unlatched at cycle end allows extended page boundary and two-dimensional chip select**
- **Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability**
- **On-chip latches for Addresses and Data-in**
- **Pin compatible with Intel 2118 and MCM4517**

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB8118 BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} pin relative to V_{SS}		V_{CC}	−1 to +7	V
Storage temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	
Power dissipation		P_D	1.0	W
Short circuit output current		—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Value			Unit	Operating Temperature
		Min	Typ	Max		
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance $A_0 \sim A_6$, D_{IN}	C_{IN1}	—	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}	—	—	8	pF
Output Capacitance D_{OUT}	C_{OUT}	—	—	7	pF

STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol	MB8118-10		MB8118-12		Unit
			Min	Max	Min	Max	
OPERATING CURRENT Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min)	1	I_{CC1}	—	33	—	29	mA
STANDBY CURRENT Average Power Supply Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, D_{OUT} = High Impedance)		I_{CC2}	—	3.0	—	3.0	mA
REFRESH CURRENT Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = Min)	1	I_{CC3}	—	25	—	22	mA
PAGE MODE CURRENT Average Power Supply Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = Min)	1	I_{CC4}	—	25	—	22	mA
INPUT LEAKAGE CURRENT Input Leakage Current, any input (0V ≤ V_{IN} ≤ 5.5) Input pins not under test = 0V, 4.5V ≤ V_{CC} ≤ 5.5V, V_{SS} = 0V		I_{IL}	−10	10	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{OL}	−10	10	−10	10	μA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}	—	0.4	—	0.4	V
OUTPUT LEVEL Output High Voltage (I_{OH} = −5 mA)		V_{OH}	2.4	—	2.4	—	V

Note: 1 I_{CC} is dependent on output loading. Specified values are obtained with the output open.

DYNAMIC CHARACTERISTICS NOTES 1,2,3

(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol	MB8118-10 Min	MB8118-10 Typ	MB8118-10 Max	MB8118-12 Min	MB8118-12 Typ	MB8118-12 Max	Unit
Time Between Refresh		t_{REF}	—	—	2	—	—	2	ms
Random Read/Write Cycle Time		t_{RC}	235	—	—	270	—	—	ns
Read-Write Cycle Time		t_{RWC}	285	—	—	320	—	—	ns
Page Mode Cycle Time		t_{PC}	125	—	—	145	—	—	ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}	—	—	100	—	—	120	ns
Access Time from $\overline{CAS}$	5 6	t_{CAC}	—	—	55	—	—	65	ns
Output Buffer Turn Off Delay		t_{OFF}	0	—	45	0	—	50	ns
Transition Time		t_T	3	—	50	3	—	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	110	—	—	120	—	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	115	—	10000	140	—	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	70	—	—	85	—	—	ns
$\overline{CAS}$ Prechange Time (all cycles except page mode)		t_{CPN}	50	—	—	55	—	—	ns
$\overline{CAS}$ Precharge Time (Page mode only)		t_{CP}	60	—	—	70	—	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	55	—	10000	65	—	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	100	—	—	120	—	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7 8	t_{RCD}	25	—	45	25	—	55	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	—	0	—	—	ns
Row Address Set Up Time		t_{ASR}	0	—	—	0	—	—	ns
Row Address Hold Time		t_{RAH}	15	—	—	15	—	—	ns
Column Address Set Up Time		t_{ASC}	0	—	—	0	—	—	ns
Column Address Hold Time		t_{CAH}	15	—	—	15	—	—	ns
Column Address Hold Time Referenced to $\overline{RAS}$		t_{AR}	60	—	—	70	—	—	ns
Read Command Set Up Time		t_{RCS}	0	—	—	0	—	—	ns
Read Command Hold Time		t_{RCH}	0	—	—	0	—	—	ns
Write Command Set Up Time	9	t_{WCS}	0	—	—	0	—	—	ns
Write Command Hold Time		t_{WCH}	30	—	—	35	—	—	ns
Write Command Hold Time Referenced to $\overline{RAS}$		t_{WCR}	75	—	—	90	—	—	ns
Write Command Pulse Width		t_{WP}	30	—	—	35	—	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	60	—	—	65	—	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	45	—	—	50	—	—	ns
Data In Set Up Time		t_{DS}	0	—	—	0	—	—	ns
Data In Hold Time		t_{DH}	30	—	—	35	—	—	ns
Data In Hold Time Referenced to $\overline{RAS}$		t_{DHR}	75	—	—	90	—	—	ns
$\overline{CAS}$ to $\overline{WE}$ Delay	9	t_{CWD}	55	—	—	65	—	—	ns
$\overline{RAS}$ to $\overline{WE}$ Delay	9	t_{RWD}	120	—	—	120	—	—	ns
Read Command Hold Time Referenced to $\overline{RAS}$		t_{RRH}	20	—	—	25	—	—	ns

Notes:

1 An initial pause of 200μs is required. Then several cycles are required after power up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.

2 Dynamic measurements assume t_T=5ns.

3 V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

4 Assumes that $t_{RCD}<t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

5 Assumes that $t_{RCD}>t_{RCD}$ (max).

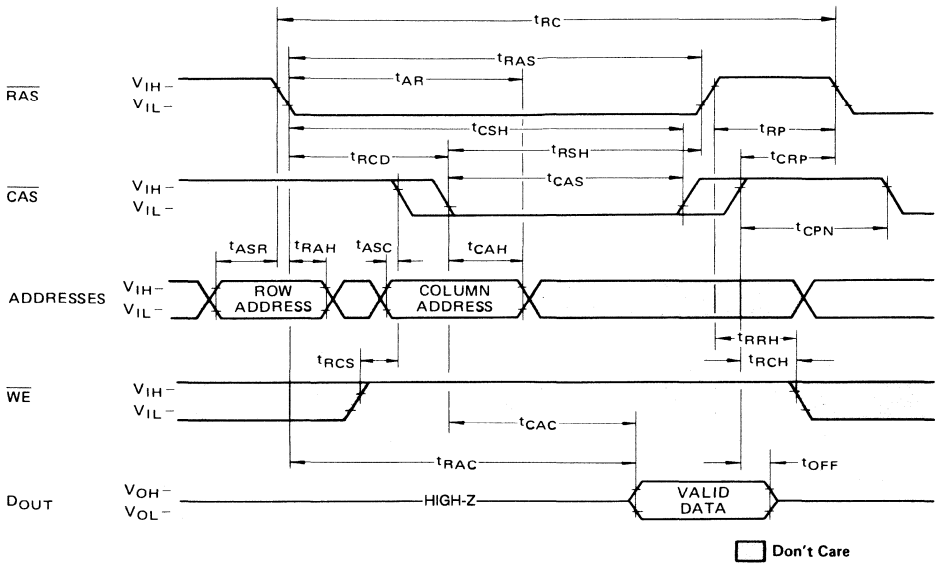
6 Measured with a load equivalent to 2 TTL loads and 100pF.

7 Operation within the t_{RCD} (max) limit insures that t_{RCD} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

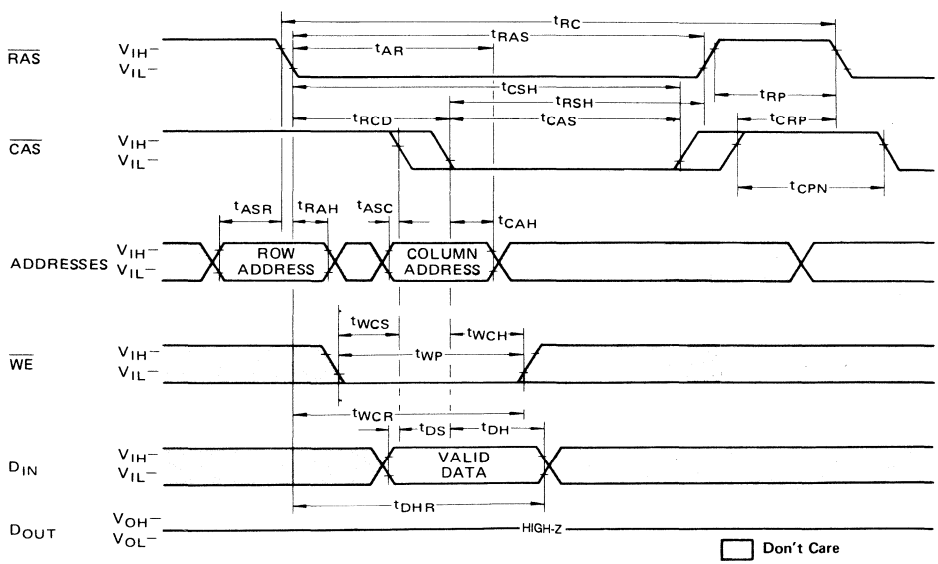
8 $t_{RCD}(min)=t_{RAH}(min)+2t_T(t_T=5ns)+t_{ASC}(min)$.

9 t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS}>t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle. If $t_{CWD}>t_{CWD}$ (min) and $t_{RWD}>t_{RWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.

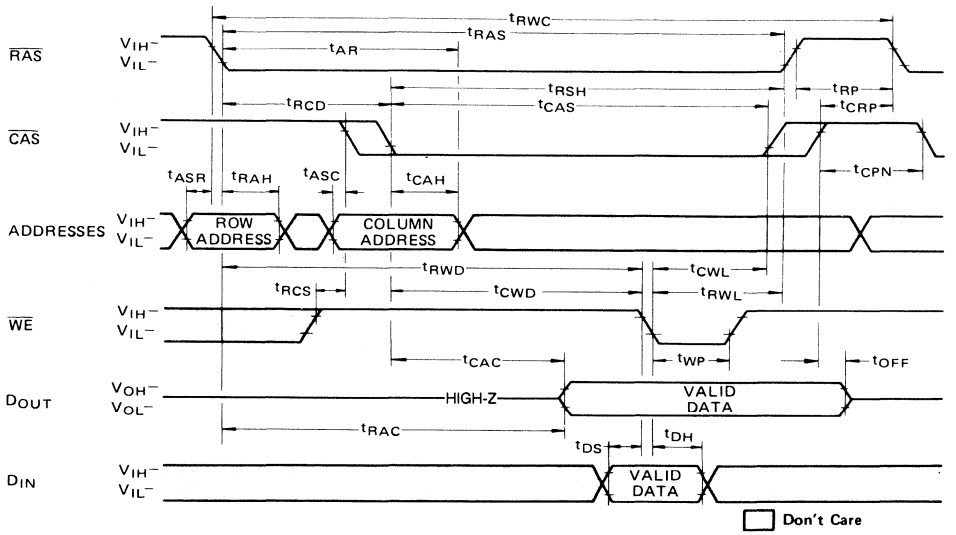
READ CYCLE TIMING DIAGRAM



WRITE CYCLE (EARLY WRITE)

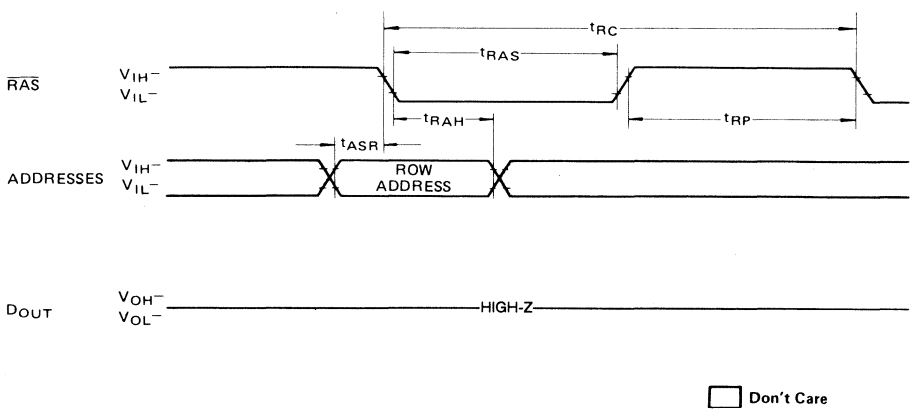


READ-WRITE/READ-MODIFY-WRITE CYCLE

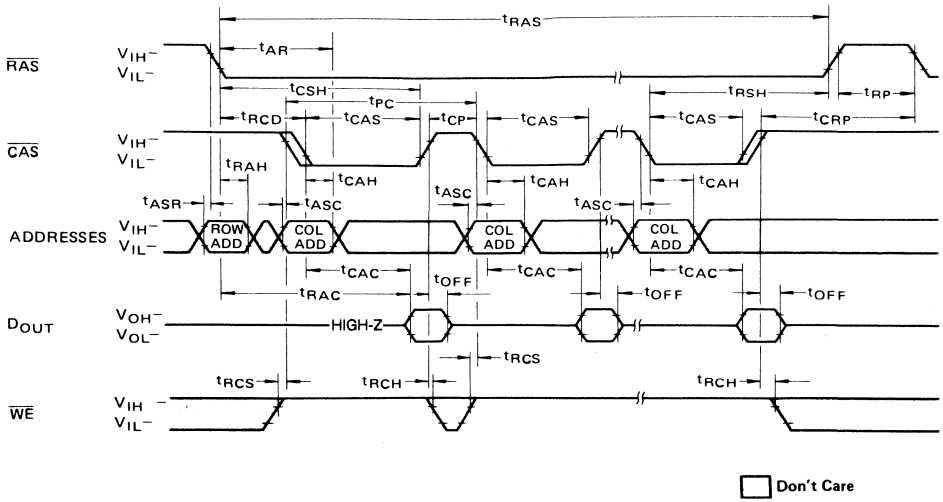


"RAS-ONLY" REFRESH CYCLE

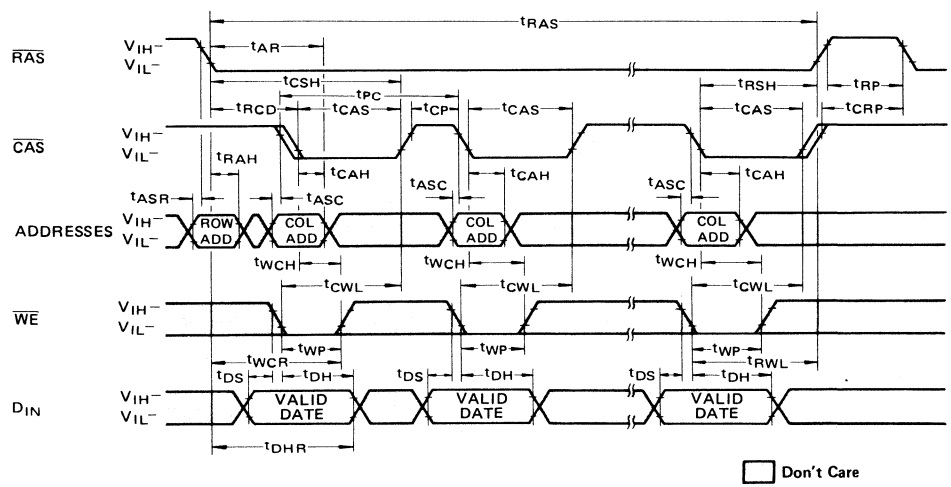
NOTE: $\overline{CAS}$ = V_{IH}, $\overline{WE}$ = Don't care



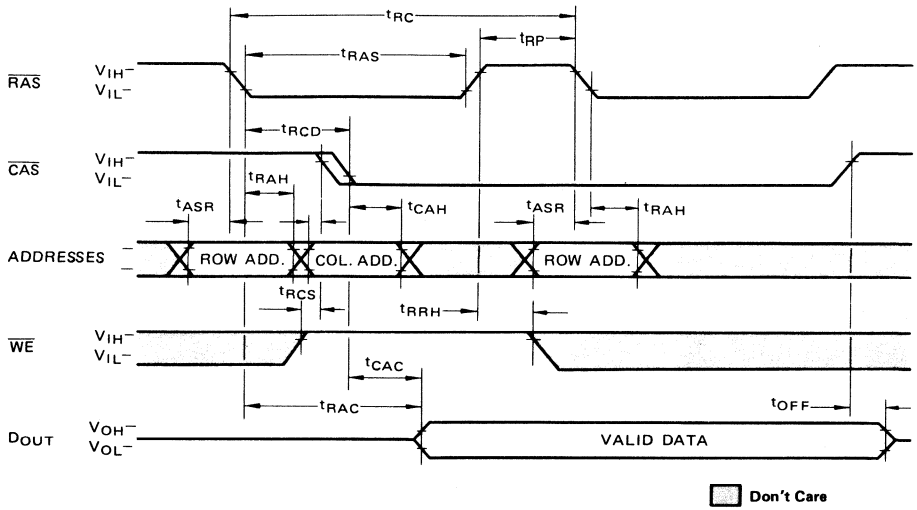
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



HIDDEN $\overline{RAS}$-ONLY REFRESH CYCLE TIMING DIAGRAM



DESCRIPTION

Address Inputs

A total of fourteen binary input address bits are required to decode any one of 16,384 storage cell locations within the MB8118. Seven row-address bits are established on the input pins (A_0 through A_6) and latched with the Row Address Strobe ($\overline{RAS}$). Seven column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read mode or write mode is selected with the $\overline{WE}$ input. A logic "high" on $\overline{WE}$ dictates read mode; logic "low" dictates write mode. Data input is disabled when read mode is selected. $\overline{WE}$ can be driven by standard TTL circuits without a pull-up resistor.

Data Input:

Data is written into the MB8118 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page-Mode

Page-mode operation permits latching the row-address into the MB8118 and maintaining $\overline{RAS}$ at a logic "low" throughout all successive memory operations in which the row-address doesn't change. This saves the power required by a $\overline{RAS}$ cycle. Access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$-Only Refresh

Refresh of the dynamic memory is accomplished by performing a memory cycle at each of the 128 row-addresses at least every two milliseconds. $\overline{RAS}$-only refresh prevents any output during refresh because the output buffer is in the high impedance state since $\overline{CAS}$ is at V_{IH}. Strobing each of the 128 row-addresses with $\overline{RAS}$ will cause all bits in the memory to be refreshed. $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

Hidden Refresh

$\overline{RAS}$-ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} from a previous memory read cycle. (See Figure 1 below)

FIG. 1–HIDDEN REFRESH

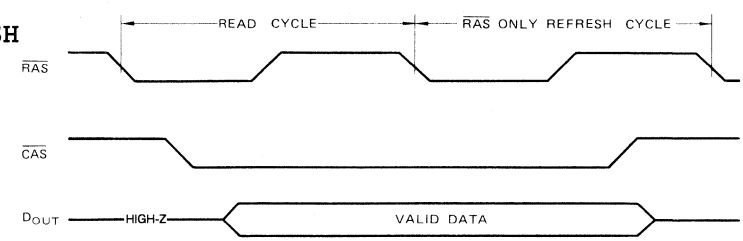
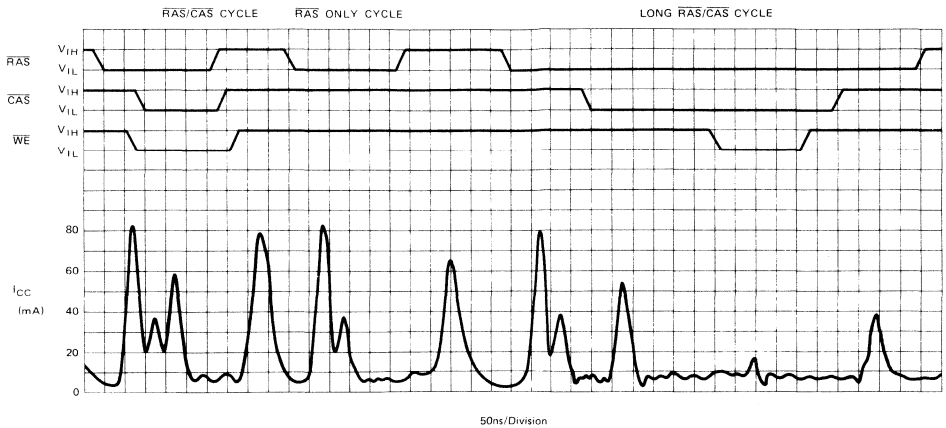
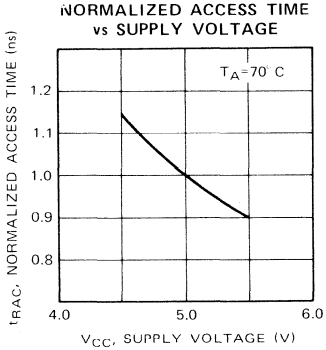


FIG. 2 — CURRENT WAVEFORMS (V_{CC} = 5.0V, T_A = 25°C)

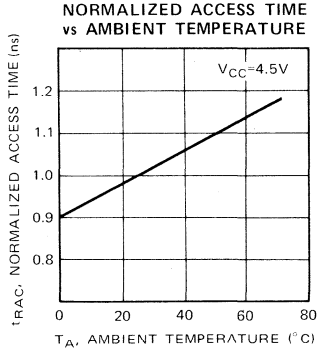


TYPICAL CHARACTERISTICS CURVES

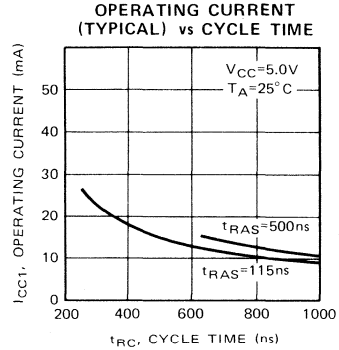
NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE



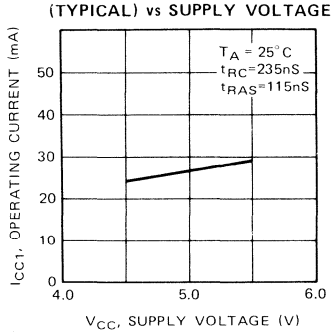
NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE



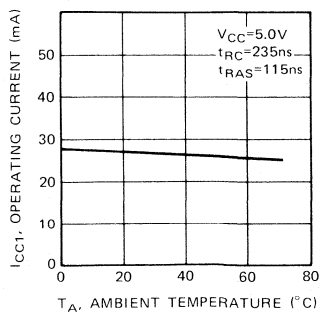
OPERATING CURRENT (TYPICAL) vs CYCLE TIME



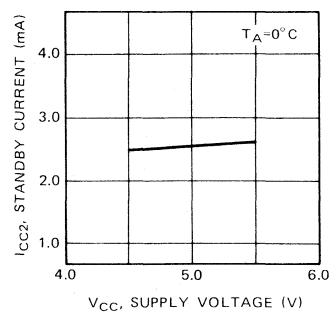
OPERATING CURRENT (TYPICAL) vs SUPPLY VOLTAGE



OPERATING CURRENT (TYPICAL) vs AMBIENT TEMPERATURE

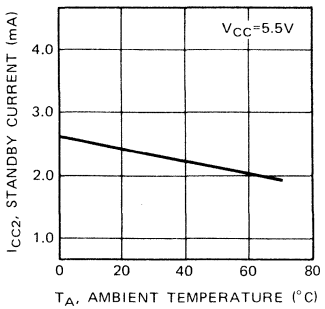


STANDBY CURRENT (TYPICAL) vs SUPPLY VOLTAGE

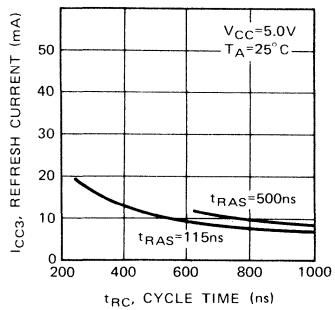


TYPICAL CHARACTERISTICS CURVES (continued)

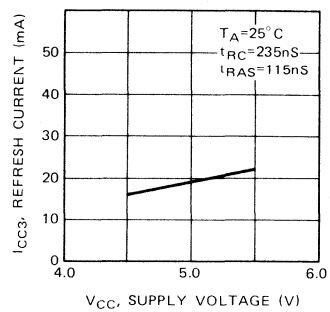
STANDBY CURRENT (TYPICAL) vs AMBIENT TEMPERATURE



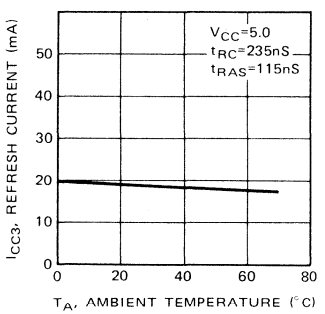
REFRESH CURRENT (TYPICAL) vs CYCLE TIME



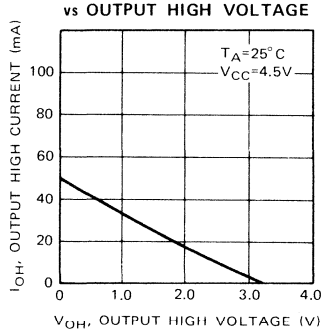
REFRESH CURRENT (TYPICAL) vs SUPPLY VOLTAGE



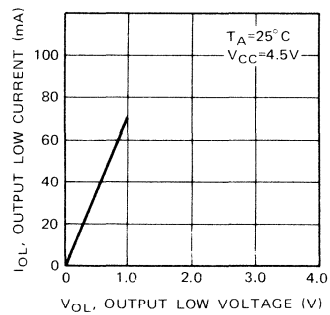
REFRESH CURRENT (TYPICAL) vs AMBIENT TEMPERATURE



OUTPUT HIGH CURRENT vs OUTPUT HIGH VOLTAGE

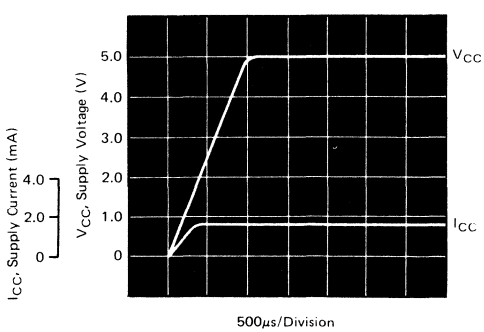


OUTPUT LOW CURRENT vs OUTPUT LOW VOLTAGE

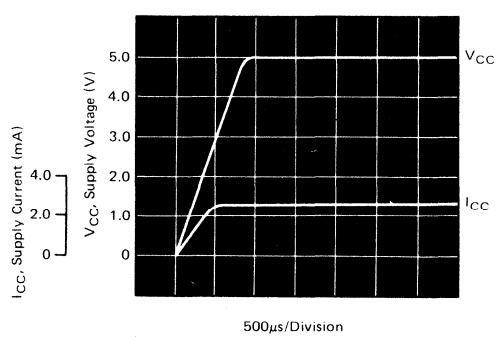


TYPICAL SUPPLY CURRENT vs SUPPLY VOLTAGE DURING POWER UP

1) $\overline{RAS}$=V_{CC}, $\overline{CAS}$=V_{CC}

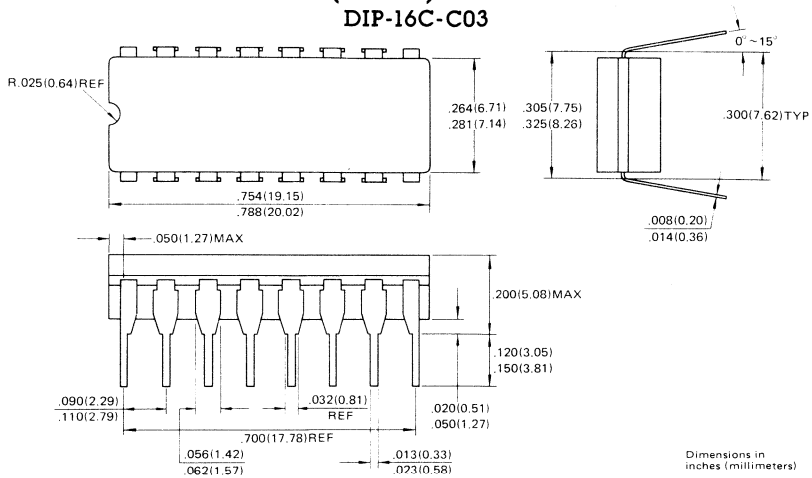


2) $\overline{RAS}$=V_{SS}, $\overline{CAS}$=V_{SS}

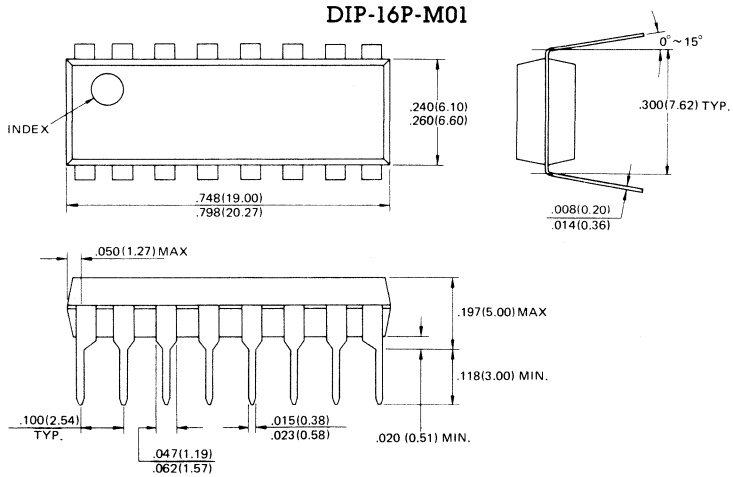


PACKAGE DIMENSIONS Dimensions in inches (millimeters)

16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
DIP-16C-C03



16-LEAD PLASTIC DUAL IN-LINE PACKAGE
DIP-16P-M01



MB81256-10, MB81256-12, MB81256-15

NMOS 262,144-Bit Dynamic Random Access Memory

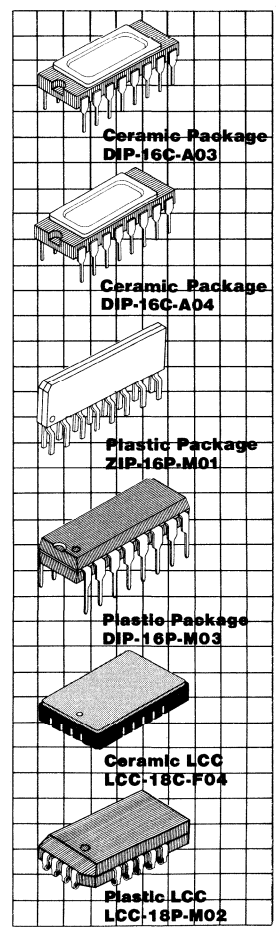
Description

The Fujitsu MB81256 is a fully decoded, dynamic NMOS random access memory organized as 262,144 one-bit words. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

The MB81256 features "page mode" which allows high speed random access of up to 512-bits within the same row. Additionally, the MB81256 offers new functional enhancements that make it more versatile than previous dynamic RAMs. Multiplexed row and column address inputs permit the MB81256 to be housed in a Jedec standard 16-pin dual in-line package and 18-pad LCC.

The MB81256 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-layer Polysilicon process. This process, coupled with single transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is used in the design, including dynamic sense amplifiers.

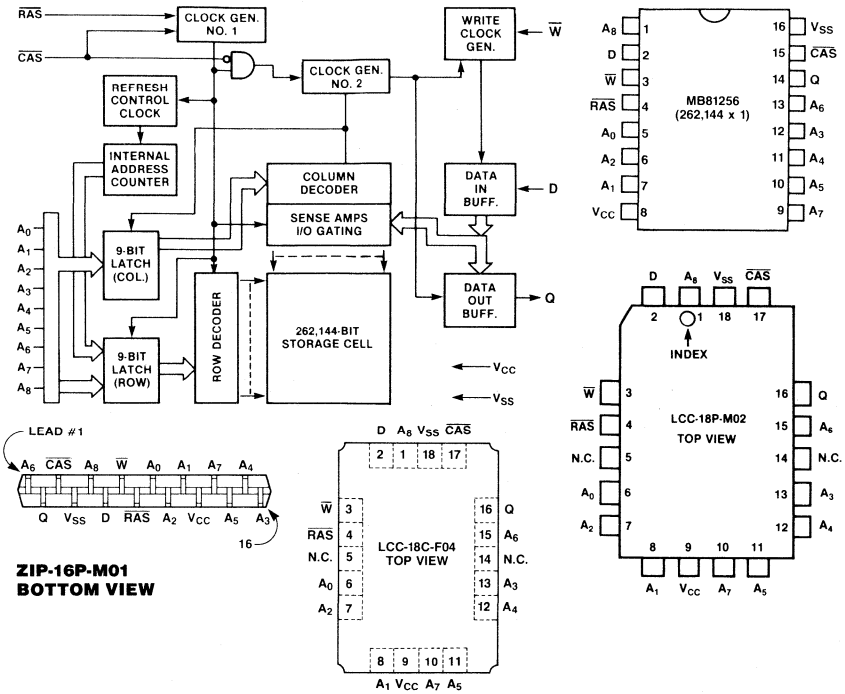
Clock timing requirements are noncritical, and the power supply tolerance is very wide. All inputs are TTL compatible.



Features

- 262,144 x 1-bit organization
- Row Access Time/Cycle Time:
  MB81256-10
  100 ns Max/200 ns Min.
  MB81256-12
  120 ns Max/220 ns Min.
  MB81256-15
  150 ns Max/260 ns Min.
- Low Power Dissipation:
  314 mW max. (t_{RC} = 260 ns)
  25 mW (Standby)
- +5V supply voltage, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- Common I/O capability using "Early Write" operation
- On-chip substrate bias generator
- Page Mode Capability
- Fast Read-Write Cycle, TRWC = TRC
- t_{AR}, t_{WCR}, t_{DHR}, t_{RWD} eliminated
- $\overline{CAS}$-before-$\overline{RAS}$ on chip refresn
- Hidden $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh
- $\overline{RAS}$-only refresh
- 4 ms/256 cycle refresh
- Output unlatched at cycle end allows two dimensional chip select
- On-chip Address and Data-in latches
- Industry standard 16-pin package

MB81256 Block Diagram and Pin Assignments



NOTE: The following IEEE Std. 662-1980 symbols are used in this data sheet: D = Data In, $\overline{W}$ = Write Enable, Q = Data Out.

Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Voltage on Any Pin relative to V_{SS}		V_{IN}, V_{OUT}, V_{CC}	−1.0 to 7.0	V
Operating Temperature (ambient)		T_{OP}	0 to 70	°C
Storage Temperature	Ceramic Plastic	T_{STG}	−55 to +150 −55 to +125	°C
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		I_{OS}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Value Min	Value Typ	Value Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C (ambient)
	V_{SS}	0	0	0	V	
Input High Voltage All Inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage All Inputs	V_{IL}	−2.0		0.8	V	

Capacitance
($T_A = 25\,°C$)

Parameter	Symbol	Value Min	Value Typ	Value Max	Unit
Input Capacitance A_0 to A_8, D	C_{IN1}			7	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$	C_{IN2}			10	pF
Output Capacitance Q	C_{OUT}			7	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81256-10 Min	MB81256-10 Max	MB81256-12 Min	MB81256-12 Max	MB81256-15 Min	MB81256-15 Max	Unit
OPERATING CURRENT *1 Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min.)	I_{CC1}		70		65		57	mA
STANDBY CURRENT Power Supply Current ($\overline{RAS}/\overline{CAS} = V_{IH}$)	I_{CC2}		4.5		4.5		4.5	mA
REFRESH CURRENT 1*1 Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$; t_{RC} = Min.)	I_{CC3}		60		55		50	mA
PAGE MODE CURRENT*1 Average Power Supply Current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; t_{PC} = Min.)	I_{CC4}		35		30		25	mA
REFRESH CURRENT 2*1 Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = Min.)	I_{CC5}		65		60		55	mA
INPUT LEAKAGE CURRENT Any Input, (V_{IN} = 0V to 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)	I_{IL}	−10	10	−10	10	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data is disabled, V_{OUT} = 0V to 5.5V)	I_{OL}	−10	10	−10	10	−10	10	μA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}		0.4		0.4		0.4	V
OUTPUT LEVEL Output High Voltage (I_{OH} = −5.0 mA)	V_{OH}	2.4		2.4		2.4		V

Note: *1 I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC Characteristics[*1,2,3]
(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol Alternate	Symbol *Standard	MB81256-10 Min	MB81256-10 Max	MB81256-12 Min	MB81256-12 Max	MB81256-15 Min	MB81256-15 Max	Unit
Time between Refresh		t_{REF}	TRVRV		4		4		4	ms
Random Read/Write Cycle Time		t_{RC}	TRELREL	200		220		260		ns
Read-Write Cycle Time		t_{RWC}	TRELREL	200		220		260		ns
Access Time from $\overline{RAS}$[*4,6]		t_{RAC}	TRELQV		100		120		150	ns
Access Time from $\overline{CAS}$[*5,6]		t_{CAC}	TCELQV		50		60		75	ns
Output Buffer Turn off Delay		t_{OFF}	TCEHQZ	0	25	0	25	0	30	ns
Transition Time		t_T	TT	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	TREHREL	85		90		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	TRELREH	105	100000	120	100000	150	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	TCELREH	55		60		75		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	TCELCEH	55	100000	60	100000	75	100000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	TRELCEH	105		120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time[*4,7]		t_{RCD}	TRELCEL	20	50	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	TCEXREL	10		10		10		ns
Row Address Set Up Time		t_{ASR}	TAVREL	0		0		0		ns
Row Address Hold Time		t_{RAH}	TRELAX	10		12		15		ns
Column Address Set Up Time		t_{ASC}	TAVCEL	0		0		0		ns
Column Address Hold Time		t_{CAH}	TCELAX	15		20		25		ns
Read Command Set Up Time		t_{RCS}	TWHCEL	0		0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$[*10]		t_{RCH}	TCEHWX	0		0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$[*10]		t_{RRH}	TREHWX	20		20		20		ns
Write Command Set Up Time[*8]		t_{WCS}	TWLCEL	0		0		0		ns
Write Command Pulse Width		t_{WP}	TWLWH	15		20		25		ns
Write Command Hold Time		t_{WCH}	TCELWH	15		20		25		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	TWLREH	35		40		45		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	TWLCEH	35		40		45		ns
Data In Set Up Time		t_{DS}	TDVCEL	0		0		0		ns
Data In Hold Time		t_{DH}	TCELDX	15		20		25		ns
$\overline{CAS}$ to $\overline{W}$ Delay[*8]		t_{CWD}	TCELWL	15		20		25		ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$		t_{FCS}	TCELREL	20		20		20		ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$		t_{FCH}	TRELCEX	20		25		30		ns
Page Mode Read/Write Cycle Time		t_{PC}	TCELCEL	100		120		145		ns
Page Mode Read-Write Cycle Time		t_{PRWC}	TCEHCEH	100		120		145		ns
Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	TCEHCEL	40		50		60		ns
Refresh Counter Test $\overline{RAS}$ Pulse Width[*9]		t_{TRAS}	TRELREH	230	10000	265	10000	320	10000	ns
Refresh Counter Test Cycle Time[*9]		t_{RTC}	TRELREL	330		375		430		ns
RAS Precharge to $\overline{CAS}$ Active Time		t_{RPC}	TREHCEL	20		20		20		ns
Refresh Counter Test $\overline{CAS}$ Precharge Time[*9]		t_{CPT}	TCEHCEL	50		60		70		ns
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle		t_{CPR}	TCEHCEL	20		25		30		ns

Notes: *These symbols are described in IEEE STD. 662-1980: IEEE Standard terminology for semiconductor memory.

AC Characteristics
(Continued)

Notes:

*1 An initial pause of 200μs is required after power up, followed by any 8 $\overline{RAS}$ cycles, before device operation is achieved.
If the internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh initialization cycles are required.

*2 AC characteristics assume t_T = 5 ns.

*3 V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

*4 t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$ (Max.) the specified maximum value of t_{RAC} (Max.) can be met. If $t_{RCD} > t_{RCD}$ (Max.) then t_{RAC} is increased by the amount that t_{RCD} exceeds t_{RCD} (Max.).

*5 Assumes that $t_{RCD} > t_{RCD}$ (Max.).

*6 Measured with a load equivalent to 2 TTL loads and 100pF.

*7 t_{RCD} (Min.) = t_{RAH} (Min.) + $2t_T$ + t_{ASC} (Min.).

*8 t_{WCS} and t_{CWD} are nonrestrictive operating parameters, and are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (Min.), the cycle is an early write cycle, and the data out pin will remain open circuit (High Impedance) throughout the entire cycle.

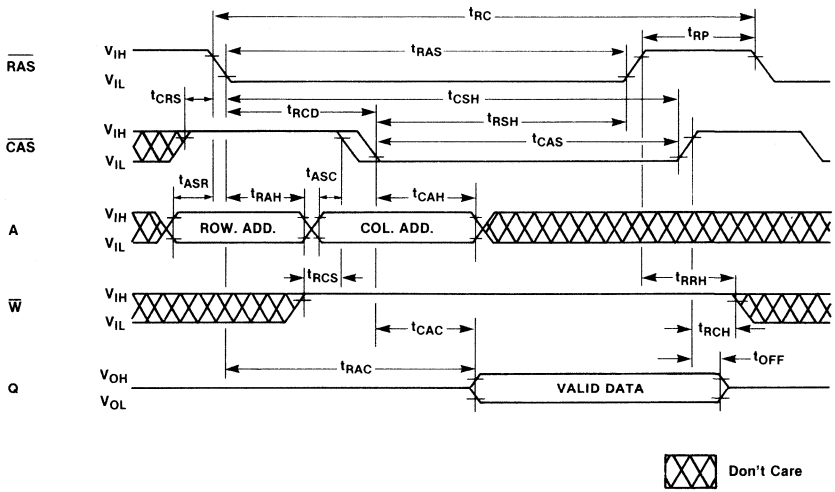
If $t_{CWD} > t_{CWD}$ (Min.), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.

*9 Test mode write cycle only.

*10 Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

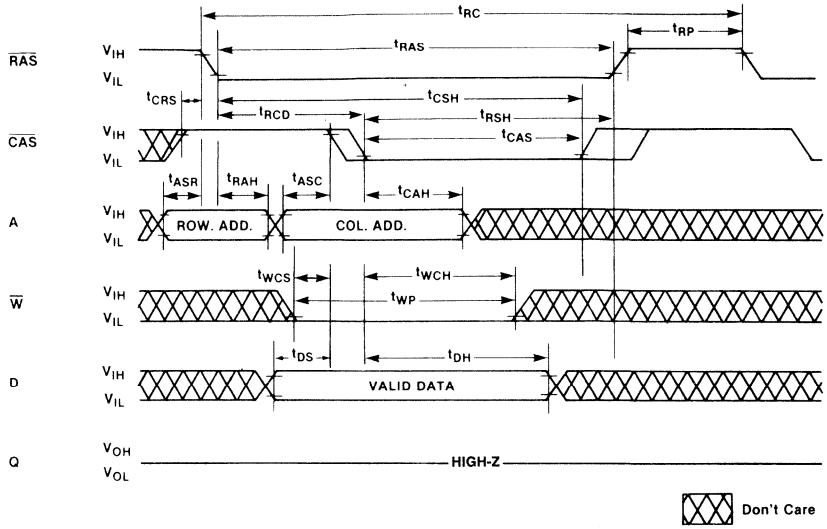
Timing Diagrams

Read Cycle

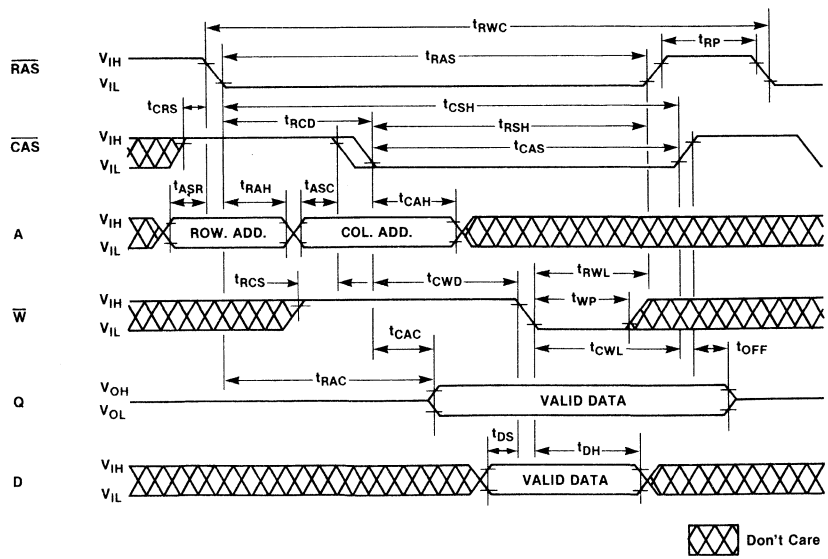


Timing Diagrams
(Continued)

Write Cycle (Early Write)



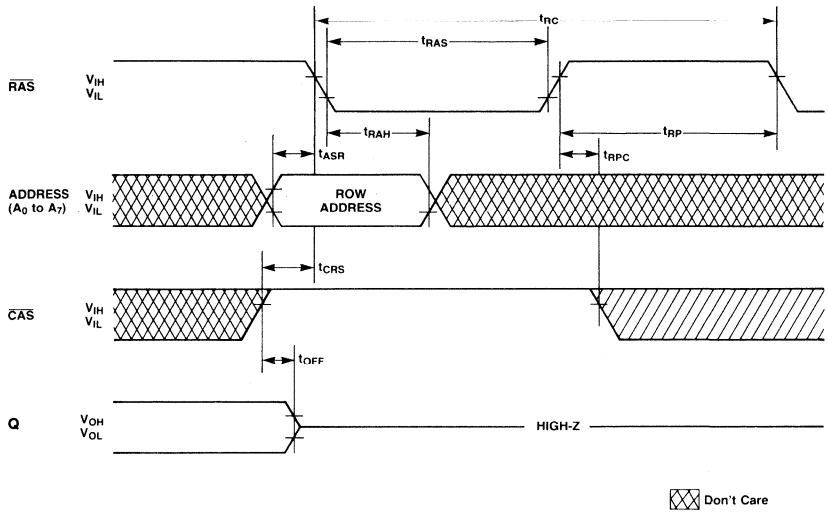
Read-Write/Read-Modify-Write Cycle



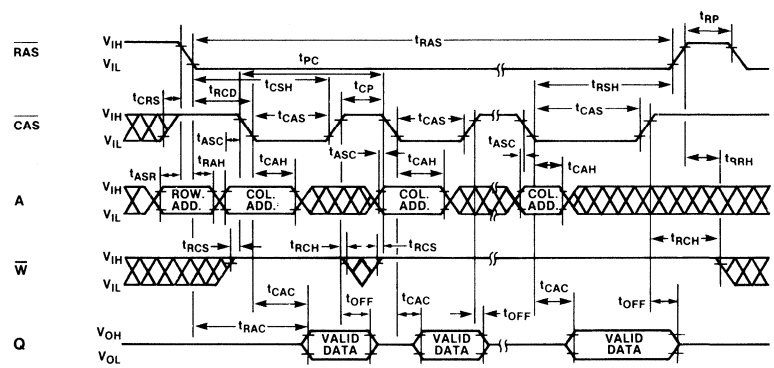
Timing Diagrams
(Continued)

"$\overline{RAS}$-Only" Refresh Cycle

NOTE: W, D = Don't Care, A_8, V_{IH} or V_{IL}

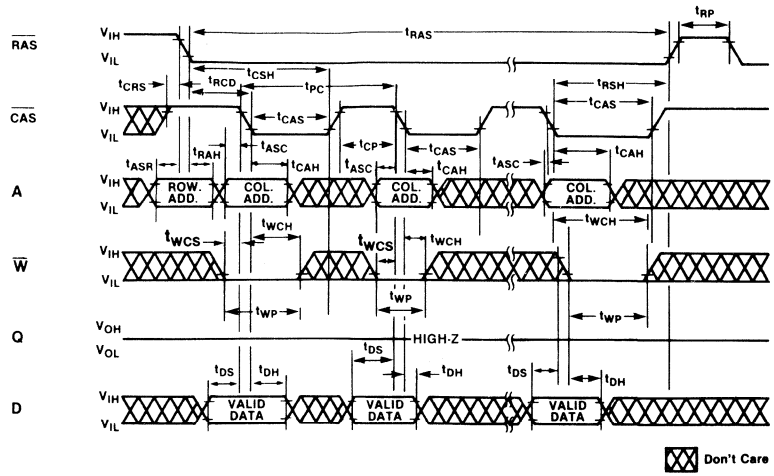


Page Mode Read Cycle

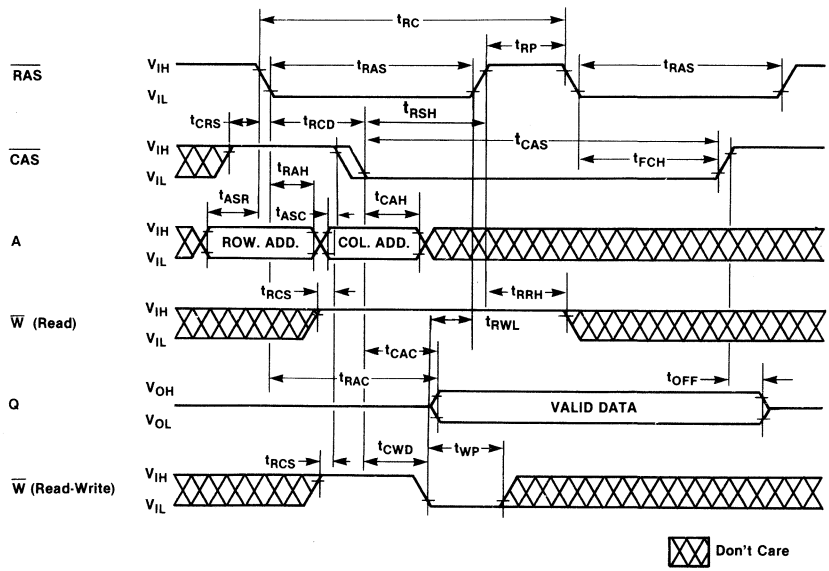


Timing Diagrams
(Continued)

Page Mode Write Cycle

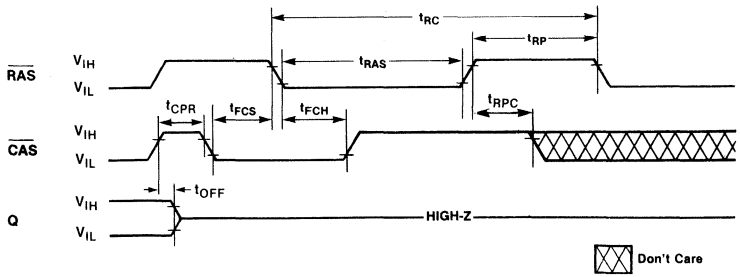


Hidden Refresh Cycle

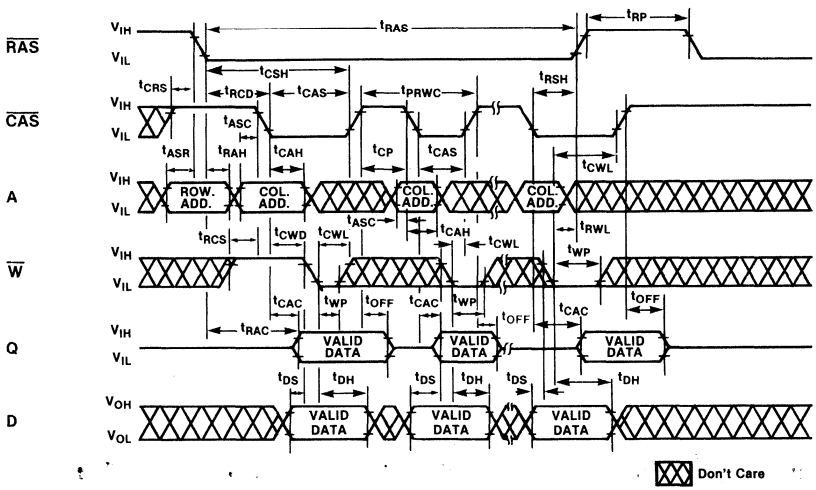


Timing Diagrams
(Continued)

"$\overline{CAS}$-Before-$\overline{RAS}$" Refresh Cycle
NOTE: A, $\overline{W}$, D = Don't Care

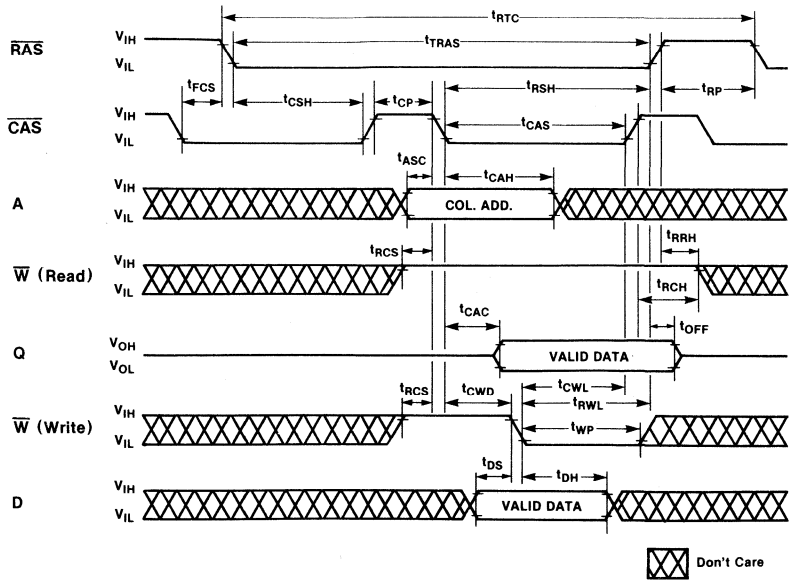


Page Mode Read-Write Cycle



Timing Diagrams
(Continued)

"$\overline{CAS}$-Before-$\overline{RAS}$" Refresh Counter Test Cycle



Description

Simplified Timing Requirement
The MB81256 has improved circuitry that eases timing requirements for high speed access operations. The MB81256 can operate under the condition of t_{RCD} (max) = t_{CAC}, thus providing optimal timing for address multiplexing. In addition, the MB81256 has minimal hold times for Addresses (t_{CAH}), Write-Enable (t_{WCH}) and Data-in (t_{DH}). The MB81256 provides higher throughput in inter-leaved memory system applications. Fujitsu has made the timing requirements that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the Column Address, D and $\overline{W}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{W}$ Delay) are not restricted by t_{RCD}.

Fast Read-Write Cycle
The MB81256 has a fast read-modify-write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{W}$ when $\overline{CAS}$ goes "low". When $\overline{W}$ is "low' during a $\overline{CAS}$ transition to "low", the MB81256 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. When $\overline{W}$ goes "low", after t_{CWD} following a $\overline{CAS}$ transition to "low", the MB81256 goes into the delayed write mode. The output then contains the data from the cell selected and the data from D is written into the cell selected. Therefore, a very fast read-write cycle ($t_{RWC} = t_{RC}$) is possible with the MB81256.

Address Inputs
A total of eighteen binary input address bits are required to decode any 1 of 262,144 cell locations within the MB81256. Nine row-address bits are established on the input pins (A_0 through A_8) and are latched with the Row Address Strobe ($\overline{RAS}$). Nine column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All row addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold/Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

Write Enable
The read or write mode is selected with the $\overline{W}$ input. A logic "high" on $\overline{W}$ dictates read mode. A logic "low" dictates write mode. The data input is disabled when the read mode is selected.

Data Input
Data is written into the MB81256 during a write or read-write cycle. The last falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the data-in (D) register. In a write cycle, if $\overline{W}$ is brought "low" (write mode) before $\overline{CAS}$, D is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{W}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D is strobed by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$.

Data Output
The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when $t_{RCD(max)}$ is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after $t_{RCD(max)}$. Data remains valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Page Mode
Page mode operation permits strobing the row address into the MB81256 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row address doesn't change. Thus, the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

$\overline{RAS}$-Only Refresh
Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-adresses ($A_0 \sim A_7$) at least every 4 ms. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought "low". Strobing each of the 256 row-addresses ($A_0 \sim A_7$) with $\overline{RAS}$ will cause all bits in each row to be refreshed. $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh
$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB81256 offers an alternate refresh method. If $\overline{CAS}$ is held "low" for the specified period (t_{FCS}) before $\overline{RAS}$ goes to "low", on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Hidden Refresh
A hidden refresh cycle may take place while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time. For the MB81256, a hidden refresh cycle is a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The internal refresh address counter provides the refresh addresses as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle
A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

Description
(Continued)

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to "high" and then goes to "low" again while $\overline{RAS}$ is held "low", the read and write operation are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 9 row address bits and 9 column address bits defined as follows:

A ROW ADDRESS
Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set "high" internally.

A COLUMN ADDRESS
All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure
The timing, as shown in the $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle, is used for all the following operations:

(1). Initialize the internal refresh counter. For this operation, 8 cycles are required.

(2). Write a test pattern of "low"s into memory cells at a single column address and 256 row address.

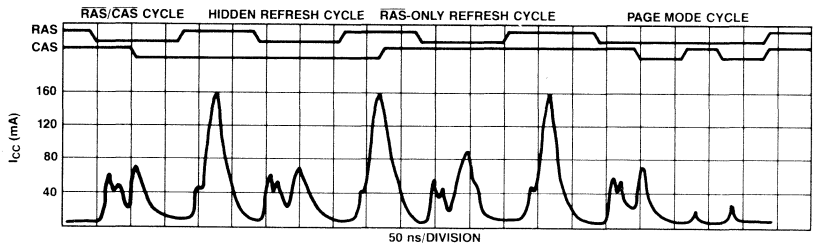
(3). Using a read-modify-write cycle, read the "low" written at the last operation (Step 2) and write a new "high" in the same cycle. This cycle is repeated 256 times, and "high"s are written into the 256 memory cells.

(4). Read the "high"s written at the last operation (Step 3).

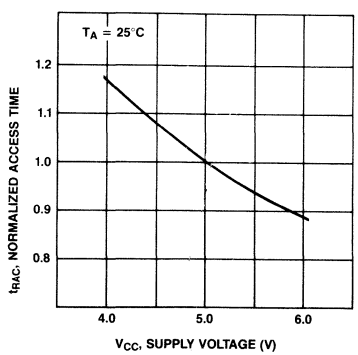
(5). Complement the test pattern and repeat steps (2), (3) and (4).

Typical Characteristics Curves

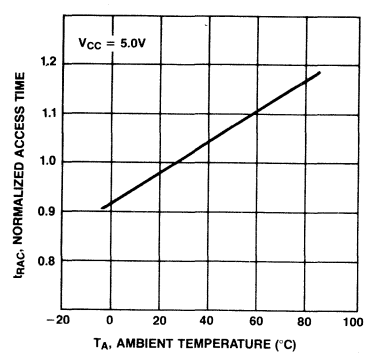
Current Waveforms (V_{CC} = 5.5V, T_A = 25°C)



Normalized Access time vs. Supply Voltage

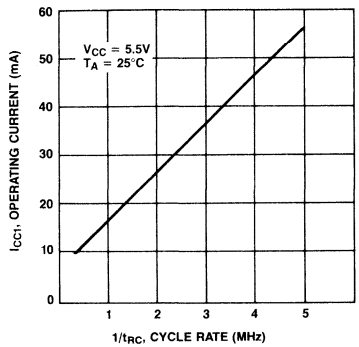


Normalized Access Time vs. Ambient Temperature

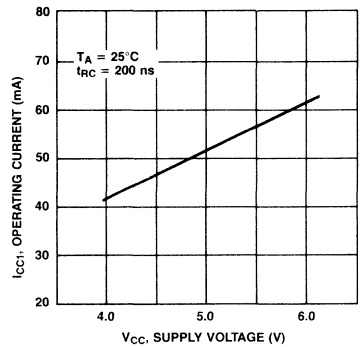


Typical Characteristics Curves
(Continued)

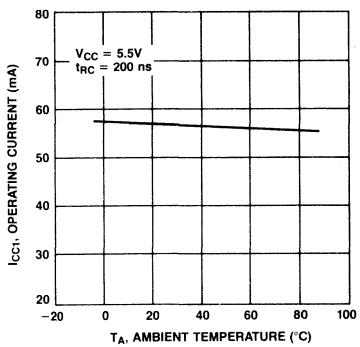
Operating Current vs. Cycle Rate



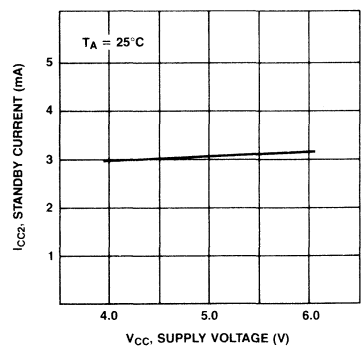
Operating Current vs. Supply Voltage



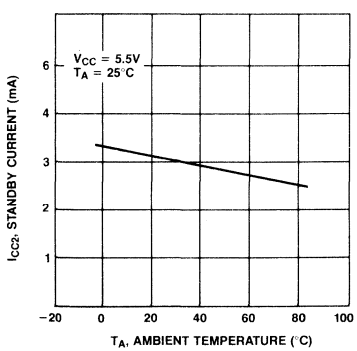
Operating Current vs. Ambient Temperature



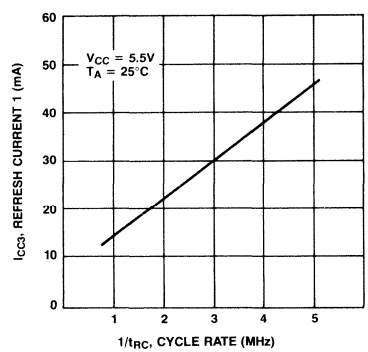
Standby Current vs. Supply Voltage



Standby Current vs. Ambient Temperature

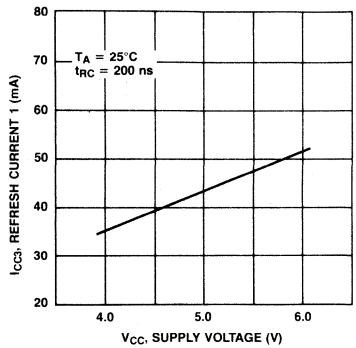


Refresh Current 1 vs. Cycle Rate

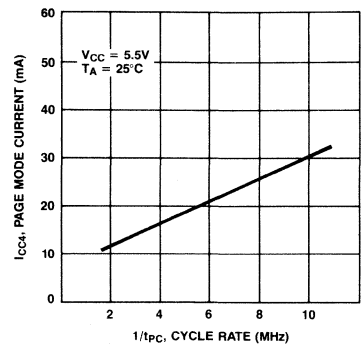


Typical Characteristics Curves
(Continued)

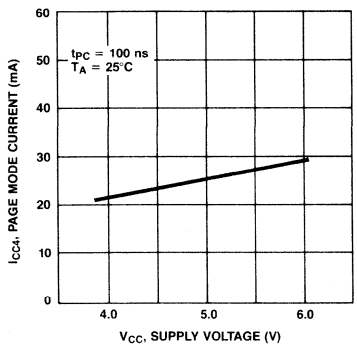
Refresh Current 1 vs. Supply Voltage



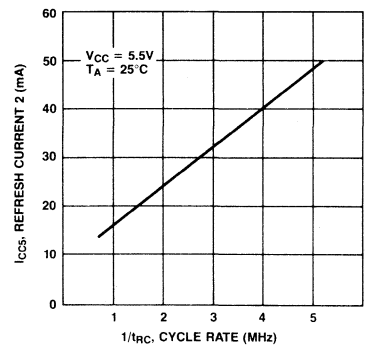
Page Mode Current vs. Cycle Rate



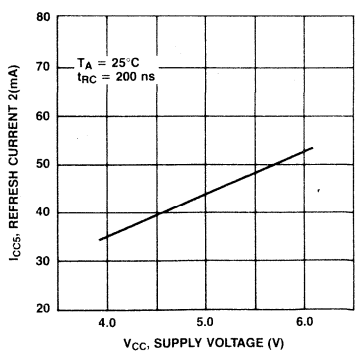
Page Mode Current vs. Supply Voltage



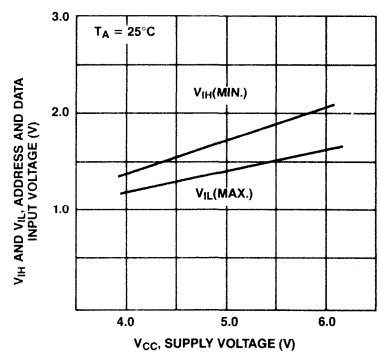
Refresh Current 2 vs. Cycle Rate



Refresh Current 2 vs. Supply Voltage

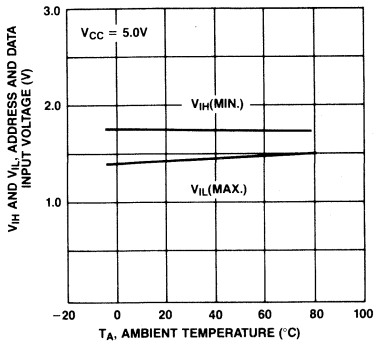


Address and Data Input Voltage vs. Supply Voltage

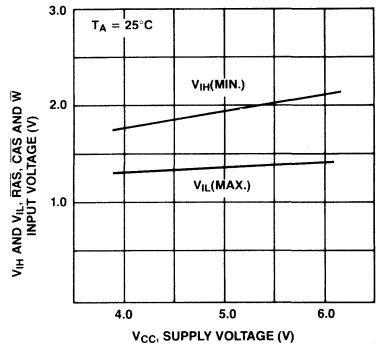


Typical Characteristics Curves
(Continued)

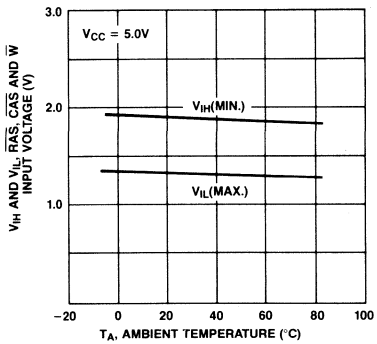
Address and Data Input Voltage vs. Ambient Temperature



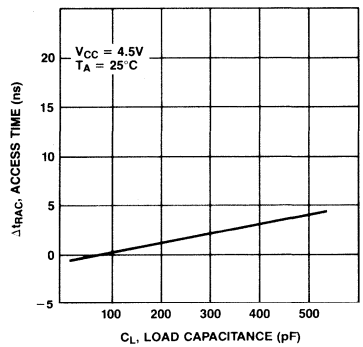
$\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ Input Voltage vs. Supply Voltage



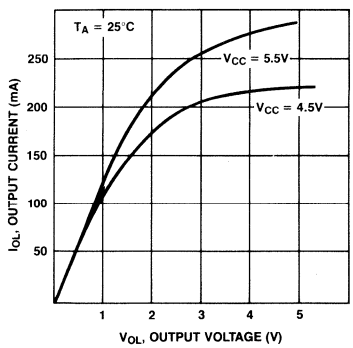
$\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ Input Voltage vs. Ambient Temperature



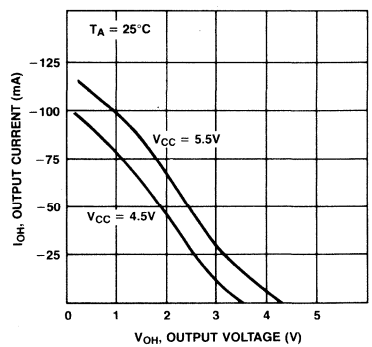
Access Time vs. Load Capacitance



Output Current vs. Output Voltage

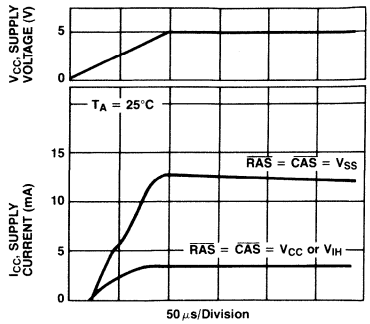


Output Current vs. Output Voltage

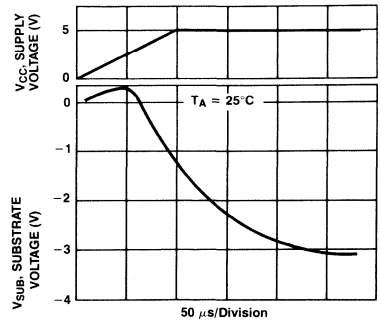


Typical Characteristics Curves
(Continued)

Current Waveform During Power Up

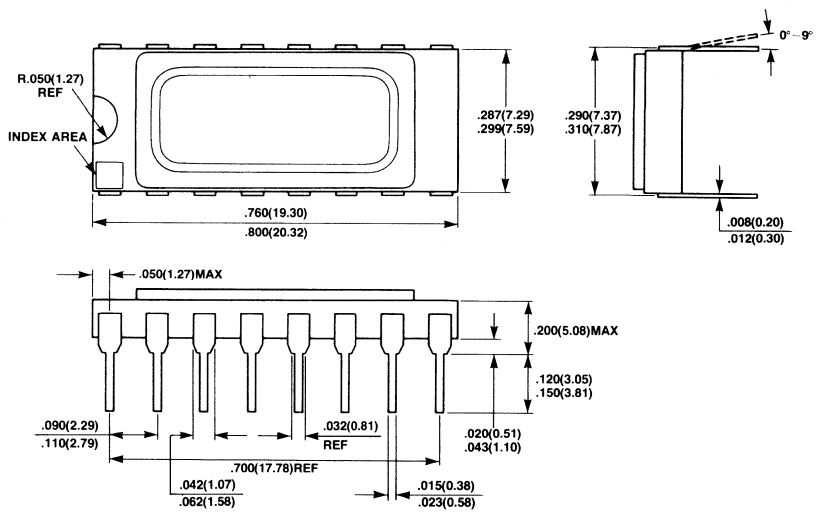


Substrate Voltage During Power Up



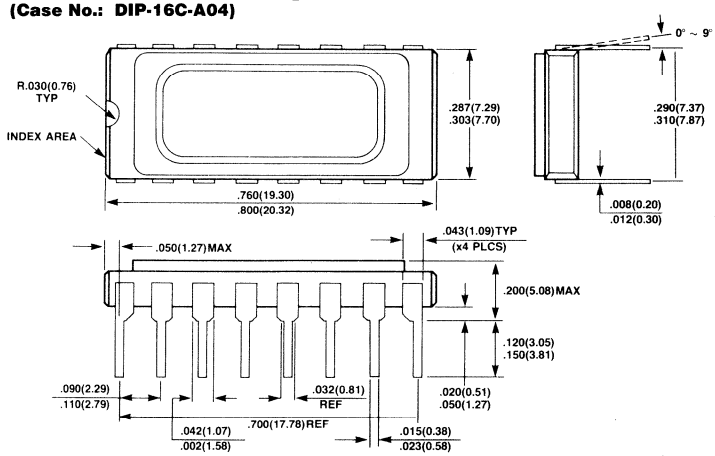
Package Dimensions
Dimensions in inches
(millimeters)

16-Lead Ceramic (Metal Seal) Dual In-Line Package (Case No.: DIP-16C-A03)

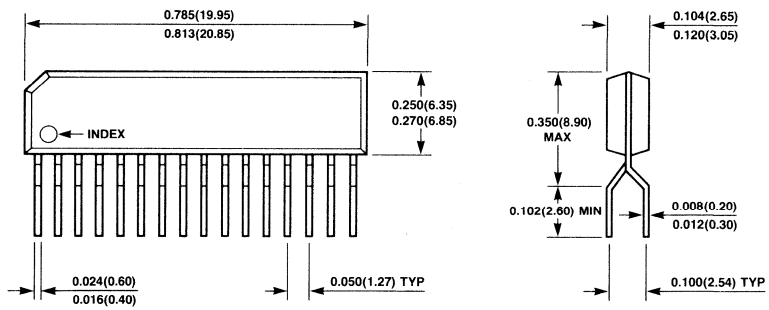


Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

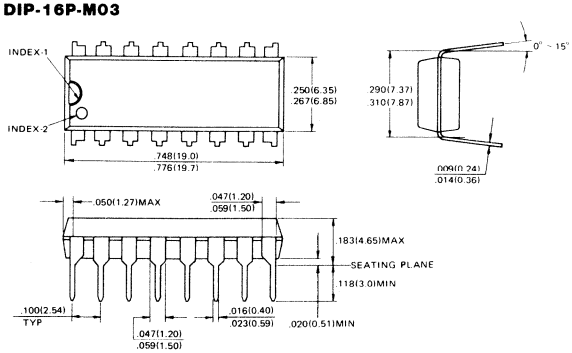
16-Lead Seam Weld DIP Package
(Case No.: DIP-16C-A04)



16 Lead Plastic Zig-Zag In-Line Package
ZIP-16P-M01

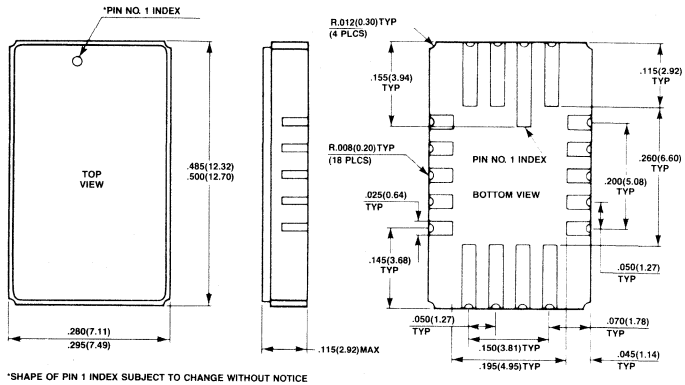


16-Lead Plastic Dual In-Line Package
DIP-16P-M03



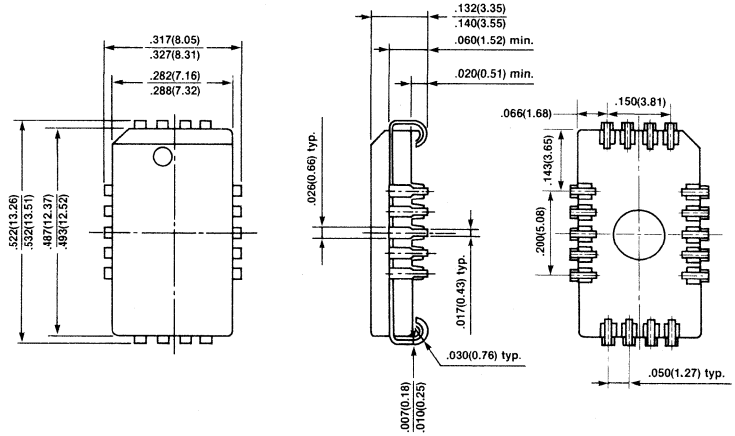
Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

18-Pad Ceramic Leadless Chip Carrier
LCC-18C-F04



*SHAPE OF PIN 1 INDEX SUBJECT TO CHANGE WITHOUT NOTICE

18-Lead Plastic Chip Carrier
LCC-18P-M02



MB81257-10, MB81257-12, MB81257-15

NMOS 262,144-Bit Dynamic Random Access Memory With Nibble Mode

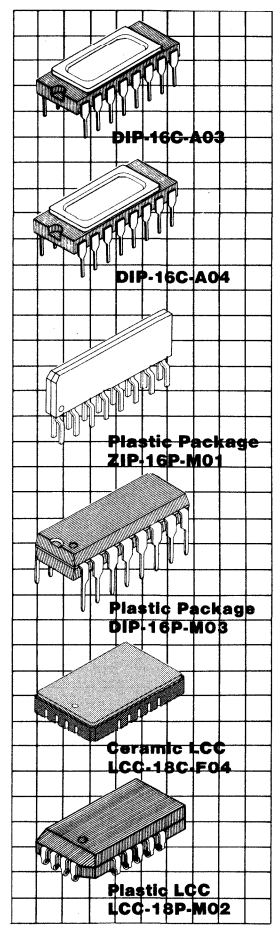
Description

The Fujitsu MB81257 is a fully decoded, dynamic NMOS random access memory organized as 262,144 one-bit words. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

The MB81257 features "nibble mode" which allows high speed serial access of up to four bits of data. Additionally, the MB81257 offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability that is an upward compatible version of the MB8266A. Multiplexed row and column address inputs permit the MB81257 to be housed in a Jedec standard 16-pin dual in-line package and 18-pad LCC.

The MB81257 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-layer Polysilicon process. This process, coupled with single transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is used in the design, including dynamic sense amplifiers.

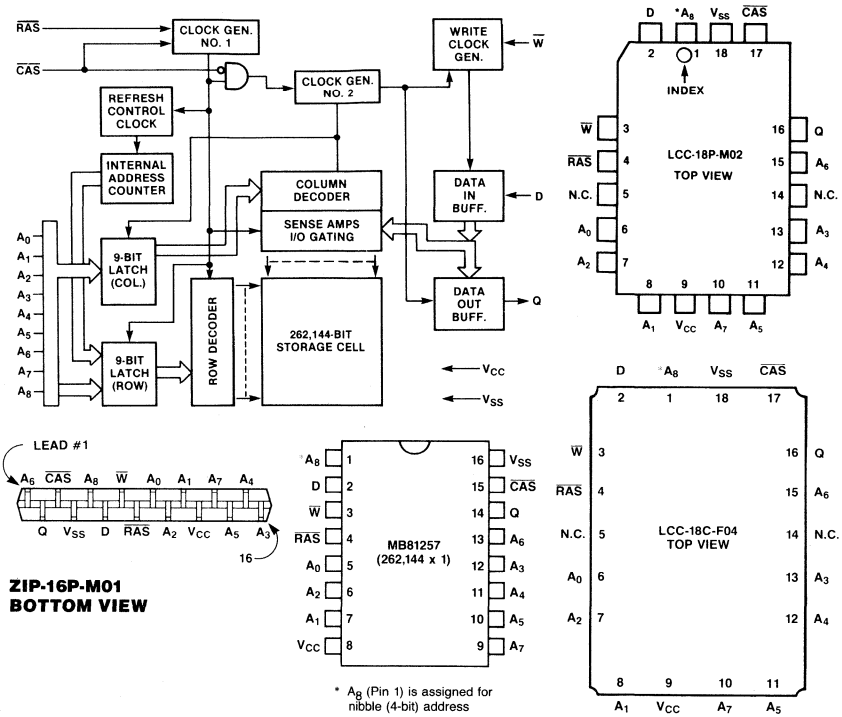
Clock timing requirements are noncritical, and the power supply tolerance is very wide. All inputs are TTL compatible.



Features

- 262,144 x 1-bit organization
- Row Access Time/Cycle Time:
  - MB81257-10 100 ns Max/ 200 ns Min.
  - MB81257-12 120 ns Max/ 220 ns Min.
  - MB81257-15 150 ns Max/ 260 ns Min.
- Low Power Dissipation:
  - 314 mW max. (t_{RC} = 260 ns)
  - 25 mW (Standby)
- +5V supply voltage, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- Common I/O capability using "Early Write" operation
- On-chip substrate bias generator
- Nibble mode capability for faster access
- Fast Read-Write Cycle, TRWC = TRC
- t_{AR} t_{WCR}, t_{DHR}, t_{RWD} eliminated
- $\overline{CAS}$-before-$\overline{RAS}$ on chip refresh
- Hidden $\overline{CAS}$ before-$\overline{RAS}$ on-chip refresh
- $\overline{RAS}$-only refresh
- Refresh 4 ms/256 cycles
- Output unlatched at cycle end allows two dimensional chip select
- On-chip Address and Data-in latches
- Industry standard 16-pin package

MB81257 Block Diagram and Pin Assignments



NOTE: The following IEEE Std. 662-1980 symbols are used in this data sheet: D = Data In, $\overline{W}$ = Write Enable, Q = Data Out.

Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Voltage on Any Pin relative to V_{SS}		V_{IN}, V_{OUT}, V_{CC}	−1.0 to 7.0	V
Operating Temperature (ambient)		T_{OP}	0 to 70	°C
Storage Temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		I_{OS}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Value Min	Value Typ	Value Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C ambient
	V_{SS}	0	0	0	V	
Input High Voltage All Inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage All Inputs	V_{IL}	−2.0		0.8	V	

Capacitance
($T_A = 25°C$)

Parameter	Symbol	Value Min	Value Typ	Value Max	Unit
Input Capacitance A_0 to A_8, D	C_{IN1}			7	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$	C_{IN2}			10	pF
Output Capacitance Q	C_{OUT}			7	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81257-10 Min	MB81257-10 Max	MB81257-12 Min	MB81257-12 Max	MB81257-15 Min	MB81257-15 Max	Unit
OPERATING CURRENT*1 Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min.)	I_{CC1}		70		65		57	mA
STANDBY CURRENT Power Supply Current ($\overline{RAS}/\overline{CAS} = V_{IH}$)	I_{CC2}		4.5		4.5		4.5	mA
REFRESH CURRENT 1*1 Average Power Supply current ($\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$; t_{RC} = Min.)	I_{CC3}		60		55		50	mA
NIBBLE MODE CURRENT*1 Average Power Supply current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; t_{NC} = Min.)	I_{CC4}		22		20		18	mA
REFRESH CURRENT 2*1 Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = Min.)	I_{CC5}		65		60		55	mA
INPUT LEAKAGE CURRENT Any Input, (V_{IN} = 0V to 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)	I_{IL}	−10	10	−10	10	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data is disabled, V_{OUT} = 0V to 5.5V)	I_{OL}	−10	10	−10	10	−10	10	μA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}		0.4		0.4		0.4	V
OUTPUT LEVEL Output High Voltage (I_{OH} = −5.0 mA)	V_{OH}	2.4		2.4		2.4		V

Note: *1 I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC Characteristics[*1,2,3]
(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol Alternate	Symbol *Standard	MB81257-10 Min	MB81257-10 Max	MB81257-12 Min	MB81257-12 Max	MB81257-15 Min	MB81257-15 Max	Unit
Time between Refresh		t_{REF}	TRVRV		4		4		4	ms
Random Read/Write Cycle Time		t_{RC}	TRELREL	200		220		260		ns
Read-Write Cycle Time		t_{RWC}	TRELREL	200		220		260		ns
Access Time from $\overline{RAS}$[*4,6]		t_{RAC}	TRELQV		100		120		150	ns
Access Time from $\overline{CAS}$[*5,6]		t_{CAC}	TCELQV		50		60		75	ns
Output Buffer Turn off Delay		t_{OFF}	TCEHQZ	0	25	0	25	0	30	ns
Transition Time		t_T	TT	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	TREHREL	85		90		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	TRELREH	105	100000	120	100000	150	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	TCELREH	55		60		75		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	TCELCEH	55	100000	60	100000	75	100000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	TRELCEH	105		120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time[*4,7]		t_{RCD}	TRELCEL	20	50	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	TCEHREL	10		10		10		ns
Row Address Set Up Time		t_{ASR}	TAVREL	0		0		0		ns
Row Address Hold Time		t_{RAH}	TRELAX	10		12		15		ns
Column Address Set Up Time		t_{ASC}	TAVCEL	0		0		0		ns
Column Address Hold Time		t_{CAH}	TCELAX	15		20		25		ns
Read Command Set Up Time		t_{RCS}	TWHCEL	0		0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$[*10]		t_{RCH}	TCEHWX	0		0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$[*10]		t_{RRH}	TREHWX	20		20		20		ns
Write Command Set Up Time[*8]		t_{WCS}	TWLCEL	0		0		0		ns
Write Command Pulse Width		t_{WP}	TWLWH	15		20		25		ns
Write Command Hold Time		t_{WCH}	TCELWH	15		20		25		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	TWLREH	35		40		45		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	TWLCEH	20		30		35		ns
Data In Set Up Time		t_{DS}	TDVCEL	0		0		0		ns
Data In Hold Time		t_{DH}	TCELDX	15		20		25		ns
$\overline{CAS}$ to $\overline{W}$ Delay[*8]		t_{CWD}	TCELWL	15		20		25		ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$		t_{FCS}	TCELREL	20		20		20		ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$		t_{FCH}	TRELCEX	20		25		30		ns

Notes: *These symbols are described in IEEE STD. 662-1980: IEEE Standard terminology for semiconductor memory.

*1 An initial pause of 200μs is required after power up, followed by any 8 $\overline{RAS}$ cycles, before proper device operation is achieved. If the internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh initialization cycles are required.

*2 AC characteristics assume t_T = 5ns.

*3 V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} and V_{IL}.

*4 t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$ (Max.) the specified maximum value of t_{RAC} (Max.) can be met. If $t_{RCD} > t_{RCD}$ (Max.) then t_{RAC} is increased by the amount that t_{RCD} exceeds t_{RCD} (Max.).

*5 Assumes that $t_{RCD} > t_{RCD}$ (Max.).

*6 Measured with a load equivalent to 2 TTL loads and 100pF.

*7 t_{RCD} (Min.) = t_{RAH} (Min.) + $2t_T$ + t_{ASC} (Min.).

*8 t_{WCS} and t_{CWD} are nonrestrictive operating parameters, and are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (Min.), the cycle is an early write cycle, and the data out pin will remain open circuit (High Impedance) throughout the entire cycle.

If $t_{CWD} > t_{CWD}$ (Min.), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.

*10 Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

AC Characteristics

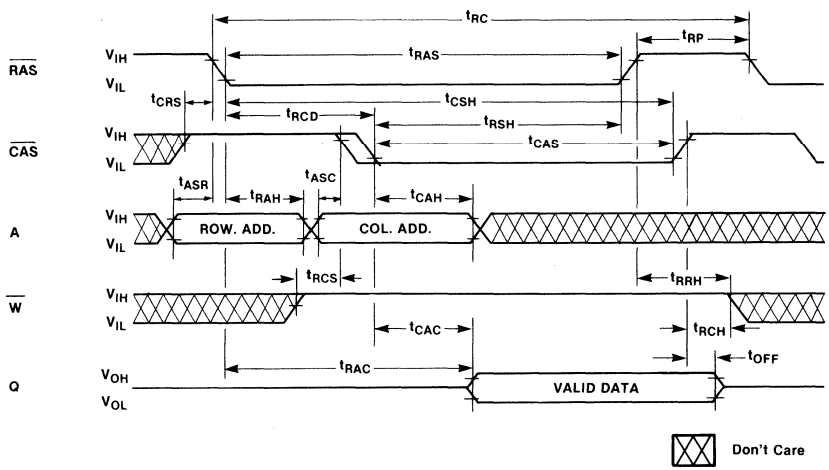
(Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol Alternate	Symbol *Standard	MB81257-10 Min	MB81257-10 Max	MB81257-12 Min	MB81257-12 Max	MB81257-15 Min	MB81257-15 Max	Unit
Nibble Mode Read-Write Cycle Time		t_{NRWC}	TCEHCEH	45		50		60		ns
Nibble Mode Read/Write Cycle Time		t_{NC}	TCEHCEH	45		50		60		ns
Nibble Mode Access Time		t_{NCAC}	TCELQV		20		25		30	ns
Nibble Mode $\overline{CAS}$ Pulse Width		t_{NCAS}	TCELCEH	20		25		30		ns
Nibble Mode $\overline{CAS}$ Precharge Time		t_{NCP}	TCEHCEL	15		15		20		ns
Nibble Mode Read $\overline{RAS}$ Hold Time		t_{NRRSH}	TCELREH	20		25		30		ns
Nibble Mode $\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$		t_{RNH}	TREHCEL	20		20		20		ns
Nibble Mode Write $\overline{RAS}$ Hold Time		t_{NWRSH}	TCELREH	35		40		45		ns
Refresh Counter Test Cycle Time*9		t_{RTC}	TRELREL	330		375		430		ns
Refresh Counter Test $\overline{CAS}$ Precharge Time*9		t_{CPT}	TCEHCEL	50		60		70		ns
Refresh Counter Test $\overline{RAS}$ Pulse Width*9		t_{TRAS}	TRELREH	230	10000	265	10000	320	10000	ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time		t_{RPC}	TREHCEL	20		20		20		ns
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle		t_{CPR}	TCEHCEL	20		25		30		ns

Notes: *9 Test mode cycle only.

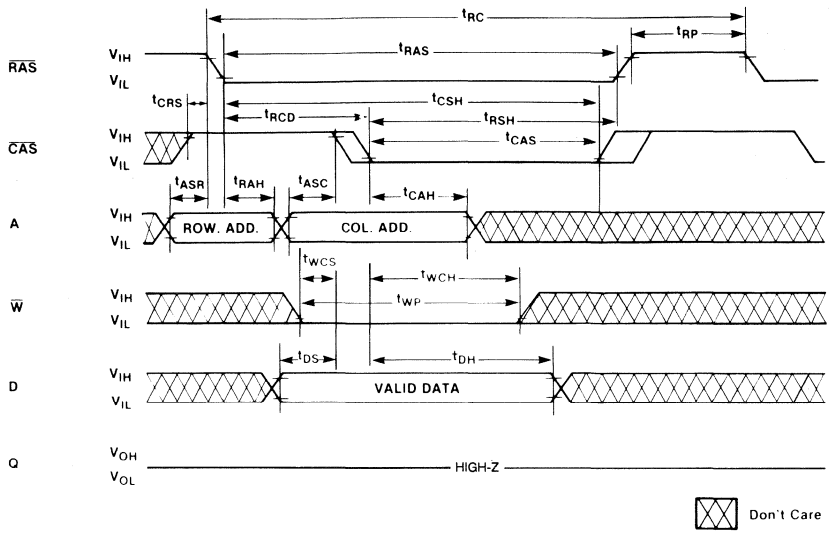
Timing Diagrams

Read Cycle

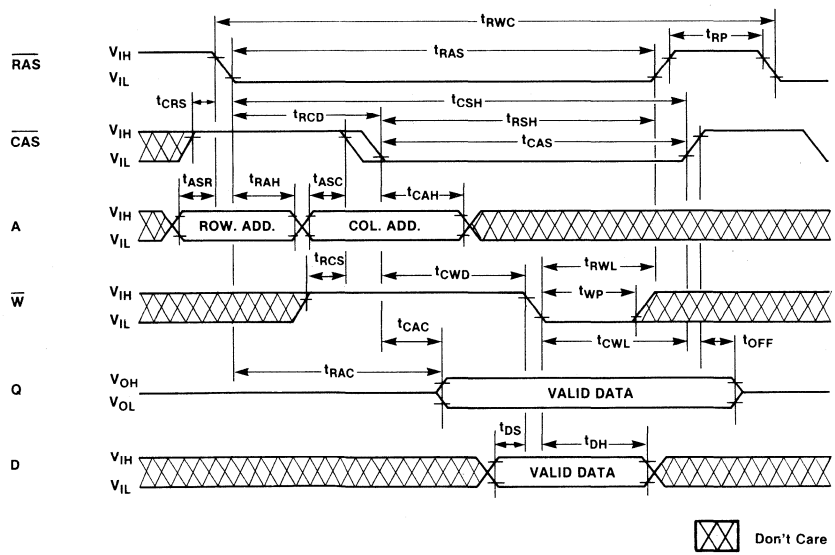


Timing Diagrams
(Continued)

Write Cycle (Early Write)



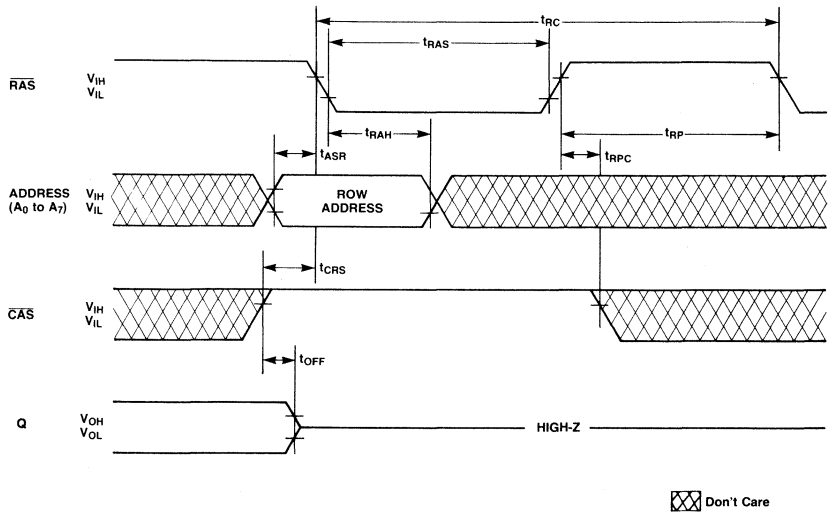
Read-Write/Read-Modify-Write Cycle



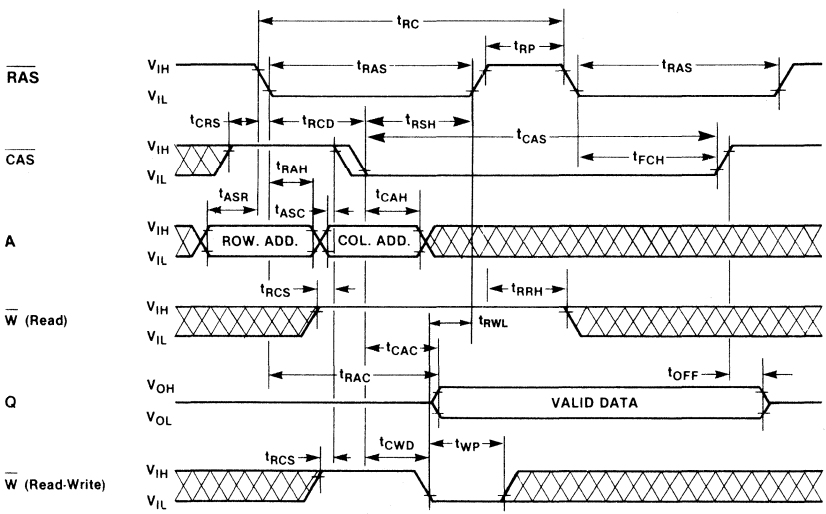
Timing Diagrams
(Continued)

"$\overline{RAS}$-Only" Refresh Cycle

Note: $\overline{W}$, IN = Don't Care, $A_8 = V_{IH}$ or V_{IL}

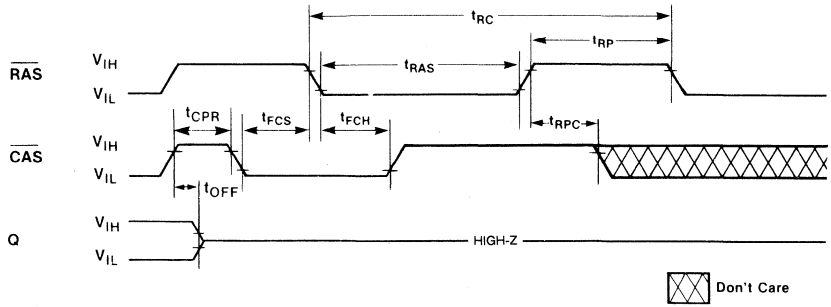


Hidden Refresh Cycle

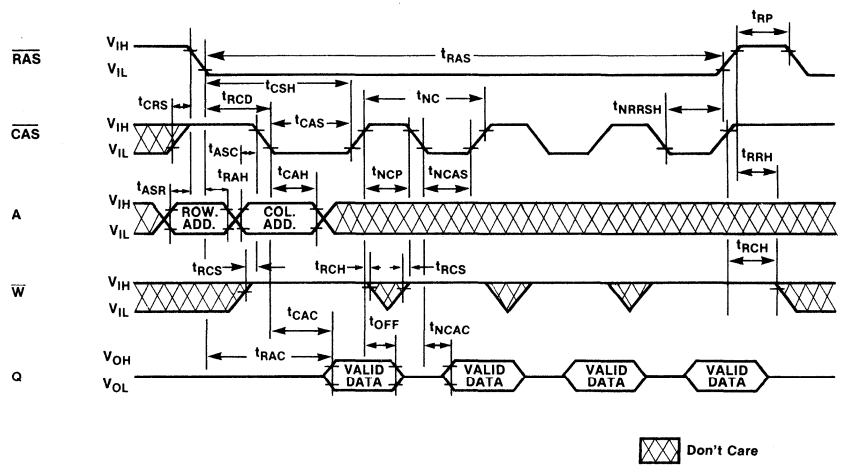


Timing Diagrams
(Continued)

"$\overline{CAS}$-Before-$\overline{RAS}$" Refresh Cycle
NOTE: Address, $\overline{W}$, D = Don't Care

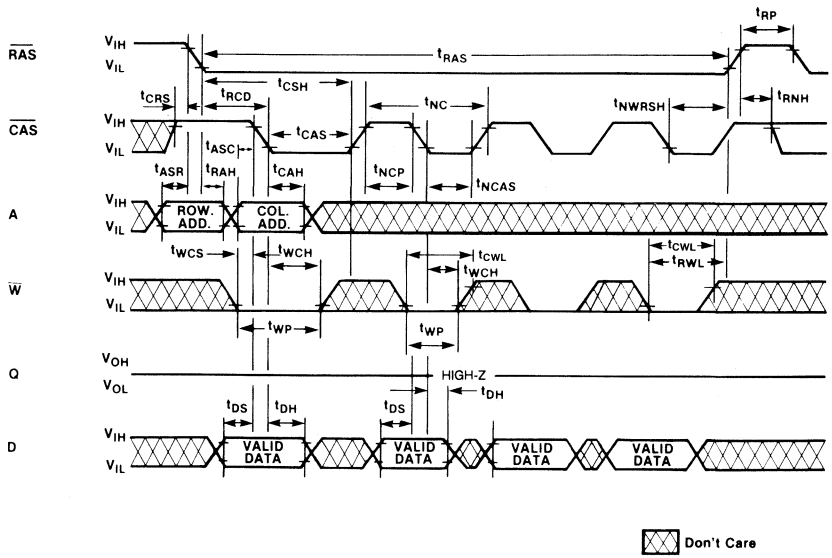


Nibble Mode Read Cycle

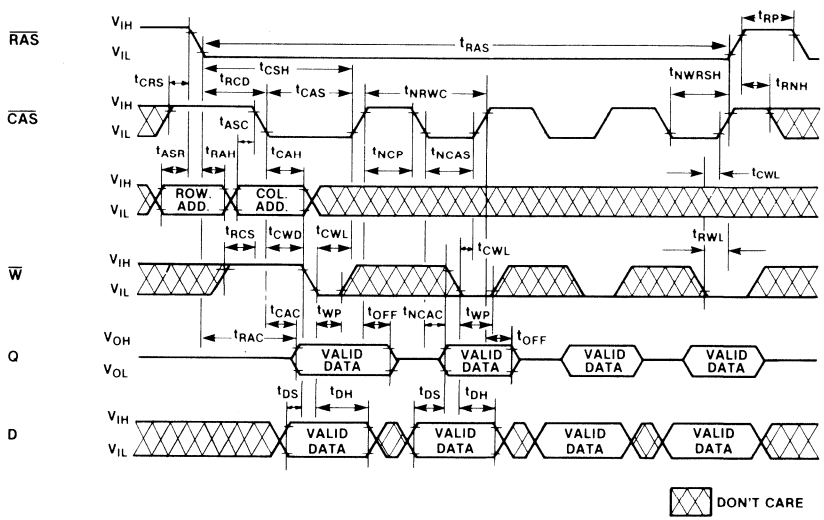


Timing Diagrams
(Continued)

Nibble Mode Write Cycle

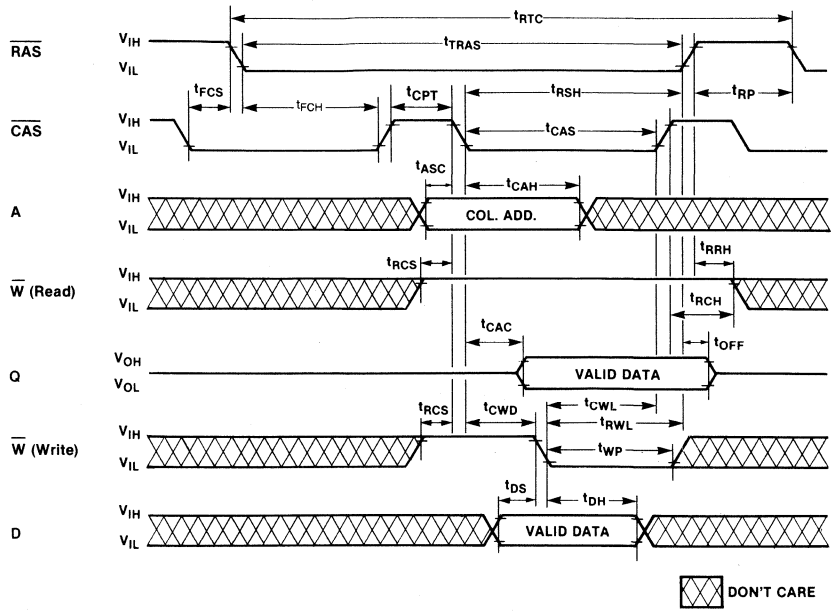


Nibble Mode Read-Write Cycle



Timing Diagrams
(Continued)

"$\overline{CAS}$-Before-$\overline{RAS}$" Refresh Counter Test Cycle



Description

Simplified Timing Requirement
The MB81257 has improved circuitry that eases timing requirements for high speed access operations. The MB81257 can operate under the condition of t_{RCD} (max) = t_{CAC}, thus providing optimal timing for address multiplexing. In addition, the MB81257 has minimal hold times for Addresses (t_{CAH}), Write-Enable (t_{WCH}) and Data-in (t_{DH}). The MB81257 provides higher throughput in interleaved memory system applications. Fujitsu has made the timing requirements that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the Column Address, D and $\overline{W}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{W}$ Delay) are not restricted by t_{RCD}.

Fast Read-Write Cycle
The MB81257 has a fast read-modify-write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{W}$ when $\overline{CAS}$ goes "low". When $\overline{W}$ is "low" during a $\overline{CAS}$ transition to "low", the MB81257 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. When $\overline{W}$ goes "low", after t_{CWD} following a $\overline{CAS}$ transition to "low", the MB81257 goes into the delayed write mode. The output then contains the data from the cell selected and the data from D is written into the cell selected. Therefore, a very fast read-write cycle ($t_{RWC} = t_{RC}$) is possible with the MB81257.

Address Inputs
A total of eighteen binary input address bits are required to decode any 1 of 262,144 cell locations within the MB81257. Nine row address bits are established on the input pins (A_0 through A_8) and are latched with the Row Address Strobe ($\overline{RAS}$). Nine column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold/Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

Write Enable
The read or write mode is selected with the $\overline{W}$ input. A logic "high" on $\overline{W}$ dictates read mode. A logic "low" dictates write mode. The data input is disabled when the read mode is selected.

Data Input
Data is written into the MB81257 during a write or read-write cycle. The last falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the Data-in (D) register. In a write cycle, if $\overline{W}$ is brought "low" (write mode) before $\overline{CAS}$, D is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{W}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D is strobed by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$.

Data Output
The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when $t_{RCD(max)}$ is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after $t_{RCD(max)}$. Data remains valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Nibble Mode
Nibble mode allows high speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 row addresses and the 8 column addresses. The 2 bits of addresses (CA_8, RA_8) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by the normal mode, the remaining nibble bits may be accessed by toggling $\overline{CAS}$ "high" then "low" while $\overline{RAS}$ remains "low". Toggling $\overline{CAS}$ causes RA_8 and CA_8 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. (See table I below).

If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on subsequent access, the new data will be written into the selected cell location.

In nibble mode, the three-state control of the D_{OUT} pin is determined by the first normal access cycle.

The data output is controlled

Table 1
Nibble Mode Address Sequence Example

Sequence	Nibble Bit	RA_8	Row Address	CA_8	Column Address	Comments
$\overline{RAS}/\overline{CAS}$ (normal mode)	1	0	10101010	0	10101010	input addresses
toggle $\overline{CAS}$ (nibble mode)	2	1	10101010	0	10101010	
toggle $\overline{CAS}$ (nibble mode)	3	0	10101010	1	10101010	generated internally
toggle $\overline{CAS}$ (nibble mode)	4	1	10101010	1	10101010	
toggle $\overline{CAS}$ (nibble mode)	1	0	10101010	0	10101010	sequence repeats

Description
(Continued)

only by the $\overline{W}$ state referenced at the $\overline{CAS}$ negative transition of the normal cycle (first nibble bit). That is, when $t_{WCS} > t_{WCS}$(min.) is met, the data output will remain in the high-impedance state throughout the succeeding nibble cycle regardless of the $\overline{W}$ state. When $t_{CWD} > t_{CWD}$(min.) is met, the data output will contain data from the cell selected during the succeeding nibble cycle regardless of the $\overline{W}$ state. The write operation is done during the period in which the $\overline{W}$ and $\overline{CAS}$ clocks are low. Therefore, the write operation can be performed bit by bit during each nibble operation regardless of the timing conditions of $\overline{W}$ (t_{WCS} and t_{CWD}) during the normal cycle (first nibble bit). (See table 2 and Figure 1 below).

$\overline{RAS}$-Only Refresh
Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-adresses ($A_0 \sim A_7$) at least every 4 ms. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought "low". Strobing each of the 256 row-addresses ($A_0 \sim A_7$) with $\overline{RAS}$ will cause all bits in each row to be refreshed. $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh
$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB81257 offers an alternate refresh method. If $\overline{CAS}$ is held "low" for the specified period (t_{FCS}) before $\overline{RAS}$ goes to "low", on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place.

After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Hidden Refresh
A hidden refresh cycle may take place while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time. For the MB81257, a hidden refresh cycle is a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The internal refresh address counter provides the refresh addresses as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle
A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to "high" and then goes to "low" again while $\overline{RAS}$ is held "low", the read and write operation are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 9 row address bits and 9 column address bits defined as follows:

A ROW ADDRESS
Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set "high" internally.

A COLUMN ADDRESS
All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure
The timing, as shown in the $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle, is used for all the following operations:

(1). Initialize the internal refresh counter. For this operation, 8 cycles are required.

(2). Write a test pattern of "low"s into memory cells at a single column address and 256 row address.

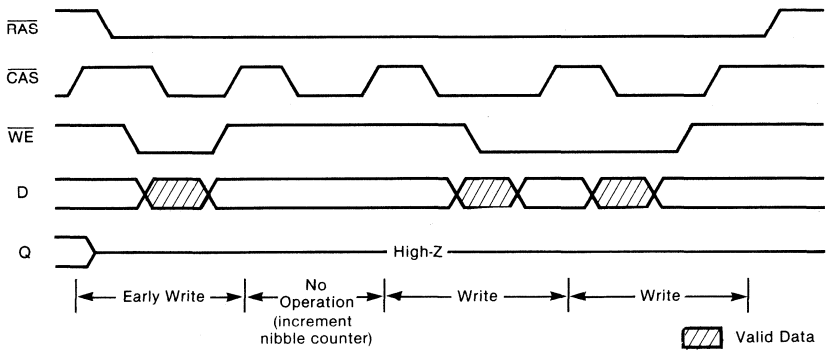
(3). Using a read-modify-write cycle, read the "low" written at the last operation (Step (2)) and write a new "high" in the same cycle. This cycle is repeated 256 times, and "high"s are written into the 256 memory cells.

(4). Read the "high"s written at the last operation (Step 3).

(5). Complement the test pattern and repeat steps (2), (3) and (4).

Figure 1
Nibble Mode

1) In this case the first nibble cycle is an Early Write cycle.



2) In this case the first nibble cycle is a delayed write (Read-Write) cycle.

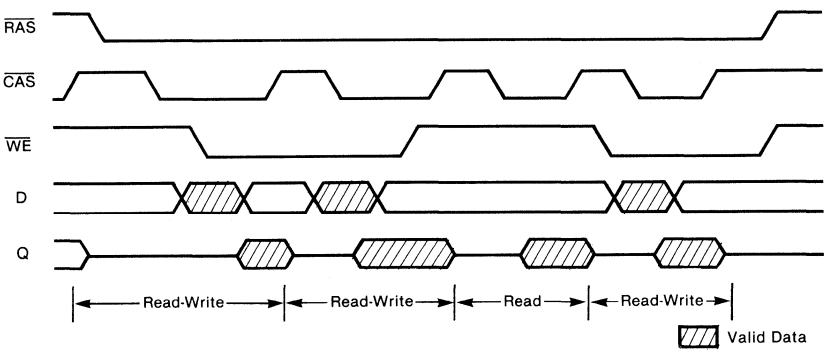
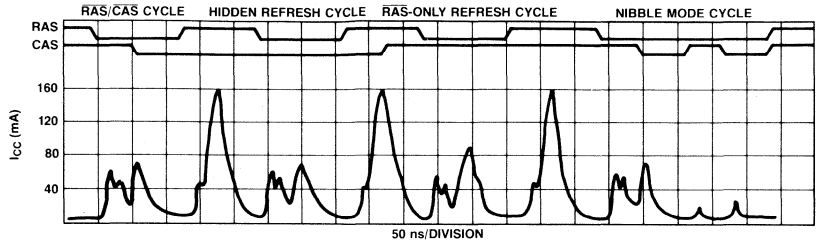


Table 2
Functional Truth Table

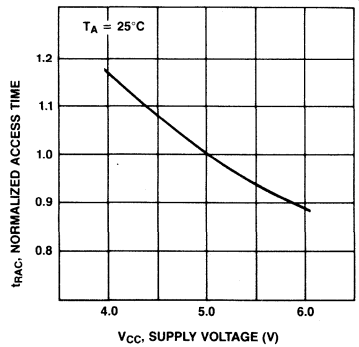
$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	D_{IN}	D_{OUT}	Read	Write	Refresh	Note
H	H	Don't Care	Don't Care	High-Z	No	No	No	Standby.
L	L	H	Don't Care	Valid Data	Yes	No	Yes	Read.
L	L	L	Valid Data	High-Z	No	Yes	Yes	Early Write $t_{WCS} \geq t_{WCS}$ (min).
L	L	L	Valid Data	Valid Data	Yes	Yes	Yes	Delayed Write or Read-Write $t_{CWD} \geq t_{CWD}$ (min).
L	H	Don't Care	Don't Care	High-Z	No	No	Yes	$\overline{RAS}$ Only Refresh.
L	L	Don't Care	Don't Care	Valid Data	No	No	Yes	$\overline{CAS}$-before-$\overline{RAS}$ Refresh. Valid data selected at previous Read or Read-Write cycle is held.
H	L	Don't Care	Don't Care	High-Z	No	No	No	$\overline{CAS}$ disturb.

Typical Characteristics Curves

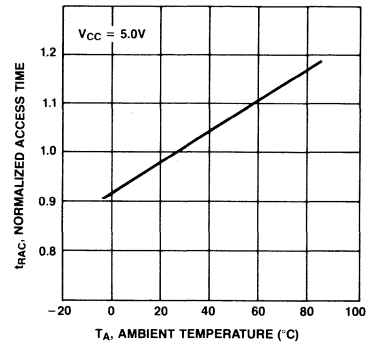
Current Waveform (V_{CC} = 5.5V, T_A = 25°C)



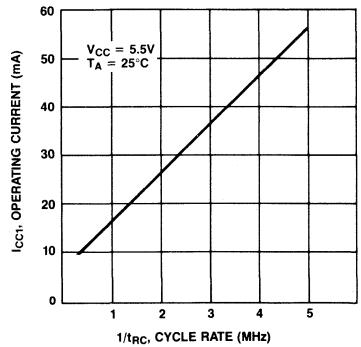
Normalized Access Time vs. Supply Voltage



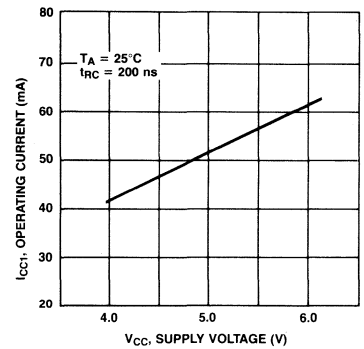
Normalized Access Time vs. Ambient Temperature



Operating Current vs. Cycle Rate

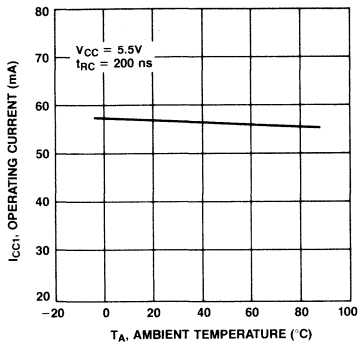


Operating Current vs. Supply Voltage

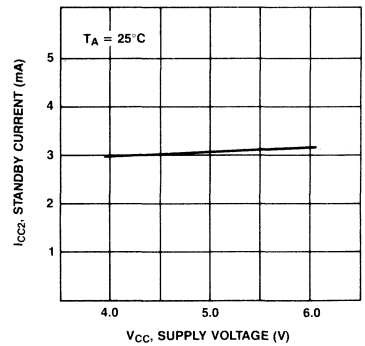


Typical Characteristics Curves
(Continued)

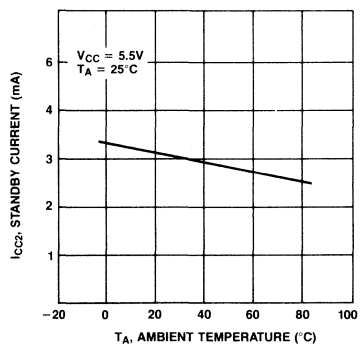
Operating Current vs. Ambient Temperature



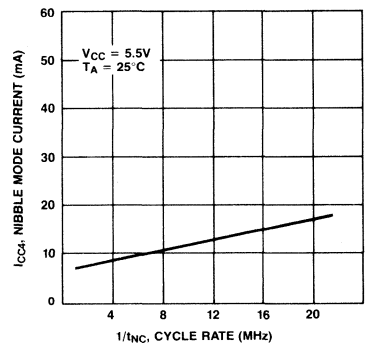
Standby Current vs. Supply Voltage



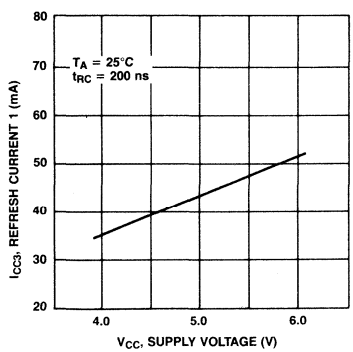
Standby Current vs. Ambient Temperature



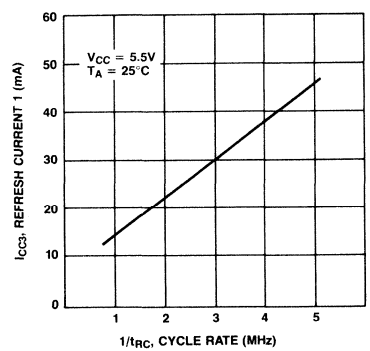
Nibble Mode Current vs. Cycle Rate



Refresh Current 1 vs. Supply Voltage

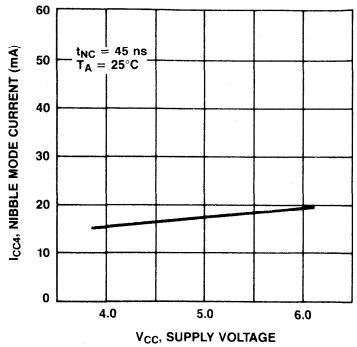


Refresh Current 1 vs. Cycle Rate

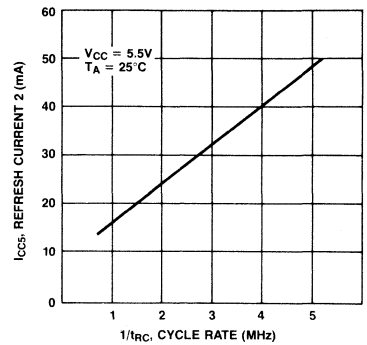


Typical Characteristics Curves
(Continued)

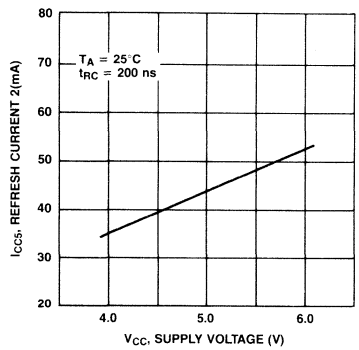
Nibble Mode Current vs. Supply Voltage



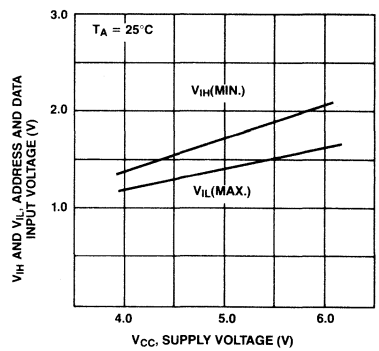
Refresh Current 2 vs. Cycle Rate



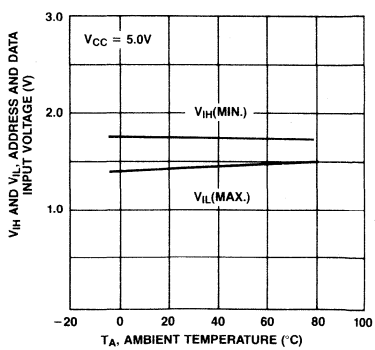
Refresh Current 2 vs. Supply Voltage



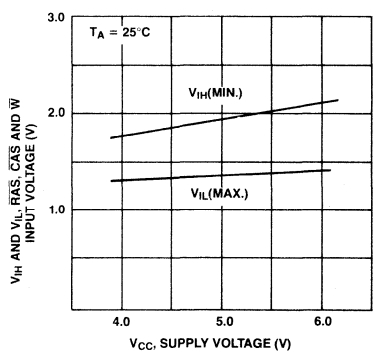
Address and Data Input Voltage vs. Supply Voltage



Address and Data Input Voltage vs. Ambient Temperature

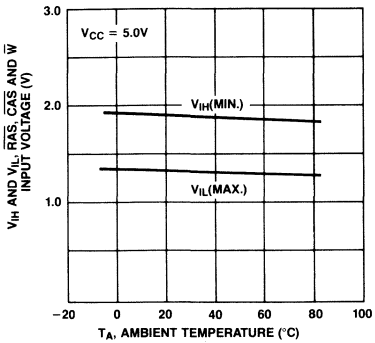


$\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ Input Voltage vs. Supply Voltage

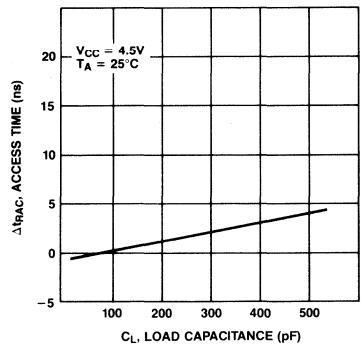


Typical Characteristics Curves
(Continued)

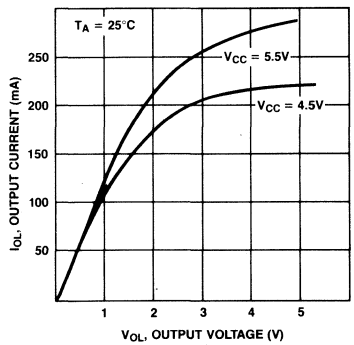
$\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ Input Voltage vs. Ambient Temperature



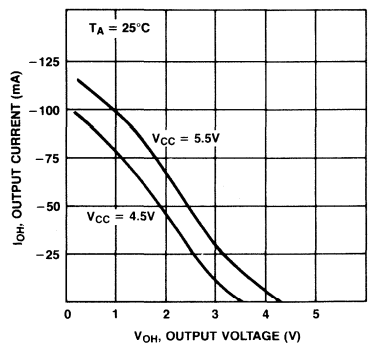
Access Time vs. Load Capacitance



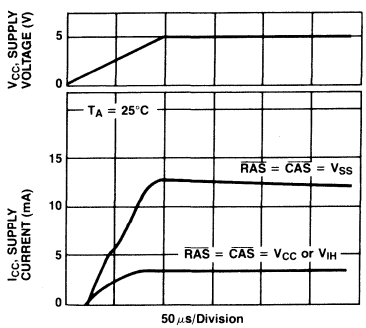
Output Current vs. Output Voltage



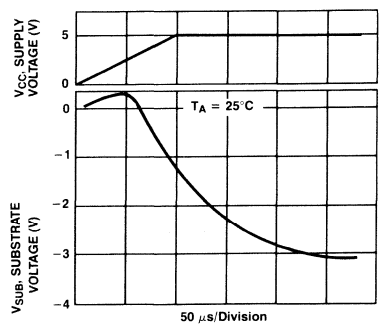
Output Current vs. Output Voltage



Current Waveform During Power Up

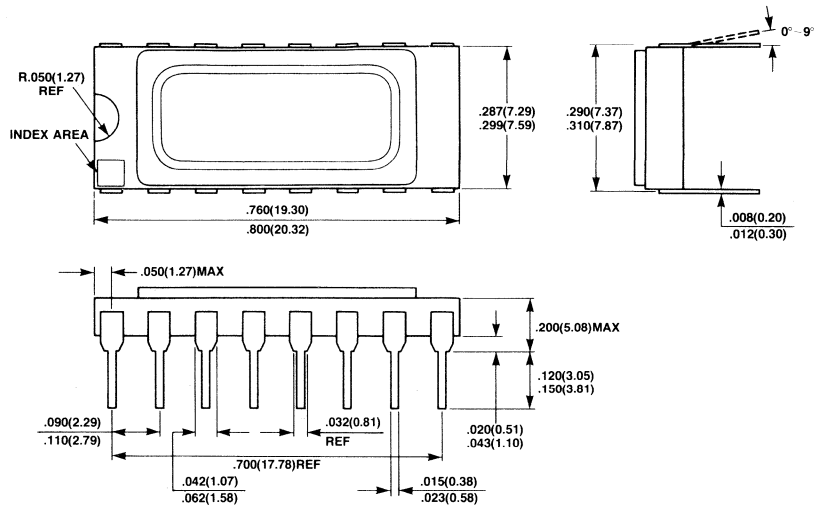


Substrate Voltage During Power Up

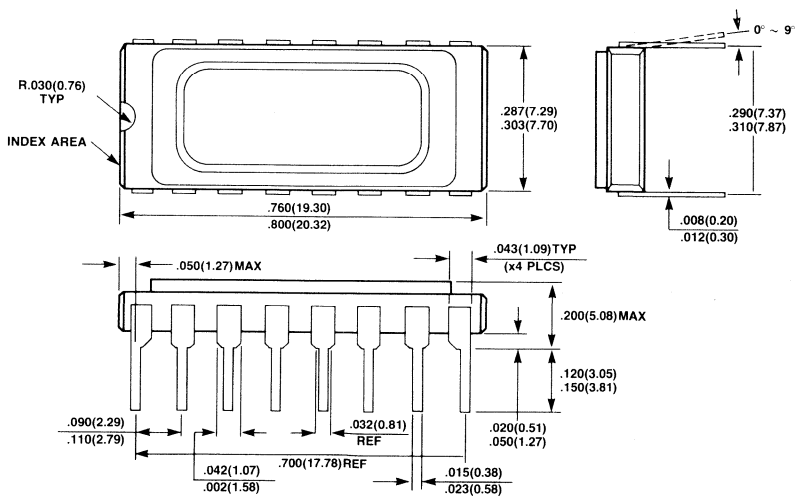


Package Dimensions
Dimensions in inches
(millimeters)

16-Lead Ceramic (Metal Seal) Dual In-Line Package
(Case No.: DIP-16C-A03)

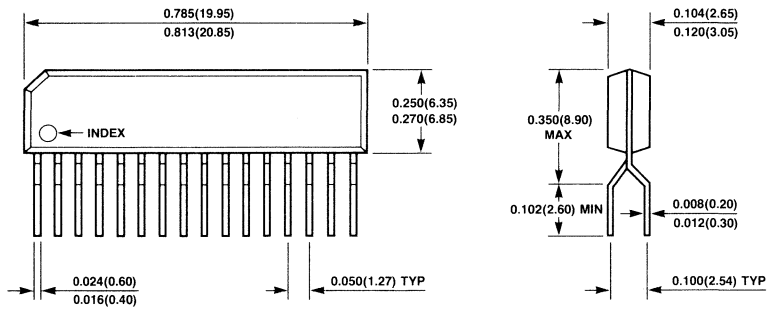


16-Lead Seam Weld DIP Package
(Case No.: DIP-16C-A04)

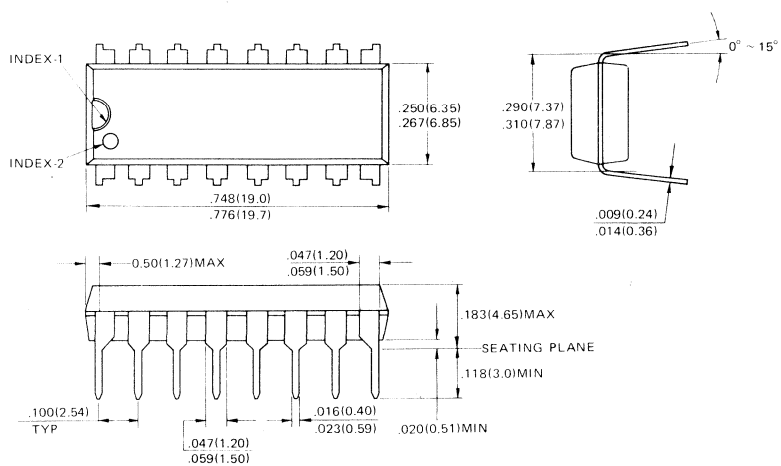


Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

16 Lead Plastic Zig-Zag In-Line Package
ZIP-16P-M01

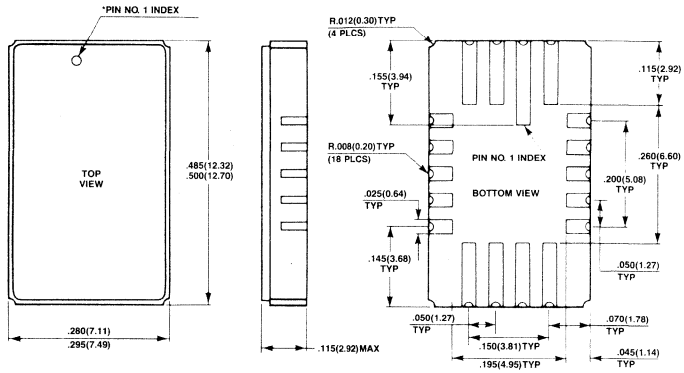


16-Lead Plastic Dual In-Line Package
DIP-16P-M03



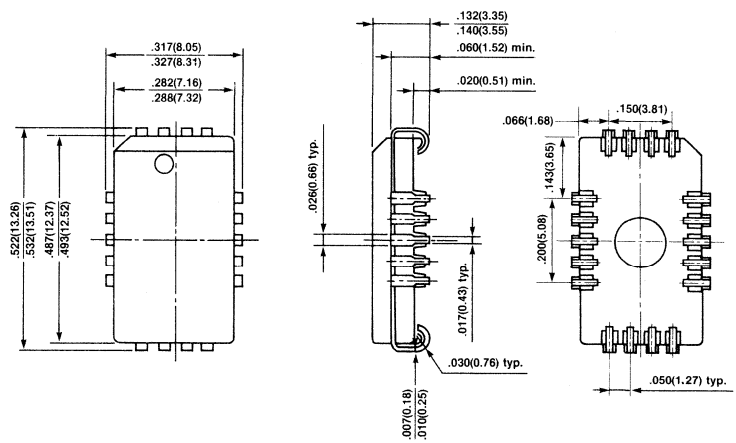
Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

18-Pad Ceramic Leadless Chip Carrier
LCC-18C-F04



*SHAPE OF PIN 1 INDEX SUBJECT TO CHANGE WITHOUT NOTICE

18-Lead Plastic Chip Carrier
LCC-18P-M02



■ MB81256-12-W, MB81256-15-W

NMOS 262,144-Bit Dynamic Random Access Memory

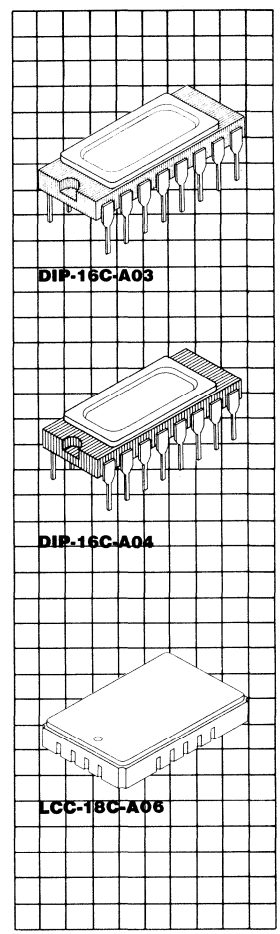
Description

The Fujitsu MB81256-W is a fully decoded, dynamic NMOS random access memory organized as 262,144 one-bit words. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

The MB81256-W features "page mode" which allows high speed random access of up to 512-bits within the same row. Additionally, the MB81256-W offers new functional enhancements that make it more versatile than previous dynamic RAMs. Multiplexed row and column address inputs permit the MB81256-W to be housed in a Jedec standard 16-pin dual in-line package and 18-pad LCC.

The MB81256-W is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-layer Polysilicon process. This process, coupled with single transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is used in the design, including dynamic sense amplifiers.

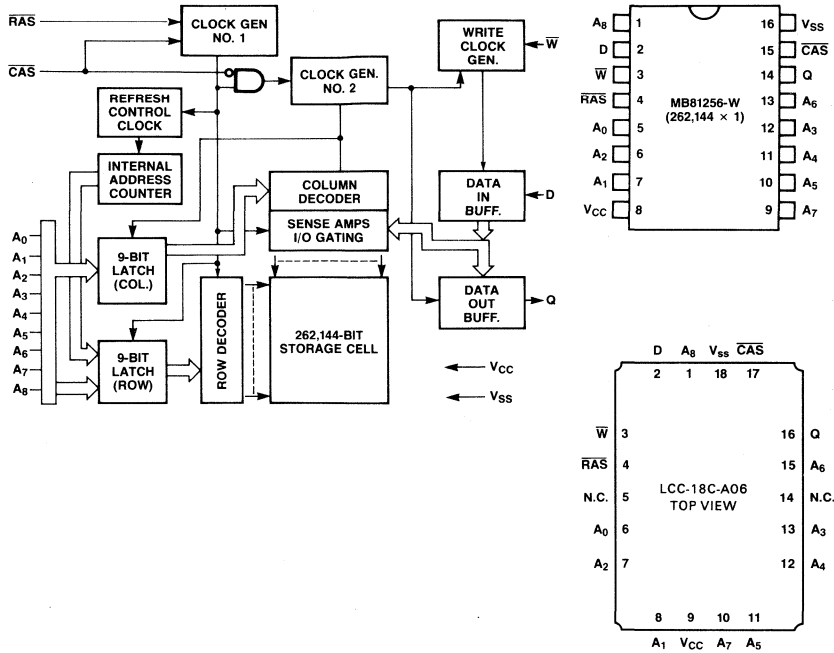
Clock timing requirements are noncritical, and the power supply tolerance is very wide. All inputs are TTL compatible.



Features

- **Wide temperature range: T_C = −55°C to +110°C**
- **262,144 x 1-bit organization**
- **Row Access Time/Cycle Time:**
  MB81256-12-W
  120 ns max./250 ns min.
  MB81256-15-W
  150 ns max./280 ns min.
- **Page cycle time**
  MB81256-12-W 120 ns max.
  MB81256-15-W 150 ns max.
- **Low Power Dissipation:**
  347 mW max. (t_{RC} = 280 ns)
  33 mW (Standby)
- **+5V supply voltage, ±10% tolerance**
- **All inputs TTL compatible, low capacitive load**
- **Three-state TTL compatible output**
- **Common I/O capability using "Early Write" operation**
- **On-chip substrate bias generator**
- **Page Mode Capability**
- **Fast Read-Write Cycle, t_{RWC} = t_{RC}**
- **t_{AR}, t_{WCR}, t_{DHR}, t_{RWD} eliminated**
- **$\overline{CAS}$-before-$\overline{RAS}$ on chip refresh**
- **Hidden $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh**
- **$\overline{RAS}$-only refresh**
- **2 ms/256 cycle refresh**
- **Output unlatched at cycle end allows two dimensional chip select**
- **On-chip Address and Data-in latches**
- **Industry standard 16-pin package**

MB81256 Block Diagram and Pin Assignments



Note: The following IEEE Std. 662-1980 symbols are used in this data sheet: D = Data In, $\overline{W}$ = Write Enable, Q = Data Out.

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}, V_{CC}	−1.0 to 7.0	V
Operating temperature (case)	T_{OP}	−55 to 110	°C
Storage temperature	T_{STG}	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage high than maximum rated voltages to this high impedance circuit.

Description

Simplifed Timing Requirement

The MB81256-W has improved circuitry that eases timing requirements for high speed access operations. The MB81256-W can operate under the condition of t_{RCD} (max) = t_{CAC}, thus providing optimal timing for address multiplexing. In addition, the MB81256-W has minimal hold times for Addresses (t_{CAH}), Write-Enable (t_{WCH}) and Data-in (t_{DH}). The MB81256-W provides higher throughput in inter-leaved memory system applications. Fujitsu has made the timing requirements that are referenced to $\overline{RAS}$ nonrestrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the Column Address, D and $\overline{W}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{W}$ Delay) are not restricted by t_{RCD}.

Fast Read-Write Cycle

The MB81256-W has a fast read-modify-write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{W}$ when $\overline{CAS}$ goes "low". When $\overline{W}$ is "low" during a $\overline{CAS}$ transition to "low", the MB81256-W goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. When $\overline{W}$ goes "low", the MB81256-W goes into the delayed write mode. The output then contains the data from the cell selected and the data from D is written into the cell selected. Therefore, a very fast read-write cycle (t_{RWC} = t_{RC}) is possible with the MB81256-W.

Address Inputs

A total of eighteen binary input address bits are required to decode any 1 of 262,144 cell locations within the MB81256-W. Nine row-address bits are established on the input pins (A_0 through A_8) and are latched with the Row Address Strobe ($\overline{RAS}$). Nine column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All row addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold/time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

Write Enable

The read or write mode is selected with the $\overline{W}$ input. A logic "high" on $\overline{W}$ dictates write mode. The data input is disabled when the read mode is selected.

Data Input

Data is written into the MB81256-W during a write or read-write cycle. The last falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the data-in (D) register. In a write cycle, if $\overline{W}$ is brought "low" (write mode) before $\overline{CAS}$, D is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{W}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D is strobed by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Page Mode

Page mode operation permits strobing the row address into the MB81256-W while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row address doesn't change. Thus, the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

$\overline{RAS}$-Only Refresh

Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses ($A_0 \sim A_7$) at least every 2 ms. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought "low". Strobing each of the 256 row-addresses ($A_0 \sim A_7$) with $\overline{RAS}$ will cause all bits in each row to be refreshed. $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh

$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB81256-W offers an alternate refresh method. If $\overline{CAS}$ is held "low" for the specified period (t_{FCS}) before $\overline{RAS}$ goes to "low", on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Hidden Refresh

A hidden refresh cycle may take place while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time. For the MB81256-W, a hidden refresh cycle is a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The internal refresh address counter provides the refresh addresses as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

Description
(Continued)

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to "high" and then goes to "low" again while $\overline{RAS}$ is held "low", the read and write operation are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 9 row address bits and 9 column address bits defined as follows:

A Row Address

Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set "high" internally.

A Column Address

All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

The timing, as shown in the $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle, is used for all the following operations:

1) Initialize the internal refresh counter. For this operation, 8 cycles are required.
2) Write a test pattern of "low"s into memory cells at a single column address and 256 row address.
3) Using a read-modify-write cycle, read the "low" written at the last operation (Step 2) and write a new "high" in the same cycle. This cycle is repeated 256 times, and "high"s are written into the 256 memory cells.
4) Read the "high"s written at the last operation (Step 3).
5) Complement the test pattern and repeat steps (2), (3) and (4).

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Value Min	Value Typ	Value Max	Unit	Operating Temperature (T_C)
Supply voltage	V_{CC}	4.5	5.0	5.5	V	−55°C to +110°C (case)
	V_{SS}	0	0	0	V	
Input high voltage all inputs	V_{IH}	2.4		6.5	V	
Input low voltage all inputs	V_{IL}	−2.0		0.8	V	

Capacitance
(T_A = 25°C)

Parameter	Symbol	Value Min	Value Typ	Value Max	Unit
Input capacitance A_0 to A_8, D	C_{IN1}			7	pF
Input capacitance $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$	C_{IN2}			10	pF
Output capacitance Q	C_{OUT}			7	pF

DC Characteristics

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81256-12-W Min	MB81256-12-W Max	MB81256-15-W Min	MB81256-15-W Max	Unit
Operating current*1 Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		72		63	mA
Standby current Power supply current ($\overline{RAS}/\overline{CAS}$ = V_{IH})	I_{CC2}		6.0		6.0	mA
Refresh current*1 Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}		61		55	mA
Page mode current*1 Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	I_{CC4}		33		28	mA
Refresh current 2*1 Average power supply current ($\overline{CAS}$ before $\overline{RAS}$, t_{RC} = min.)	I_{CC5}		66		61	mA
Input leakage current Any input, (V_{IN} = 0V to 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)	I_{IL}	−10	10	−10	10	μA
Output leakage current (Data is disabled, V_{OUT} = 0V to 5.5V)	I_{OL}	−10	10	−10	10	μA
Output level Output low voltage (I_{OL} = 4.2 mA)	V_{OL}		0.4		0.4	V
Output level Output high voltage (I_{OH} = −5.0 mA)	V_{OH}	2.4		2.4		V

Note: *1 I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC Characteristics

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol Alternate	Symbol *Standard	MB81256-12-W Min	MB81256-12-W Max	MB81256-15-W Min	MB81256-15-W Max	Unit
Time between refresh	t_{REF}	TRVRV		2		2	ms
Random read/write cycle time	t_{RC}	TRELREL	250		280		ns
Read-write cycle time	t_{RWC}	TRELREL	250		280		ns
Access time from $\overline{RAS}$*4,6	t_{RAC}	TRELQV		120		150	ns
Access time from $\overline{CAS}$*5,6	t_{CAC}	TCELQV		60		75	ns
Output buffer turn off delay	t_{OFF}	TCEHQZ	0	25	0	30	ns
Transition time	t_T	TT	3	50	3	50	ns

Notes: *1 An initial pause of 200μs is required after power up, followed by any 8 $\overline{RAS}$ cycles, before proper device operation is achieved. If the internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh initialization cycles are required.

*2 AC characteristics assume t_T = 5ns.

*3 V_{IH} (min.) and V_{IL} (max.) are reference levels measured between V_{IH} and V_{IL}.

*4 t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$ (max.) the specified maximum value of t_{RAC} (max.) can be met. If $t_{RCD} > t_{RCD}$ (max.) then t_{RAC} is increased by the amount that t_{RCD} exceeds t_{RCD} (max.)

*5 Assumes that $t_{RCD} > t_{RCD}$ (max.).

*6 Measured with a load equivalent to 2 TTL loads and 100 pF.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol Alternate	*Standard	MB81256-12-W Min	MB81256-12-W Max	MB81256-15-W Min	MB81256-15-W Max	Unit
$\overline{RAS}$ precharge time	t_{RP}	TREHREL	120		120		ns
$\overline{RAS}$ pulse width	t_{RAS}	TRELREH	120	10000	150	10000	ns
$\overline{RAS}$ hold time	t_{RSH}	TCELREH	60		75		ns
$\overline{CAS}$ pulse width	t_{CAS}	TCELCEH	60	10000	75	10000	ns
$\overline{CAS}$ hold time	t_{CSH}	TRELCEH	120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ delay time*4,7	t_{RCD}	TRELCEL	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ set up time	t_{CRS}	TCEXREL	20		20		ns
Row address set up time	t_{ASR}	TAVREL	0		0		ns
Row address hold time	t_{RAH}	TRELAX	12		15		ns
Column address set up time	t_{ASC}	TAVCEL	0		0		ns
Column address hold time	t_{CAH}	TCELAX	20		25		ns
Read command set up time	t_{RCS}	TWHCEL	0		0		ns
Read command hold time referenced to $\overline{CAS}$*9	t_{RCH}	TCEHWX	0		0		ns
Read command hold time referenced to $\overline{RAS}$*9	t_{RRH}	TREHWX	20		20		ns
Write command set up time*8	t_{WCS}	TWLCEL	0		0		ns
Write command pulse width	t_{WP}	TWLWH	20		25		ns
Write command hold time	t_{WCH}	TCELWH	20		25		ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	TWLREH	50		60		ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	TWLCEH	50		60		ns
Data in set up time	t_{DS}	TDVCEL	0		0		ns
Data in hold time	t_{DH}	TCELDX	20		25		ns
$\overline{CAS}$ to $\overline{W}$ delay*8	t_{CWD}	TCELWL	20		25		ns
Refresh set up time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCS}	TCELREL	25		30		ns
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCH}	TRELCEX	25		30		ns
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	TREHCEL	20		20		ns
Page mode read/write cycle time	t_{PC}	TCELCEL	120		150		ns
Page mode read-write cycle time	t_{PRWC}	TCEHCEH	120		150		ns
Page mode $\overline{CAS}$ precharge time	t_{CP}	TCEHCEL	50		65		ns
$\overline{CAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CPR}	TCEHCEL	25		30		ns

Notes: *These symbols are described in IEEE STD. 662-1980: IEEE Standard terminology for semiconductor memory.

*4 t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$ (max.) the specified maximum value of t_{RAC} (max.) can be met. If $t_{RCD} > t_{RCD}$ (max.) then t_{RAC} is increased by the amount that t_{RCD} exceeds t_{RCD} (max.)

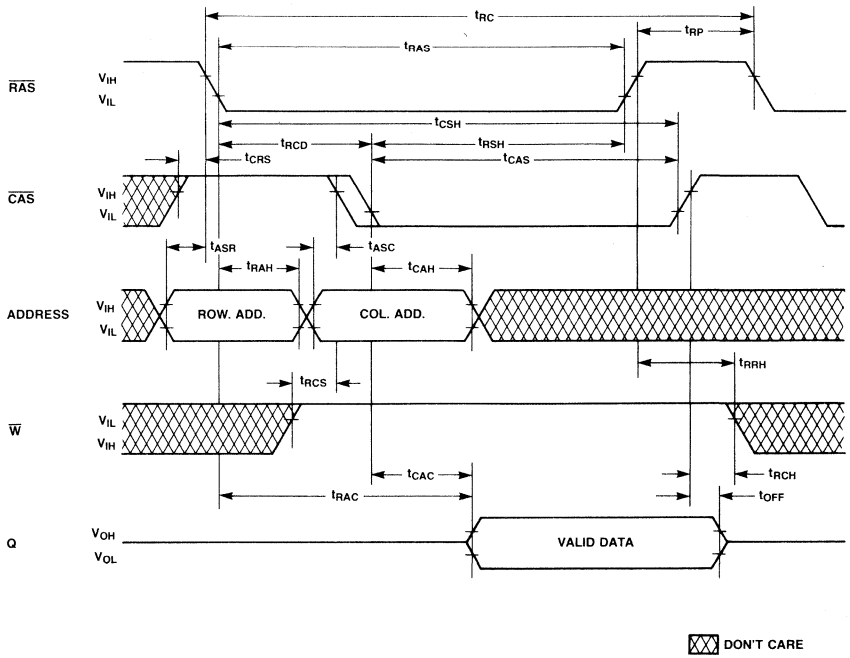
*7 t_{RCD} (min.) = t_{RAH} (min.) + $2t_T$ + t_{ASC} (min.).

*8 t_{WCS} and t_{CWD} are non restrictive operating parameters, and are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle, and the data out pin will remain open circuit (High Impedance) throughout the entire cycle. If $t_{CWD} > t_{CWD}$ (min.), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.

*9 Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

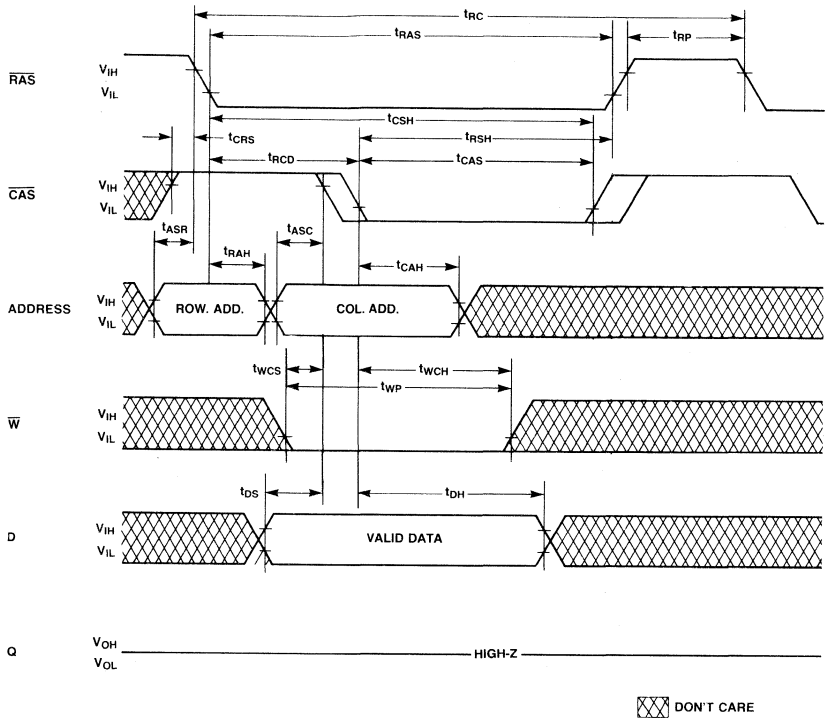
Timing Diagrams

Read Cycle



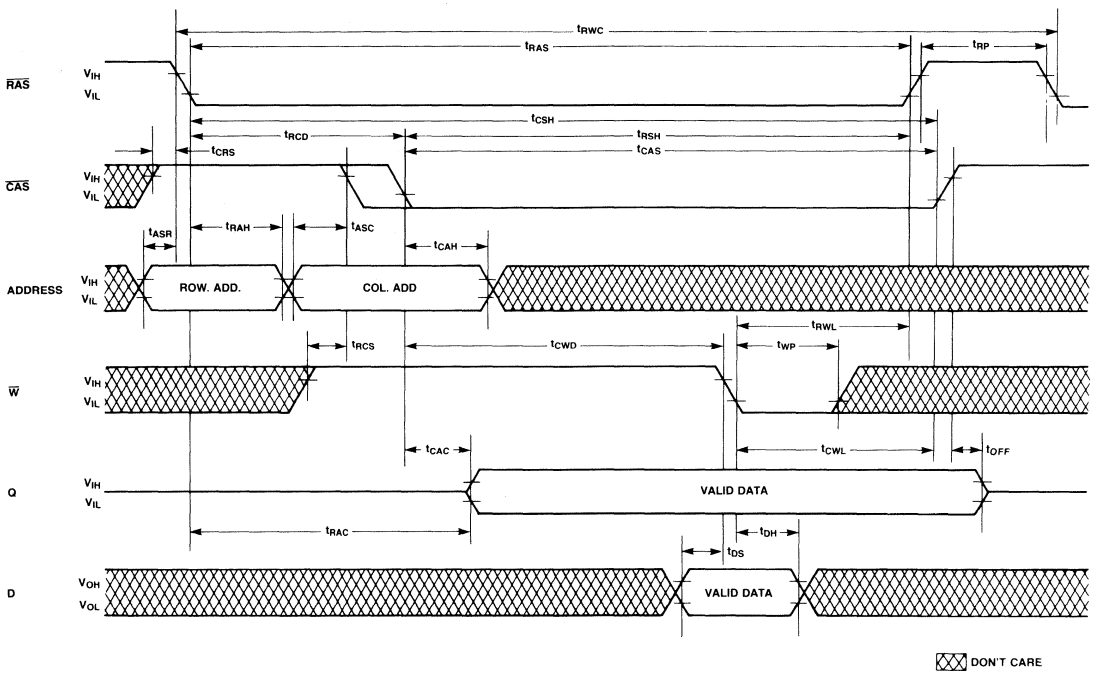
Timing Diagrams
(Continued)

Write Cycle (Early Write)



Timing Diagrams
(Continued)

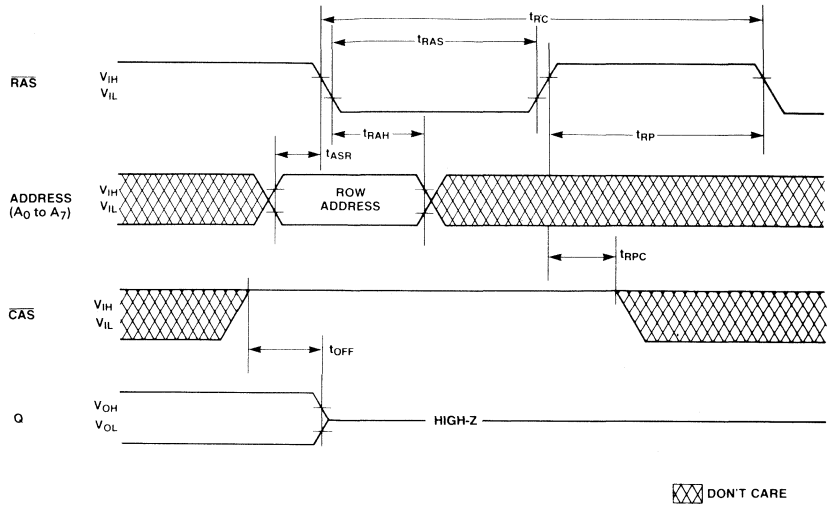
Read-Write/Read-Modify-Write Cycle



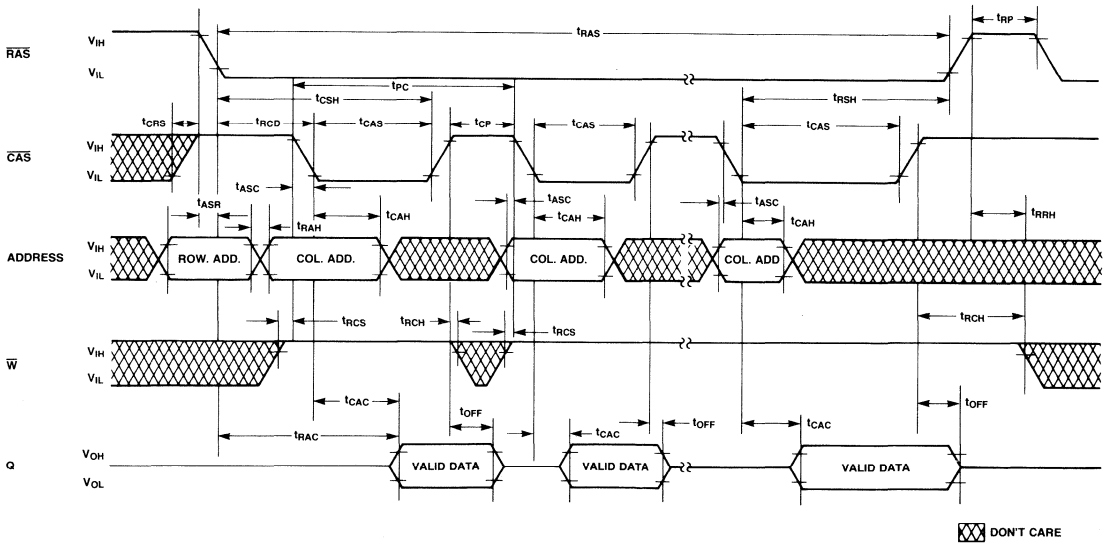
Timing Diagrams
(Continued)

"$\overline{RAS}$-Only" Refresh Cycle

Note: $\overline{CAS}$ = V_{IH}, $\overline{W}$, D = Don't Care, A_8 = V_{IL} or V_{IH}

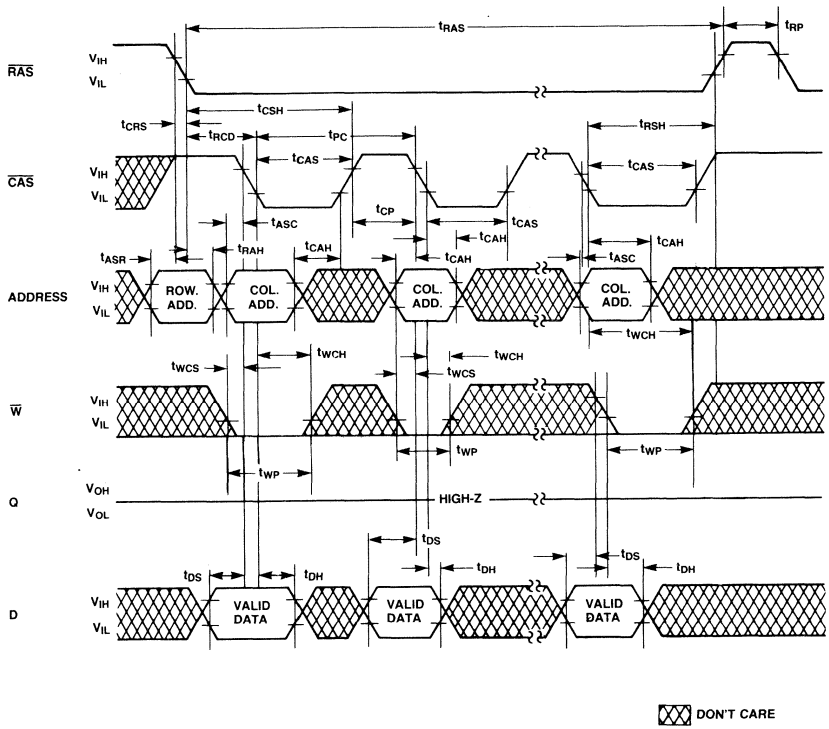


Page Mode Read Cycle



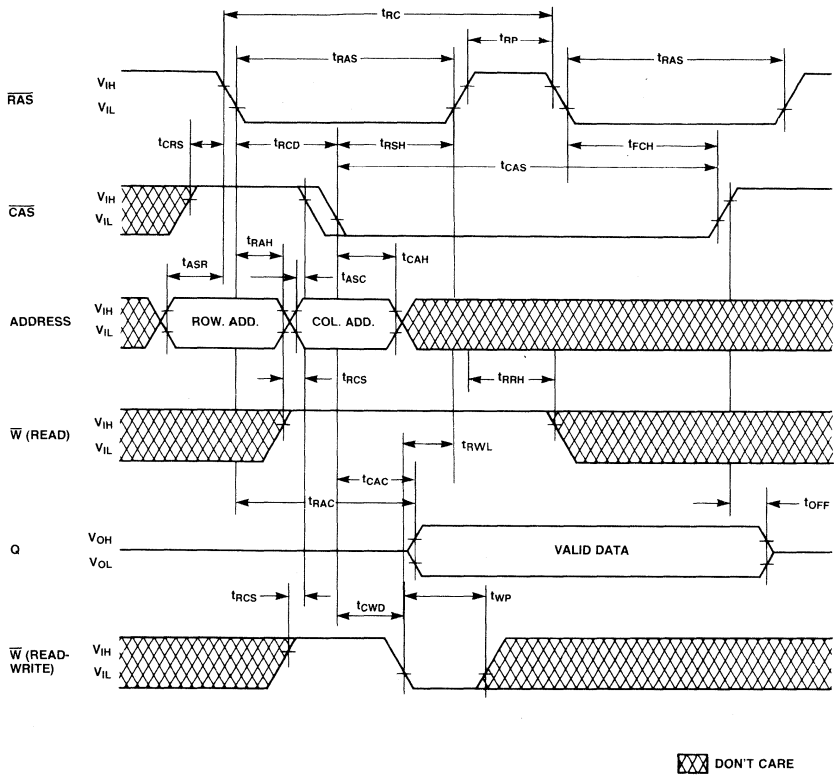
Timing Diagrams
(Continued)

Page Mode Write Cycle



Timing Diagrams
(Continued)

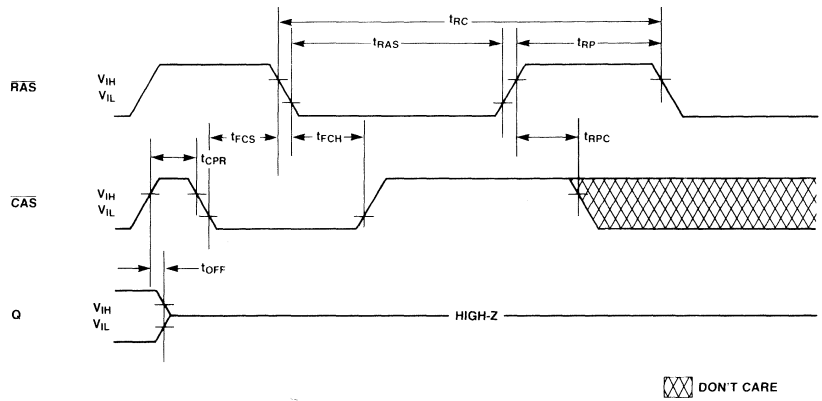
Hidden Refresh Cycle



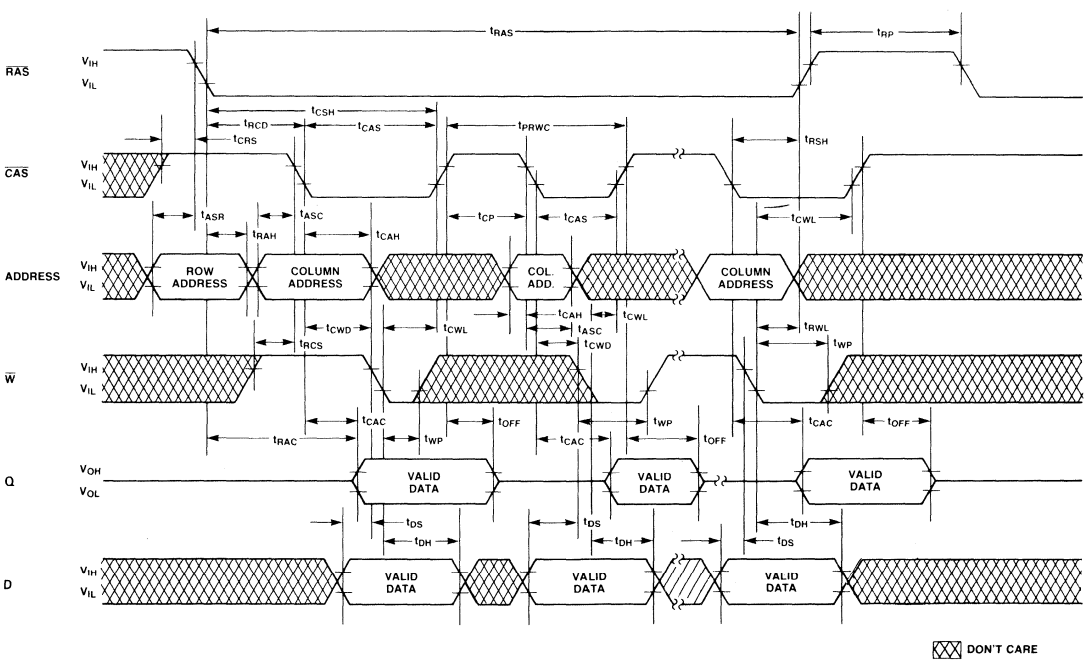
Timing Diagrams
(Continued)

"$\overline{CAS}$-Before-$\overline{RAS}$" Refresh Cycle

Note: A, $\overline{W}$, D = Don't Care

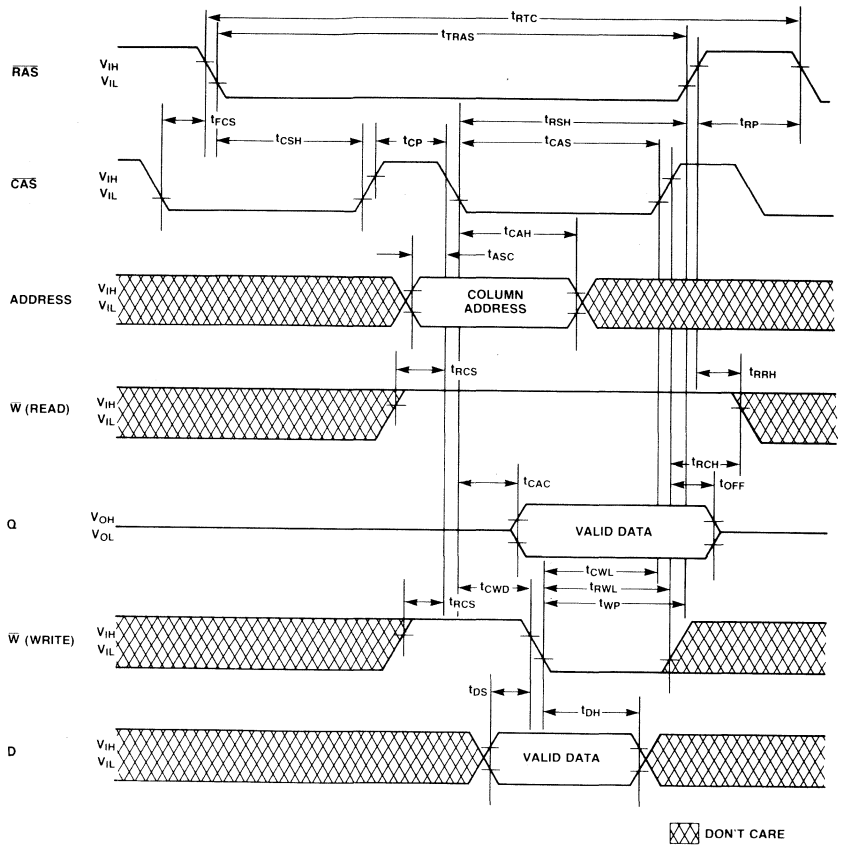


Page Mode Read-Write Cycle



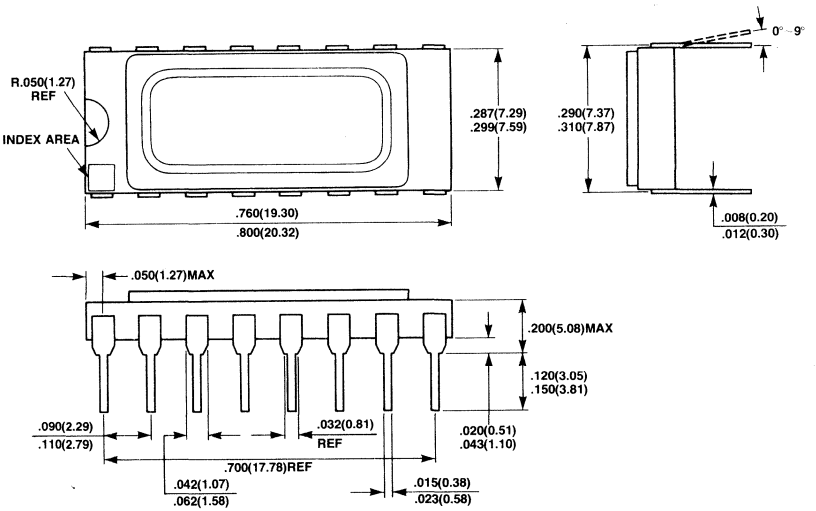
Timing Diagrams
(Continued)

"$\overline{CAS}$-Before-$\overline{RAS}$" Refresh Counter Test Cycle

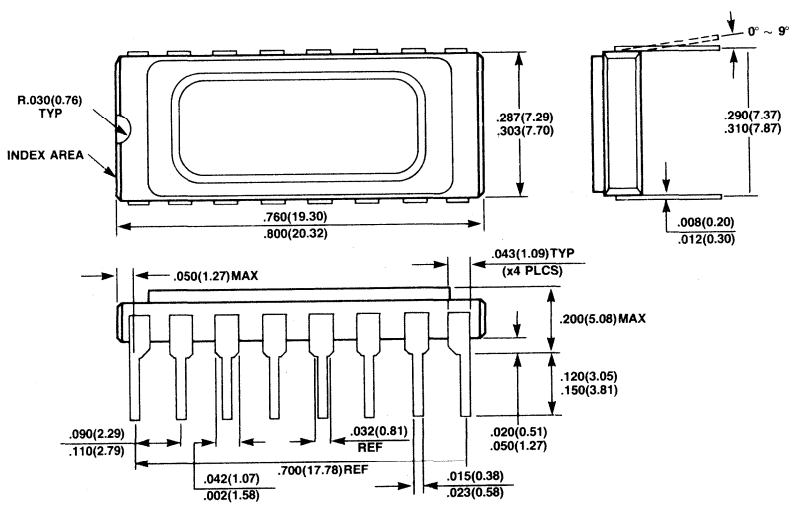


Package Dimensions
Dimensions in inches
(millimeters)

16-Lead Ceramic (Metal Seal) Dual In-Line Package
(Case No.: DIP-16C-A03)

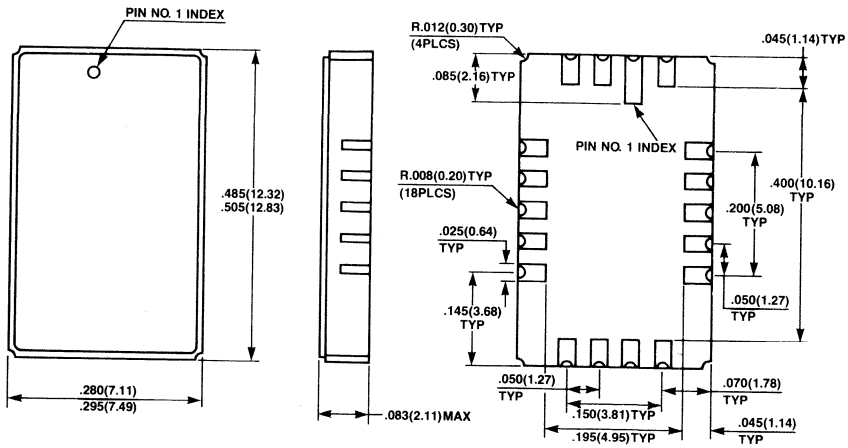


16-Lead Seam Weld Dip Package
(Case No.: DIP-16C-A04)



Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

18-Pad Ceramic Leadless Chip Carrier
LCC-18C-A06)



MB81257-12-W, MB81257-15-W

NMOS 262,144-Bit Dynamic Random Access Memory With Nibble Mode

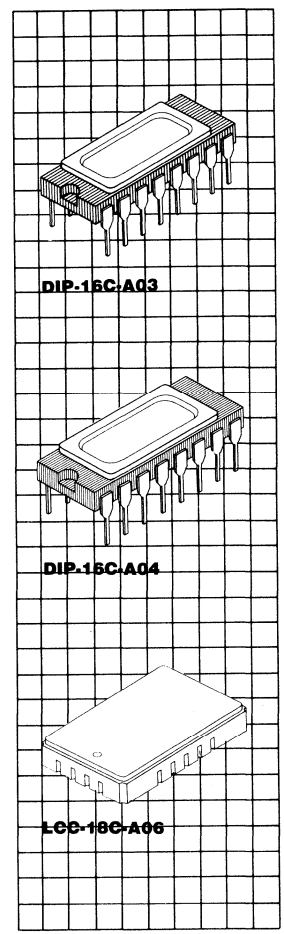
Description

The Fujitsu MB81257-W is a fully decoded, dynamic NMOS random access memory organized as 262,144 one-bit words. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

The MB81257-W features "nibble mode" which allows high speed serial access of up to four bits of data. Additionally, the MB81257-W offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability that is an upward compatible version of the MB8266A. Multiplexed row and column address inputs permit the MB81257-W to be housed in a Jedec standard 16-pin dual in-line package and 18-pad LCC.

The MB81257-W is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-layer Polysilicon process. This process, coupled with single transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is used in the design, including dynamic sense amplifiers.

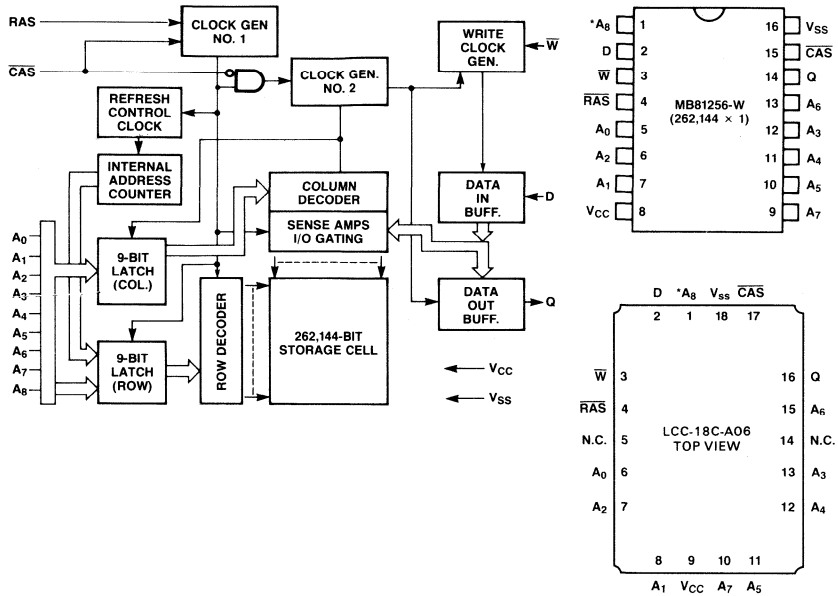
Clock timing requirements are noncritical, and the power supply tolerance is very wide. All inputs are TTL compatible.



Features

- **Wide temperature range: T_C = −55°C to 110°C**
- **262,144 x 1-bit organization**
- **Row Access Time/Cycle Time:**
  MB81257-12-W
  120 ns max./250 ns min.
  MB81257-15-W
  150 ns max./280 ns min.
- **Low Power Dissipation:**
  347 mW max. (t_{RC} = 280 ns)
  33 mW (Standby)
- **Nibble cycle time:**
  MB81257-12-W 65 ns max.
  MB81257-15-W 80 ns max.
- **+5V supply voltage, ±10% tolerance**
- **All inputs TTL compatible, low capacitive load**
- **Three-state TTL compatible output**
- **Common I/O capability using "Early Write" operation**
- **On-chip substrate bias generator**
- **Nibble mode capability for faster access**
- **Fast Read-Write Cycle, t_{RWC} = t_{RC}**
- **t_{AR}, t_{WCR}, t_{DHR}, t_{RWD} eliminated**
- **$\overline{CAS}$-before-$\overline{RAS}$ on chip refresh**
- **Hidden $\overline{CAS}$-before-$\overline{RAS}$ on-chip refresh**
- **$\overline{RAS}$-only refresh**
- **Refresh 2 ms/256 cycle refresh**
- **Output unlatched at cycle end allows two dimensional chip select**
- **On-chip Address and Data-in latches**
- **Industry standard 16-pin package**

MB81257 Block Diagram and Pin Assignments



Note: The following IEEE Std. 662-1980 symbols are used in this data sheet: D = Data In, $\overline{W}$ = Write Enable, Q = Data Out.

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}, V_{CC}	−1.0 to 7.0	V
Operating temperature (case)	T_{OP}	−55 to 110	°C
Storage temperature	T_{STG}	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage high than maximum rated voltages to this high impedance circuit.

Description

Simplified Timing Requirement

The MB81257 has improved circuitry that eases timing requirements for high speed access operations. The MB81257 can operate under the condition of t_{RCD} (max.) = t_{CAC}, thus providing optimal timing for address multiplexing. In addition, the MB81257 has minimal hold times for Addresses (t_{CAH}), Write-Enable (t_{WCH}) and Data-in (t_{DH}). The MB81257 provides higher throughput in interleaved memory system applications. Fujitsu has made the timing requirements that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the Column Address, D and $\overline{W}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{W}$ Delay) are not restricted by t_{RCD}.

Fast Read-Write Cycle

The MB81257 has a fast read-modify-write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{W}$ when $\overline{CAS}$ goes "low". When $\overline{W}$ is "low" during a $\overline{CAS}$ transition to "low", the MB81257 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. When $\overline{W}$ goes "low", after t_{CWD} following a $\overline{CAS}$ transition to "low", the MB81257 goes into the delayed write mode. The output then contains the data from the cell selected and the data from D is written into the cell selected. Therefore, a very fast read-write cycle (t_{RWC} = t_{RC}) is possible with the MB81257.

Address Inputs

A total of eighteen binary input address bits are required to decode any 1 of 262,144 cell locations within the MB81257. Nine row address bits are established on the input pins (A_0 through A_8) and are latched with the Row Address Strobe ($\overline{RAS}$). Nine column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold/Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

Write Enable

The read or write mode is selected with the $\overline{W}$ input. A logic "high" on $\overline{W}$ dictates read mode. A logic "low" dictates write mode. The data input is disabled when the read mode is selected.

Data Input

Data is written into the MB81257 during a write or read-write cycle. The last falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the Data-in (D) register. In a write cycle, if $\overline{W}$ is brought "low" (write mode) before $\overline{CAS}$, D is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{W}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D is strobed by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RAC} from transition of $\overline{RAS}$ when $t_{RCD(max.)}$ is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after $t_{RCD(max.)}$. Data remains valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Nibble Mode

Nibble mode allows high speed serial read, write or read-modify-write access of 2-, 3- or 4-bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 row addresses and the 8 column addresses. The 2-bits of addresses (CA_8, RA_8) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by the normal mode, the remaining nibble bits may be accessed by toggling $\overline{CAS}$ "high" then "low" while $\overline{RAS}$ remains "low". Toggling $\overline{CAS}$ causes RA_8 and CA_8 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. (See table I below).

If more than 4-bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on subsequent access, the new data will be written into the selected cell location.

Nibble Mode Address Sequence Example

SEQUENCE	NIBBLE BIT	RA_8	ROW ADDRESS	CA_8	COLUMN ADDRESS	COMMENTS
$\overline{RAS}$/$\overline{CAS}$ (normal mode)	1	0	10101010	0	10101010	input addresses
toggle $\overline{CAS}$ (nibble mode)	2	1	10101010	0	10101010	
toggle $\overline{CAS}$ (nibble mode)	3	0	10101010	1	10101010	generated internally
toggle $\overline{CAS}$ (nibble mode)	4	1	10101010	1	10101010	
toggle $\overline{CAS}$ (nibble mode)	1	0	10101010	0	10101010	sequence repeats

Description
(Continued)

In nibble mode, the three-state control of the D_{OUT} pin is determined by the first normal access cycle.

The data output is controlled only by the $\overline{W}$ state referenced at the $\overline{CAS}$ negative transition of the normal cycle (first nibble bit). That is, when $t_{WCS} > t_{WCS}$ (min.) is met, the data output will remain open circuit throughout the succeeding nibble cycle regardless of the $\overline{W}$ state. When $t_{CWD} > t_{CWD}$(min.) is met, the data output will contain data from the cell selected during the succeeding nibble cycle regardless of the $\overline{W}$ state. The write operation is done during the period in which the $\overline{W}$ and $\overline{CAS}$ clocks are low. Therefore, the write operation can be performed bit by bit during each nibble operation regardless of the timing conditions of $\overline{W}$ (t_{WCS} and t_{CWD}) during the normal cycle (first nibble bit). (See table II and Figure 2 below).

$\overline{RAS}$-Only Refresh

Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses ($A_0 \sim A_7$) at least every 4 ms. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought "low". Strobing each of the 256 row-addresses ($A_0 \sim A_7$) with $\overline{RAS}$ will cause all bits in each row to be refreshed. $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh

$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB81257 offers an alternate refresh method. If $\overline{CAS}$ is held "low" for the specified period (t_{FCS}) before $\overline{RAS}$ goes to "low", on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Hidden Refresh

A hidden refresh cycle may take place while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time. For the MB81257, a hidden refresh cycle is a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The internal refresh address counter provides the refresh addresses as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to "high" and then goes to "low" again while $\overline{RAS}$ is held "low", the read and write operation are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 9 row address bits and 9 column address bits defined as follows:

A Row Address

Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set "high" internally.

A Column Address

All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of $\overline{CAS}$.

Suggested CAS-before-RAS Refresh Counter Test Procedure

The timing, as shown in the $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle, is used for all the following operations:

1) Initialize the internal refresh counter. For this operation, 8 cycles are required.
2) Write a test pattern of "low"s into memory cells at a single column address and 256 row address.
3) Using a read-modify-write cycle, read the "low" written at the last operation (Step 2) and write a new "high" in the same cycle. This cycle is repeated 256 times, and "high"s are written into the 256 memory cells.
4) Read the "high"s written at the last operation (Step 3).
5) Complement the test pattern and repeat steps 2, 3, and 4.

Functional Truth Table

$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	IN	OUT	Read	Write	Refresh	Note
H	H	Don't Care	Don't Care	High-Z	No	No	No	Standby
L	L	H	Don't Care	Valid Data	Yes	No	Yes	Read
L	L	L	Valid Data	High-Z	No	Yes	Yes	Early Write $t_{WCS} \geq t_{WCS}$ (min.)
L	L	L	Valid Data	Valid Data	Yes	Yes	Yes	Delayed Write or Read-Write $t_{CWD} \geq t_{CWD}$ (min.)
L	H	Don't Care	Don't Care	High-Z	No	No	Yes	$\overline{RAS}$-only Refresh
L	L	Don't Care	Don't Care	Valid Data	No	No	Yes	$\overline{CAS}$-before-$\overline{RAS}$ Refresh. Valid data selected at previous Read or Read-Write cycle is held
H	L	Don't Care	Don't Care	High-Z	No	No	No	$\overline{CAS}$ disturb

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Value Min	Value Typ	Value Max	Unit	Operating Temperature (T_C)
Supply voltage	V_{CC}	4.5	5.0	5.5	V	−55°C to +110°C (case)
	V_{SS}	0	0	0	V	
Input high voltage all inputs	V_{IH}	2.4		6.5	V	
Input low voltage all inputs	V_{IL}	−2.0		0.8	V	

Capacitance
(T_A = 25°C)

Parameter	Symbol	Value Min	Value Typ	Value Max	Unit
Input capacitance A_0 to A_8, D	C_{IN1}			7	pF
Input capacitance $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$	C_{IN2}			10	pF
Output capacitance Q	C_{OUT}			7	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81257-12-W Min	MB81257-12-W Max	MB81257-15-W Min	MB81257-15-W Max	Unit
Operating Current*1 Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		72		63	mA
Standby Current Power supply current ($\overline{RAS}/\overline{CAS}$ = V_{IH})	I_{CC2}		6.0		6.0	mA
Refresh Current 1*1 Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}		61		55	mA
Nibble Mode Current*1 Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{NC} = min.)	I_{CC4}		22		20	mA
Refresh Current 2*1 Average power supply current ($\overline{CAS}$ before $\overline{RAS}$, t_{RC} = min.)	I_{CC5}		66		61	mA
Input Leakage Current Any input, (V_{IN} = 0V to 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)	I_{IL}	−10	10	−10	10	μA
Output Leakage Current (Data is disabled, V_{OUT} = 0V to 5.5V)	I_{OL}	−10	10	−10	10	μA
Output Level Output low voltage (I_{OL} = 4.2 mA)	V_{OL}		0.4		0.4	V
Output Level Output high voltage (I_{OH} = −5.0 mA)	V_{OH}	2.4		2.4		V

Note: *1 I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol Alternate	*Standard	MB81257-12-W Min	MB81257-12-W Max	MB81257-15-W Min	MB81257-15-W Max	Unit
Time between refresh	t_{REF}	TRVRV		2		2	ms
Random read/write cycle time	t_{RC}	TRELREL	250		280		ns
Read-write cycle time	t_{RWC}	TRELREL	250		280		ns
Access time from $\overline{RAS}$*4,6	t_{RAC}	TRELQV		120		150	ns
Access time from $\overline{CAS}$*5,6	t_{CAC}	TCELQV		60		75	ns
Output buffer turn off delay	t_{OFF}	TCEHQZ	0	25	0	30	ns
Transition time	t_T	TT	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	TREHREL	120		120		ns
$\overline{RAS}$ pulse width	t_{RAS}	TRELREH	120	100000	150	100000	ns
$\overline{RAS}$ hold time	t_{RSH}	TCELREH	60		75		ns
$\overline{CAS}$ pulse width	t_{CAS}	TCELCEH	60	100000	75	100000	ns
$\overline{CAS}$ hold time	t_{CSH}	TRELCEH	120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ delay time*4,7	t_{RCD}	TRELCEL	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ set up time	t_{CRS}	TCEHREL	20		20		ns
Row address set up time	t_{ASR}	TAVREL	0		0		ns
Row address hold time	t_{RAH}	TRELAX	12		15		ns
Column address set up time	t_{ASC}	TAVCEL	0		0		ns
Column address hold time	t_{CAH}	TCELAX	20		25		ns
Read command set up time	t_{RCS}	TWHCEL	0		0		ns
Read command hold time referenced to $\overline{CAS}$*10	t_{RCH}	TCEHWX	0		0		ns
Read command hold time referenced to $\overline{RAS}$*10	t_{RRH}	TREHWX	20		20		ns
Write command set up time*8	t_{WCS}	TWLCEL	0		0		ns
Write command pulse width	t_{WP}	TWLWH	20		25		ns
Write command hold time	t_{WCH}	TCELWH	20		25		ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	TWLREH	50		60		ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	TWLCEH	30		40		ns

Notes:
- * These symbols are described in IEEE STD. 662-1980: IEEE Standard terminology for semiconductor memory.
- *1 An initial pause of 200 μs is required after power up, followed by any 8 $\overline{RAS}$ cycles, before proper device operation is achieved. If the internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh initialization cycles are required.
- *2 AC characteristics assume t_T = 5 ns.
- *3 V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
- *4 t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$ (max.) the specified maximum value of t_{RAC} (max.) can be met. If $t_{RCD} > t_{RCD}$ (max.) then t_{RAC} is increased by the amount that t_{RCD} exceeds t_{RCD} (max.).
- *5 Assumes that $t_{RCD} > t_{RCD}$ (max.)
- *6 Measured with a load equivalent to 2 TTL loads and 100 pF.
- *7 t_{RCD} (min.) = t_{RAH} (min.) + $2t_T$ + t_{ASC} (min.).
- *8 t_{WCS} and t_{CWD} are non restrictive operating parameters, and are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle, and the data out pin will remain open circuit (High Impedance) throughout the entire cycle. If $t_{CWD} > t_{CWD}$ (min.), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.
- *10 Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol Alternate	*Standard	MB81257-12-W Min	MB81257-12-W Max	MB81257-15-W Min	MB81257-15-W Max	Unit
Data in set up time	t_{DS}	TDVCEL	0		0		ns
Data in hold time	t_{DH}	TCELDX	20		25		ns
$\overline{CAS}$ to $\overline{W}$ delay*8	t_{CWD}	TCELWL	20		25		ns
Refresh set up time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCS}	TCELREL	25		30		ns
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCH}	TRELCEX	25		30		ns
Nibble mode read-write cycle time	t_{NRWC}	TCEHCEH	65		80		ns
Nibble mode read/write cycle time	t_{NC}	TCEHCEH	65		80		ns
Nibble mode access time	t_{NCAC}	TCELQV		30		40	ns
Nibble mode $\overline{CAS}$ pulse width	t_{NCAS}	TCELCEH	30		40		ns
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	TCEHCEL	25		30		ns
Nibble mode read $\overline{RAS}$ hold time	t_{NRRSH}	TCELREH	30		40		ns
Nibble mode $\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{RNH}	TREHCEL	20		20		ns
Nibble mode write $\overline{RAS}$ hold time	t_{NWRSH}	TCELREH	50		60		ns
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	TREHCEL	20		20		ns
$\overline{CAS}$ precharge time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CPR}	TCEHCEL	25		30		ns

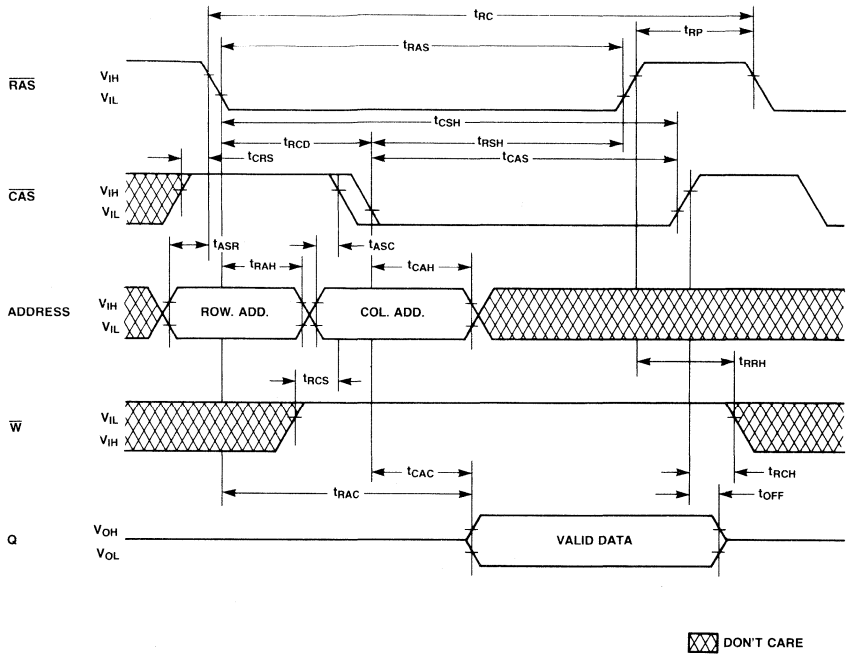
Notes: * These symbols are described in IEEE STD. 662-1980: IEEE Standard terminology for semiconductor memory.

*8 t_{WCS} and t_{CWD} are non restrictive operating parameters, and are included in the data sheet as electrical characteristics only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is an early write cycle, and the data out pin will remain open circuit (High Impedance) throughout the entire cycle. If $t_{CWD} > t_{CWD}$ (min.), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.

*9 Test mode cycle only.

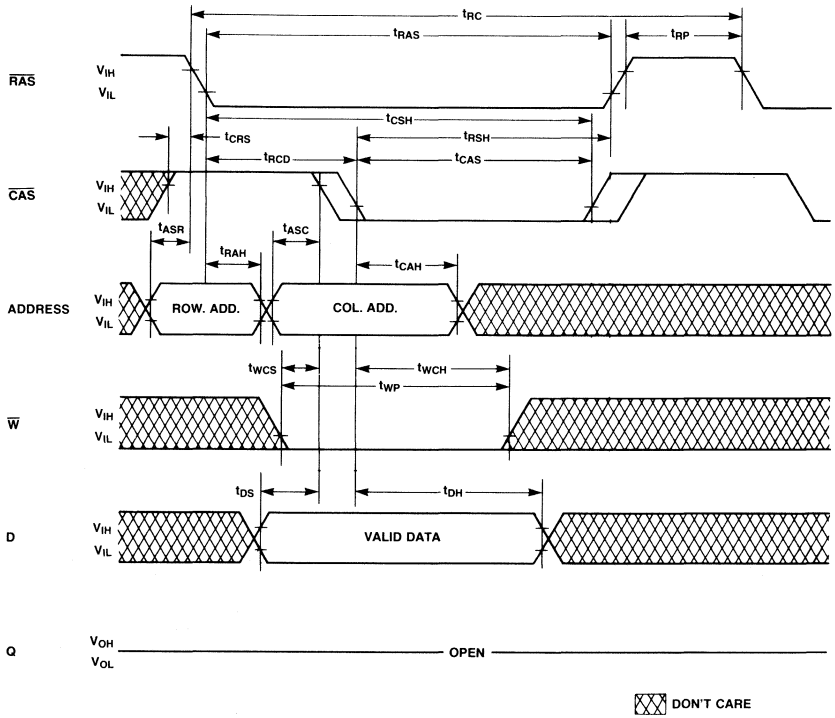
Timing Diagrams

Read Cycle



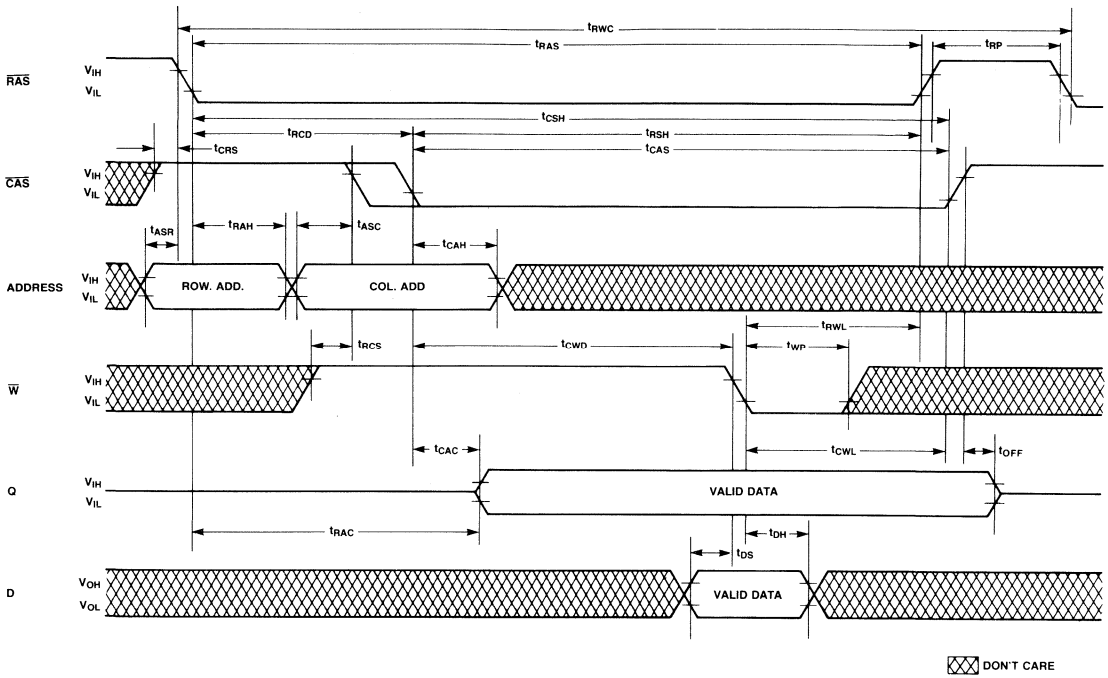
Timing Diagrams
(Continued)

Write Cycle (Early Write)



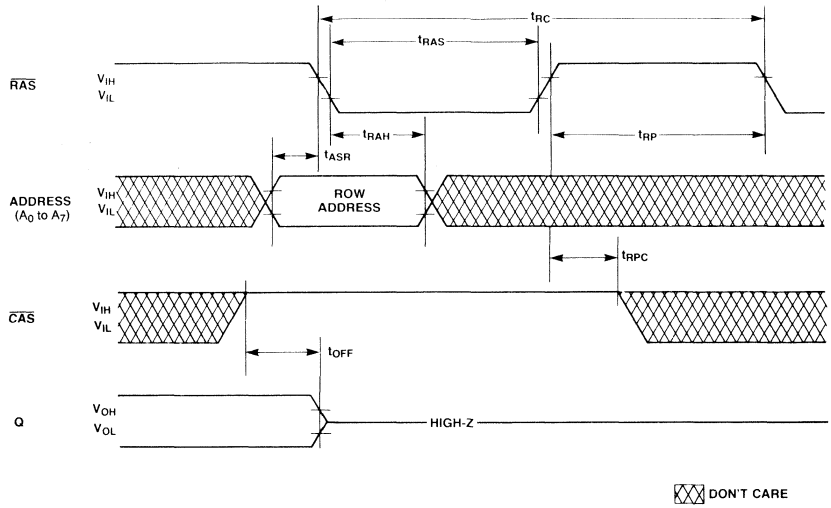
Timing Diagrams
(Continued)

Read-Write/Read-Modify-Write Cycle

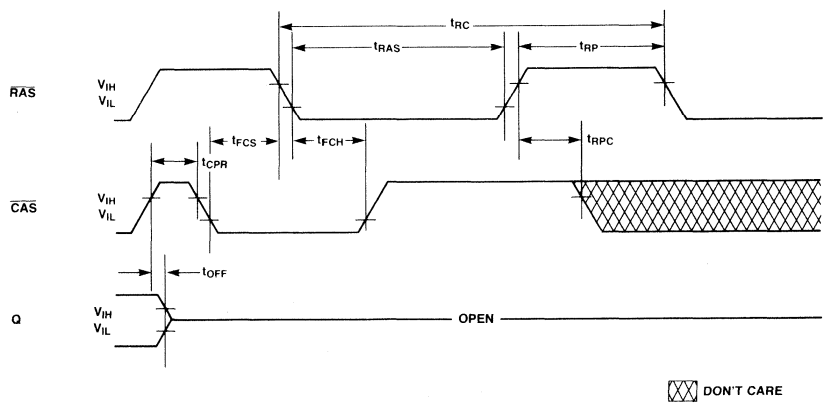


Timing Diagrams
(Continued)

"$\overline{RAS}$-Only" Refresh Cycle
Note: $\overline{W}$, D = Don't Care, $V_8 = V_{IH}$ or V_{IL}

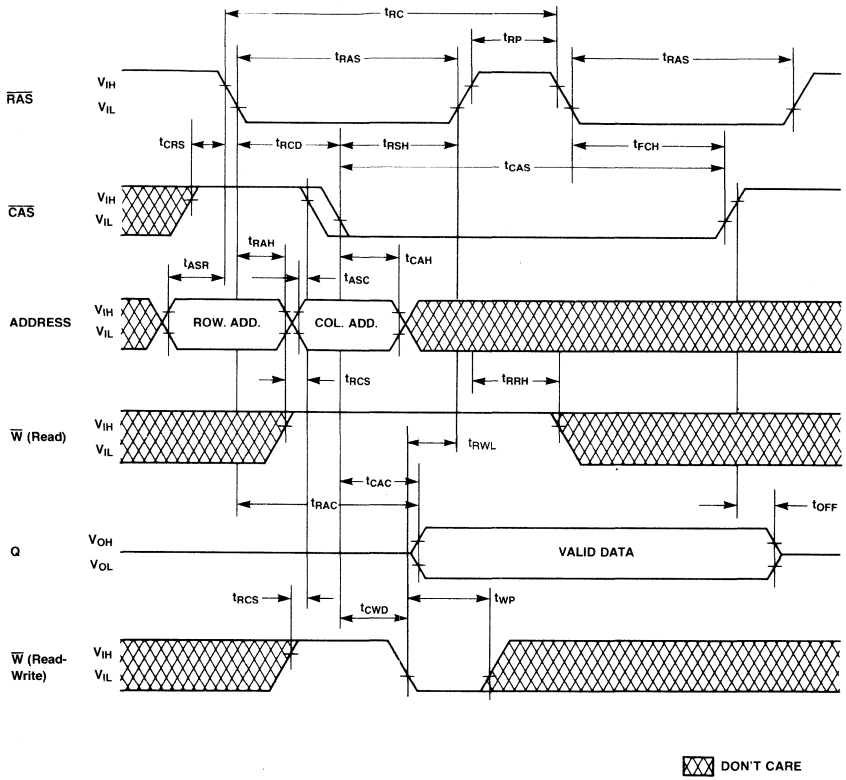


"$\overline{CAS}$-Before-$\overline{RAS}$" Refresh Cycle
Note: Address, $\overline{W}$, D = Don't Care



Timing Diagrams
(Continued)

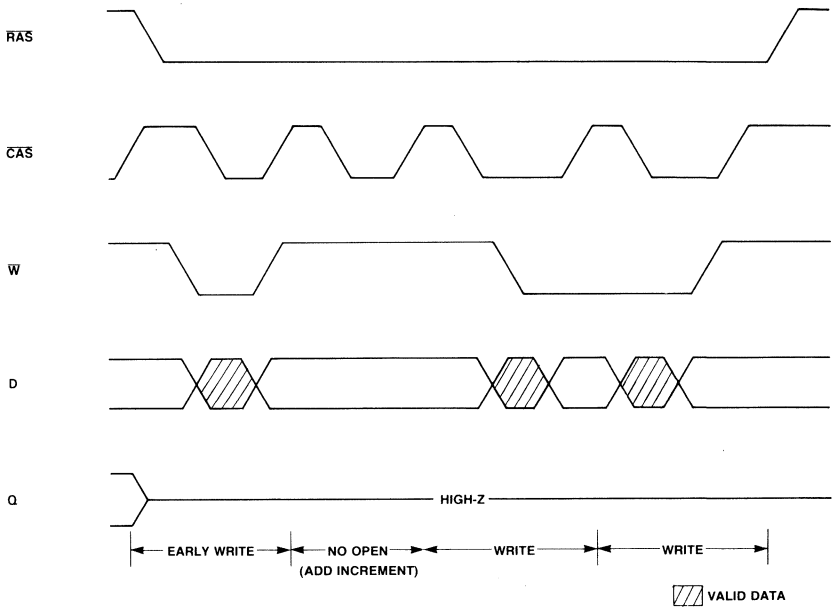
Hidden Refresh Cycle



Timing Diagrams
(Continued)

Nibble Mode

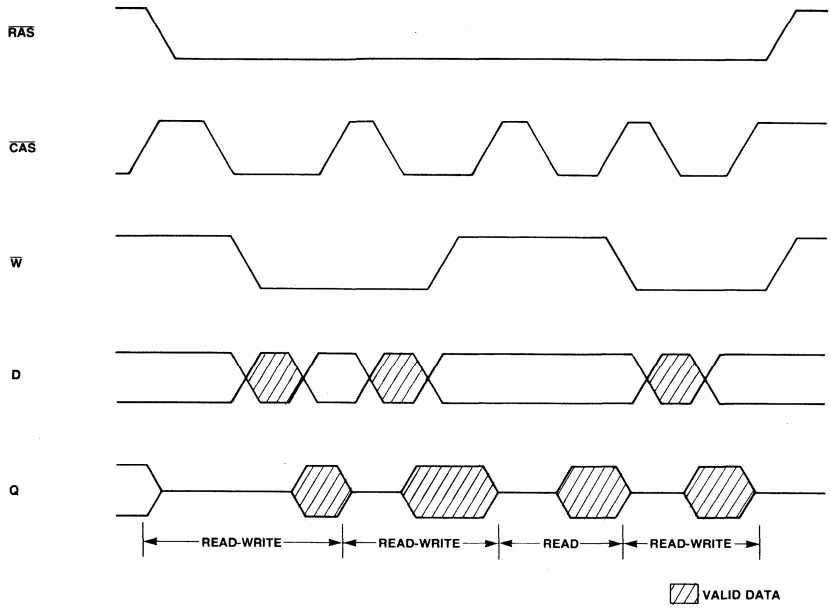
*1 THE CASE OF FIRST NIBBLE CYCLE IS EARLY WRITE



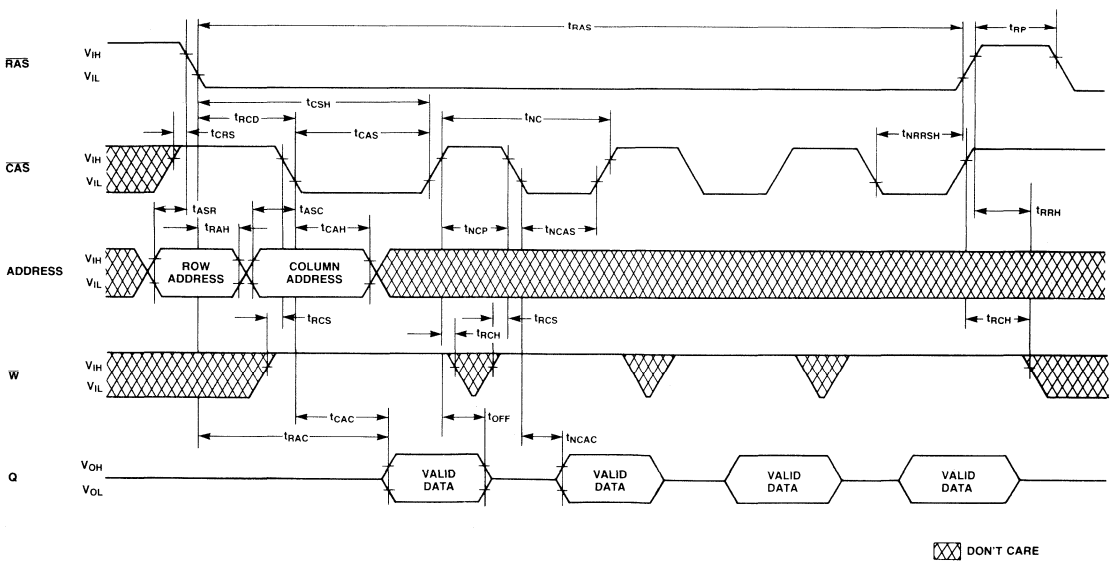
Timing Diagrams
(Continued)

Nibble Mode

*2 THE CASE OF FIRST NIBBLE CYCLE IS DELAYED WRITE (READ-WRITE)

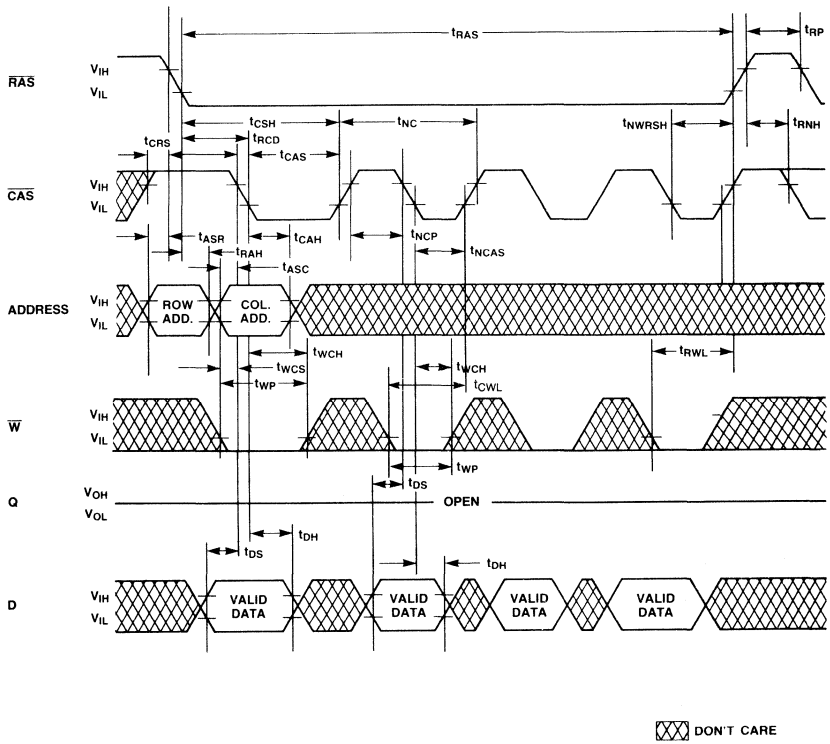


Nibble Mode Read Cycle



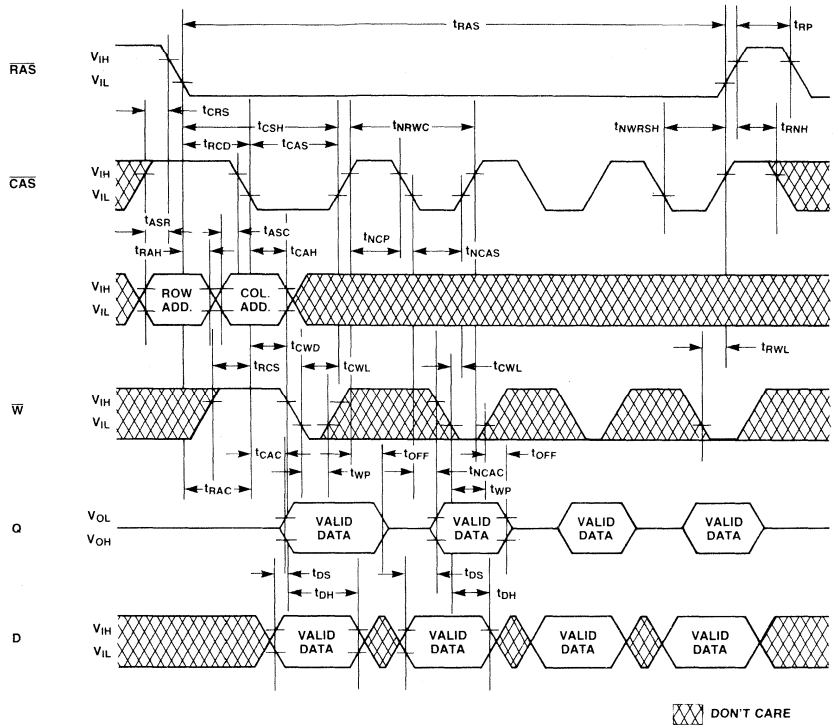
Timing Diagrams
(Continued)

Nibble Mode Write Cycle



Timing Diagrams
(Continued)

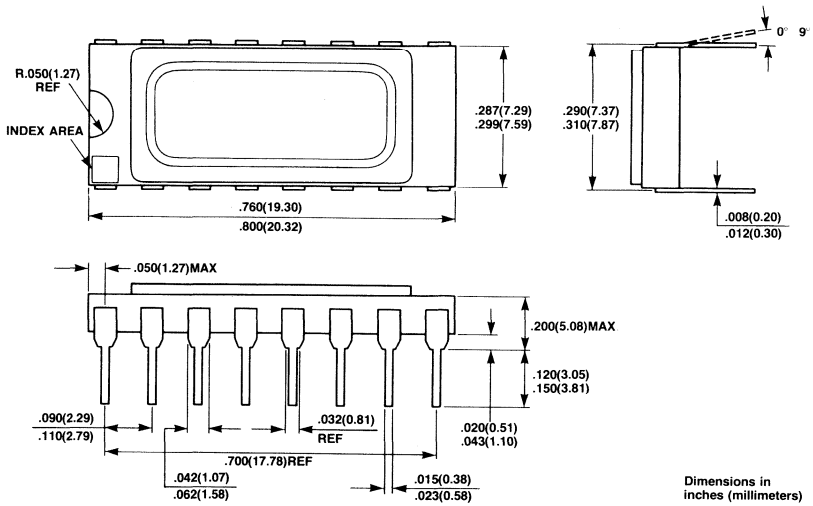
Nibble Mode Read-Write Cycle



Package Dimensions

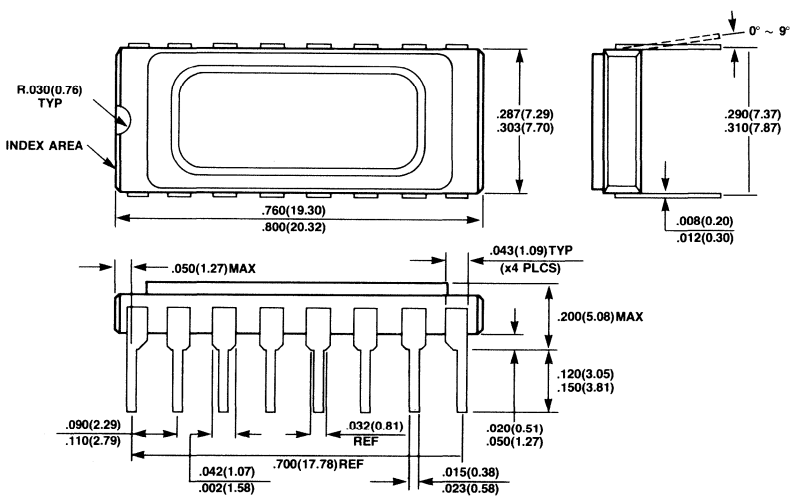
Dimension in inches
(millimeters)

16-Lead Ceramic (Metal Seal) Dual In-Line Package (Case No.: DIP-16C-A03)



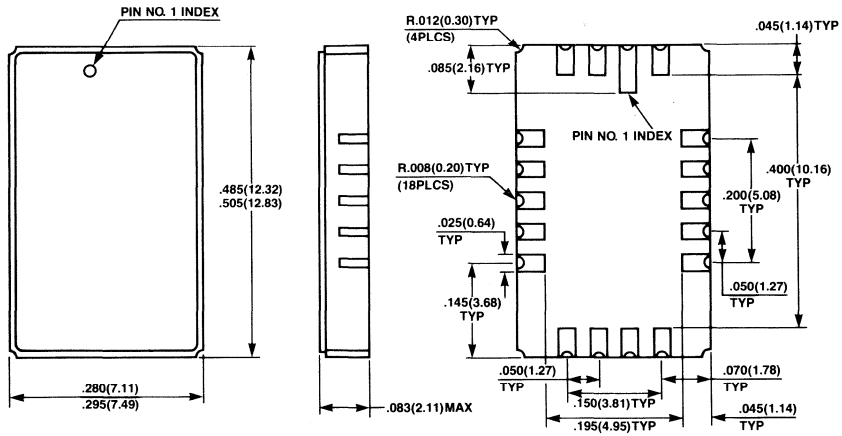
Dimensions in inches (millimeters)

16-Lead Seam Weld DIP Package (Case No.: DIP-16C-A04)



Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

18-Pad Ceramic Leadless Chip Carrier
LCC-18C-A06



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

■ MB81416-10, MB81416-12, MB81416-15

NMOS 65,536-Bit Dynamic Random Access Memory

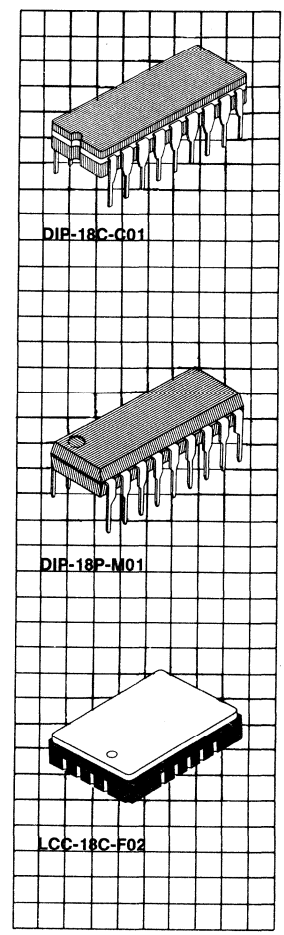
Description

The Fujitsu MB81416 is a fully decoded, dynamic NMOS random access memory organized as 16384 words by 4-bits. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

Multiplexed row and column address inputs permit the MB81416 to be housed in a standard 18-pin DIP that is compatible with the JEDEC approved pinout. Greater refresh versatility is provided by a new $\overline{CAS}$ before $\overline{RAS}$ on-chip refresh capability. The MB81416 also features "page mode" which allows high speed random access of up to 64 nibble wide words within the same row address.

The MB81416 is fabricated using silicon gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are non-critical, and the power supply tolerance is very wide. All inputs and outputs are TTL compatible.

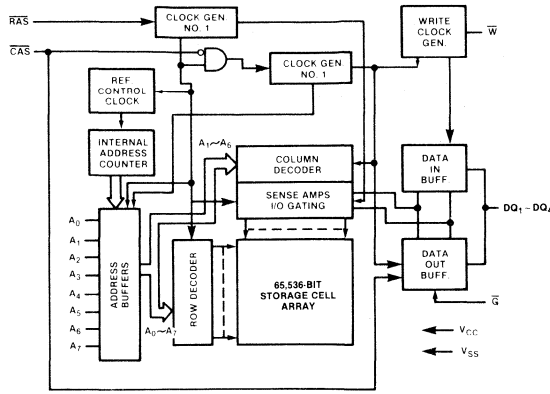


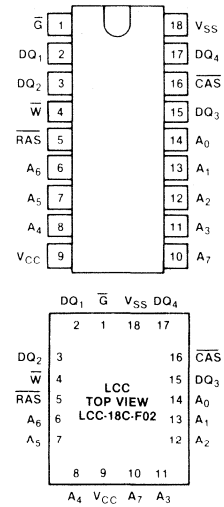
Features

- Organized as 16384 words by 4-bits
- Row Access Time/Cycle Time:
  MB81416-10 100nsec max/200 min.
  MB81416-12 120nsec max/230 min.
  MB81416-15 150nsec max/260 min.
- Low Active Power (t_{RC} = min)
  MB81416-10 303mW (max.)
  MB81416-12 275mW (max.)
  MB81416-15 248mW (max.)
  All devices 25mW standby
- Single +5V ±10% Power Supply
- $\overline{CAS}$ before $\overline{RAS}$ Refresh
- $\overline{RAS}$ Only Refresh
- Hidden $\overline{CAS}$ before $\overline{RAS}$ Refresh
- 2ms/128 cycle Refresh ($A_0 \sim A_6$)
- Read-Modify-Write Capability
- Page Mode Capability for faster access
- Output unlatched at cycle end
- Early Write or Output Enable controls output buffer impedance
- On Chip Address and Data-In latches
- Standard 18-pin DIP
- All Inputs TTL Compatible, low capacitive load
- Three-State TTL Compatible Outputs
- On-chip Substrate Bias Generator

NOTE: The following IEEE Std. 662-1980 Symbols are used in this data sheet: DQ = Data I/O, $\overline{G}$ = Output Enable and $\overline{W}$ = Write Enable.

MB81416 Block Diagram and Pin Configurations





Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	−1 to +7	V
Storage Temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	
Power Dissipation		P_D	1.0	W
Short Circuit Output Current		—	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Capacitance
($T_A = 25\,°C$)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance $A_0 \sim A_7$,	C_{IN1}	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{G}$	C_{IN2}	—	8	pF
Output Capacitance $DQ_1 \sim DQ_4$	C_D	—	7	pF

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs except DQ	V_{IL}	−2.0	—	0.8	V	
Input Low Voltage, DQ	V_{ILD}*	−1.0	—	0.8	V	

*The device will withstand undershoots to the −2.0V level with a maximum pulse width the 20ns at the −1.5V level.

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
OPERATING CURRENT*	MB81416-10			55	
Average power supply current	MB81416-12	I_{CC1}		50	mA
($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB81416-15			45	
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}		4.5	mA
REFRESH CURRENT1*	MB81416-10			38	
Average power supply current	MB81416-12	I_{CC3}		35	mA
($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	MB81416-15			32	
PAGE MODE CURRENT	MB81416-10			38	
Average power supply current	MB81416-12	I_{CC4}		35	mA
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min)	MB81416-15			32	
REFRESH CURRENT 2*	MB81416-10			42	
Average power supply current	MB81416-12	I_{CC5}		38	mA
($\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$)	MB81416-15			35	
INPUT LEAKAGE CURRENT Input leakage current, any input ($0 \leq V_{IN} \leq 5.5V$, $V_{CC} = 5.5V$, $V_{SS} = 0V$, all other pins not under test = 0V)		I_{IL}	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)		I_{OL}	−10	10	μA
OUTPUT LEVELS					
Output high voltage (I_{OH} = −5mA)		V_{OH}	2.4		
Output low voltage (I_{OL} = 4.2mA)		V_{OL}		0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is dependent on input low voltage level V_{ILD}, $V_{ILD} > -0.5V$.

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol Alternate	*Standard	MB81416-10 Min	MB81416-10 Max	MB81416-12 Min	MB81416-12 Max	MB81416-15 Min	MB81416-15 Max	Unit
Time between Refresh		t_{REF}	TRVRV	—	2	—	2	—	2	ms
Random Read/Write Cycle Time		t_{RC}	TRELREL	200	—	230	—	260	—	ns
Read-Write Cycle Time		t_{RWC}	TRELREL	290	—	330	—	375	—	ns
Access Time from $\overline{RAS}$	(4), (6)	t_{RAC}	TRELQV	—	100	—	120	—	150	ns
Access Time from $\overline{CAS}$	(5), (6)	t_{CAC}	TCELQV	—	50	—	60	—	75	ns
Output Buffer Turn Off Delay		t_{OFF}	TCEHQZ	0	30	0	35	0	40	ns
Transition Time		t_T	TT	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	TREHREL	90	—	100	—	100	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	TRELREH	100	10000	120	10000	150	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	TCELREH	50	—	60	—	75	—	ns
$\overline{CAS}$ Precharge Time (Page Mode only)		t_{CP}	TCEHCEL	45	—	50	—	60	—	ns
$\overline{CAS}$ Precharge Time (All cycles except page mode)		t_{CPN}	TCEHCEL	40	—	45	—	55	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	TCELCEH	50	10000	60	10000	75	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	TRELCEH	100	—	120	—	150	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	(4), (7)	t_{RCD}	TRELCEL	20	50	20	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	TCEHREL	20	—	25	—	30	—	ns
Row Address Set Up Time		t_{ASR}	TAVREL	0	—	0	—	0	—	ns
Row Address Hold Time		t_{RAH}	TRELAX	10	—	10	—	15	—	ns
Column Address Set Up Time		t_{ASC}	TAVCEL	0	—	0	—	0	—	ns
Column Address Hold Time		t_{CAH}	TCELAX	15	—	15	—	20	—	ns
Read Command Set Up Time		t_{RCS}	TWHCEL	0	—	0	—	0	—	ns
Read Command Hold Time Referenced to $\overline{RAS}$	(9)	t_{RRH}	TREHWX	20	—	20	—	20	—	ns
Read Command Hold Time Referenced to $\overline{CAS}$	(9)	t_{RCH}	TCEHWX	0	—	0	—	0	—	ns
Write Command Set Up Time		t_{WCS}	TWLCEL	−5	—	−5	—	−5	—	ns
Write Command Hold Time		t_{WCH}	TCELWH	20	—	25	—	30	—	ns
Write Command Pulse Width		t_{WP}	TWLWH	20	—	25	—	30	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	TWLREH	45	—	50	—	60	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	TWLCEH	45	—	50	—	60	—	ns
Data In Set Up Time		t_{DS}	TDVCEL	0	—	0	—	0	—	ns
Data In Hold Time		t_{DH}	TCELDX	20	—	25	—	30	—	ns
$\overline{CAS}$ to $\overline{W}$ Delay	(8)	t_{CWD}	TCELWL	85	—	100	—	120	—	ns
$\overline{RAS}$ to $\overline{W}$ Delay	(8)	t_{RWD}	TRELWL	135	—	160	—	195	—	ns
Access Time from $\overline{G}$		t_{OEA}	TGLQV	—	25	—	30	—	40	ns
$\overline{G}$ to Data in Delay Time		t_{OED}	TGHDV	30	—	35	—	40	—	ns
$\overline{G}$ Hold Time Referenced to $\overline{W}$		t_{OEH}	TWLGL	0	—	0	—	0	—	ns
Output Buffer Turn Off Delay from $\overline{G}$		t_{OEZ}	TGHQZ	0	30	0	35	0	40	ns
Page Mode Cycle Time		t_{PC}	TCELCEL	105	—	120	—	145	—	ns
Page Mode Read-Write Cycle Time		t_{PRWC}	TCEHCEH	180	—	205	—	240	—	ns
$\overline{CAS}$ Set Up Time Referenced to $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		t_{FCS}	TCELREL	20	—	25	—	30	—	ns
$\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		t_{FCH}	TRELCEH	20	—	25	—	30	—	ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time		t_{RPC}	TREHCEL	20	—	20	—	20	—	ns
Refresh Counter Test $\overline{RAS}$ Pulse Width	(10)	t_{TRAS}	TRELREH	280	—	325	—	390	—	ns
Refresh Counter Test Cycle Time	(10)	t_{RTC}	TRELREL	380	—	435	—	500	—	ns
$\overline{G}$ to $\overline{RAS}$ Inactive Setup Time		t_{OES}	TGLREH	0	—	0	—	0	—	ns
Data in to $\overline{CAS}$ Delay Time	(11)	t_{DZC}	TDXCEL	0	—	0	—	0	—	ns
Data in to $\overline{G}$ Delay Time	(11)	t_{DZO}	TDXGL	0	—	0	—	0	—	ns
$\overline{CAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ cycle)		t_{CPR}	TCEHCEL	25	—	30	—	30	—	ns

Notes: See notes on next page.

*These symbols are described in IEEE Std. 662-1980: IEEE Standard Terminology for Semiconductor Memory.

AC Characteristics
(Continued)

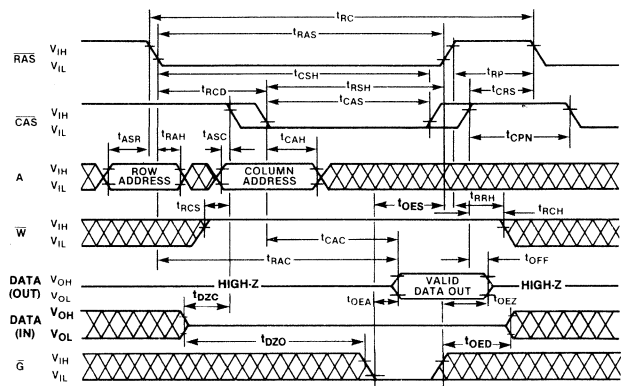
Notes:

1. An initial pause of 200μs is required after power up, followed by any 8 $\overline{RAS}$ cycles, before proper operation is achieved. If the internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC measurements assume t_T = 5ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min.) and V_{IL} (max.).
4. t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$ (max.) the specified maximum value of t_{RAC} (max.) can be met. If $t_{RCD} > t_{RCD}$ (max.) then t_{RAC} is increased by the amount that t_{RCD} exceeds t_{RCD} (max.).
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max.).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. t_{RCD} (min.) = t_{RAH} (min.) + $2t_T$ + t_{ASC} (min.): t_T = 5ns.
8. t_{WCS}, t_{CWD} and t_{RWD} are non-restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.

   If $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. Refresh counter test cycle only.
11. Either t_{DZC} or t_{DZO} must be satisfied for all cycles.

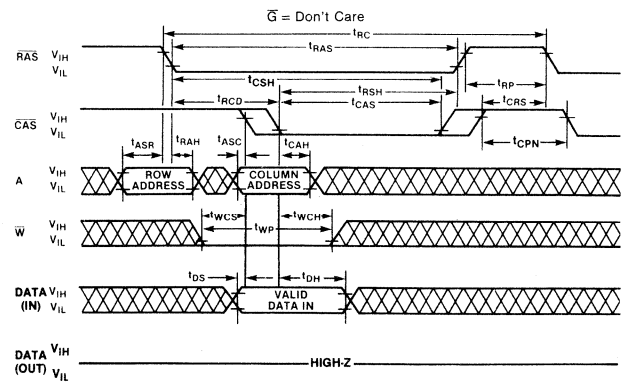
Timing Diagrams

Read Cycle



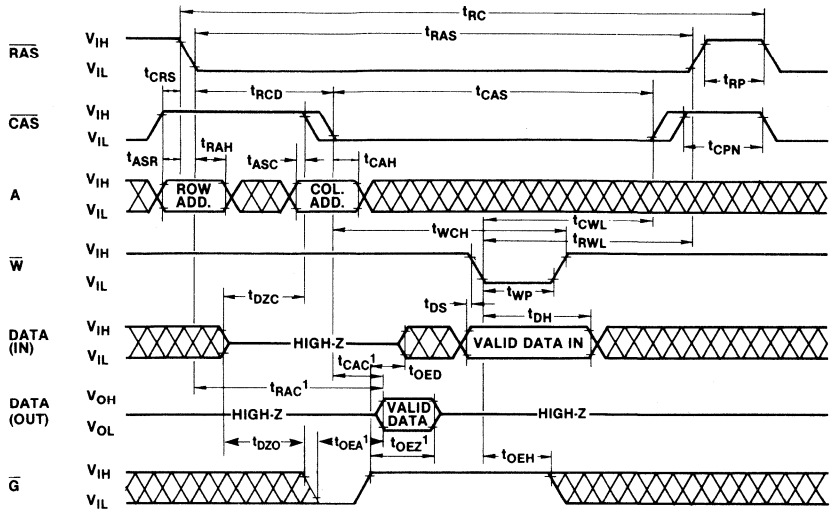
Write Cycle (Early Write)

$\overline{G}$ = Don't Care



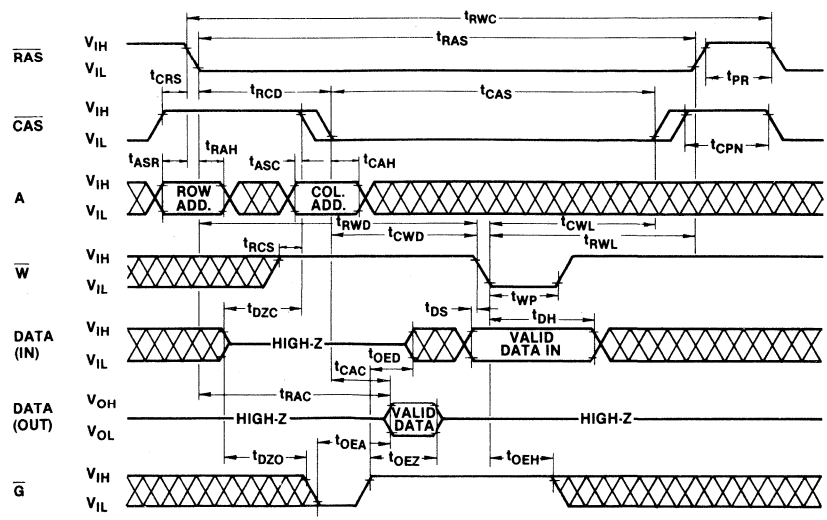
Timing Diagrams
(Continued)

Write Cycle
(Output Enable Controlled)



Note 1: When t_{CWD} is satisfied and $\overline{G}$ is low (Delayed-Write Cycle), the data out will be "VALID". But when t_{CWD} is not satisfied, the data out will be "INVALID".

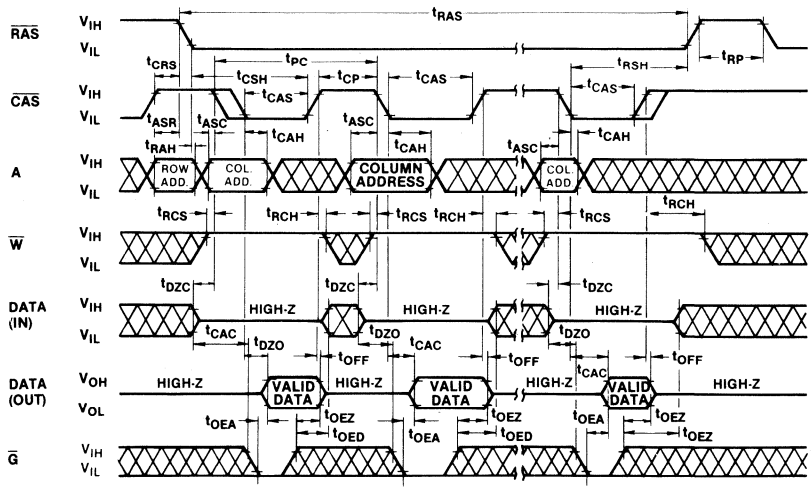
Read-Write/Read-Modify-Write Cycle



Don't Care

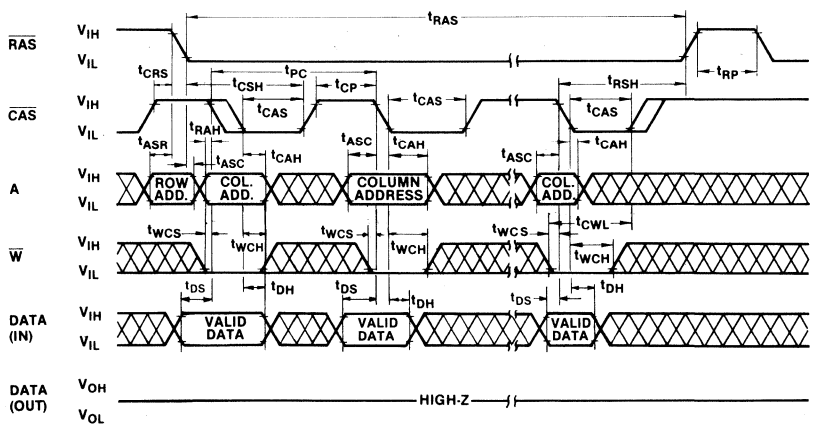
Timing Diagrams
(Continued)

Page Mode Read Cycle



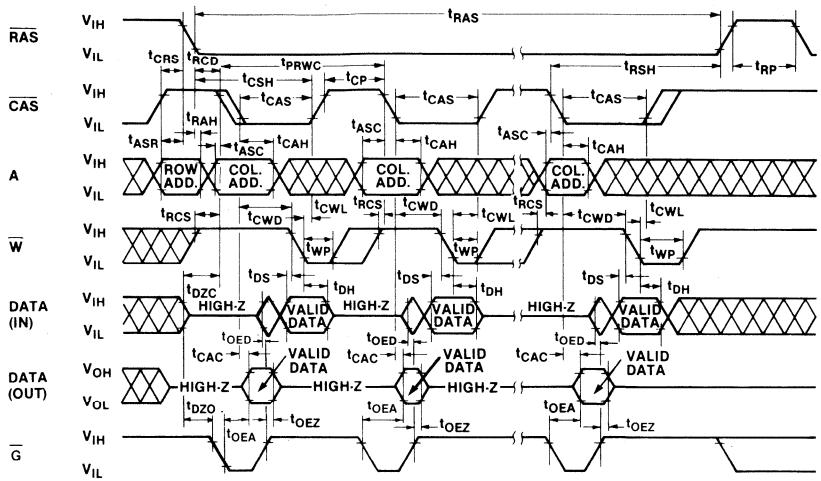
Page Mode Write Cycle

(G = Don't Care)

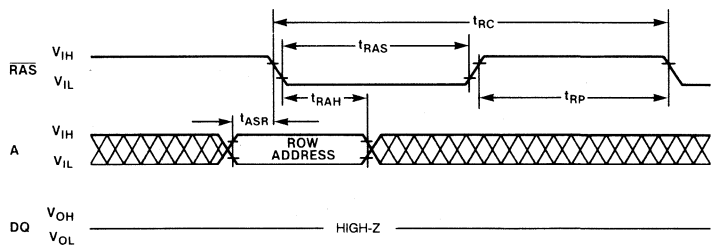


Timing Diagrams
(Continued)

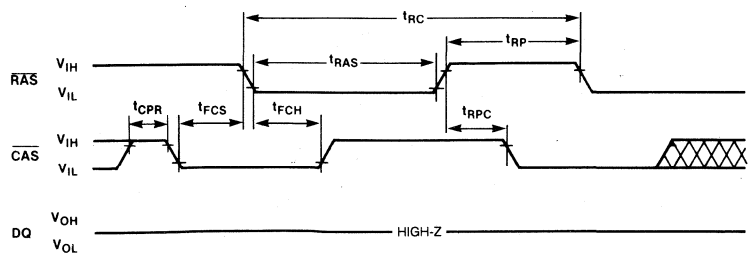
Page Mode Read-Write Cycle



RAS Only Refresh Cycle
NOTE: $\overline{CAS} = V_{IH}$: A_7, $\overline{W}$, $\overline{G}$ = Don't Care



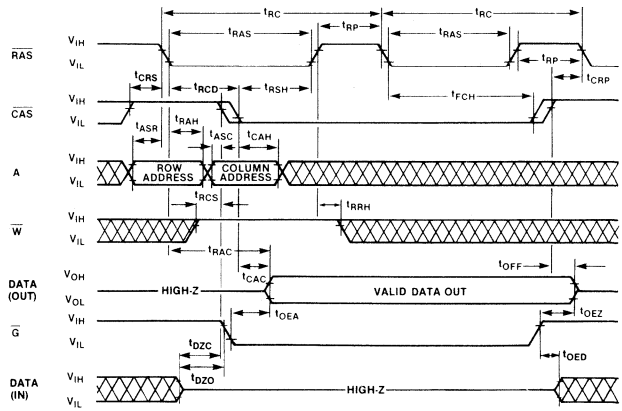
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle
NOTE: A, $\overline{W}$, $\overline{G}$ = Don't Care



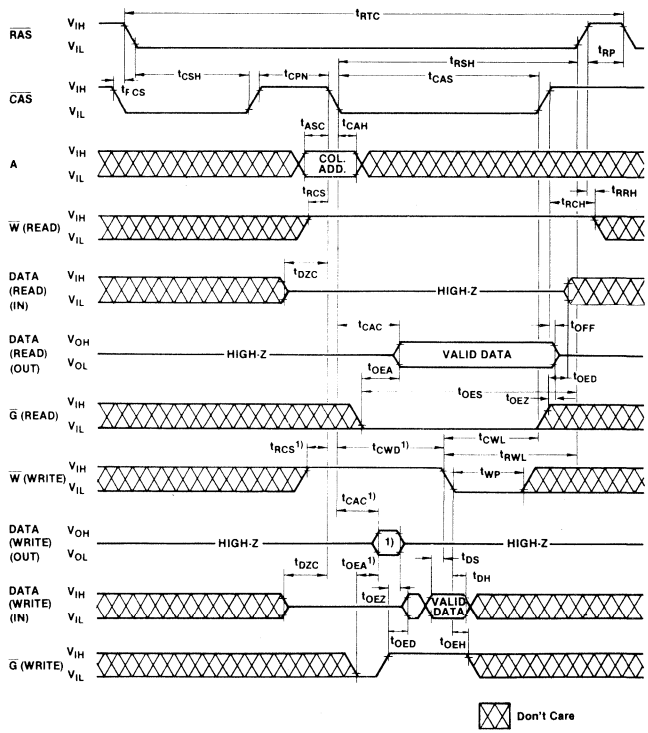
Don't Care

Timing Diagrams
(Continued)

Hidden Refresh Cycle



CAS-Before-RAS Refresh Counter Test Cycle



Note 1: When t_{CWD} is satisfied and $\overline{G}$ is Low (Delayed-Write Cycle), the data out will be "VALID". But when t_{CWD} is not satisfied, the data out will be "INVALID".

Description

Address Inputs

A total of 14 binary input address bits are needed to decode any one of 16,384 nibble wide words from the MB81416's 65,536 memory cells. Addressing a Random 4-bit word is initiated by establishing 8 row address bits on the address input pins, (A_0 through A_7), and after they are stable, latching these address bits with the falling edge of the Row Address Strobe ($\overline{RAS}$). Then 6 column address bits are established on the address input pins A_1 through A_6. After the addresses are stable, they are latched with the falling edge of the Column Address Strobe ($\overline{CAS}$). Address timing is made non-critical by the MB81416's "gated $\overline{CAS}$" circuitry which automatically inhibits $\overline{CAS}$ until the Row Address Hold time (t_{RAH}) has been satisfied and the address inputs have changed from row to column addresses.

Data Input/Output

The MB81416 has 4 common I/O pins (DQ_1, DQ_2, DQ_3, and DQ_4). Read or write modes are selected with the write enable pin ($\overline{W}$). An output enable pin ($\overline{G}$) controls the state of the output buffers making delayed write and read-modify-write cycles possible. The DQ pins provide TTL compatible inputs and three-state TTL compatible outputs with a fan-out of two standard TTL loads. Data-out has the same polarity as data-in.

Write Enable

The read mode or write modes are determined by the state of the write enable pin ($\overline{W}$). A logic high on $\overline{W}$ selects the read mode and a logic low on $\overline{W}$ selects the write mode. When $\overline{W}$ is high (read mode), the data inputs are disabled. If $\overline{W}$ goes low and satisfies the write command set-up time (t_{WCS}) before $\overline{CAS}$ goes low, the data outputs will remain in the high-impedance state for the duration of the cycle. This allows a write cycle to occur regardless of the state of the output enable ($\overline{G}$).

Output Enable

The output buffers are controlled by both $\overline{CAS}$ and output enable ($\overline{G}$). If either $\overline{CAS}$ or $\overline{G}$ are high the output buffers are in the high impedance state. During a read or read-modify-write cycle if both $\overline{CAS}$ and $\overline{G}$ are low, the output buffers are enabled. During an early write cycle $\overline{G}$ has no effect on the output buffers.

Data Inputs

Data may be written into the MB81416 during a write or read-modify-write cycle. The last falling edge of $\overline{CAS}$ or $\overline{W}$, strobes the data into the 4 on-chip data latches. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$, and the data is strobed in by $\overline{CAS}$ with both the set-up time (t_{DS}) and hold time (t_{DH}) referenced to the falling edge of $\overline{CAS}$. The outputs are in the high impedance state regardless of $\overline{G}$'s state. In a delayed write or a read-modify-write cycle, $\overline{W}$ is brought low after $\overline{CAS}$, data is strobed-in by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$. To avoid buss contention on I/O pins, it is necessary during a delayed write or a read-modify-write cycle for $\overline{G}$ to be high prior to data input so that the output buffers are in the high impedance state when data is being written.

Data Outputs

Data can be read from the MB81416 with either a read or a read-modify-write cycle. These cycles begin with the outputs in the high impedance state. The outputs contain active, valid data only after both $\overline{CAS}$ and $\overline{G}$ have been brought low and have satisfied the minimum access time from $\overline{RAS}$ (t_{RAC}) and the minimum access time from the output enable t_{OED}. Outputs contain valid data as long as both $\overline{CAS}$ and $\overline{G}$ are held low. They return to the high impedance state when either $\overline{CAS}$ or $\overline{G}$ go high.

$\overline{RAS}$-Only Refresh

The MB81416's dynamic memory cells may be refreshed by performing any memory cycle at each of the 128 row addresses (A_0 through A_6) at least every 2 milliseconds. When a row is accessed all bits in the row are refreshed. During refresh, A_7 (Pin 10) is not used and either V_{IH} or V_{IL} may be applied to this pin.

$\overline{RAS}$-only Refresh is a simplified cycle that consists of strobing a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. During a $\overline{RAS}$-only Refresh cycle, $\overline{CAS}$ is high and the output buffers are in the high impedance state. Strobing each of the 128 row addresses (A_0 through A_6) with $\overline{RAS}$ will refresh all 65,536 memory cells in the MB81416. $\overline{RAS}$-only Refresh results in a substantial reduction in power dissipation compared to a full $\overline{RAS}/\overline{CAS}$ memory cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh*

$\overline{CAS}$ before $\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified set-up time (t_{FCS}) before $\overline{RAS}$ goes low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden $\overline{CAS}$ Before $\overline{RAS}$ Refresh

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{CAS}$ before $\overline{RAS}$ refresh capability.

***Note:** $\overline{CAS}$ Before $\overline{RAS}$ refresh available on request.

Description,
(Continued)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Cycle provides a convenient way to verify the functionality of the $\overline{CAS}$ before $\overline{RAS}$ refresh circuitry. The cycle begins with a $\overline{CAS}$ before $\overline{RAS}$ operation. Then $\overline{CAS}$ is cycled "high" and then "low". This enables a read, write, or read-modify-write operation to occur. Four memory cells are accessed with the location defined as follows:

Row Address —
Bits A_0 through A_6 are supplied by the on-chip refresh counter. Bit A_7 is set low internally.

Column Address —
Bits A_1 through A_6 are strobed-in by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Procedure

The $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Cycle timing is used in each of the following steps:

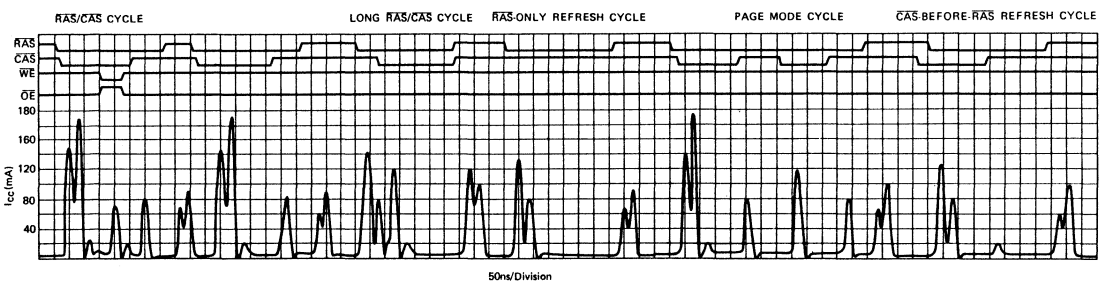
1. Initialized the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into each set of 4 memory cells at a single column address and 128 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 128 times so that "highs" are written into the 128 sets of 4 memory cells.
4. Read the highs written during step 3.
5. Compliment the test pattern and repeat steps 2, 3, and 4.

Page Mode

Page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In page mode, it is possible to read, write, or read-modify-write. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A page mode cycle begins with a normal cycle. While $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to setup and strobe sequential row addresses for the same page. Up to 64 nibble wide words may be accessed with the same row address.

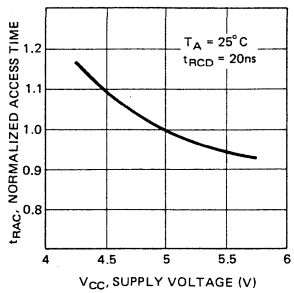
Typical Characteristics Curves

CURRENT WAVEFORM (V_{CC} = 5.5V, T_A = 25°C)

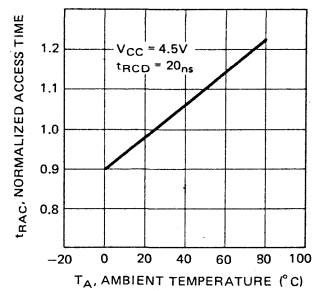


Typical Characteristics Curves
(Continued)

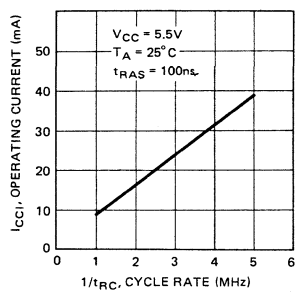
NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE



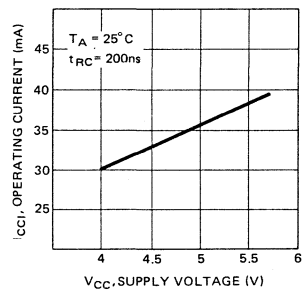
NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE



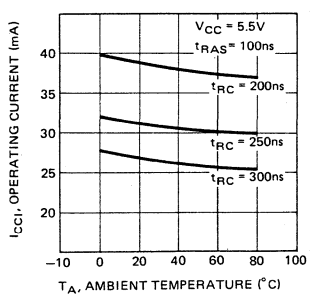
OPERATING CURRENT vs CYCLE RATE



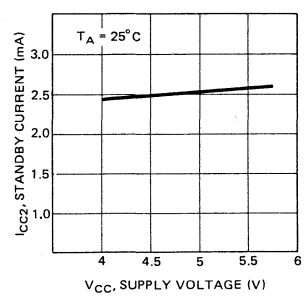
OPERATING CURRENT vs SUPPLY VOLTAGE



OPERATING CURRENT vs AMBIENT TEMPERATURE

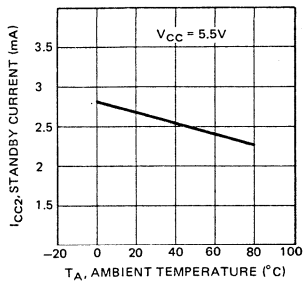


STANDBY CURRENT vs SUPPLY VOLTAGE

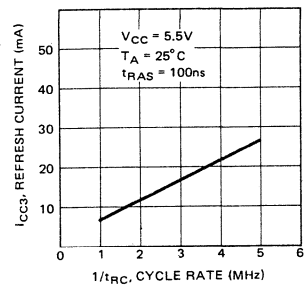


Typical Characteristics Curves
(Continued)

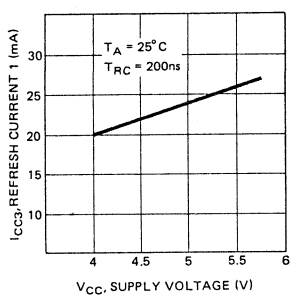
STANDBY CURRENT vs AMBIENT TEMPERATURE



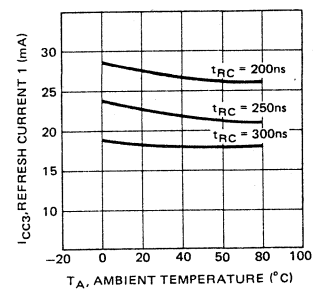
REFRESH CURRENT 1 vs CYCLE RATE



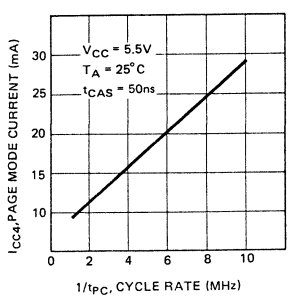
REFRESH CURRENT 1 vs SUPPLY VOLTAGE



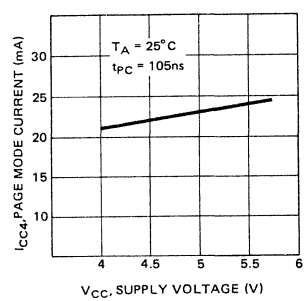
REFRESH CURRENT 1 vs AMBIENT TEMPERATURE



PAGE MODE CURRENT vs CYCLE RATE

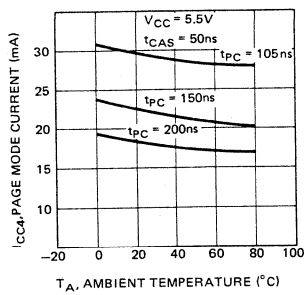


PAGE MODE CURRENT vs SUPPLY VOLTAGE

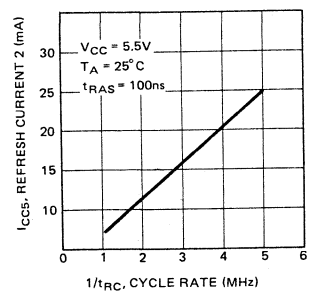


Typical Characteristics Curves
(Continued)

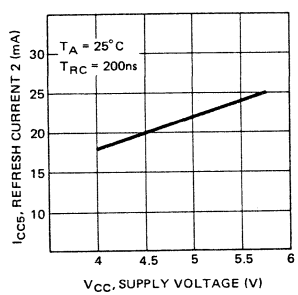
PAGE MODE CURRENT vs AMBIENT TEMPERATURE



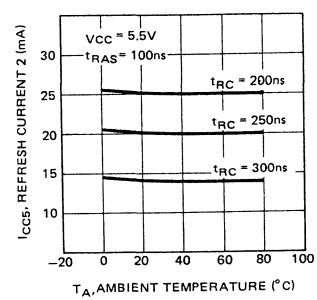
REFRESH CURRENT 2 vs CYCLE RATE



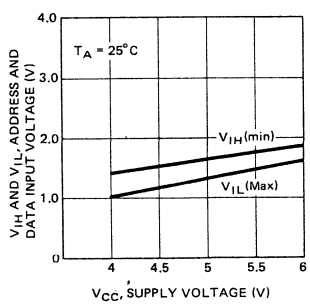
REFRESH CURRENT 2 vs SUPPLY VOLTAGE



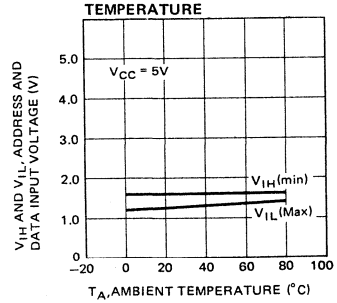
REFRESH CURRENT 2 vs AMBIENT TEMPERATURE



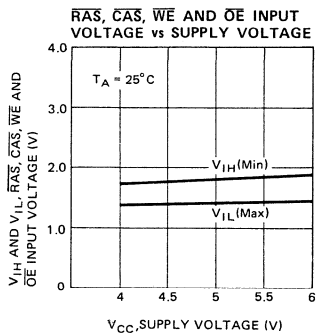
ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

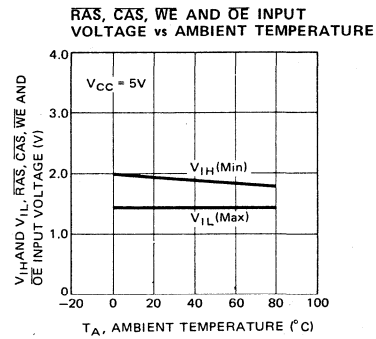


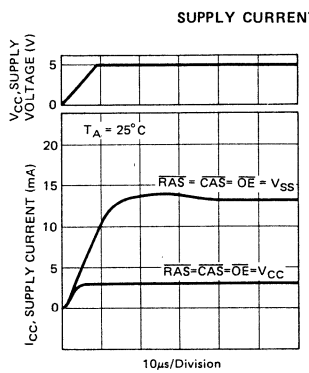
ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE

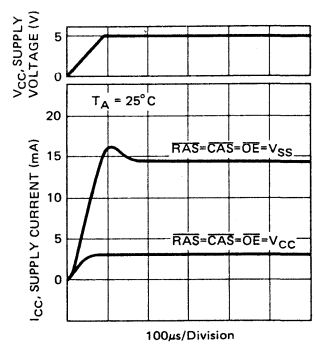


Typical Characteristics Curves
(Continued)



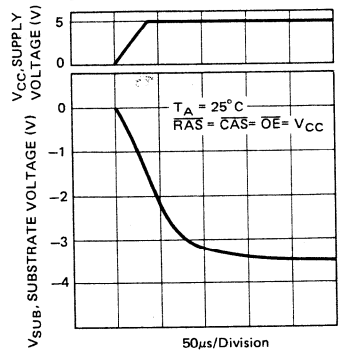




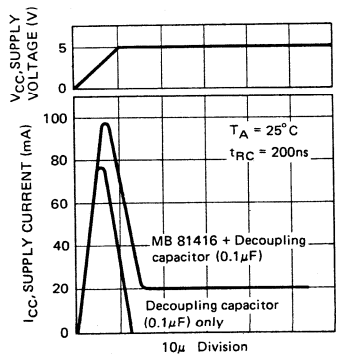


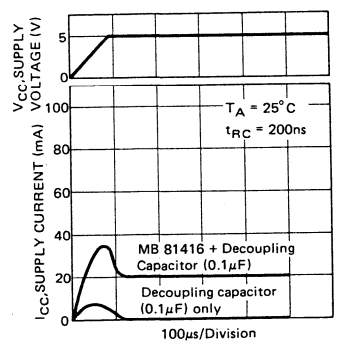
Typical Characteristics Curves
(Continued)

SUBSTARATE VOLTAGE
vs SUPPLY VOLTAGE
DURING POWER UP



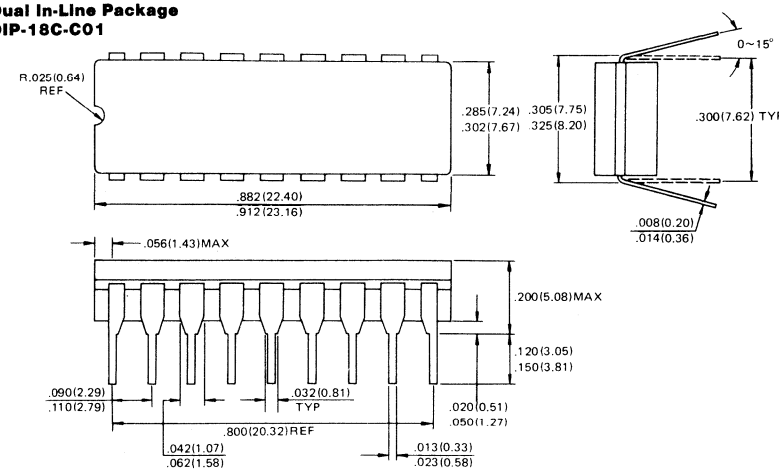
CURRENT WAVEFORM DURING POWER UP (ON MEMORY BOARD)



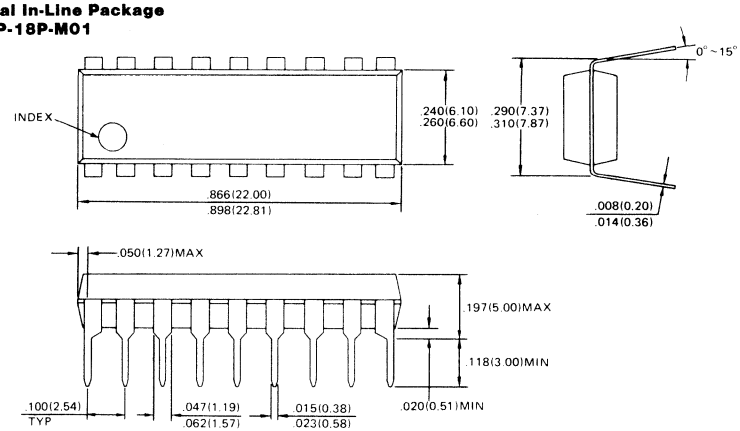


Package Dimensions
Dimensions in inches
(millimeters)

18-Lead Cerdip
Dual In-Line Package
DIP-18C-C01

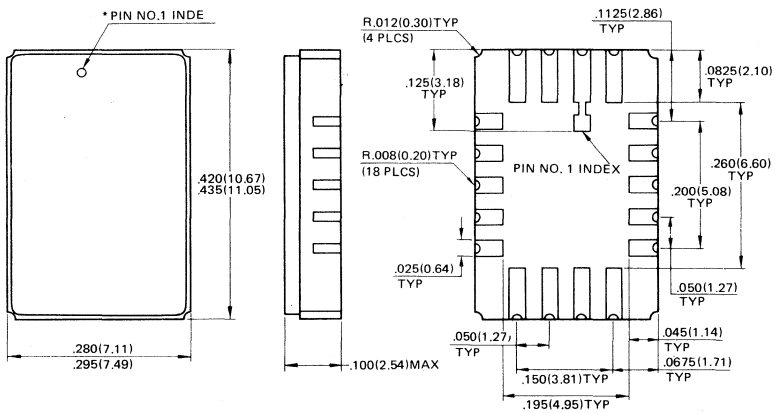


18-Lead Plastic
Dual In-Line Package
DIP-18P-M01



Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

18-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-18C-F02)



*Shape of Pin 1 index: Subject to change without notice

Preliminary

MOS Memories

FUJITSU

■ MB81461-12, MB81461-15

NMOS 262,144-Bit Dual Port Dynamic Random Access Memory

Description

The Fujitsu MB81461 is a fully decoded dual port dynamic NMOS random access memory organized as a 65,536 word by 4-bit dynamic RAM port and a 256 word by 4-bit serial access memory (SAM) port.

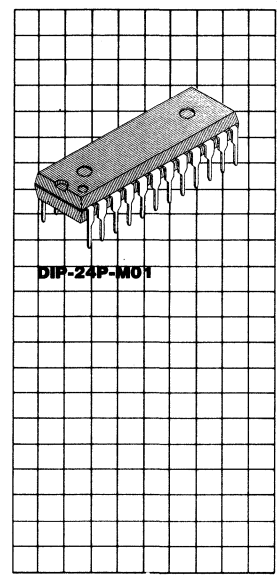
The DRAM port is identical to the Fujitsu MB81464 with four bit parallel random access I/O while the SAM port is designed as four 256-bit registers each operating as a serial I/O. The four serial registers operate in parallel with each other during SAM port operation. Internal interconnects give the device the capability to transfer data bi-directionally between the DRAM memory array and the SAM data registers.

The MB81461 offers completely asynchronous access of both the DRAM and SAM ports except when data is being transferred between them internally.

The design is optimized for high speed and performance which makes the MB81461 the most efficient solution for implementing the frame buffer of a bit-mapped video display system. Multiplexed row and column address inputs permit the MB81461 to be housed in a 400 mil wide 24 pin Dual-Inline-Package.

The MB81461 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple Layer Polysilicon process technology. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size.

All inputs and outputs are TTL compatible.



Features

- **Dual Port organization**
  64K × 4 Dynamic RAM Port (DRAM)
  256 × 4 Serial Access Memory Port (SAM)
- **DRAM Port**

	MB81461-12	MB81461-15
Access Time (t_{RAC})	120 ns max.	150 ns max.
Cycle Time (t_{RC})	230 ns min.	260 ns min.

- **SAM Port**

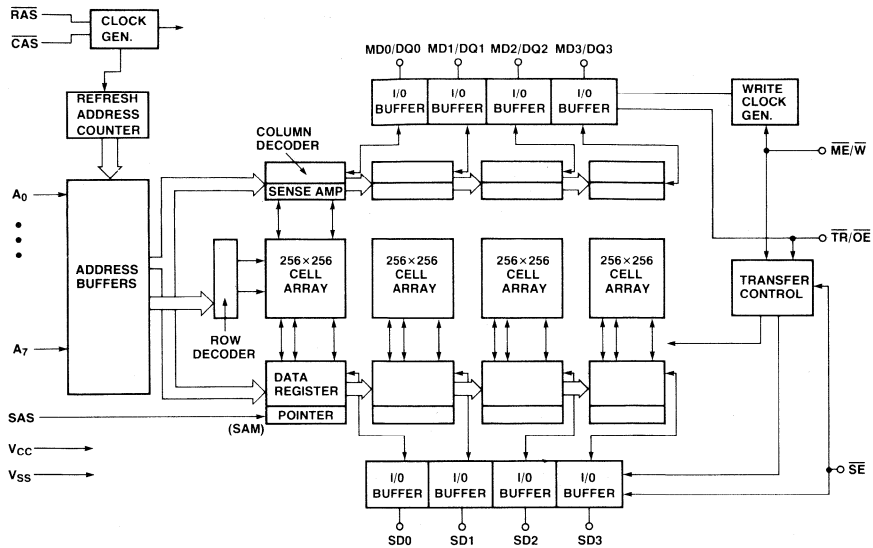
	MB81461-12	MB81461-15
Access Time (t_{SAC})	40 ns max.	60 ns max.
Cycle Time (t_{SC})	40 ns min.	60 ns min.

- **Low Power Dissipation**

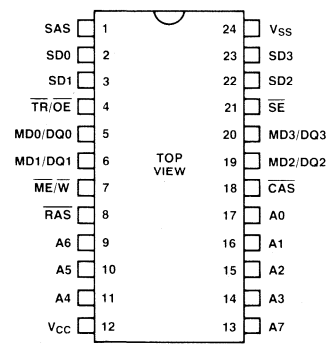
	MB81461-12	MB81461-15
DRAM Port Active	523 mW max.	468 mW max.
SAM Port Active	275 mW max.	220 mW max.
Both Ports Standby	110 mW max.	110 mW max.

- **Single +5V supply voltage, +/−10% tolerance**
- **Bi-directional Data Transfer between DRAM and SAM**
- **Fast serial access asynchronous to DRAM except transfer mode operation**
- **Real Time Read Transfer capability**
- **Read-Modify-Write capability**
- **Page mode capability for faster access**
- **Bit Mask Write mode capability**
- **Refresh 4 ms/256 cycles**
- **$\overline{RAS}$-only refresh**
- **$\overline{CAS}$-before-$\overline{RAS}$ on chip refresh**
- **All inputs and outputs TTL compatible**
- **24 pin 400 mil wide plastic package**

Block Diagram of MB81461 and Pin Assignment



Pin Number	Symbol	Parameter	Mode
1	SAS	Serial access memory strobe	Input
2,3,22,23	SD0 to SD3	Serial data I/O	I/O
4	$\overline{TR}/\overline{OE}$	Transfer enable/ output enable	Input
5,6,19,20	MD0/DQ0 to MD3/DQ3	Mask data/ data I/O	I/O
7	$\overline{ME}/\overline{W}$	Mask mode enable/ write enable	Input
8	$\overline{RAS}$	Row address strobe	Input
9,10,11,13 14,15,16,17	A_0-A_7	Address input	Input
12	V_{CC}	Supply voltage +5V	Power supply
18	$\overline{CAS}$	Column address strobe	Input
21	$\overline{SE}$	Serial port enable	Input
24	V_{SS}	Ground	Power supply



Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} relative to V_{SS}	V_{CC}	−1 to +7	V
Storage Temperature	T_{STG}	−55 to +125	°C
Power Dissipation	P_D	1.0	W
Short Circuit output current		50	mA

DRAM Operation

$\overline{RAS}$;
This pin is used to strobe eight row-address inputs from A_0 to A_7 and is used to select the operation mode of subsequent cycle, such as DRAM operation or transfer operation (by $\overline{TR}/\overline{OE}$) and bit mask write cycle or not (by $\overline{ME}/\overline{W}$ and MD0/DQ0 to MD3/DQ3). Since $\overline{RAS}$ = "L" is the active condition of circuit, maintaining $\overline{RAS}$ = "H" (Standby condition) lowers power dissipation.

$\overline{CAS}$;
This pin is used to strobe eight column address inputs at the falling edge. The $\overline{CAS}$ pin also functions to enable or disable the output at "L" and "H" respectively during the read operation.

Another function of $\overline{CAS}$ is to select "early write" mode conditioned by $\overline{ME}/\overline{W}$ = "L".

$\overline{ME}/\overline{W}$;
This pin is used to select read or write cycle. $\overline{ME}/\overline{W}$ = "L" selects write mode and $\overline{ME}/\overline{W}$ = "H" selects read mode. This pin is also used to enable bit mask write cycle. If $\overline{ME}/\overline{W}$ = "L" at the falling edge of $\overline{RAS}$, bit mask write is enabled.

$\overline{TR}/\overline{OE}$;
This pin is used to select Transfer operation or not at the falling edge of $\overline{RAS}$. $\overline{TR}/\overline{OE}$ = "H" enables DRAM operation and $\overline{TR}/\overline{OE}$ = "L" enables Transfer operation between DRAM and SAM. After the falling of $\overline{RAS}$ with t_{YH}, this pin is used for output enable.

The TR/OE controls the impedance of the output buffers. TR/OE = "H" forces the output buffers to high impedance state. TR/OE = "L" brings the output buffers to low impedance state. However, in early write cycle, the output buffers are in high impedance state even if TR/OE is low.

A_0 to A_7;
These are multiplexed address input pins and used to select 4 bits of 262,144 memory cell locations in parallel within the MB81461. The eight row address inputs are strobed by $\overline{RAS}$ and the following eight column address inputs are strobed by $\overline{CAS}$. These inputs are also used to select the start address of serial access memory.

MD0/DQ0 to MD3/DQ3;
These are common I/O pins of the DRAM port. I/O mode is as specified for each functional mode in the truth table.

Data Outputs;
The output buffers have three-state capability, "H", "L" and "High-Z". To get valid output data on the pins, one of the read operations is selected such as "read-modify-write" mode. During a refresh cycle, if $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ mode is selected, output buffers are set in "High-Z" state.

Data Inputs;
These are used as data input pins when a data write mode such as "Early-Write", "$\overline{OE}$-Write" or "Read-modify-write" is selected. In any of the above cases, these pins are set at high-Z state to enable data-in without any bus conflict.

In any operation mode; read, write, refresh, transfer and their combined functions, output states "H", "L", "High-Z" are set by control signals $\overline{RAS}$, $\overline{CAS}$, $\overline{ME}/\overline{W}$ and/or $\overline{TR}/\overline{OE}$. When "Bit mask write" mode is set, these pins are used as a control signal for inhibit with MDi/DQi = "L" on selected bit i.

Page Mode;
The page mode operates by strobing the column address while $\overline{RAS}$ is maintained at "L" through all the accessive memory operations if the row address doesn't change. This mode can lower power dissipation and improve access time due to elimination of $\overline{RAS}$ function.

Refresh;
Refresh of the DRAM cells is performed for all 256 rows every 4 milliseconds.

The MB81461 offers the following three types of refresh.

1) $\overline{RAS}$-Only refresh; The $\overline{RAS}$-Only refresh is performed with $\overline{CAS}$ = "H" condition. Strobing all 256 row addresses, $\overline{RAS}$ will complete all bits of memory array to be refreshed while all outputs are invalid due to "High-Z" state. Further, $\overline{RAS}$-only refresh lowers power dissipation substantially.

DRAM Operation
(continued)

2 $\overline{CAS}$-before-$\overline{RAS}$ refresh; The $\overline{CAS}$-before-$\overline{RAS}$ refresh offers an alternate refresh method. If $\overline{CAS}$ is set low for the specified period (t_{FCS}) before the falling edge of $\overline{RAS}$, refresh control clock generator and refresh address counter are enabled, and a refresh operation is performed. After the refresh operation is performed, the refresh address counter is incremented automatically for the the next $\overline{CAS}$-before-$\overline{RAS}$ refresh.

3 Hidden refresh; The hidden refresh is performed by maintaining the valid data of last read cycle at MD/DQ pins while extending $\overline{CAS}$ low. The hidden refresh is equivalent to $\overline{CAS}$-before-$\overline{RAS}$ refresh because $\overline{CAS}$ stays low when $\overline{RAS}$ goes low in the next cycle.

Bit Mask Write;
This mode is used when some of the bits should be inhibited to be written into cells. The bit mask write mode is executed by setting $\overline{ME}/\overline{W}$ = "L" at the falling edge of $\overline{RAS}$ during write mode (early, $\overline{OE}$-write or read-modify-write cycle). The bits to be masked (or inhibited to write) are determined by MD/DQ state at the falling edge of $\overline{RAS}$. For example, if MD0/DQ0 and $\overline{ME}/\overline{W}$ are both low at the falling edge of $\overline{RAS}$, the data on MD0/DQ0 pin is not written into the cell during the cycle.

Example of Bit Mask Write Operation

FALLING EDGE OF $\overline{RAS}$						FUNCTION
$\overline{TR}/\overline{OE}$	$\overline{ME}/\overline{W}$	MD0/DQ0	MD1/DQ1	MD2/DQ2	MD3/DQ3	
H	H	X	X	X	X	WRITE ENABLE
	L	H	L	H	L	WRITE ENABLE FOR DQ0 AND DQ2 WRITE DISABLE FOR DQ1 AND DQ3

X: DON'T CARE

Functional Truth Table for DRAM Operation

$\overline{RAS}$	$\overline{CAS}$	$\overline{ME}/\overline{W}$	$\overline{TR}/\overline{OE}$	Address	DQ0 to DQ3	Function
H	H	X	X	X	X	Standby
L	L	H	H→L	Valid	Valid Data Out	Read
L	L	L	H→X	Valid	Valid Data In	Early Write
L	L	H→L	H→X→H	Valid	Valid Data In	$\overline{OE}$-Write
L	L	H→L	H→L→H	Valid	Valid Data Out →Valid Data In	Read-Modify-Write
L	H	X	H→X	Row address	High-Z	$\overline{RAS}$-Only Refresh
H→L	L	X	H→X	X	High-Z	$\overline{CAS}$-before-$\overline{RAS}$ Refresh

Transfer Operation

The transfer operation featured in the MB81461 is used to transfer 256x4 data from DRAM to SAM or from SAM to DRAM. The direction of transfer is determined by the state of $\overline{ME}/\overline{W}$ at the falling edge of $\overline{RAS}$. $\overline{ME}/\overline{W}$ = "H" defines the transfer from DRAM to SAM (Read Transfer Cycle) and $\overline{ME}/\overline{W}$ = "L" defines the transfer from SAM to DRAM (Write Transfer Cycle).
I/O mode of SD0 to SD3 is determined while the transfer operation is set ($\overline{TR}/\overline{OE}$ = "L") in conjunction with $\overline{ME}/\overline{W}$ state.

$\overline{TR}/\overline{OE}$;
This pin is used to enable transfer operation at the falling edge of $\overline{RAS}$. $\overline{TR}/\overline{OE}$ = "L" enables the transfer operation.

$\overline{ME}/\overline{W}$;
This pin is used to select the direction of transfer at the falling edge of $\overline{RAS}$.

A_0 to A_7;
These pins are used to select the row address of DRAM port to be transfered from or to, and the start address of SAM port for the serial read or write operation. The row address is strobed by $\overline{RAS}$ and the start address is strobed by $\overline{CAS}$.

Pseudo Write Transfer;
To start serial write cycle, the SD pins must be set to input mode. To do this, a write transfer cycle should be executed. This pseudo write transfer cycle changes the SD pins to input mode without data transfer from SAM to DRAM.

Serial Access Operation

The MB81461 has a 256 word by 4-bit Serial Access Memory (SAM) corresponding to the 64K word by 4-bit DRAM. The fast serial read/write access feature is achieved by this SAM architecture. Read or write cycle is determined by the last transfer operation. If the last transfer operation was read transfer, the serial port is in the output mode until the next write or pseudo write transfer cycle is executed. On the other hand, if the last transfer operation was write or pseudo write transfer, the serial port is in the input mode. In the serial write operation, 256 word by 4-bit data stored in the SAM can be transferred to the DRAM under $\overline{SE}$ = "L" condition. The $\overline{SE}$ = "H" condition disables data transfer from SAM to DRAM. The serial access operation can run asynchronously from the DRAM port.

SAS;
This pin is used as a shift clock for SAM port. The serial access is triggered by the rising edge of SAS. In the write cycle, the data on the SD pins are strobed by the rising edge of SAS and written into the selected cell. In the read cycle, output data become valid after t_{SAC} from the rising edge of SAS and the data remain valid until the next cycle is defined. The SAS clock increments the SAM address automatically. When the SAM address exceeds #255 (Most Significant Address) it returns to #0 (Least Significant Address).

$\overline{SE}$;
This pin is used to enable serial access operation. $\overline{SE}$ = "H" disables serial access operation. In the serial read operation, this pin is used for output enable, i.e., $\overline{SE}$ = "H" drives SD pins to "High-Z" state. $\overline{SE}$ = "L" drives SD pins to valid data with specified access time. In the serial write operation, this pin works as write enable control pin.

SD0 to SD3;
These are used as data input/output pins for SAM port. Input or output mode is determined by the previous transfer operation. If the previous operation was read transfer mode, they are in output mode. If the write transfer mode was set, SD pins are enabled to write data into SAM.

Refresh;
Since the SAM is composed of dynamic memory cells, refresh is necessary to maintain the data in it. The refresh of SAM must be done by 256 cycles of SAS clock/4 ms in either output or input mode. $\overline{SE}$ = "H" allows refresh of SAM with SD pins at "High-Z" state.

Real Time Read Transfer;
This feature is used to obtain continuous valid data output when the row address is changed. Data flow is continuous from the last bit of the previous row to the first bit of the new row with no timing loss. Data transfer from DRAM to SAM is triggered by the rising edge of $\overline{TR}/\overline{OE}$ after the preparation of internal circuitry for this operation. The SAM port can continue its read operation asynchronously from the above mentioned internal operation. Once $\overline{TR}/\overline{OE}$ returns to "H" with the restricted timing specifications t_{TSL} and t_{TSD} referred to SAS clock, SD pins can output valid data continuously. The key to achieving this feature is to apply the SAS clock continuously while giving consideration to the timing requirements referenced to the rising edge of $\overline{TR}/\overline{OE}$.

Functional Truth Table for Serial Access

(Asynchronous from DRAM port)

Falling edge of $\overline{RAS}$					
$\overline{TR}/\overline{OE}$	$\overline{ME}/\overline{W}$	SAS	$\overline{SE}$	SD0 to SD3	Function
H	X	Clock	L	Input/output*	Sequential access enable
		Clock	H	Input/output*	Sequential access disable

NOTE: * The read or write operation of SAM port is pre-determined by the last occurred transfer cycle. Input mode is for write operation. Output mode is for read operation.
X; DON'T CARE

Recommended Operating Conditions

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating temperature
Supply voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.4		6.5	V	
Input low voltage	V_{IL}	−2.0		0.8	V	

Capacitance
(T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input capacitance (A_0 to A_7)	C_{IN1}		7	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{SAS}$)	C_{IN2}		8	pF
Input capacitance ($\overline{SE}$, $\overline{TR}/\overline{OE}$)	C_{IN3}		10	pF
Input/output capacitance (DQ0 to DQ3)	C_{IO1}		7	pF
Input/output capacitance (SD0 to SD3)	C_{IO2}		7	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Sam Standby $\overline{SE}$ = V_{IH}, SAS = V_{IL}

Parameter		Symbol	Min	Max	Unit
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB81461-12	I_{CC1}		95	mA
	MB81461-15			85	
Standby Current Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}		20	mA
Refresh Current*1 Average power supply current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	MB81461-12	I_{CC3}		77	mA
	MB81461-15			70	
Page mode current* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling, t_{PC} = min)	MB81461-12	I_{CC4}		50	mA
	MB81461-15			45	
Refresh current*2 Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$)	MB81461-12	I_{CC5}		70	mA
	MB81461-15			70	
Transfer mode current Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB81461-12	I_{CC6}		110	mA
	MB81461-15			100	

Sam Active t_{SC} = min, $\overline{SE}$ = V_{IL}

Parameter		Symbol	Min	Max	Unit
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB81461-12	I_{CC7}		130	mA
	MB81461-15			110	
Standby Current Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	MB81461-12	I_{CC8}		50	mA
	MB81461-15			40	
Refresh Current*1 Average power supply current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	MB81461-12	I_{CC9}		112	mA
	MB81461-15			95	
Page Mode Current* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = min)	MB81461-12	I_{CC10}		85	mA
	MB81461-15			70	
Refresh Current*2 Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$)	MB81461-12	I_{CC11}		112	mA
	MB81461-15			95	
Transfer Mode Current Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB81461-12	I_{CC12}		145	mA
	MB81461-15			125	

Notes: * I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

*1 An initial pause of 200 μs is required after power-up followed by any 8 $\overline{RAS}$ and $\overline{SAS}$ cycles before proper device operation is achieved. When using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of $\overline{RAS}$-cycles is required.

*2 AC characteristics assume t_T = 5 ns.

DC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit
Input Leakage Current Input leakage current, any input ($0 \leq V_{IN} \leq 5.5V$, $V_{CC} = 5.5V$, $V_{SS} = 0V$, all other pins not under test = 0V)	$I_{I(L)}$	−10	10	μA
Output Leakage Current (Data out is disabled, $0 \leq V_{OUT} \leq 5.5V$)	$I_{O(L)}$	−10	10	μA
Output Level 3 Output high voltage $I_{OH} = -5$ mA for DQ pins $I_{OH} = -2$ mA for SD pins	V_{OH}	2.4		V
Output low voltage ($I_{OL} = 4.2$ mA)	V_{OL}		0.4	

AC Characteristics *1,2,3
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81461-12 Min	MB81461-12 Max	MB81461-15 Min	MB81461-15 Max	Unit
Time between refresh	t_{REF}		4		4	ns
Random read/write cycle time	t_{RC}	230		260		ns
Read-modify-write cycle time	t_{RWC}	305		345		ns
Page mode cycle time	t_{PC}	120		145		ns
Page mode read-modify-write cycle time	t_{PRWC}	195		225		ns
Access time from $\overline{RAS}$*4,6	t_{RAC}		120		150	ns
Access time from $\overline{CAS}$*5,6	t_{CAC}		60		75	ns
Output buffer turn off delay	t_{OFF}	0	25	0	35	ns
Transition time	t_T	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	100		100		ns
$\overline{RAS}$ pulse width	t_{RAS}	120	10000	150	10000	ns
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns
$\overline{CAS}$ precharge time (page mode only)	t_{CP}	50		60		ns
$\overline{CAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$ mode only)	t_{CPR}	25		30		ns
$\overline{CAS}$ pulse width	t_{CAS}	60	10000	75	10000	ns
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ delay time*7,8	t_{RCD}	22	60	25	75	ns

Notes: *1 An initial pause of 200 μs is required after power-up followed by any 8 $\overline{RAS}$ and $\overline{SAS}$ cycles before proper device operation is achieved, When using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles is required.

*2 AC characteristics assume $t_T = 5$ ns.

*3 V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min.) and V_{IL} (max.).

*4 Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.

*5 Assumes the $t_{RCD} \geq t_{RCD}$ (max.).

*6 Measured with a load equivalent to 2 TTL load and 100 pF.

*7 Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.

*8 t_{RCD} (min.) = t_{RAH} (min.) + $2t_T$ + t_{ASC} (min.).

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81461-12 Min	MB81461-12 Max	MB81461-15 Min	MB81461-15 Max	Unit
$\overline{CAS}$ to $\overline{RAS}$ set up time	t_{CRS}	10		10		ns
Row address set up time	t_{ASR}	0		0		ns
Row address hold time	t_{RAH}	12		15		ns
Column address set up time	t_{ASC}	0		0		ns
Column address hold time	t_{CAH}	20		25		ns
Read command set up time	t_{RCS}	0		0		ns
Read command hold time referenced to $\overline{RAS}$*10	t_{RRH}	20		20		ns
Read command hold time referenced to $\overline{CAS}$*10	t_{RCH}	0		0		ns
Write command set up time	t_{WCS}	−5		−5		ns
Write command hold time	t_{WCH}	30		35		ns
Write command pulse width	t_{WP}	30		35		ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		45		ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		45		ns
Data in set up time	t_{DS}	0		0		ns
Data in hold time	t_{DH}	30		35		ns
Access time from $\overline{OE}$*6	t_{OEA}		35		40	ns
$\overline{OE}$ to data in delay time	t_{OED}	25		30		ns
Output buffer turn off delay from $\overline{OE}$	t_{OEZ}	0	25	0	30	ns
$\overline{OE}$ hold time referenced to $\overline{WE}$	t_{OEH}	0		0		ns
$\overline{OE}$ to $\overline{RAS}$ inactive set up time	t_{OES}	0		0		ns
Data in to $\overline{CAS}$ delay time	t_{DZC}	0		0		ns
Data in to $\overline{OE}$ delay time	t_{DZO}	0		0		ns
Refresh set up time for $\overline{CAS}$ referenced to $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCS}	25		30		ns
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCH}	25		30		ns
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	20		20		ns
Serial clock cycle time	t_{SC}	40	50000	60	50000	ns
Access time from SAS*11	t_{SAC}		40		60	ns
Access time from $\overline{SE}$*11	t_{SEA}		40		50	ns
SAS precharge time	t_{SP}	10		20		ns
SAS pulse width	t_{SAS}	10		20		ns
$\overline{SE}$ precharge time	t_{SEP}	25		45		ns
$\overline{SE}$ pulse width	t_{SE}	25		45		ns
Serial data out hold time after SAS high	t_{SOH}	10		10		ns

Notes: *6 Measured with a load equivalent to 2 TTL loads and 100 pF.
*10 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
*11 Measured with a load equivalent to 2 TTL loads and 50 pF.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81461-12 Min	MB81461-12 Max	MB81461-15 Min	MB81461-15 Max	Unit
Serial output buffer turn off delay from $\overline{SE}$	t_{SEZ}	0	25	0	30	ns
Serial data in set up time*16	t_{SDS}	0		0		ns
Serial data in hold time*16	t_{SDH}	20		25		ns
Transfer command (TR) to $\overline{RAS}$ set up time	t_{TS}	0		0		ns
Transfer command (TR) to $\overline{RAS}$ hold time	t_{RTH}	90		110		ns
Transfer command (TR) to $\overline{CAS}$ hold time	t_{CTH}	30		35		ns
Transfer command (TR) to SAS lead time	t_{TSL}	5		10		ns
Transfer command (TR) to $\overline{RAS}$ lead time	t_{TRL}	130		140		ns
Transfer command (TR) to $\overline{RAS}$ delay time	t_{TRD}	−65		−50		ns
First SAS edge to transfer command delay time	t_{TSD}	25		35		ns
$\overline{W}$ to $\overline{RAS}$ set up time	t_{WSR}	0		0		ns
$\overline{W}$ to $\overline{RAS}$ hold time	t_{RWH}	12		15		ns
Mask data (DQ) to $\overline{RAS}$ set up time	t_{MS}	0		0		ns
Mask data (DQ) to $\overline{RAS}$ hold time	t_{MH}	25		45		ns
Serial output buffer turn off delay from $\overline{RAS}$*13	t_{SDZ}	10	60	10	75	ns
SAS to $\overline{RAS}$ set up time*16	t_{SRS}	40		60		ns
$\overline{RAS}$ to SAS delay time*13	t_{SRD}	30		45		ns
Serial data input to $\overline{SE}$ delay time	t_{SZE}	0		0		ns
Serial data input delay from $\overline{RAS}$*13	t_{SDD}	60		75		ns
Serial data input to $\overline{RAS}$ delay time*15	t_{SZS}	0		0		ns
Pseudo transfer command ($\overline{SE}$) to $\overline{RAS}$ set up time*14	t_{ESR}	0		0		ns
Pseudo transfer command ($\overline{SE}$) to $\overline{RAS}$ hold time*14	t_{REH}	12		15		ns

Notes: *13 Write transfer and Pseudo write transfer only.
*14 Pseudo write transfer only.
*15 Read transfer only in the case that the previous transfer was write transfer.
*16 Input mode only.

AC Characteristics

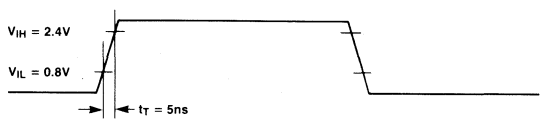
(Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81461-12 Min	MB81461-12 Max	MB81461-15 Min	MB81461-15 Max	Unit
Serial write enable set up time*16	t_{SWS}	20		30		ns
Serial write enable hold time*16	t_{SWH}	80		120		ns
Serial write disable set up time	t_{SWIS}	20		30		ns
Serial write disable hold time*16	t_{SWIH}	40		60		ns
Asynchronous command (TR) to $\overline{RAS}$ set up time	t_{YS}	0		0		ns
Asychronous command (TR) to $\overline{RAS}$ hold time	t_{YH}	12		15		ns
RAS to SD buffer turn on Time	t_{SRO}	0		0		ns
Time between Transfer cycle	t_{REFT}		4		4	ms
Write Transfer Command Hold Time Referenced to $\overline{RAS}$	t_{RTHW}	12		15		ns
$\overline{CAS}$ Precharge Time for Normal Cycle	t_{CPN}	40		50		ns

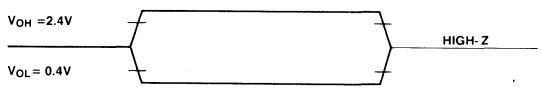
Note: *16 Input mode only.

AC Test Conditions

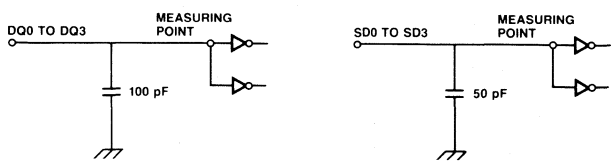
1) INPUT



2) OUTPUT

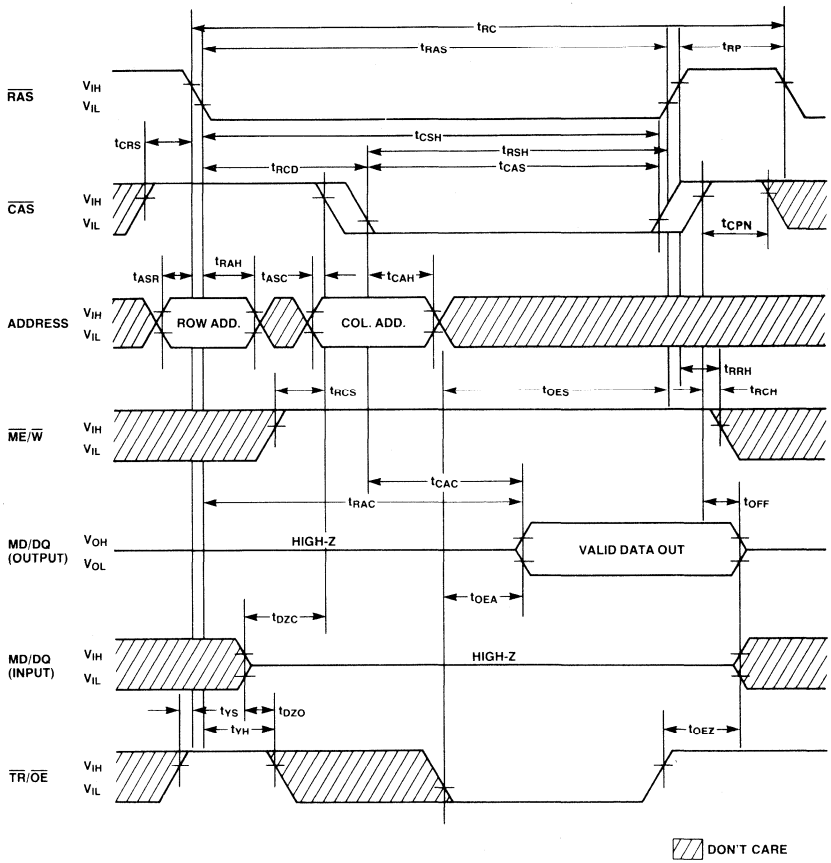


3) OUTPUT LOAD



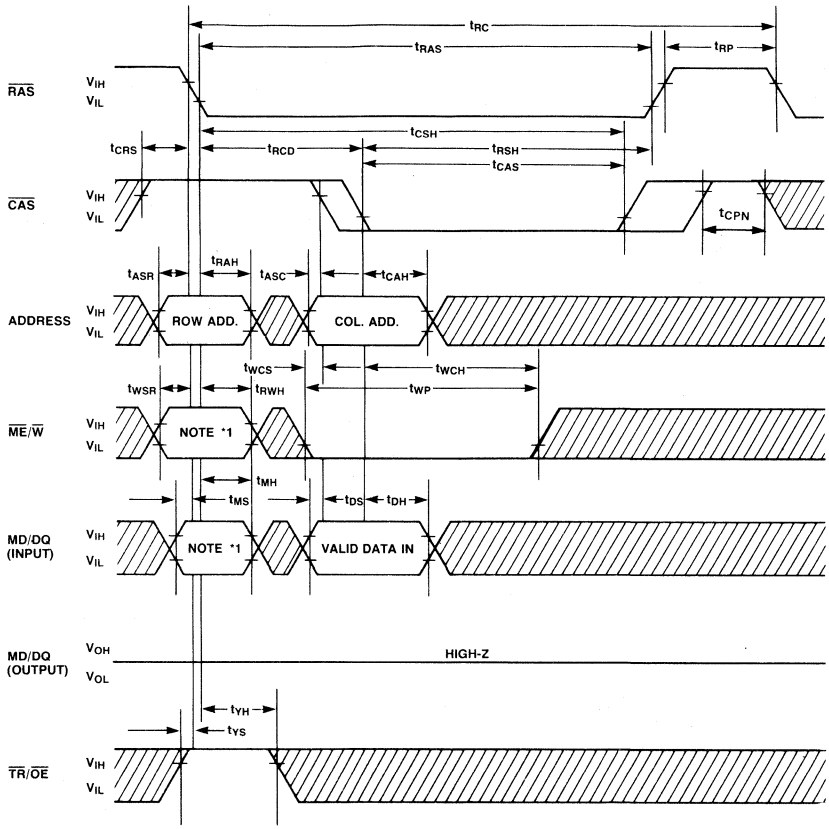
Timing Diagrams

Read Cycle



Timing Diagrams
(Continued)

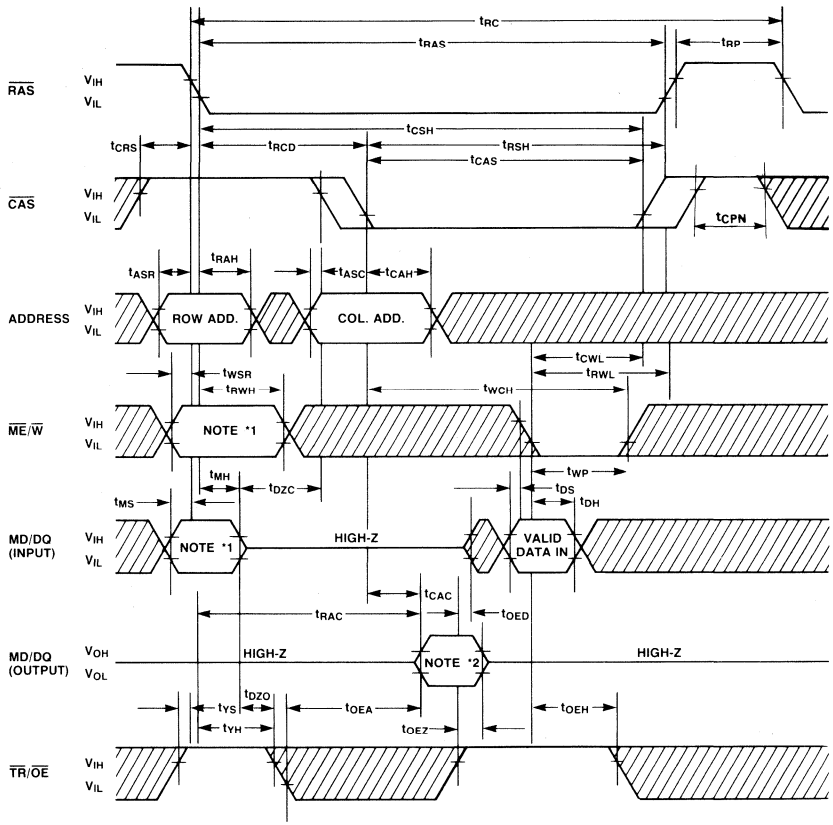
Write Cycle (Early Write)



NOTE: *1 WHEN $\overline{ME}/\overline{W}$ = "H", ALL DATA ON THE MD/DQ CAN BE WRITTEN INTO THE CELL.
WHEN $\overline{ME}/\overline{W}$ = "L", THE DATA ON THE MD/DQ ARE NOT WRITTEN (MASKED)
EXCEPT WHEN MD/DQ = "H" AT THE FALLING EDGE OF $\overline{RAS}$.

DON'T CARE

$\overline{OE}$ Write Cycle

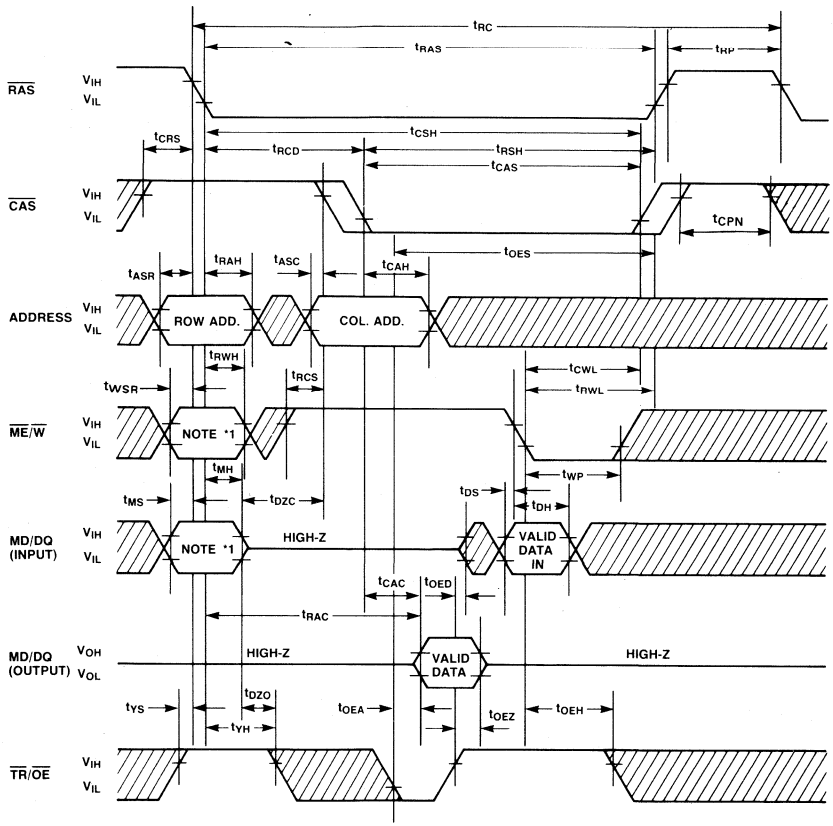


NOTES: *1 WHEN $\overline{ME}/\overline{W}$ = "H", ALL DATA ON THE MD/DQ CAN BE WRITTEN INTO THE CELL.
WHEN $\overline{ME}/\overline{W}$ = "L", THE DATA ON THE MD/DQ ARE NOT WRITTEN (MASKED) EXCEPT WHEN MD/DQ = "H" AT THE FALLING EDGE OF RAS.
*2 WHEN $\overline{TR}/\overline{OE}$ IS KEPT "H" THROUGH A CYCLE, MD/DQ IS KEPT IN HIGH-Z STATE.

DON'T CARE

Timing Diagrams
(Continued)

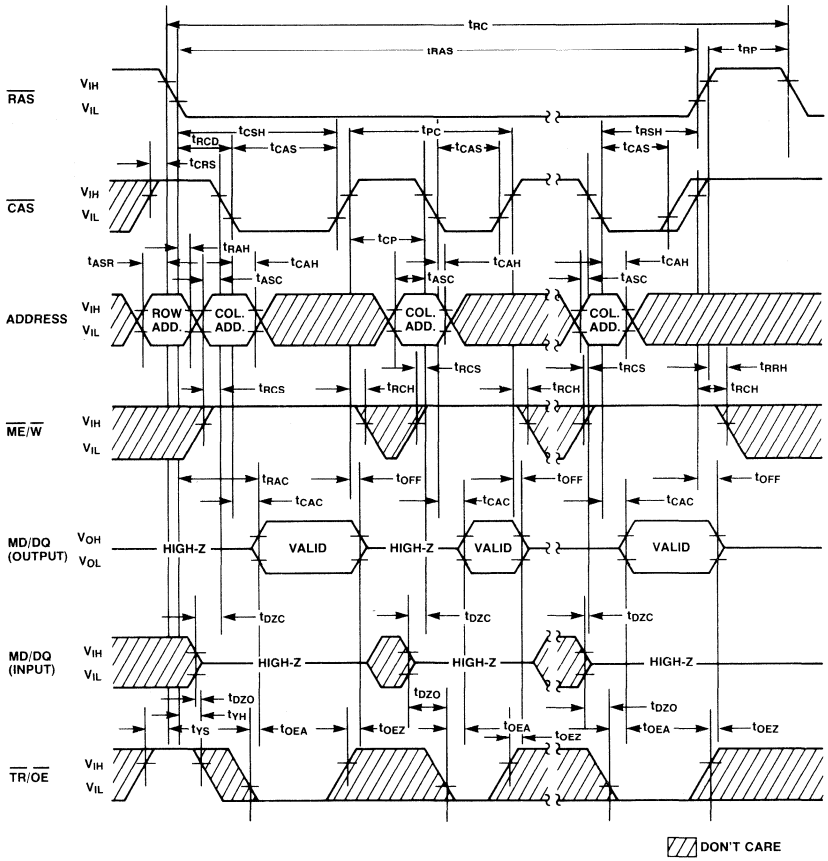
Read-Modify-Write Cycle



NOTE: *1 WHEN $\overline{ME}/\overline{W}$ = "H", ALL DATA ON THE MD/DQ CAN BE WRITTEN INTO THE CELL.
WHEN $\overline{ME}/\overline{W}$ = "L", THE DATA ON THE MD/DQ ARE NOT WRITTEN (MASKED)
EXCEPT WHEN MD/DQ = "H" AT THE FALLING EDGE OF $\overline{RAS}$.

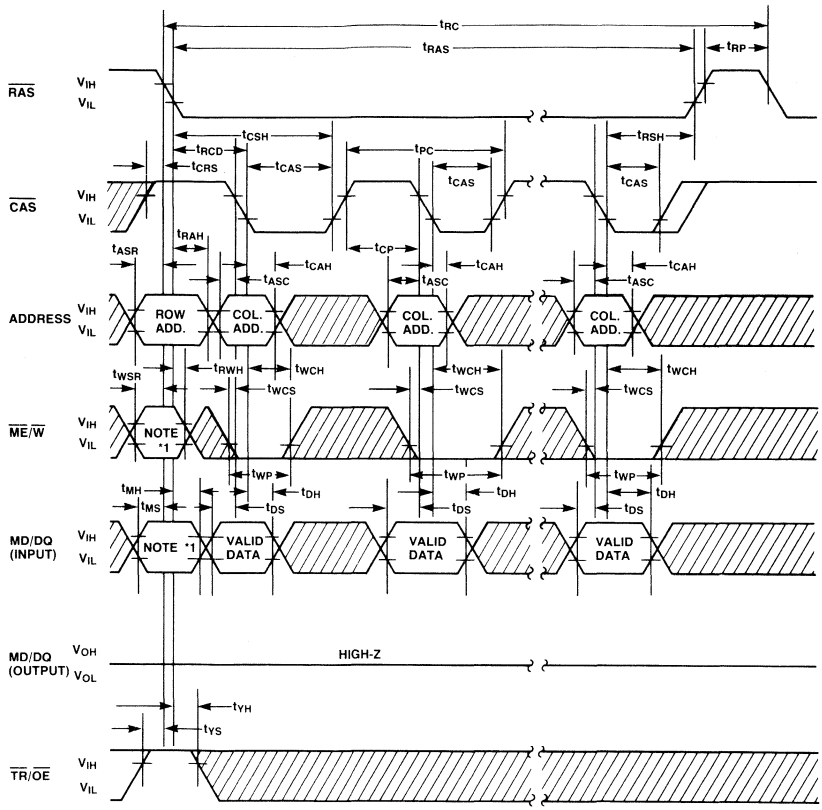
▨ DON'T CARE

Page Mode Read Cycle



Timing Diagrams
(Continued)

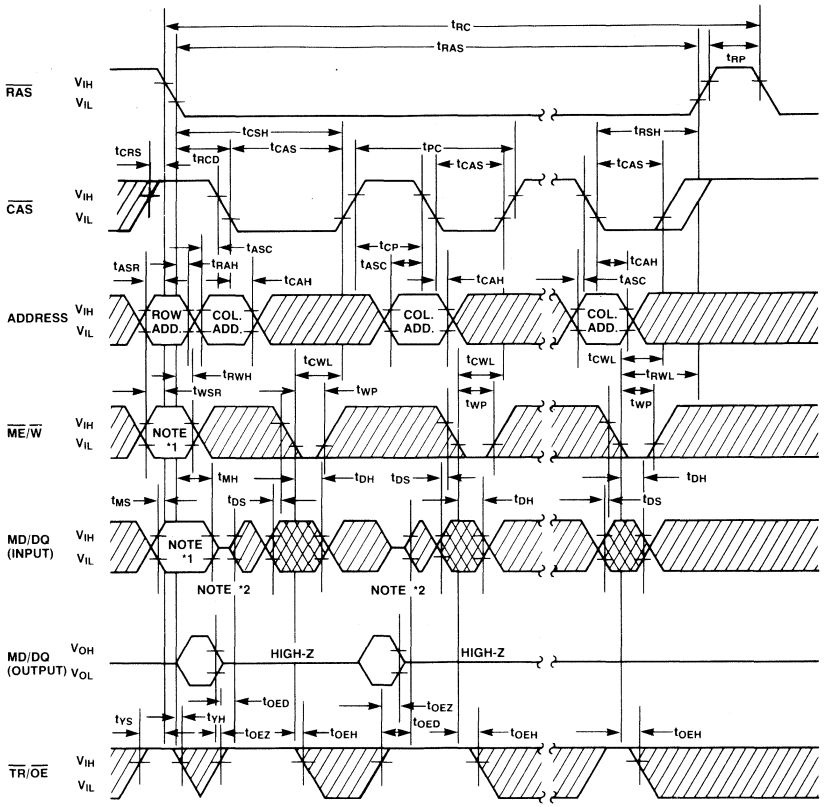
Page Mode Write Cycle (Early Write)



NOTE: *1 WHEN $\overline{ME}/\overline{W}$ = "H", ALL DATA ON THE MD/DQ CAN BE WRITTEN INTO THE CELL.
WHEN $\overline{ME}/\overline{W}$ = "L", THE DATA ON THE MD/DQ ARE NOT WRITTEN (MASKED)
EXCEPT WHEN MD/DQ = "H" AT THE FALLING EDGE OF $\overline{RAS}$.

▨ DON'T CARE

Page Mode $\overline{OE}$ Write Cycle

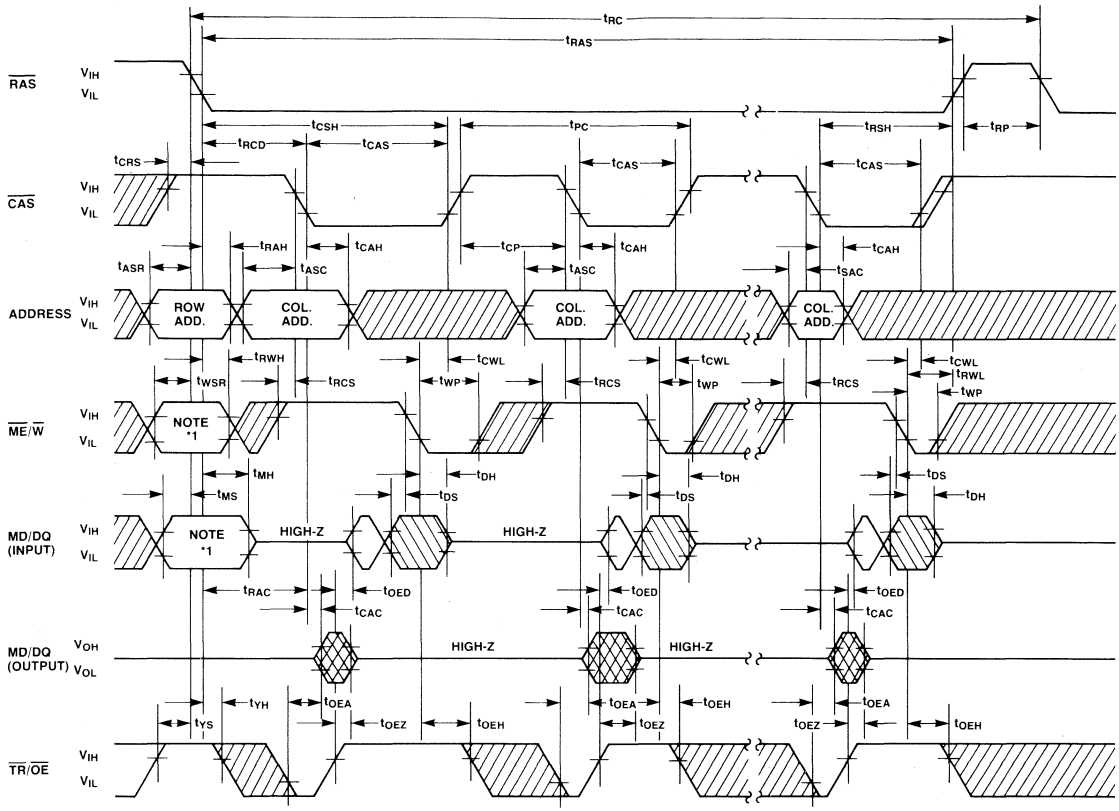


NOTES: *1 WHEN $\overline{ME}/\overline{W}$ = "H", ALL DATA ON THE MD/DQ CAN BE WRITTEN INTO THE CELL.
WHEN $\overline{ME}/\overline{W}$ = "L", THE DATA ON THE MD/DQ ARE NOT WRITTEN (MASKED) EXCEPT WHEN MD/DQ = "H" AT THE FALLING EDGE OF $\overline{RAS}$.
*2 WHEN $\overline{TR}/\overline{OE}$ IS KEPT "H" THROUGH A CYCLE, MD/DQ IS KEPT IN HIGH-Z STATE.

DON'T CARE
VALID DATA IN

Timing Diagrams
(Continued)

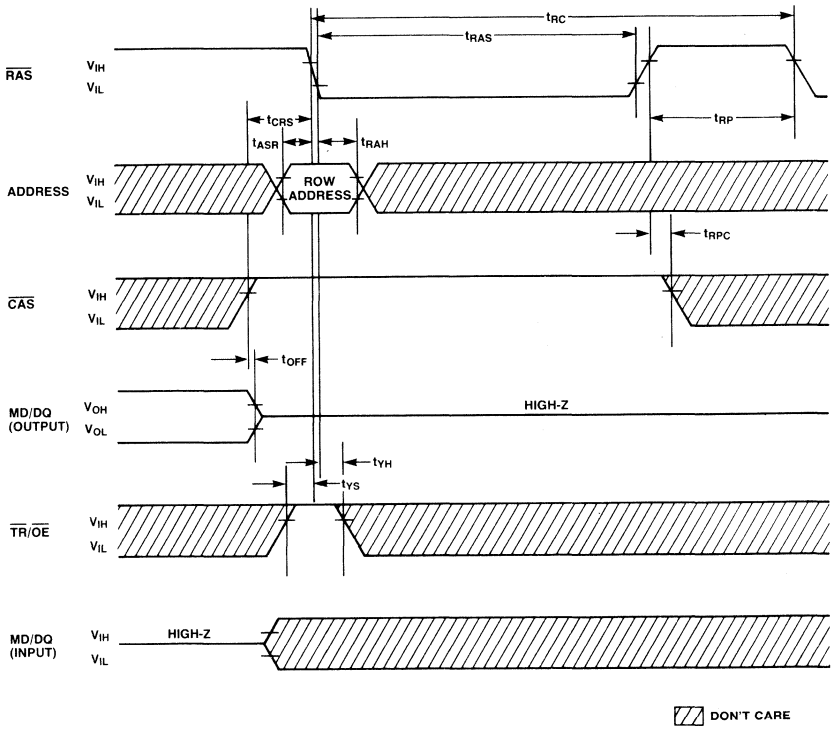
Page Mode Read-Modify-Write Cycle



NOTE: *1 WHEN $\overline{ME}/\overline{W}$ = "H", ALL DATA ON THE MD/DQ CAN BE WRITTEN INTO THE CELL.
WHEN $\overline{ME}/\overline{W}$ = "L", THE DATA ON THE MD/DQ ARE NOT WRITTEN (MASKED)
EXCEPT WHEN MD/DQ = "H" AT THE FALLING EDGE OF $\overline{RAS}$.

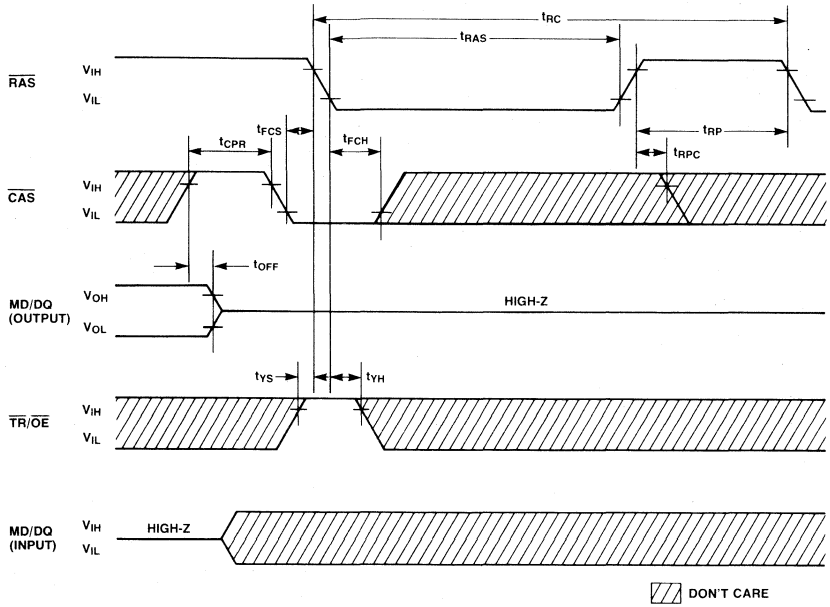
DON'T CARE
VALID DATA IN
VALID DATA OUT

$\overline{RAS}$-Only Refresh Cycle
($\overline{ME}$/$\overline{W}$ = Don't Care)

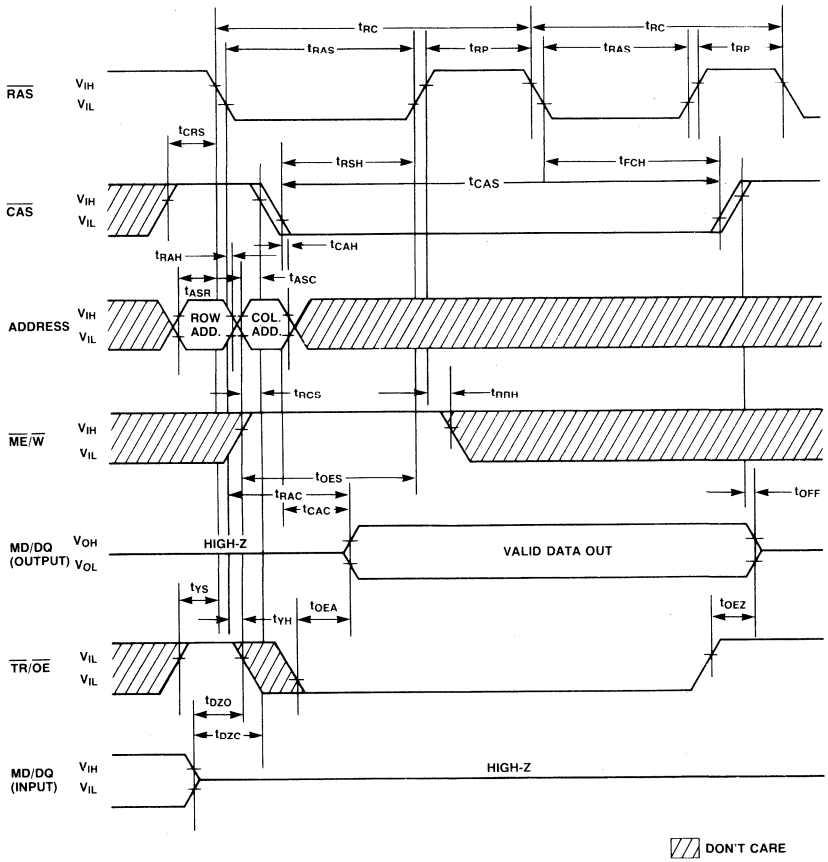


Timing Diagrams
(Continued)

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle (Address, $\overline{ME}/\overline{W}$ = Don't Care)

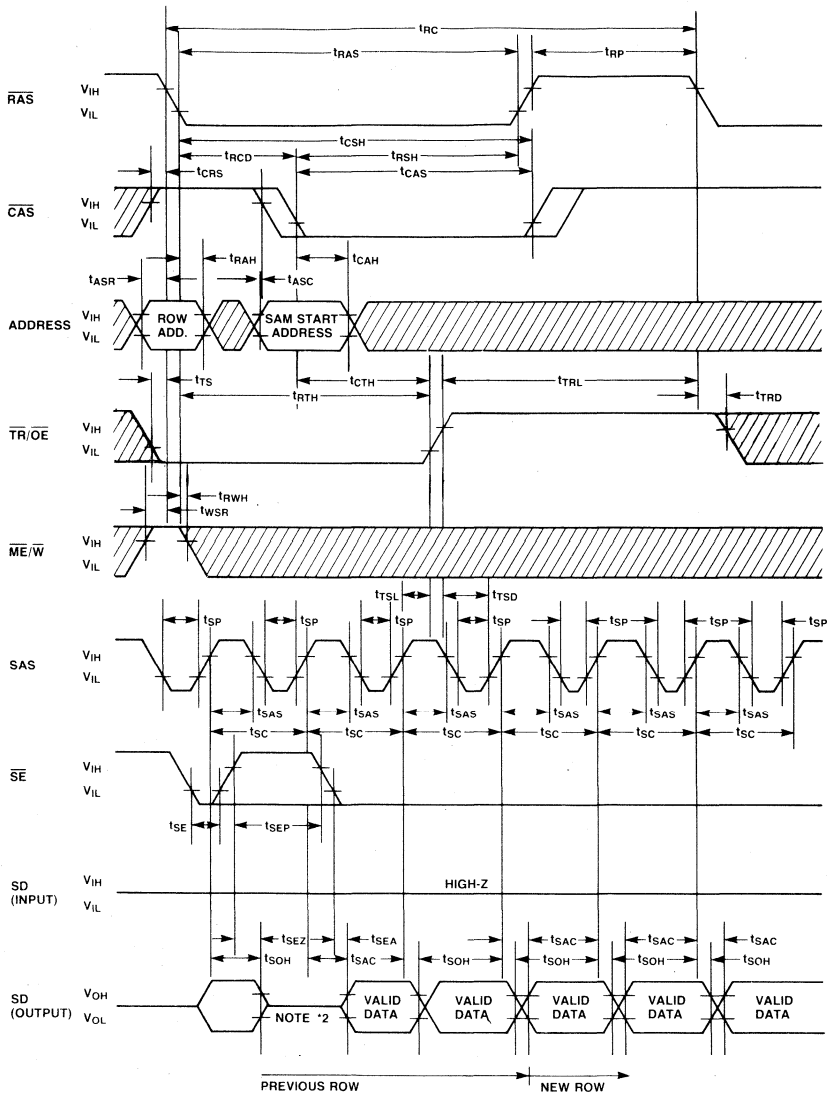


Hidden Refresh Cycle



Timing Diagrams
(Continued)

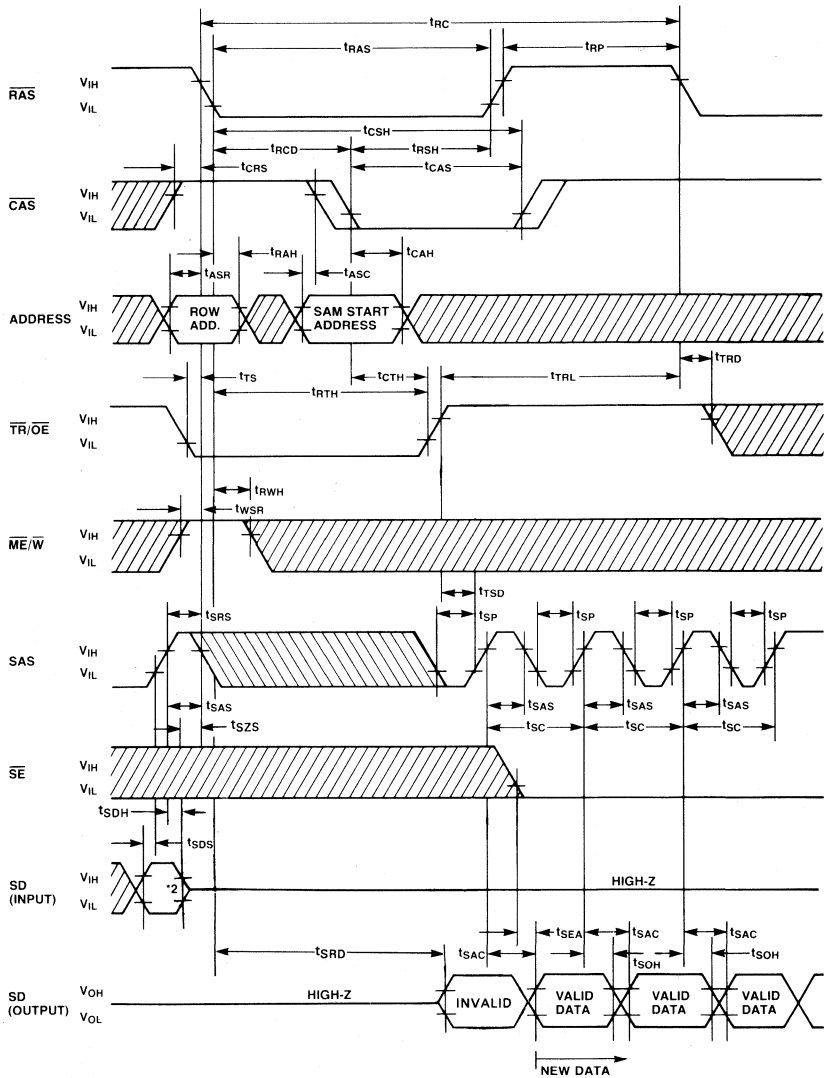
Read Transfer Cycle *1
(DQ = Don't Care)



NOTES: *1 IN THE CASE THAT THE PREVIOUS TRANSFER IS READ TRANSFER.
*2 IF $\overline{SE}$ IS LOW, THE VALID DATA WILL APPEAR WITHIN t_{SAC} or t_{SEA}.

DON'T CARE

Read Transfer Cycle*1
(DQ = Don't Care)



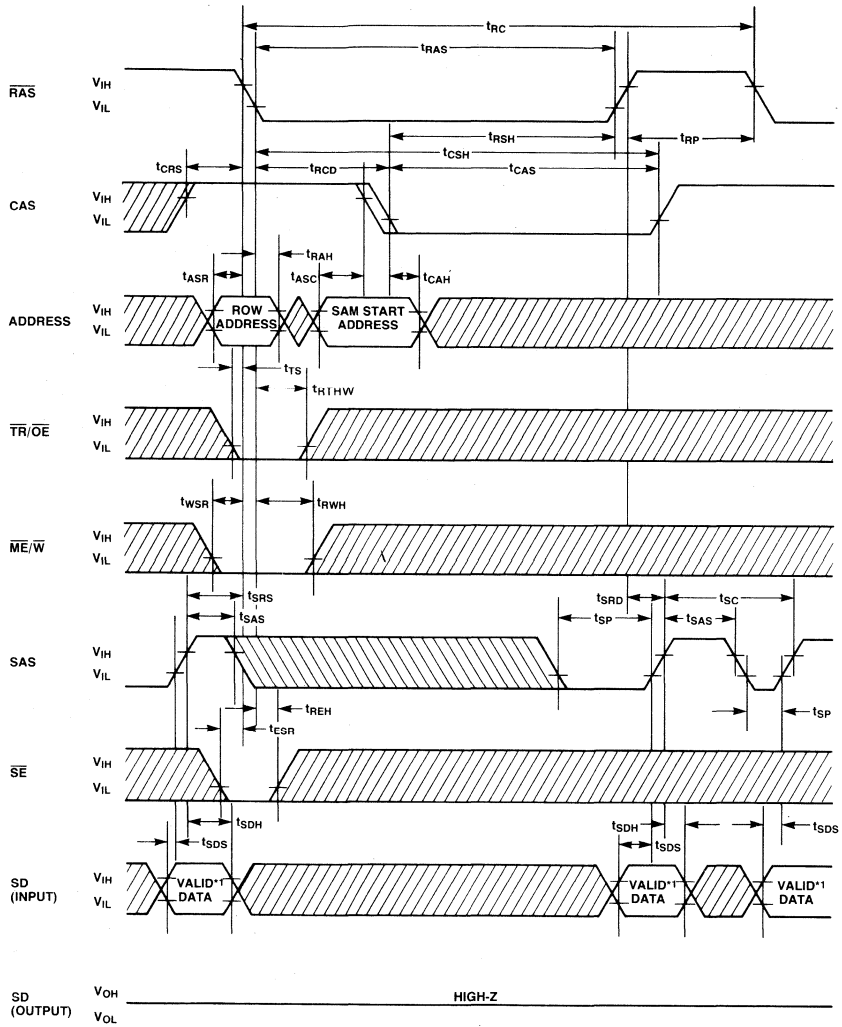
NOTES: *1 IN THE CASE THAT THE PREVIOUS TRANSFER IS WRITE TRANSFER.
*2 IF $\overline{SE}$ IS LOW AND THE PREVIOUS CYCLE IS SERIAL WRITE CYCLE, THIS SHOULD BE VALID DATA INPUT.

DON'T CARE

INHIBIT TRANSITION V_{IL} TO V_{IH}

Timing Diagrams
(Continued)

Write Transfer Cycle*

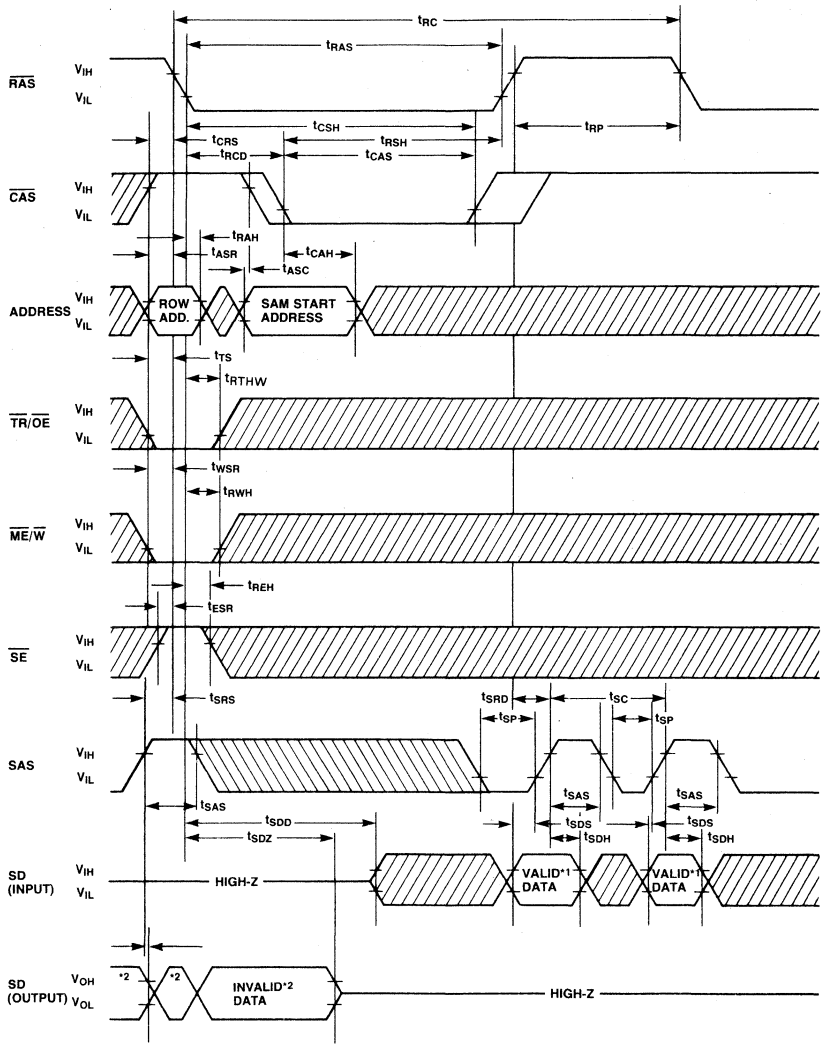


NOTE: *1 IF $\overline{SE}$ IS HIGH THIS DATA IS NOT WRITTEN INTO THE SAM.
*IN THE CASE THAT THE PREVIOUS TRANSFER IS WRITE TRANSFER.

DON'T CARE

INHIBIT TRANSITION V_{IL} TO V_{IH}

Pseudo Transfer Cycle



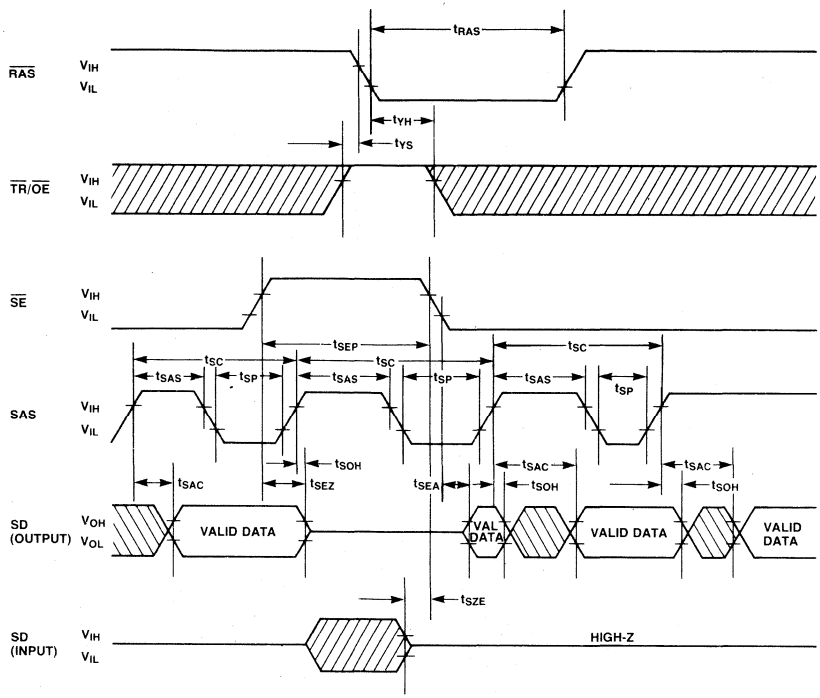
NOTES: *1 IF $\overline{SE}$ IS HIGH, THIS DATA IS NOT WRITTEN INTO SAM.
*2 IF $\overline{SE}$ IS HIGH, SD (SD0 TO SD3) ARE IN HIGH-Z STATE AFTER t_{SEZ}.

DON'T CARE

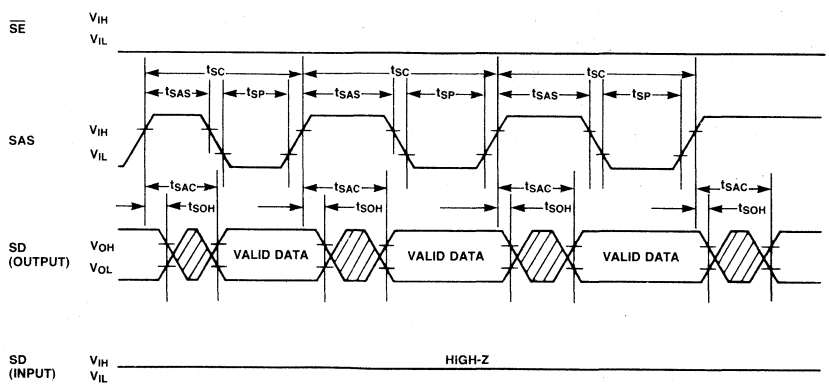
INHIBIT TRANSITION V_{IL} TO V_{IH}

Timing Diagrams
(Continued)

Serial Read Cycle

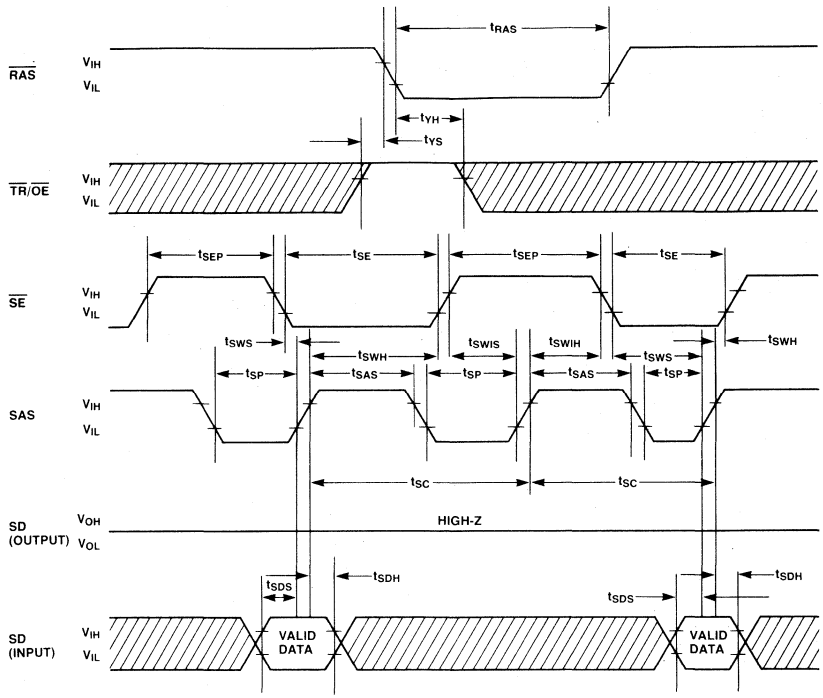


IN THE CASE OF $\overline{SE}$ = "L"

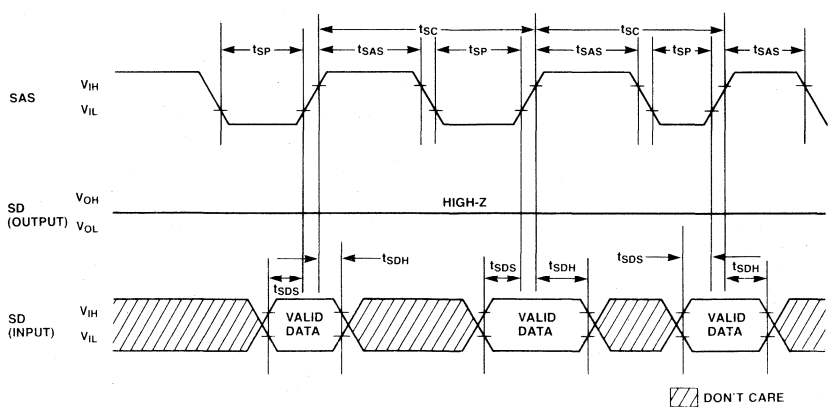


DON'T CARE
INVALID DATA

Serial Write Cycle



IN THE CASE OF $\overline{SE}$ = "L"



Preliminary

FUJITSU

■ MB81464-10, MB81464-12, MB81464-15

NMOS 65,536 Word By 4-Bit Dynamic Random Access Memory

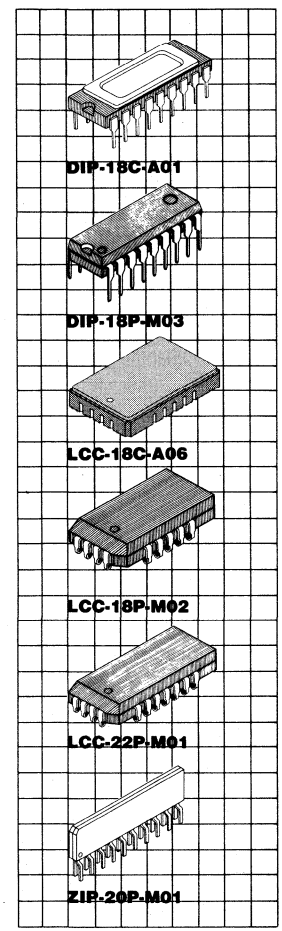
Description

The Fujitsu MB81464 is a fully decoded, dynamic NMOS random access memory organized as 65,536 words by 4 bits. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MB81464 to be housed in a standard 18-pin DIP and 18-pad LCC. Other package options include a 20-pin plastic zig zag in-line package, 18 and 22-pin PLCC packages, and a 22-pad LCC. Additionally, the MB81464 offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability. The MB81464 also features "page mode" which allows high speed random access up to 256 bits within a same row.

The MB81464 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

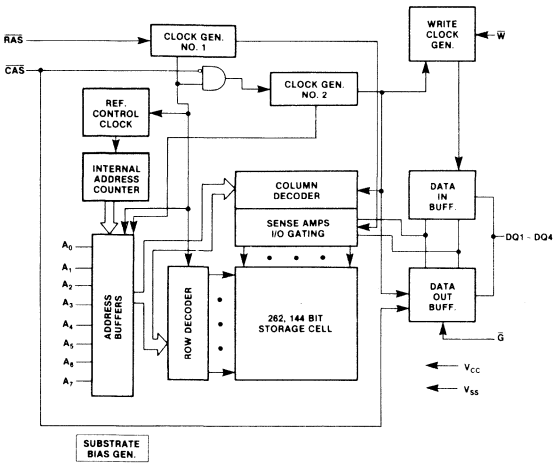
Clock timing requirements are non-critical, and power supply tolerance is very wide. All inputs and outputs are TTL compatible.

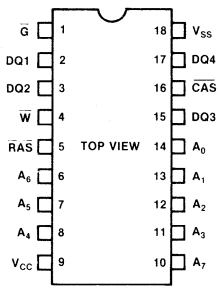


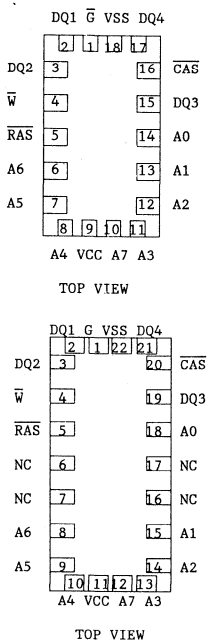
Features

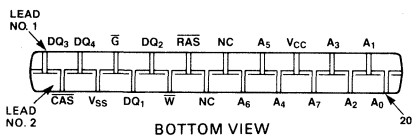
- **65,536 x 4 RAM, 18 pin package**
- **Silicon-gate, Triple Poly NMOS, single transistor cell**
- **Row access time**
  100 ns max. (MB81464-10)
  120 ns max. (MB81464-12)
  150 ns max. (MB81464-15)
- **Cycle time**
  200 ns min. (MB81464-10)
  220 ns min. (MB81464-12)
  260 ns min. (MB81464-15)
- **Single +5V Supply, ±10% tolerance**
- **Low power, (Active)**
  385mW max. (MB81464-10)
  358mW max. (MB81464-12)
  314mW max. (MB81464-15)
  27.5mW max. (standby)
- **On chip substrate bias generator for high performance**
- **All inputs TTL compatible**
- **Three state TTL compatible outputs**
- **4ms/256 refresh cycles**
- **Output unlatched at cycle end**
- **Early Write or $\overline{G}$ to Control Output buffer impedance**
- **"$\overline{CAS}$-before-$\overline{RAS}$ and $\overline{RAS}$-Only refresh capability**
- **Read-Modify-Write, page mode capability**
- **On-chip latches for Address and DQ**

MB81464 Block Diagram and Pin Assignments









Absolute Maximum Rating
(See Note)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	−1 to +7	V
Storage temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	
Power dissipation		P_D	1.0	W
Short circuit output current		—	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Capacitance ($T_A = 25\,°C$)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance $A_0 \sim A_7$	C_{IN1}	—	7	pF
Input Capacitance RAS, W, G, CAS	C_{IN2}	—	10	pF
Data I/O Capacitance DQ1 ~ DQ4	C_D	—	7	pF

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to 70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs except DQ	V_{IL}	−2.0	—	0.8	V	
Input Low Voltage, DQ	V_{ILD}*	−1.0	—	0.8	V	

*The device will withstand undershoots to the −2.0V level with a maximum pulse width of 20ns at the −1.5V level.

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81464-10 Min	MB81464-10 Max	MB81464-12 Min	MB81464-12 Max	MB81464-15 Min	MB81464-15 Max	Unit
Operating current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		70		65		57	mA
Standby current Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		5.0		5.0		5.0	mA
Refresh current 1* Average power supply current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	I_{CC3}		60		55		50	mA
Page mode current* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling; t_{PC} = min)	I_{CC4}		40		35		30	mA
Refresh current 2* Average power supply current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min)	I_{CC5}		65		60		55	mA
Input leakage current Input leakage current, any input (0 ≤ V_{IN} ≤ 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test—0V)	$I_{I(L)}$	−10	10	−10	10	−10	10	μA
Output leakage current (Data out is disabled, 0V ≤ V_{OUT} = 5.5V)	$I_{DQ(L)}$	−10	10	−10	10	−10	10	μA
Output levels Output high voltage (I_{OH} = −5mA)	V_{OH}	2.4		2.4		2.4		V
Output low voltage (I_{OL} = 4.2mA)	V_{OL}		0.4		0.4		0.4	

Note: * I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is dependent on input low voltage level V_{ILD}. V_{ILD} > −0.5V.

AC Characteristics[*1,2,3]
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81464-10 Min	MB81464-10 Max	MB81464-12 Min	MB81464-12 Max	MB81464-15 Min	MB81464-15 Max	Unit
Time between refresh	t_{REF}		4		4		4	ms
Random read/write cycle time	t_{RC}	200		220		260		ns
Read-modify-write cycle time	t_{RWC}	270		305		345		ns
Page mode cycle time	t_{PC}	100		120		145		ns
Page mode read-modify-write cycle time	t_{PRWC}	170		195		225		ns
Access time from $\overline{RAS}$[*4,6]	t_{RAC}		100		120		150	ns
Access time from $\overline{CAS}$[*5,6]	t_{CAC}		50		60		75	ns
Output buffer turn off delay	t_{OFF}	0	25	0	25	0	30	ns
Transition time	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	80		90		100		ns
$\overline{RAS}$ pulse width	t_{RAS}	100	100000	120	100000	150	100000	ns
$\overline{RAS}$ hold time	t_{RSH}	50		60		75		ns
$\overline{CAS}$ precharge time (page mode only)	t_{CP}	40		50		60		ns
$\overline{CAS}$ precharge time (all cycles except page mode)	t_{CPN}	30		32		35		ns
$\overline{CAS}$ pulse width	t_{CAS}	50	100000	60	100000	75	100000	ns
$\overline{CAS}$ hold time	t_{CSH}	100		120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ delay time[*7,8]	t_{RCD}	20	50	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ set up time	t_{CRS}	10		10		10		ns
Row address set up time	t_{ASR}	0		0		0		ns
Row address hold time	t_{RAH}	10		12		15		ns
Column address set up time	t_{ASC}	0		0		0		ns
Column address hold time	t_{CAH}	15		20		25		ns
Read command set up time	t_{RCS}	0		0		0		ns
Read command hold time referenced to $\overline{RAS}$[*10]	t_{RRH}	10		15		20		ns
Read command hold time referenced to $\overline{CAS}$[*10]	t_{RCH}	0		0		0		ns
Write command set up time	t_{WCS}	−5		−5		−5		ns
Write command hold time	t_{WCH}	25		30		35		ns
Write command pulse width	t_{WP}	25		30		35		ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	35		40		45		ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	35		40		45		ns
Data in set up time	t_{DS}	0		0		0		ns
Data in hold time	t_{DH}	25		30		35		ns

See note on the following pages.
*These symbols are described in IEE 662-1980: IEE Standard terminology for semiconductor memory.

AC Characteristics,
(continued)

Parameter	Symbol	MB81464-10 Min	MB81464-10 Max	MB81464-12 Min	MB81464-12 Max	MB81464-15 Min	MB81464-15 Max	Unit
Access time from $\overline{G}$	t_{OEA}		27		30		40	ns
$\overline{G}$ to data in delay time	t_{OED}	25		25		30		ns
Output buffer turn off delay from $\overline{G}$	t_{OEZ}	0	25	0	25	0	30	ns
$\overline{G}$ hold time referenced to $\overline{W}$	t_{OEH}	0		0		0		ns
$\overline{CAS}$ set up time referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{FCS}	20		20		20		ns
$\overline{CAS}$ hold time referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{FCH}	20		25		30		ns
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	10		10		10		ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CPR}	30		30		30		ns
$\overline{G}$ to $\overline{RAS}$ in active setup time	t_{OES}	0		0		0		ns
IN to $\overline{CAS}$ delay time*11	t_{DZC}	0		0		0		ns
IN to $\overline{G}$ delay time*11	t_{DZO}	0		0		0		ns

Notes:
*1 An initial pause of 200 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

*2 AC characteristics assume t_T = 5 ns.

*3 V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min.) and V_{IL} (max.).

*4 Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.

*5 Assumes that $t_{RCD} \geq t_{RCD}$ (max.).

*6 Measured with a load equivalent to 2 TTL loads and 100 pF.

*7 Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

*8 t_{RCD} (min.) = t_{RAH} (min.) + $2t_T$(t_T = 5 ns) + t_{ASC} (min.).

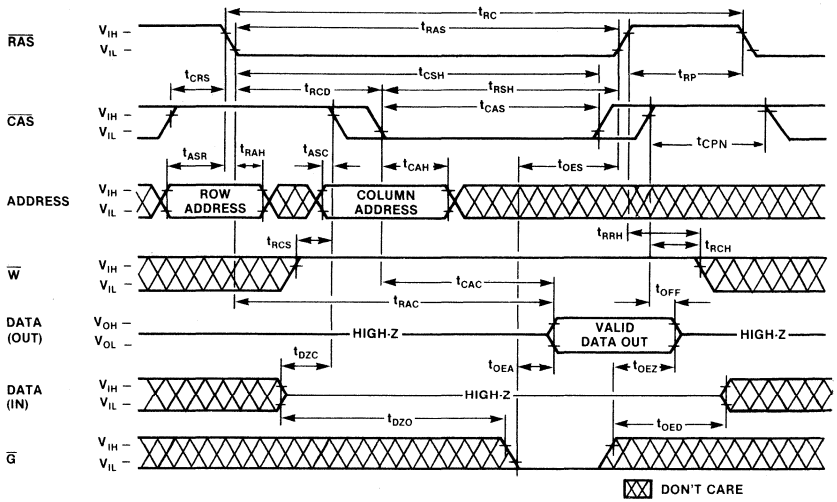
*9 t_{WCS} is not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.

*10 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

*11 Either t_{DZC} or t_{DZO} must be satisfied for all cycles.

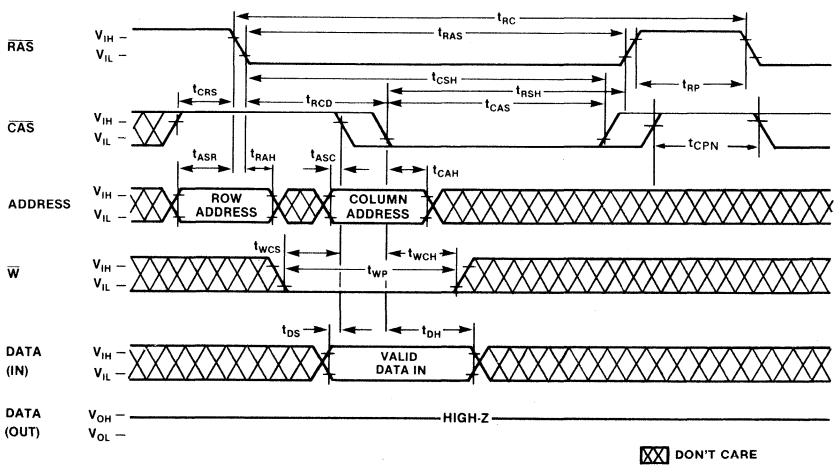
Timing Diagrams

Read Cycle



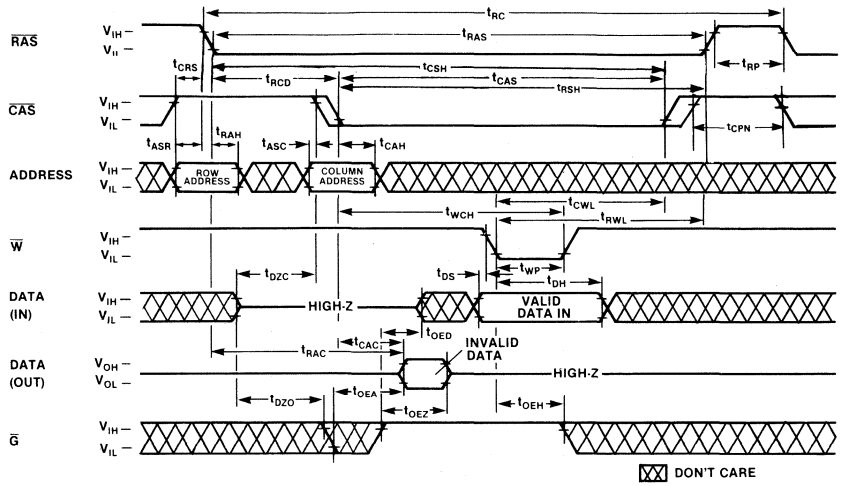
Write Cycle (Early Write)

$\overline{G}$: Don't Care

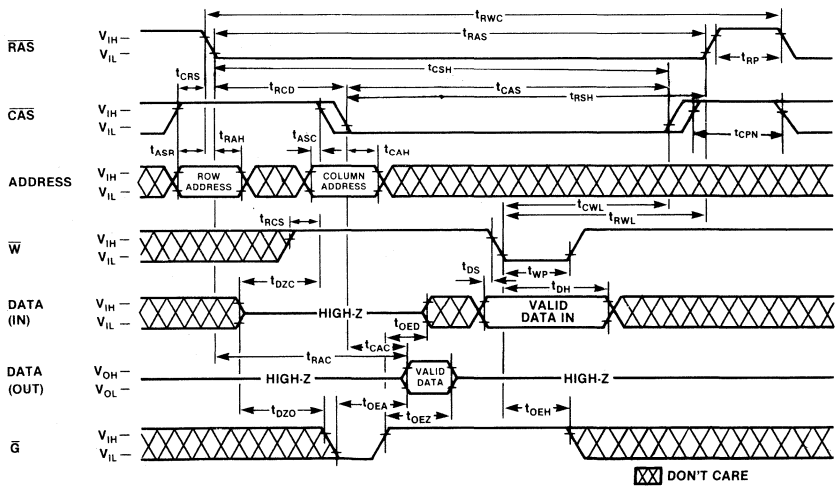


Timing Diagrams
(Continued)

$\overline{G}$ Write Cycle

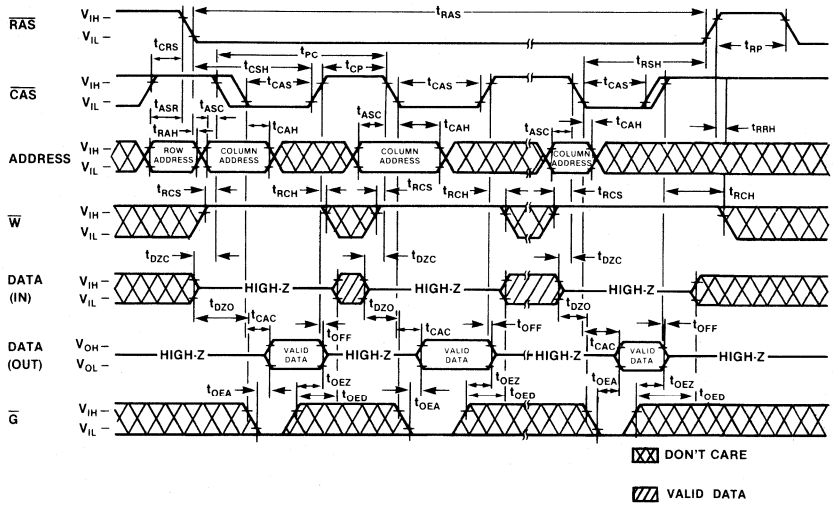


Read-Modify-Write Cycle

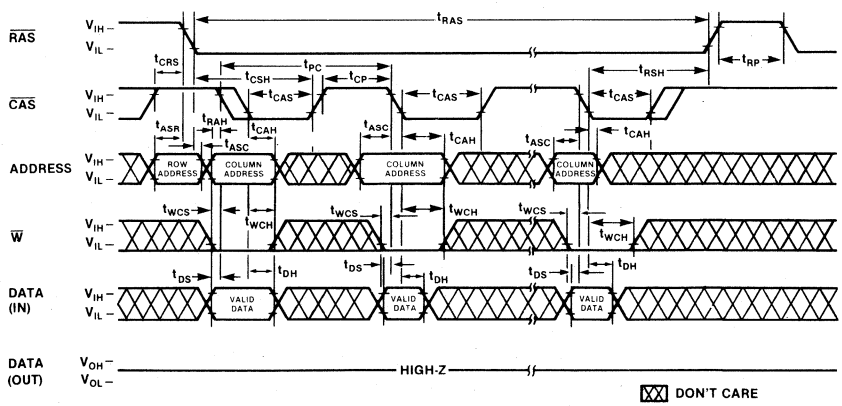


Timing Diagrams
(Continued)

Page Mode Read Cycle

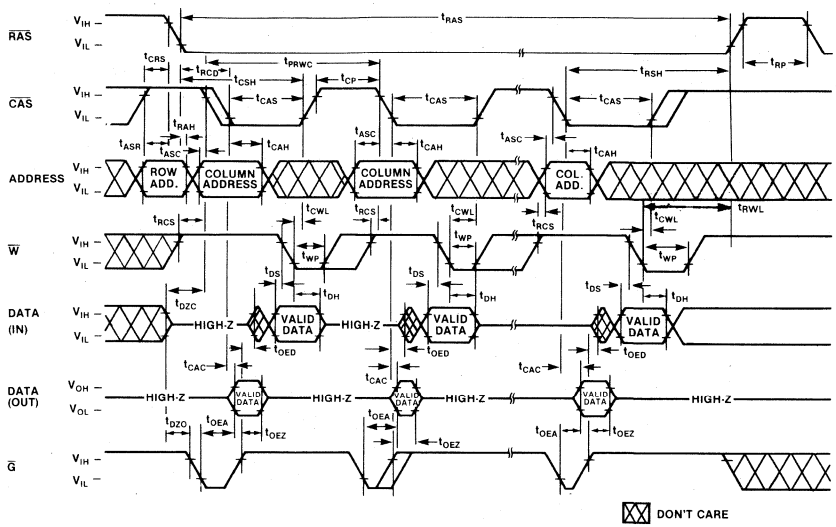


Page Mode Write Cycle
($\overline{G}$ = Don't Care)

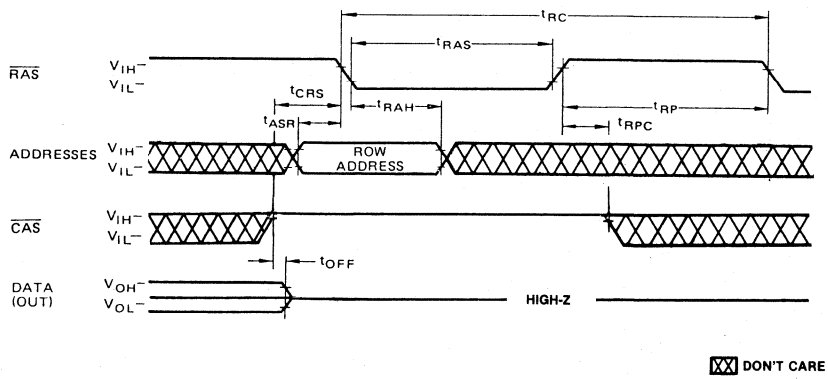


Timing Diagrams
(Continued)

Page Mode Read-Modify-Write Cycle



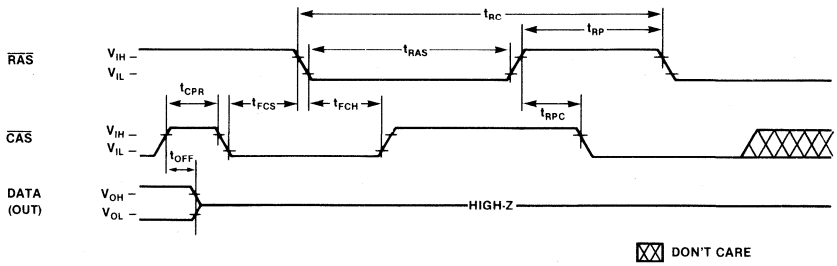
RAS-Only Refresh Cycle
(WE, OE = Don't Care)



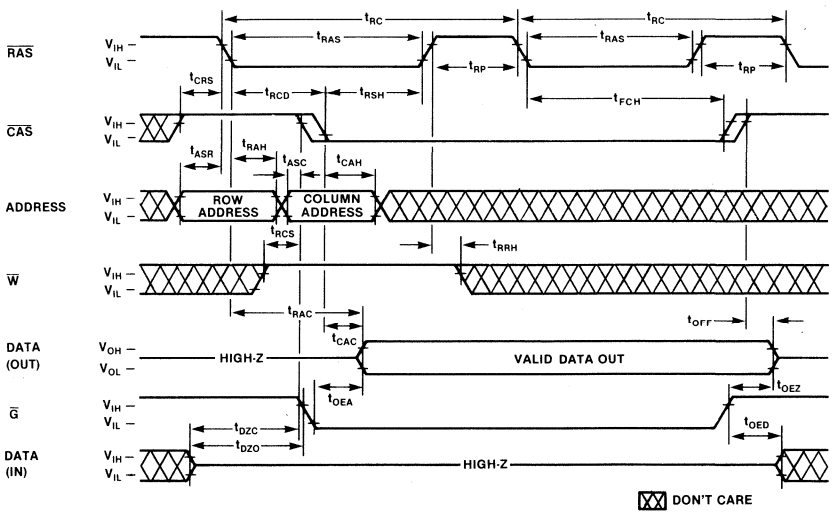
Timing Diagrams
(Continued)

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

Note: Address, $\overline{W}$, $\overline{G}$ = Don't Care



Hidden Refresh Cycle



Description

Address Inputs:

A total of sixteen binary input address bits are required to decode parallel 4 bits of 262144 storage cell locations within the MB 81464.

Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins (A_0 through A_7) and latched with the Column Address Strobe ($\overline{CAS}$).

The row and column address inputs must be stable on or before the falling edge of $\overline{RAS}$ and $\overline{CAS}$, respectively. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the Write Enable ($\overline{W}$) input. A high on $\overline{W}$ selects read mode and low selects write mode. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data-outs will remain in the high-impedance state allowing a write cycle.

Data Pins:

Data Inputs:

Data is written during a write or read-modify-write cycle. The falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data !atches. In early-write cycle, $\overline{W}$ brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to $\overline{CAS}$. In a read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to $\overline{W}$.

In a read-modify-write cycle, $\overline{G}$ must be low after t_{DZO} to change the data pins from input mode to output mode and then $\overline{G}$ must be changed to high before t_{OED} to return the data pins to input mode. In an early write cycle, data pins are in input mode regardless of the status of $\overline{G}$.

Data Outputs:

The three-state output buffers provide direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The outputs are in the high-impedance state until $\overline{CAS}$ is brought low. In a read cycle, the outputs go active after the access time interval t_{RAC} and t_{OEA} are satisfied. The outputs become valid after the access time has elapsed and remain valid while $\overline{CAS}$ and $\overline{G}$ are low. In a read operation, either $\overline{G}$ or $\overline{CAS}$ returning high brings the outputs into the high impedance state.

Output Enable:

The $\overline{G}$ controls the impedance of the output buffers. In the high state on $\overline{G}$, the output buffers are high impedance state, input mode. In the low state on $\overline{G}$, the output buffers are low impedance state, output mode. But in early write cycle, the output buffers are in high impedance state even if $\overline{G}$ is low. In the page mode read cycle, $\overline{G}$ can be allowed low through the cycle. In the page mode early write cycle, $\overline{G}$ can be allowed high throughout the cycle. In the page mode read-modify-write or delayed write cycle, $\overline{G}$ must be changed from low to high with t_{OED}.

Page Mode:

Page Mode operation permits strobing the row-address into the MB81464 while maintaining $\overline{RAS}$ at a low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$-only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 ~ A_7) at least every 4 ms. The $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each 256 row-addresses (A_0 ~ A_7) with $\overline{RAS}$ will cause bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh:

$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB81464 offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place.

After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

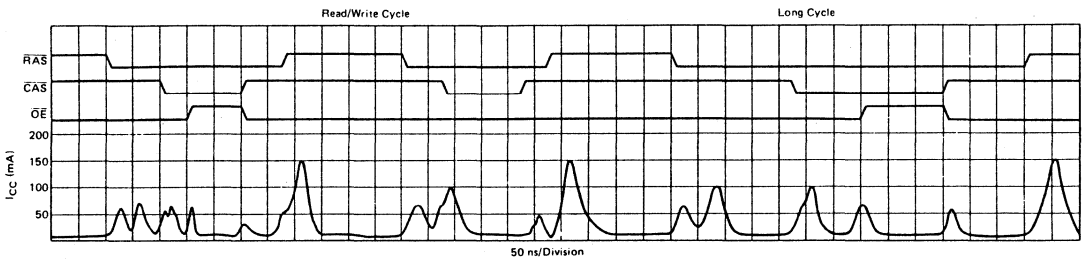
Hidden Refresh:

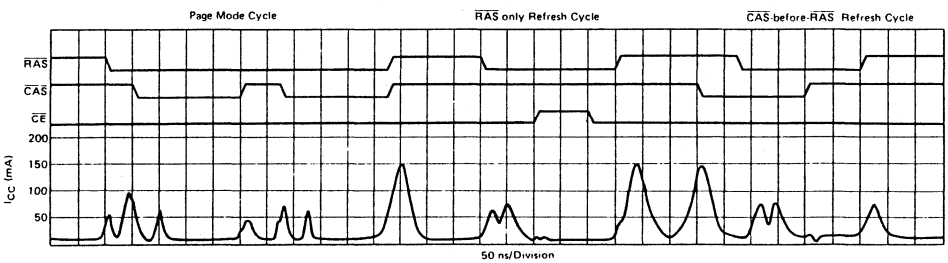
Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time.

In the MB81464, hidden refresh means $\overline{CAS}$-before-$\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses i.e., it doesn't need to apply refresh addresses, because $\overline{CAS}$ is always low when RAS goes to low in this mode.

Typical Characteristics Curves

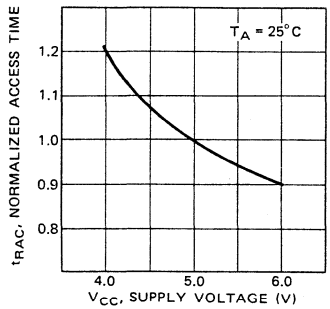
CURRENT WAVEFORM (V_{CC} = 5.5 V, T_A = 25°C)



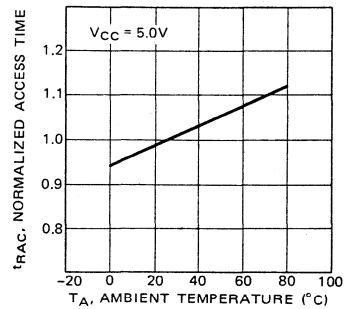


Typical Characteristics Curves
(Continued)

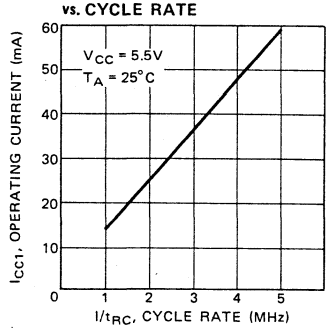
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



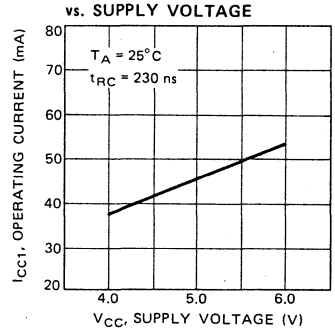
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



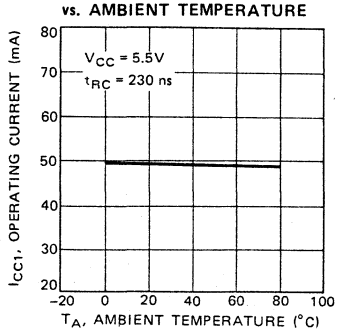
OPERATING CURRENT vs. CYCLE RATE



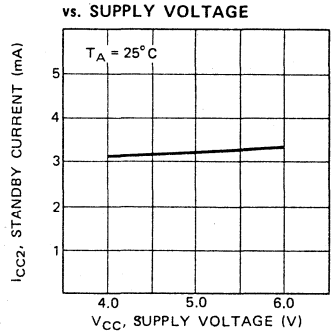
OPERATING CURRENT vs. SUPPLY VOLTAGE



OPERATING CURRENT vs. AMBIENT TEMPERATURE

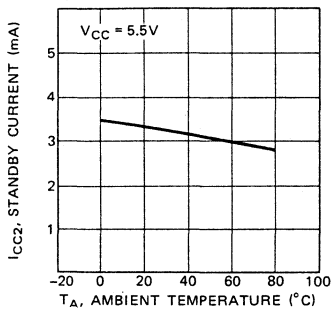


STANDBY CURRENT vs. SUPPLY VOLTAGE

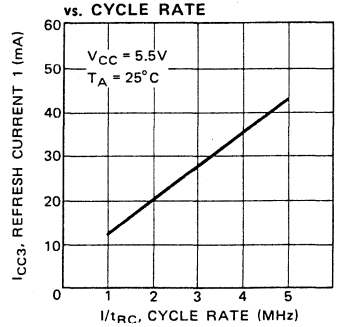


Typical Characteristics Curves
(Continued)

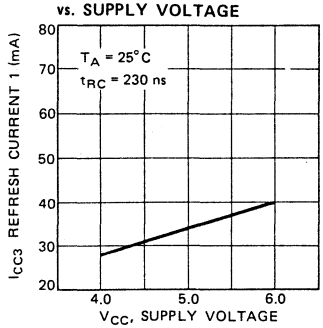
STANDBY CURRENT
vs. AMBIENT TEMPERATURE



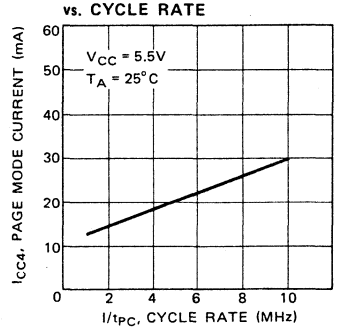
REFRESH CURRENT 1
vs. CYCLE RATE



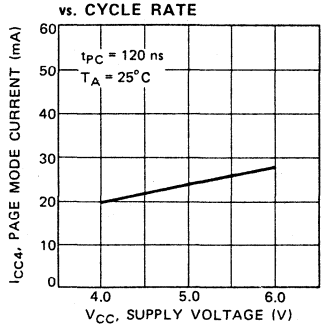
REFRESH CURRENT 1
vs. SUPPLY VOLTAGE



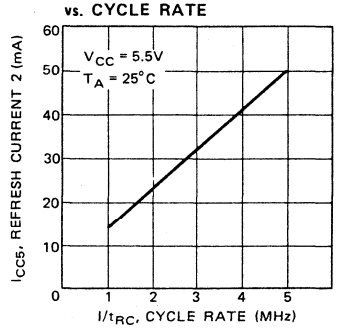
PAGE MODE CURRENT
vs. CYCLE RATE



PAGE MODE CURRENT
vs. CYCLE RATE

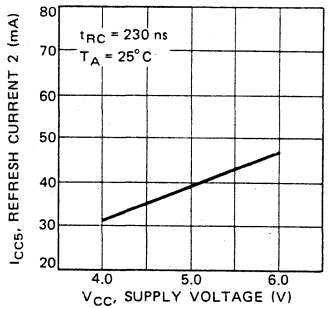


REFRESH CURRENT 2
vs. CYCLE RATE

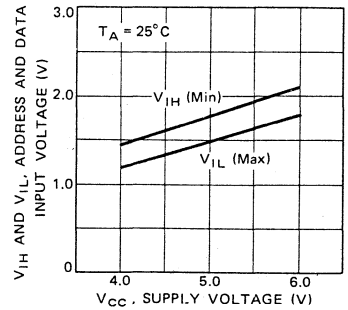


Typical Characteristics Curves
(Continued)

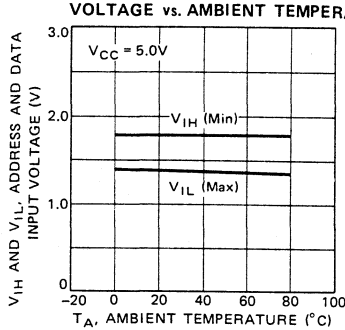
REFRESH CURRENT 2 vs. SUPPLY VOLTAGE



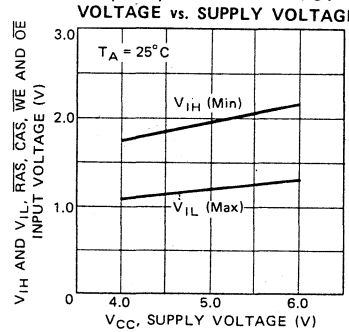
ADDRESS AND DATA INPUT VOLTAGE vs. SUPPLY VOLTAGE



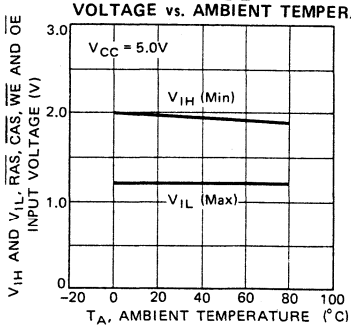
ADDRESS AND DATA INPUT VOLTAGE vs. AMBIENT TEMPERATURE



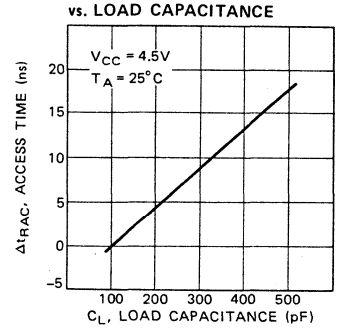
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ AND $\overline{OE}$ INPUT VOLTAGE vs. SUPPLY VOLTAGE



$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ AND $\overline{OE}$ INPUT VOLTAGE vs. AMBIENT TEMPERATURE

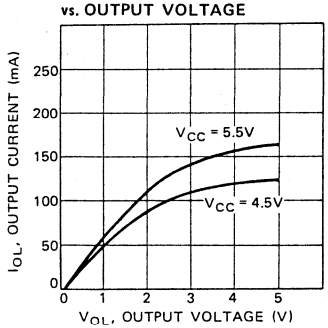


ACCESS TIME vs. LOAD CAPACITANCE

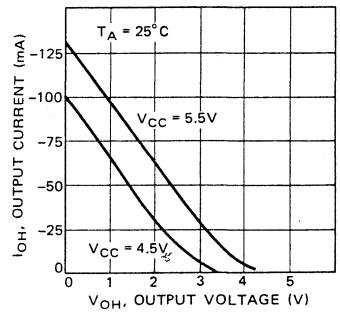


Typical Characteristics Curves
(Continued)

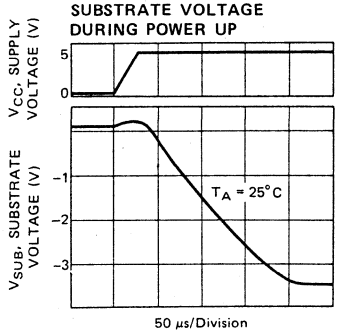
OUTPUT CURRENT vs. OUTPUT VOLTAGE



OUTPUT CURRENT vs. OUTPUT VOLTAGE

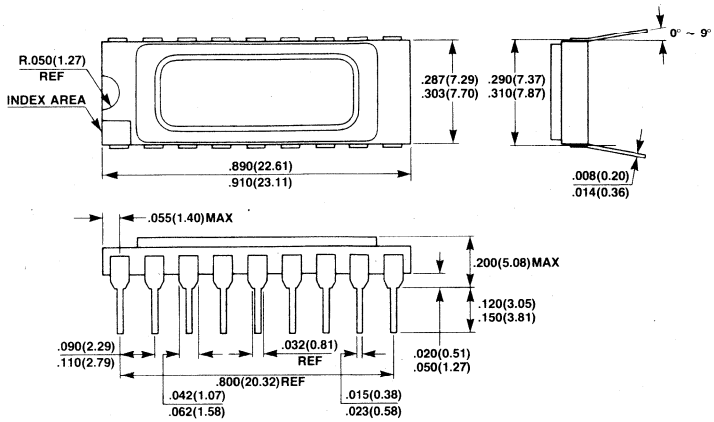


SUBSTRATE VOLTAGE DURING POWER UP

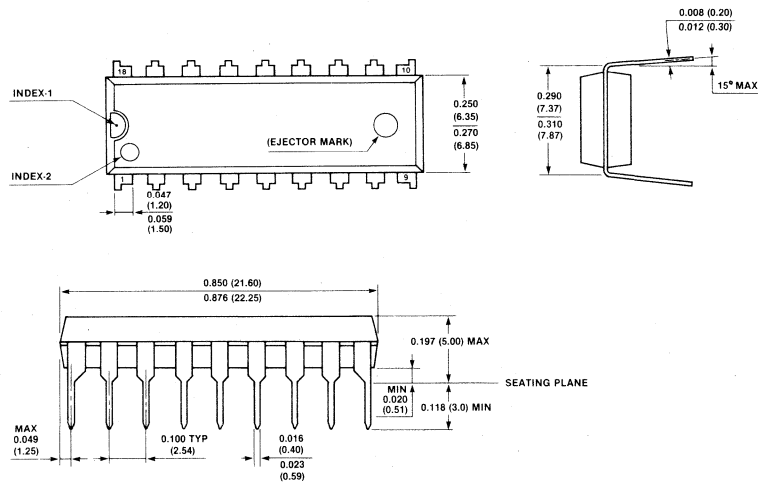


Package Dimensions
Dimensions in inches
(millimeters)

18-Lead Ceramic (Metal Seal) Dual In-Line Package
(Case No.: DIP-18C-A01)

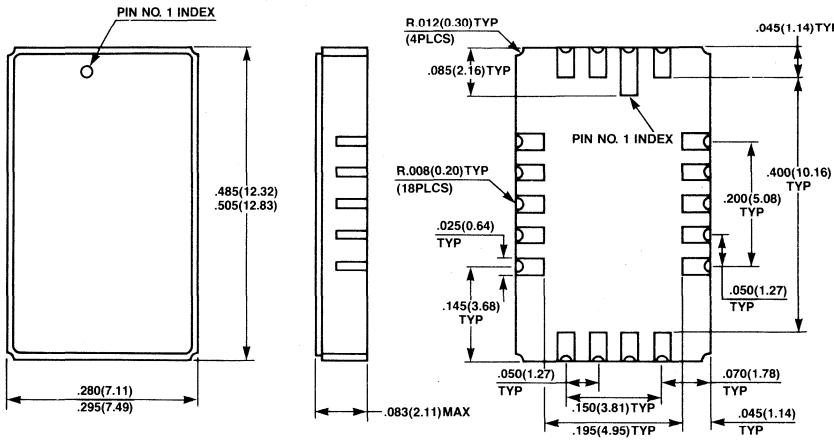


18 Lead Plastic Dual-In-Line Package
DIP-18P-M03

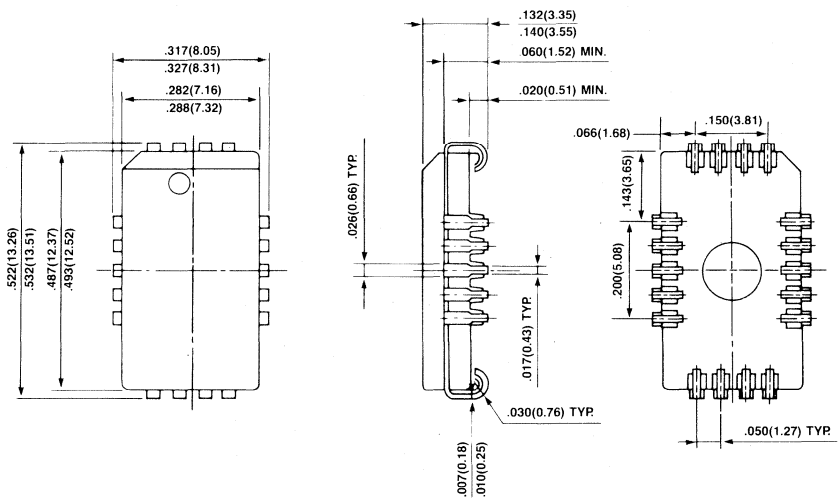


Package Dimensions
Dimensions in inches
(millimeters)

18-Pad Ceramic (Metal Seal) Leadless Chip Carrier
(Case No.: LCC-18C-A06)

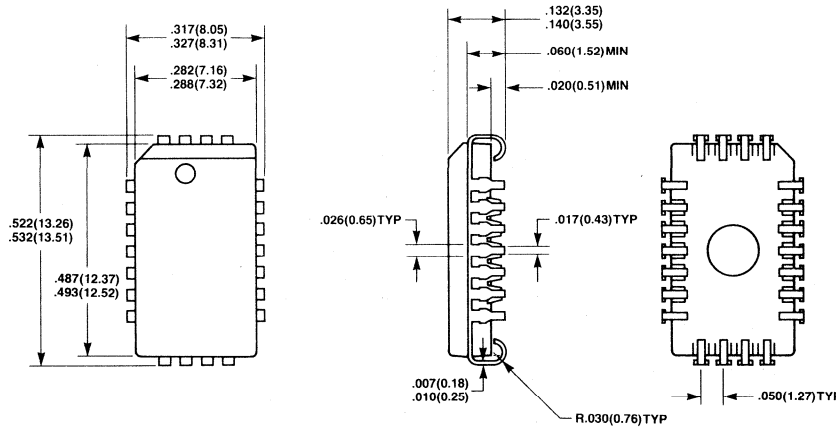


18-Lead Plastic Chip Carrier
(Case No.: LCC-18P-M02)

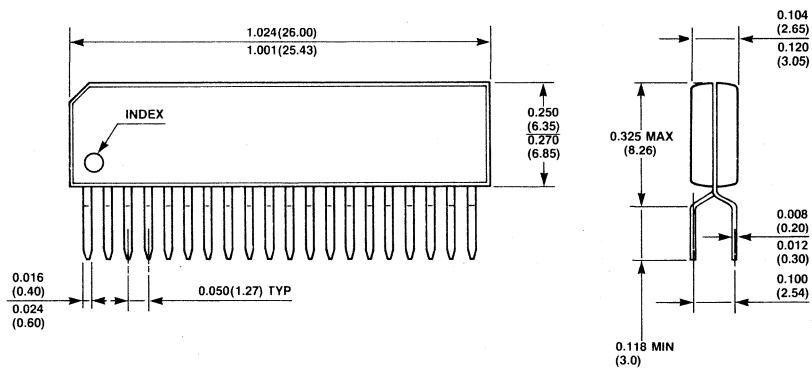


Package Dimensions
Dimensions in inches
(millimeters)

22-Lead Plastic Chip Carrier
(Case No.: LCC-22P-M01)



20-Lead Plastic ZigZag-In-Line Package
(Case No.: ZIP-20P-M01)



Preliminary

MOS Memories

FUJITSU

■ MB811000-12, MB811000-15

1,048,576-Bit Dynamic Random Access Memory

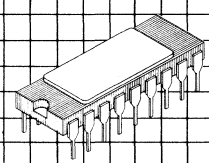
Description

The Fujitsu MB811000 is a fully decoded, dynamic NMOS random access memory organized as 1,048,576 one-bit words. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

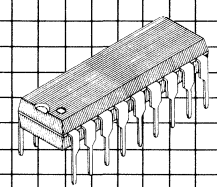
The MB811000 features "page mode" which allows high speed random access of up to 1024-bits within the same row. Additionally, the MB811000 offers new functional enhancements that make it more versatile than previous dynamic RAMs. Multiplexed row and column address inputs permits the MB811000 to be housed in a Jedec standard 18-pin dual in-line package or 20 lead SOJ package.

The MB811000 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-layer Polysilicon process. This process, coupled with an innovative stacked capacitor memory cell, permits maximum circuit density and minimal chip size. Dynamic circuitry is used in the design, including dynamic sense amplifiers.

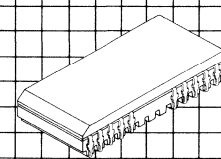
Clock timing requirements are noncritical, and the power supply tolerance is very wide. All inputs are TTL compatible.



Ceramic Package
DIP-18C-A01



Plastic Package
DIP-18P-M03

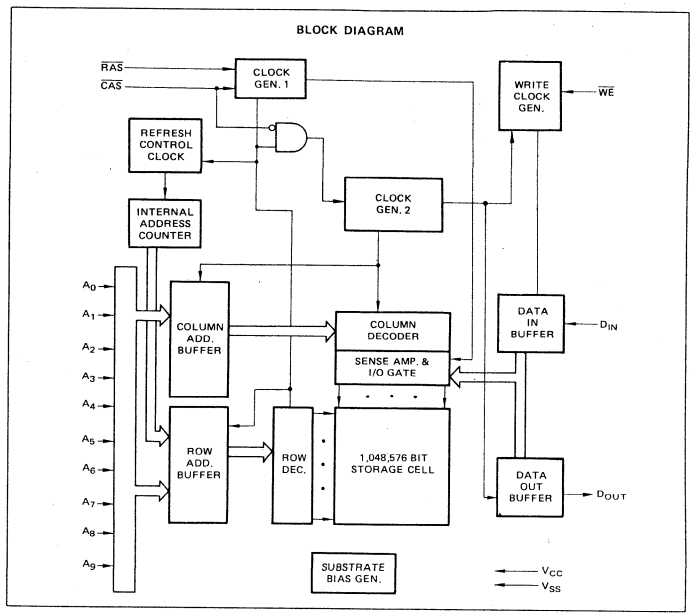


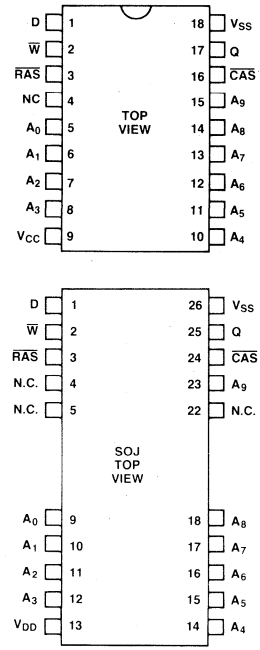
SOJ Package

Features

- 1,048,576 x 1-bit organization
- Silicon-gate, NMOS, single transistor cell
- Access time (t_{RAC})
  120 ns max. (MB811000-12)
  150 ns max. (MB811000-15)
- Cycle time (t_{RC})
  230 ns min. (MB811000-12)
  260 ns min. (MB811000-15)
- Page cycle time (t_{PC})
  120 ns min. (MB811000-12)
  150 ns min. (MB811000-15)
- Single 5V supply, ±10% tolerance
- Low power dissipation
  550 mW max. (MB811000-12)
  490 mW max. (MB811000-15)
  25 mW max. at standby
- Refresh 8 ms/512 cycles
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$ and hidden refresh capability
- High speed read-write cycle capability
- Output unlatched at cycle end allows two dimensional chip select
- On chip address and data-in latches
- Industry standard 18-pin DIP package

MB811000 Block Diagram and Pin Assignment





Absolute Maximum Ratings

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} relative to V_{SS}		V_{CC}	−1 to +7	V
Storage temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	
Power dissipation		P_D	1.0	W
Short circuit output current			50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Recommended Operating Conditions

(Referenced to V_{SS})

Parameter	Symbol	Value Min	Value Typ	Value Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C (ambient)
	V_{SS}	0	0	0	V	
Input High Voltage All Inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage All Inputs	V_{IL}	−2.0		0.8	V	

Capacitance
($T_A = 25\,°C$)

Parameter	Symbol	Value Min	Value Typ	Value Max	Unit
Input Capacitance A_0 to A_8, D	C_{IN1}			7	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$	C_{IN2}			8	pF
Output Capacitance Q	C_{OUT}			7	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB811000-12 Min	MB811000-12 Max	MB811000-15 Min	MB811000-15 Max	Unit
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min.)	I_{CC1}		100		90	mA
STANDBY CURRENT Power Supply Current ($\overline{RAS}/\overline{CAS} = V_{IH}$)	I_{CC2}		4.5		4.5	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$; t_{RC} = Min.)	I_{CC3}		90		80	mA
PAGE MODE CURRENT* Average Power Supply Current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; t_{PC} = Min.)	I_{CC4}		45		40	mA
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = Min.)	I_{CC5}		90		80	mA
INPUT LEAKAGE CURRENT Any Input, (V_{IN} = 0V to 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)	I_{IL}	−10	10	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data is disabled, V_{OUT} = 0V to 5.5V)	I_{OL}	−10	10	−10	10	μA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}		0.4		0.4	V
OUTPUT LEVEL Output High Voltage (I_{OH} = −5.0 mA)	V_{OH}	2.4		2.4		V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol Alternate	Symbol *Standard	MB811000-12 Min	MB811000-12 Max	MB811000-15 Min	MB811000-15 Max	Unit
Time between Refresh		t_{REF}	TRVRV		8		8	ms
Random Read/Write Cycle Time		t_{RC}	TRELREL	230		260		ns
Read-Write Cycle Time		t_{RWC}	TRELREL	285		325		ns
Access Time from $\overline{RAS}$ *4,6		t_{RAC}	TRELQV		120		150	ns
Access Time from $\overline{CAS}$ *5,6		t_{CAC}	TCELQV		60		75	ns
Output Buffer Turn off Delay		t_{OFF}	TCEHQZ	0	25	0	35	ns
Transition Time		t_T	TT	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	TREHREL	100		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	TRELREH	120	100000	150	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	TCELREH	60		75		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	TCELCEH	60	100000	75	100000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	TRELCEH	120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time *4,7		t_{RCD}	TRELCEL	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	TCEXREL	0		0		ns
Row Address Set Up Time		t_{ASR}	TAVREL	0		0		ns
Row Address Hold Time		t_{RAH}	TRELAX	12		15		ns
Column Address Set Up Time		t_{ASC}	TAVCEL	0		0		ns
Column Address Hold Time		t_{CAH}	TCELAX	20		25		ns
Read Command Set Up Time		t_{RCS}	TWHCEL	0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$ *10		t_{RCH}	TCEHWX	0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$ *10		t_{RRH}	TREHWX	20		20		ns
Write Command Set Up Time *8		t_{WCS}	TWLCEL	0		0		ns
Write Command Pulse Width		t_{WP}	TWLWH	20		25		ns
Write Command Hold Time		t_{WCH}	TCELWH	20		25		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	TWLREH	50		60		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	TWLCEH	50		60		ns
Data In Set Up Time		t_{DS}	TDVCEL	0		0		ns
Data In Hold Time		t_{DH}	TCELDX	20		25		ns
$\overline{CAS}$ to $\overline{W}$ Delay *8		t_{CWD}	TCELWL	60		75		ns
$\overline{CAS}$ Precharge Time (Normal Cycle)		t_{CPN}		22		25		ns
$\overline{RAS}$ to $\overline{W}$ Delay *8		t_{RWD}		120		150		ns

Notes:
*1. An initial pause of 200 μs is required after power up, followed by any 8 $\overline{RAS}$ cycles, before proper device operation is achieved. If the internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh initialization cycles are required.
*2. AC characteristics assume t_T = 5 ns.
*3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
*4. t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$ (Max.) the specified maximum value of t_{RAC} (Max.) can be met. If $t_{RCD} > t_{RCD}$ (Max.) then t_{RAC} in increased by the amount that t_{RCD} exceeds t_{RCD} (Max.)
*5. Assumes that $t_{RCD} > t_{RCD}$ (Max.).
*6. Measured with a load equivalent to 2 TTL loads and 100 pF.
*7. t_{RCD} (Min.) = t_{RAH} (Min.) + 2 t_T + t_{ASC} (Min.).
*8. t_{WCS} and t_{CWD} are non restrictive operating parameters, and are included in the data sheet as elecrical characteristics only. If $t_{WCS} > t_{WCS}$ (Min.), the cycle is an early write cycle, and the data out pin will remain open circuit (High Impedance) throughout the entire cycle.
If $t_{CWD} > t_{CWD}$ (Min.), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.
*10. Either t_{RCH} or t_{RRH} must be satisifed for a read cycle.

AC Characteristics

(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol Alternate	Symbol *Standard	MB811000-12 Min	MB811000-12 Max	MB811000-15 Min	MB811000-15 Max	Unit
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$		t_{FCS}	TCELREL	0		0		ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$		t_{FCH}	TRELCEX	20		20		ns
Page Mode Read/Write Cycle Time		t_{PC}	TCELCEL	120		150		ns
Page Mode Read-Write Cycle Time		t_{PRWC}	TCEHCEH	175		215		ns
Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	TCEHCEL	50		65		ns
RAS Precharge to $\overline{CAS}$ Active Time		t_{RPC}	TREHCEL	20		20		ns
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle		t_{CPR}	TCEHCEL	25		30		ns

Notes: *These symbols are described in IEEE STD. 662-1980: IEEE Standard terminology for semiconductor memory.

Description

Simplified Timing Requirement

The MB811000 has improved circuitry that eases timing requirements for high speed access operations. The MB811000 can operate under the conditions of t_{RCD} (max.) = t_{CAC}, thus providing optimal timing for address multiplexing. In addition, the MB811000 has minimal hold times for Addresses (t_{CAH}), Write-Enable (t_{WCH}) and Data-in (t_{DH}). The MB811000 provides higher throughput in inter-leaved memory system applications. Fujitsu has made the timing requirements that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the Column Address, D and $\overline{W}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{W}$ Delay) are not restricted by t_{RCD}.

Fast Read-Write Cycle

The MB811000 has a fast read-modify-write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{W}$ when $\overline{CAS}$ goes "low". When $\overline{W}$ is "low", the MB811000 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. When $\overline{W}$ goes "low", after t_{CWD} following a $\overline{CAS}$ transition to "low", the MB811000 goes into the delayed write mode. The output then contains the data from the cell selected and the data from D is written into the cell selected. Therefore, a very fast read-write cycle (t_{RWC} = t_{RC}) is possible with the MB811000.

Address Inputs

A total of twenty binary input address bits are required to decode any 1 of 1,048,576 cell locations within the MB811000. Ten row-address bits are established on the input pins (A_0 through A_9) and are latched with the Row Address Strobe ($\overline{RAS}$). Ten column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All row addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold/Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

Write Enable

The read or write mode is selected with the $\overline{W}$ input. A logic "high" on $\overline{W}$ dictates read mode. A logic "low" dictates write mode. The data input is disabled when the read mode is selected.

Data Input

Data is written into the MB811000 during a write or read-write cycle. The last falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the data-in (D) register. In a write cycle, if $\overline{W}$ is brought "low" (write mode) before $\overline{CAS}$, D is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{W}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D is strobed by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when $t_{RCD(max)}$ is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after $t_{RCD(max)}$. Data remains valid until $\overline{CAS}$ in returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Description
(Continued)

Page Mode

Page mode operation permits strobing the row address into the MB811000 while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row address doesn't change. Thus, the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

$\overline{RAS}$-Only Refresh

Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 512 row-addresses ($A_0 \sim A_8$) at least every 8 ms. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought "low". Strobing each of the 512 row-addresses ($A_0 \sim A_8$) with $\overline{RAS}$ will cause all bits in each row to be refreshed. $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh

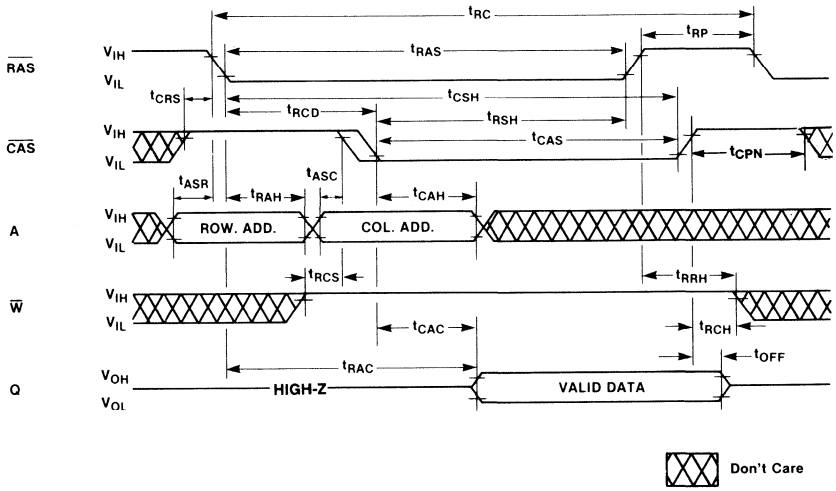
$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB811000 offers an alternate refresh method. If $\overline{CAS}$ is held "low" for the specified period (t_{FCS}) before $\overline{RAS}$ goes to "low", on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Hidden Refresh

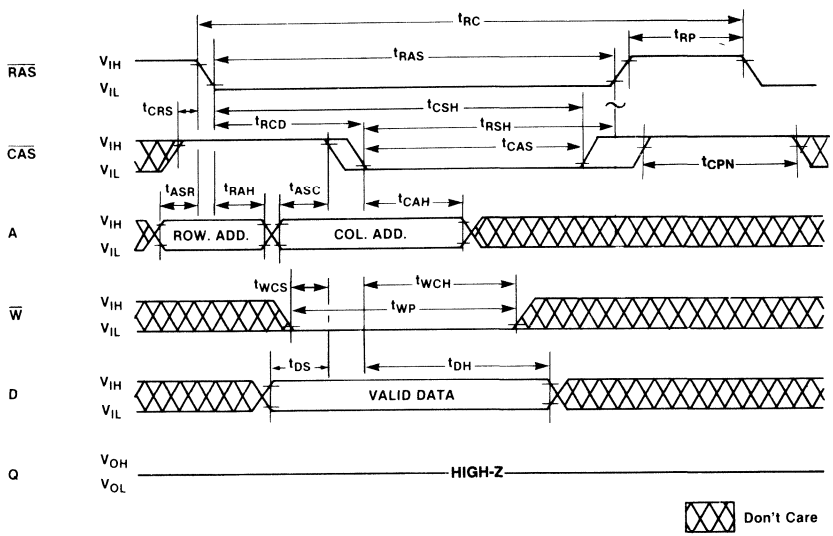
A hidden refresh cycle may take place while maintaining the latest valid data at the out-put by extending the $\overline{CAS}$ active time. For the MB811000, a hidden refresh cycle is a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The internal refresh address counter provides the refresh addresses as in a normal $\overline{CAS}$-before-$\overline{RAS}$ cycle.

Timing Diagrams

Read Cycle

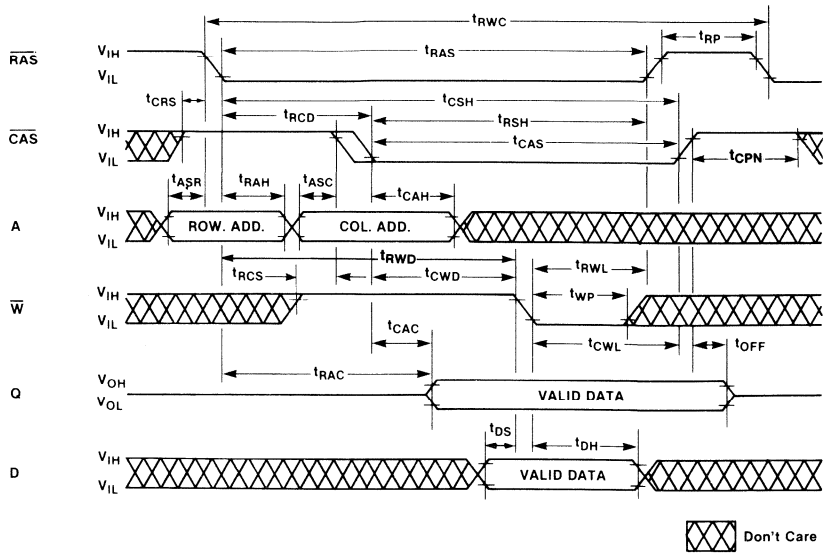


Write Cycle (Early Write)



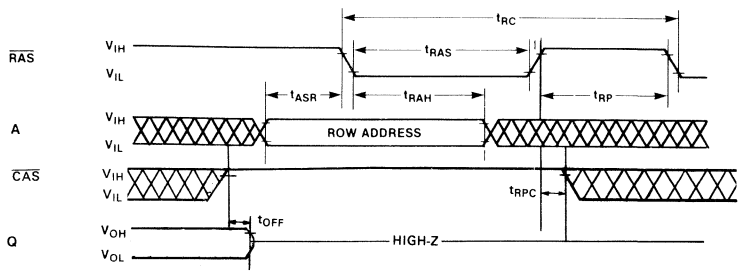
Timing Diagrams
(Continued)

Read-Write/Read-Modify-Write Cycle



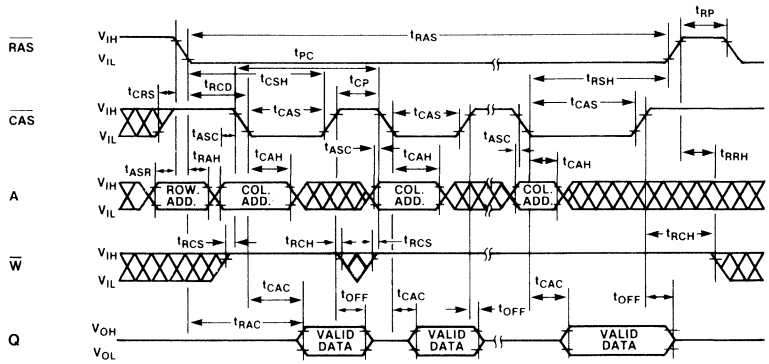
"$\overline{RAS}$-Only" Refresh Cycle

NOTE: $\overline{W}$, D = Don't Care, $A_9 = V_{IH}$ or V_{IL}

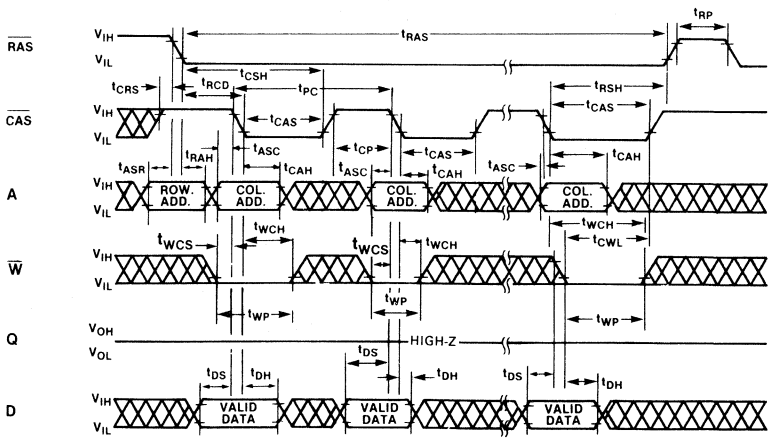


Timing Diagrams
(Continued)

Page Mode Read Cycle



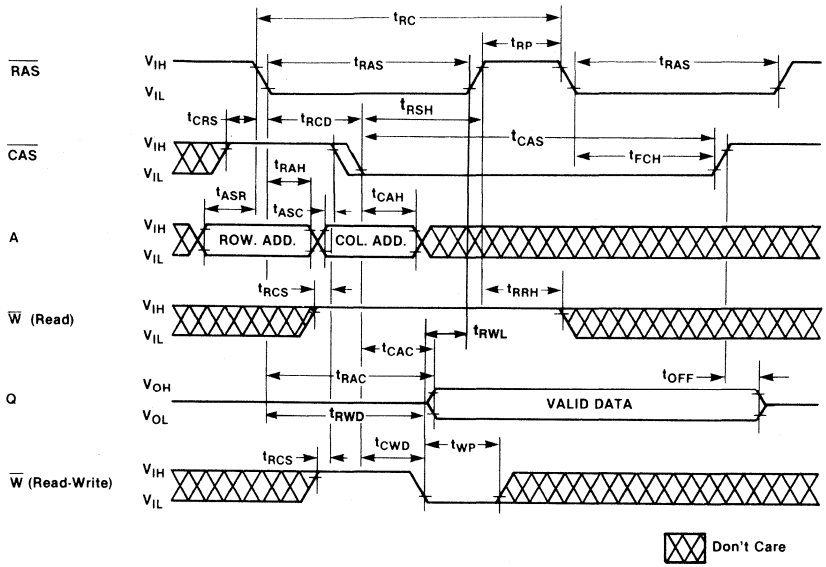
Page Mode Write Cycle



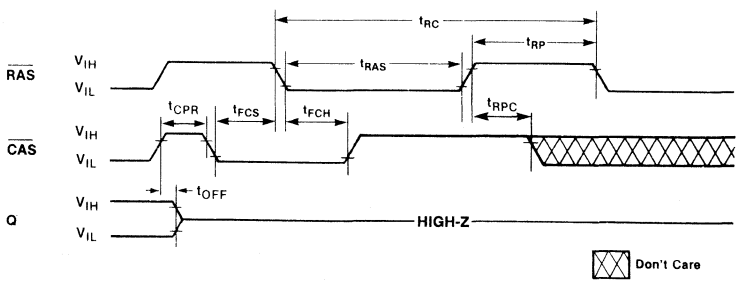
Don't Care

Timing Diagrams
(Continued)

Hidden Refresh Cycle

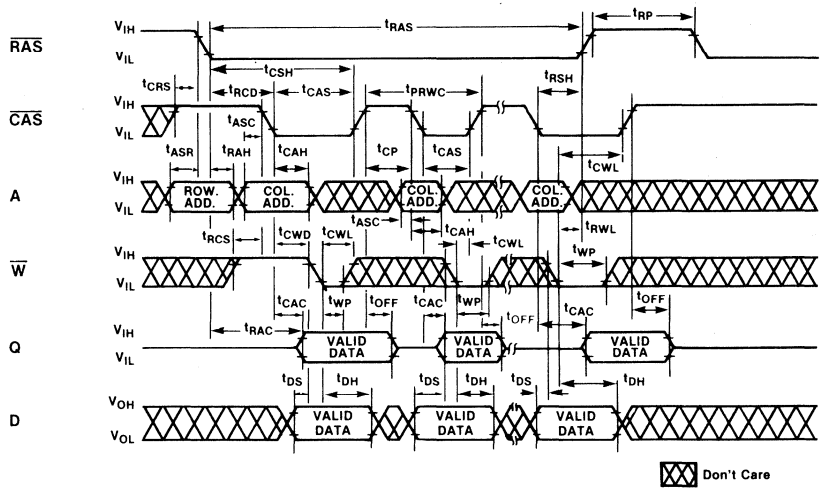


"$\overline{CAS}$-Before-$\overline{RAS}$" Refresh Cycle
NOTE: A, $\overline{W}$, D = Don't Care



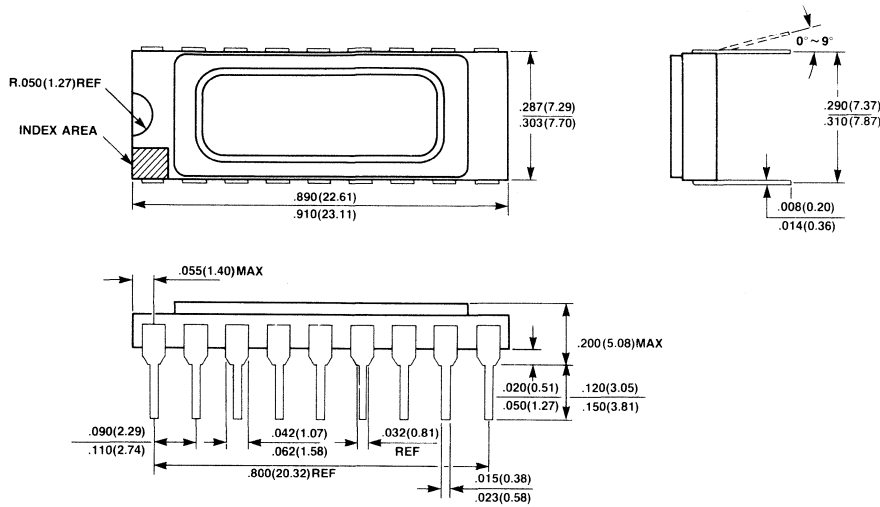
Timing Diagrams
(Continued)

Page Mode Read-Write Cycle

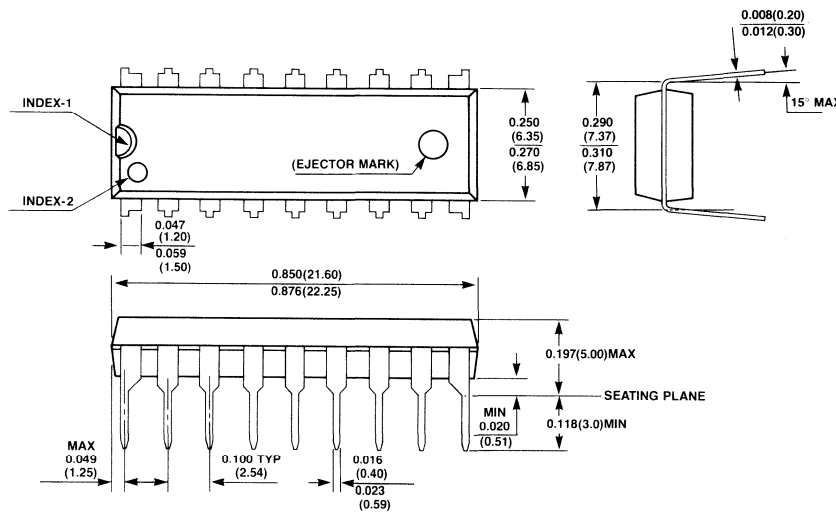


Package Dimensions
Dimensions in inches
(millimeter)

Ceramic Seam Weld Package
(DIP-18C-A01)

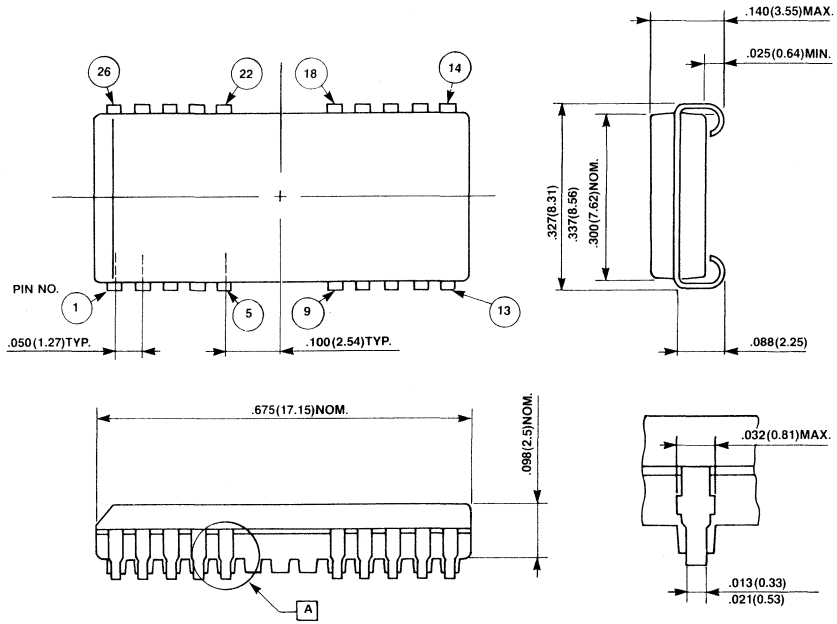


18 Lead Plastic Dual-In-Line Package
(DIP-18P-M03)



Package Dimensions
(Continued)
Dimensions in inches
(millimeter)

26 Lead SOJ Package



Advanced Information

MOS Memories

FUJITSU

■ MB811001-12, MB811001-15

1,048,576-Bit Dynamic Random Access Memory

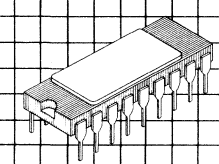
Description

The Fujitsu MB811001 is a fully decoded, dynamic NMOS random access memory organized as 1,048,576 one-bit words. The design is optimized for high speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout are required.

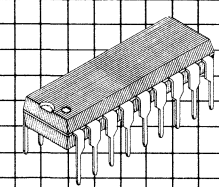
The MB811001 features "nibble mode" which allows high speed serial access of up to four bits of data. Additionally, the MB811001 offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability. Multiplexed row and column address inputs permit the MB811001 to be housed in a Jedec standard 18-pin dual in-line package or 20 lead S0J package.

The MB811001 is fabricated using silicon gate NMOS and Fujitsu's advanced Triple-layer Polysilicon process. This process, coupled with an innovative stacked capacitor memory cell, permits maximum circuit density and minimal chip size. Dynamic circuitry is used in the design including dynamic sense amplifiers.

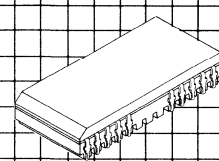
Clock timing requirements are r ·critical, and the power supply tolerance is very wide. All inputs are TTL compatible.



Plastic Package DIP-18P-M03



Ceramic Package DIP-18C-A01

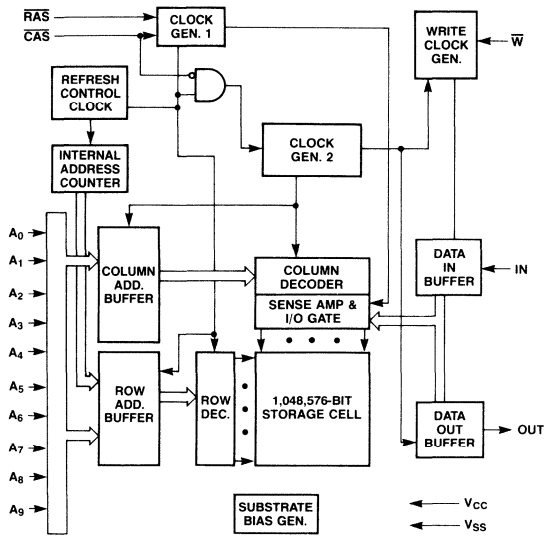


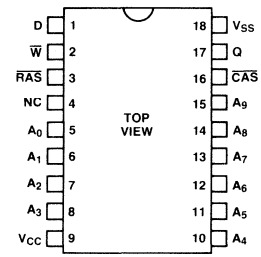
SOJ Package

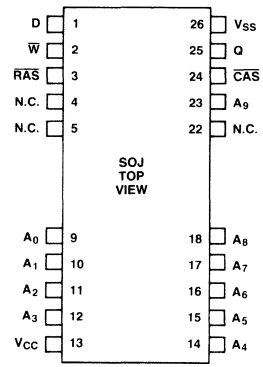
Features

- **1,048,576 x 1-bit organization**
- **Silicon-gate, NMOS, single transistor cell**
- **Access time (t_{RAC})**
  120 ns max. (MB811001-12)
  150 ns max. (MB811001-15)
- **Cycle time (t_{RC})**
  230 ns min. (MB811001-12)
  260 ns min. (MB811001-15)
- **Nibble mode capability for faster access**
- **Single 5V supply, ±10% tolerance**
- **Low power dissipation**
  550 mW max. (MB811001-12)
  490 mW max. (MB811001-15)
  25 mW max. at standby
- **Refresh 8 ms/512 cycles**
- **$\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$ and hidden refresh capability**
- **High speed read-write cycle capability**
- **On chip address and data-in latches**

MB811001 Block Diagram and Pin Assignment







Absolute Maximum Ratings

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} relative to V_{SS}		V_{CC}	−1 to +7	V
Storage temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	
Power dissipation		P_D	1.0	W
Short circuit output current			50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Recommended Operating Conditions

(Referenced to V_{SS})

Parameter	Symbol	Value Min	Value Typ	Value Max	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C ambient
	V_{SS}	0	0	0	V	
Input High Voltage All Inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage All Inputs	V_{IL}	−2.0		0.8	V	

Capacitance
($T_A = 25\,°C$)

Parameter	Symbol	Value Min	Typ	Max	Unit
Input Capacitance A_0 to A_9, D	C_{IN1}			7	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$	C_{IN2}			8	pF
Output Capacitance Q	C_{OUT}			7	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB811001-12 Min	MB811001-12 Max	MB811001-15 Min	MB811001-15 Max	Unit
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min.)	I_{CC1}		100		90	mA
STANDBY CURRENT Power Supply Current ($\overline{RAS}/\overline{CAS} = V_{IH}$)	I_{CC2}		4.5		4.5	mA
REFRESH CURRENT 1* Average Power Supply Current ($\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$; t_{RC} = Min.)	I_{CC3}		90		80	mA
NIBBLE MODE CURRENT* Average Power Supply Current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; t_{NC} = Min.)	I_{CC4}		25		23	mA
REFRESH CURRENT 2* Average Power Supply Current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = Min.)	I_{CC5}		90		80	mA
INPUT LEAKAGE CURRENT Any Input, (V_{IN} = 0V to 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)	I_{IL}	−10	10	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data is disabled, V_{OUT} = 0V to 5.5V)	I_{OL}	−10	10	−10	10	μA
OUTPUT LEVEL Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}		0.4		0.4	V
OUTPUT LEVEL Output High Voltage (I_{OH} = −5.0 mA)	V_{OH}	2.4		2.4		V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol Alternate	*Standard	MB811001-12 Min	MB811001-12 Max	MB811001-15 Min	MB811001-15 Max	Unit
Time between Refresh		t_{REF}	TRVRV		8		8	ms
Random Read/Write Cycle Time		t_{RC}	TRELREL	230		260		ns
Read-Write Cycle Time		t_{RWC}	TRELREL	285		325		ns
Access Time from $\overline{RAS}$ *4,6		t_{RAC}	TRELQV		120		150	ns
Access Time from $\overline{CAS}$ *5,6		t_{CAC}	TCELQV		60		75	ns
Output Buffer Turn off Delay		t_{OFF}	TCEHQZ	0	25	0	35	ns
Transition Time		t_T	TT	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	TREHREL	100		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	TRELREH	120	100000	150	100000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	TCELREH	60		75		ns
$\overline{CAS}$ Precharge Time (Normal Cycle)		t_{CPN}	TCELCEL	22		25		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	TCELCEH	60	100000	75	100000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	TRELCEH	120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time *4,7		t_{RCD}	TRELCEL	22	60	25	75	ns
$\overline{RAS}$ to $\overline{W}$ Delay Time *8		t_{RWD}	TRELWL	120		150		ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	TCEHREL	0		0		ns
Row Address Set Up Time		t_{ASR}	TAVREL	0		0		ns
Row Address Hold Time		t_{RAH}	TRELAX	12		15		ns
Column Address Set Up Time		t_{ASC}	TAVCEL	0		0		ns
Column Address Hold Time		t_{CAH}	TCELAX	20		25		ns
Read Command Set Up Time		t_{RCS}	TWHCEL	0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$ *10		t_{RCH}	TCEHWX	0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$ *10		t_{RRH}	TREHWX	20		20		ns
Write Command Set Up Time *8		t_{WCS}	TWLCEL	0		0		ns
Write Command Pulse Width		t_{WP}	TWLWH	20		25		ns
Write Command Hold Time		t_{WCH}	TCELWH	20		25		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	TWLREH	50		60		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	TWLCEH	50		60		ns
Data In Set Up Time		t_{DS}	TDVCEL	0		0		ns
Data In Hold Time		t_{DH}	TCELDX	20		25		ns
$\overline{CAS}$ to $\overline{W}$ Delay *8		t_{CWD}	TCELWL	60		75		ns
Refresh Set Up Time for $\overline{CAS}$ Referenced to $\overline{RAS}$		t_{FCS}	TCELREL	0		0		ns
Refresh Hold Time for $\overline{CAS}$ Referenced to $\overline{RAS}$		t_{FCH}	TRELCEX	20		20		ns

* These symbols are described in IEEE STD 662-1980 IEEE Standard terminology for semiconductor memory.

Notes: *1 An initial pause of 200 μs is required after power up, followed by any 8 $\overline{RAS}$ cycles, before proper device operation is achieved.
If the internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh initialization cycles are required.

*2 AC characteristics assume t_T = 5 ns.

*3 V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

*4 t_{RCD} is specified as a reference point only. If $t_{RCD} \leq t_{RCD}$ (Max.) the specified maximum value of t_{RAC} (Max.) can be met. If $t_{RCD} > t_{RCD}$ (Max.) then t_{RAC} is increased by the amount that t_{RCD} exceeds t_{RCD} (Max.).

*5 Assumes that $t_{RCD} > t_{RCD}$ (Max.).

*6 Measured with a load equivalent to 2 TTL loads and 100 pF.

*7 t_{RCD} (Min.) = t_{RAH} (Min.) + $2t_T$ + t_{ASC} (Min.).

*8 t_{WCS} and t_{CWD} are non restrictive operating parameters, and are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (Min.), the cycle is an early write cycle, and the data out pin will remain open circuit (High Impedance) throughout the entire cycle.

If $t_{CWD} > t_{CWD}$ (Min.), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.

*10 Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol Alternate	Symbol *Standard	MB811001-12 Min	MB811001-12 Max	MB811001-15 Min	MB811001-15 Max	Unit
Nibble Mode Read-Write Cycle Time		t_{NRWC}	TCEHCEH	105		135		ns
Nibble Mode Read/Write Cycle Time		t_{NC}	TCEHCEH	70		90		ns
Nibble Mode Access Time		t_{NCAC}	TCELQV		30		40	ns
Nibble Mode $\overline{CAS}$ Pulse Width		t_{NCAS}	TCELCEH	30		40		ns
Nibble Mode $\overline{CAS}$ Precharge Time		t_{NCP}	TCEHCEL	30		40		ns
Nibble Mode Read $\overline{RAS}$ Hold Time		t_{NRRSH}	TCELREH	30		40		ns
Nibble Mode Write $\overline{RAS}$ Hold Time		t_{NWRSH}	TCELREH	50		60		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time		t_{RPC}	TREHCEL	20		20		ns
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle		t_{CPR}	TCEHCEL	25		30		ns
Nibble Mode Write Command Set Up Time		t_{NWCC}	TWLCEL	22		25		ns
Nibble Mode Write Command to $\overline{CAS}$ Lead Time		t_{NCWL}	TWLCEH	25		35		ns
Nibble Mode $\overline{W}$ to $\overline{CAS}$ Delay Time		t_{NCWD}	TCELWL	30		40		ns

Description

Simplified Timing Requirement

The MB811001 has improved circuitry that eases timing requirements for high speed access operations. The MB811001 can operate under the condition of t_{RCD} (max.) = t_{CAC}, thus providing optimal timing for address multiplexing. In addition, the MB811001 has minimal hold times for Addresses (t_{CAH}), Write-Enable (t_{WCH}) and Data-in (t_{DH}). The MB811001 provides higher throughput in interleaved memory system applications. Fujitsu has made the timing requirements that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the Column Address, D and $\overline{W}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{W}$ Delay) are not restricted by t_{RCD}.

Fast Read-Write Cycle

The MB811001 has a fast read-modify-write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{W}$ when $\overline{CAS}$ goes "low". When $\overline{W}$ is "low" during a $\overline{CAS}$ transition to "low", the MB811001 goes into the early write mode in which the output floats and the common I/O bus can be used on the svstem level. When $\overline{W}$ goes "low", after t_{CWD} following a $\overline{CAS}$ transition to "low", the MB811001 goes into the delayed write mode. The output then contains the data from the cell selected and the data from D is written into the cell selected. Therefore, a very fast read-write cycle (t_{RWC} = t_{RC}) is possible with the MB811001.

Address Inputs

A total of twenty binary input address bits are required to decode any 1 of 1,048,576 cell locations within the MB811001. Ten row address bits are established on the input pins (A_0 through A_9) and are latched with the Row Address Strobe ($\overline{RAS}$). Ten column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold/Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

Write Enable

The read or write mode is selected with the $\overline{W}$ input. A logic "high" on $\overline{W}$ dictates read mode. A logic "low" dictates write mode. The data input is disabled when the read mode is selected.

Data Input

Data is written into the MB811001 during a write or read-write cycle. The last falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the Data-in (D) register. In a write cycle, if $\overline{W}$ is brought "low" (write mode) before $\overline{CAS}$, D is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{W}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D is strobed by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high

Description
(Continued)

impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when $t_{RCD(max)}$ is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after $t_{RCD(max)}$. Data remains valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Nibble Mode

Nibble mode allows high speed serial read, write or read-modify-write access of 2, 3, or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 column address inputs (A_0 to A_8). The 2 bits of addresses (RA_9 and CA_9), are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by the normal mode, the remaining nibble bits may be accessed by toggling $\overline{CAS}$ "high" then "low" while $\overline{RAS}$ remains "low". Toggling $\overline{CAS}$ causes RA_9 and CA_9 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. (See table 1 below.)

If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on subsequent access, the new data will be written into the selected cell location.

$\overline{RAS}$-Only Refresh

Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 512 row-addresses ($A_0 \sim A_8$) at least every 8 ms. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought "low". Strobing each of the 512 row-addresses ($A_0 \sim A_8$) with $\overline{RAS}$ will cause all bits in each row to be refreshed. $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh

$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB811001 offers an alternate refresh method. If $\overline{CAS}$ is held "low" for the specified period (t_{FCS}) before $\overline{RAS}$ goes to "low", on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place.

After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Hidden Refresh

A hidden refresh cycle may take place while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time. For the MB811001, a hidden refresh cycle is a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The internal refresh address counter provides the refresh addresses as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Table 1
Nibble Mode Address Sequence Example

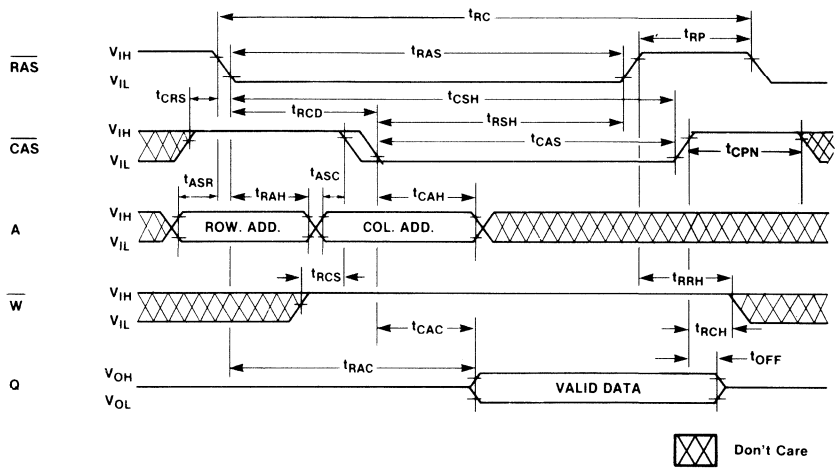
Sequence	Nibble Bit	Row Address	RA_9	Column Address	CA_9	Comments
$\overline{RAS}$/$\overline{CAS}$ (normal mode)	1	101010101	0	101010101	0	input addresses
toggle $\overline{CAS}$ (nibble mode)	2	101010101	1	101010101	0	
toggle $\overline{CAS}$ (nibble mode)	3	101010101	0	101010101	1	generated internally
toggle $\overline{CAS}$ (nibble mode)	4	101010101	1	101010101	1	
toggle $\overline{CAS}$ (nibble mode)	1	101010101	0	101010101	0	sequence repeats

Table 2
Functional Truth Table

$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	IN	OUT	Mode	Note
H	H	X	X	High-Z	Standby	
L	L	H	X	Data	Read	$t_{RCS} \geqslant t_{RCS}$ min
L	L	L	Data	High-Z	Early Write	$t_{WCS} \geqslant t_{WCS}$ min
L	L	H → L	Data	Data	Read-Write	$t_{CWD} \geqslant t_{CWD}$ min and $t_{RWD} \geqslant t_{RWD}$ min
L	H	X	X	High-Z	$\overline{RAS}$-only refresh	
L	L	X	X	High-Z	$\overline{CAS}$-before-$\overline{RAS}$ Refresh	$t_{FCS} \geqslant t_{FCS}$ min

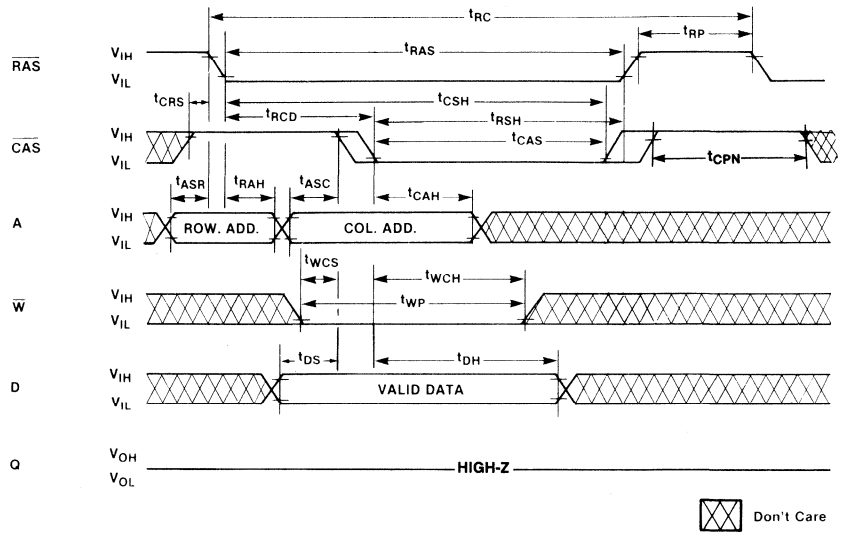
Timing Diagrams

Read Cycle

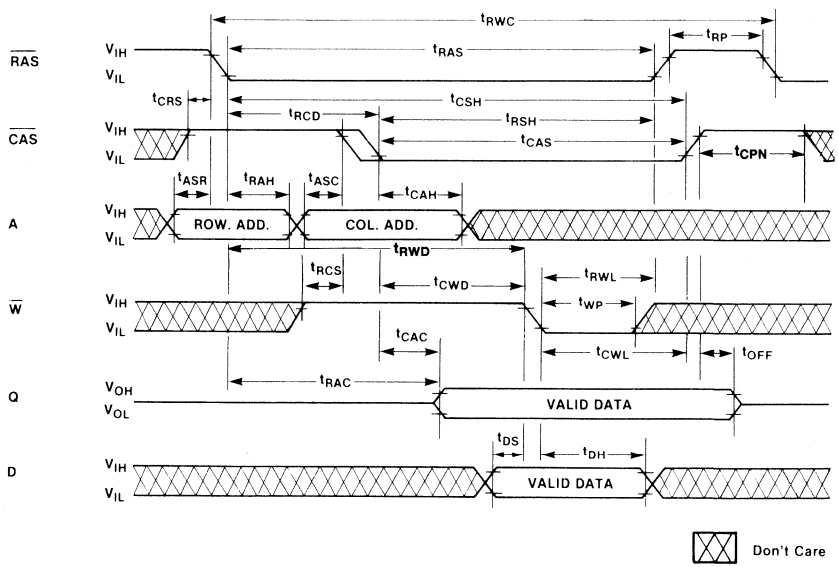


Timing Diagrams
(Continued)

Write Cycle (Early Write)

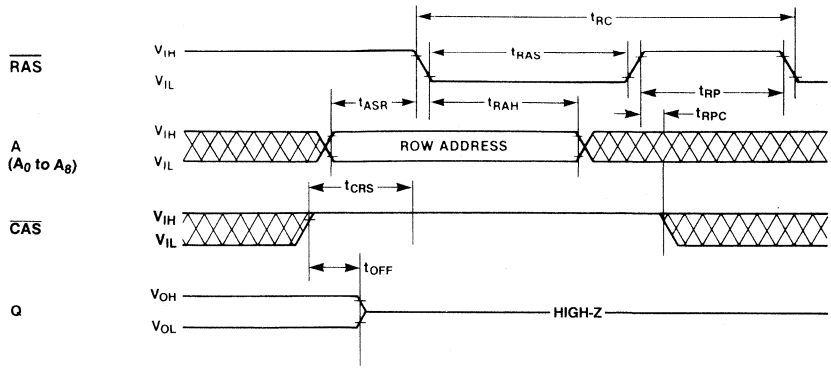


Read-Write/Read-Modify-Write Cycle

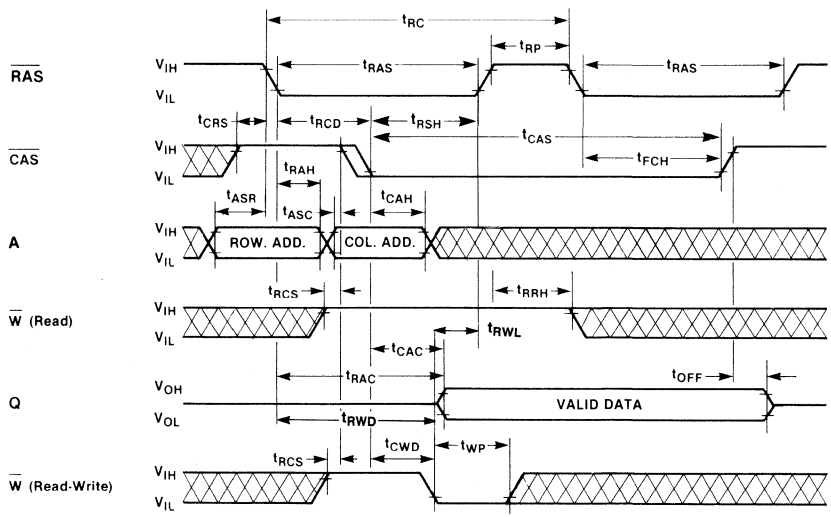


Timing Diagrams
(Continued)

"$\overline{RAS}$-Only" Refresh Cycle
NOTE: $A_9 = V_{IH}$ or V_{IL}, W, D = Don't Care



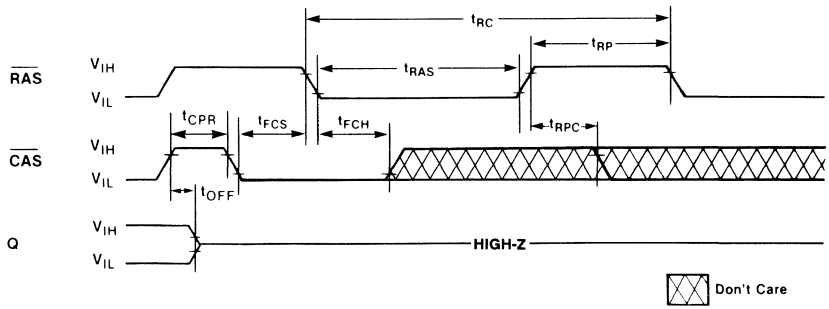
Hidden Refresh Cycle



Timing Diagrams
(Continued)

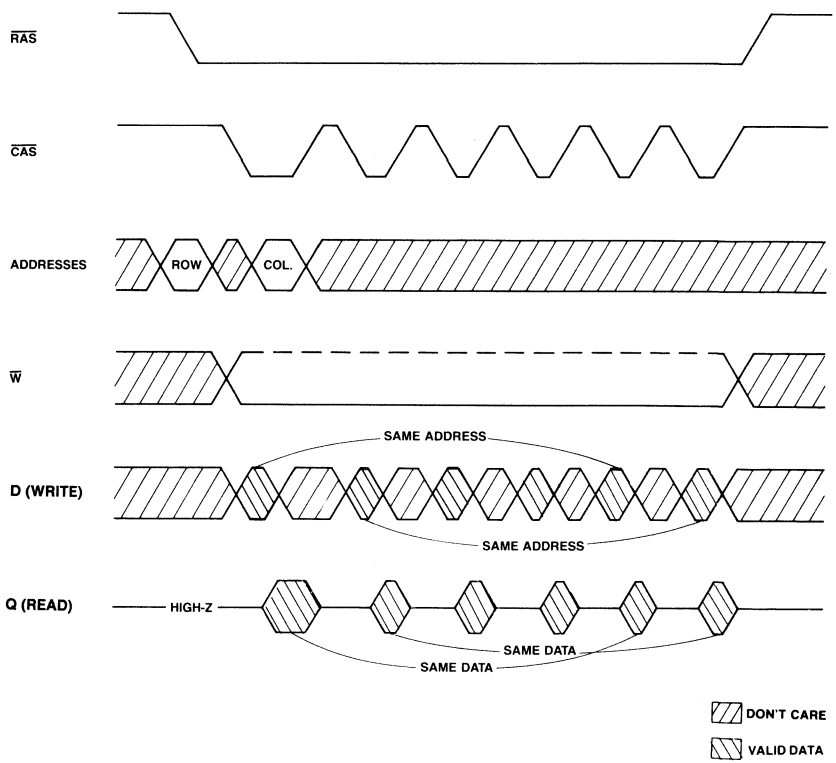
"$\overline{CAS}$-Before-$\overline{RAS}$" Refresh Cycle

NOTE: Address, $\overline{W}$, D = Don't Care



Nibble Mode

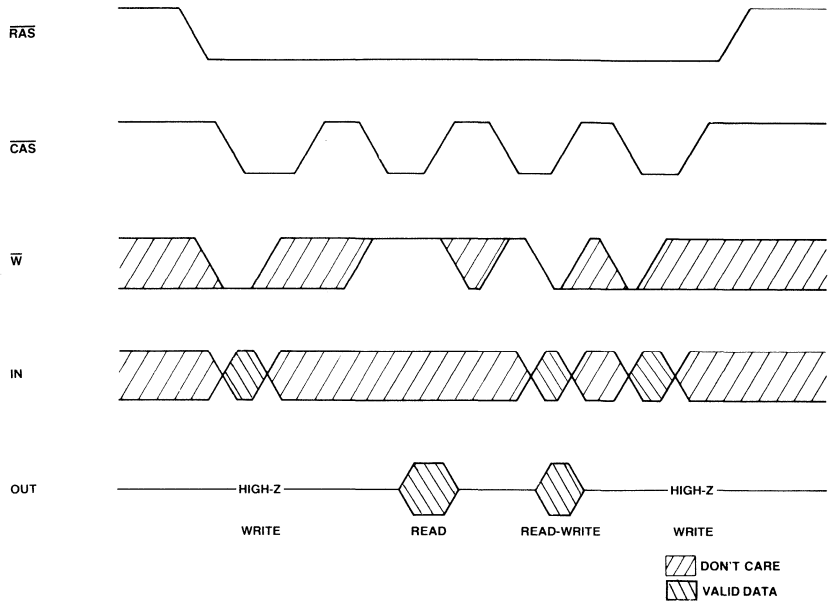
1) REPEATED NIBBLE MODE



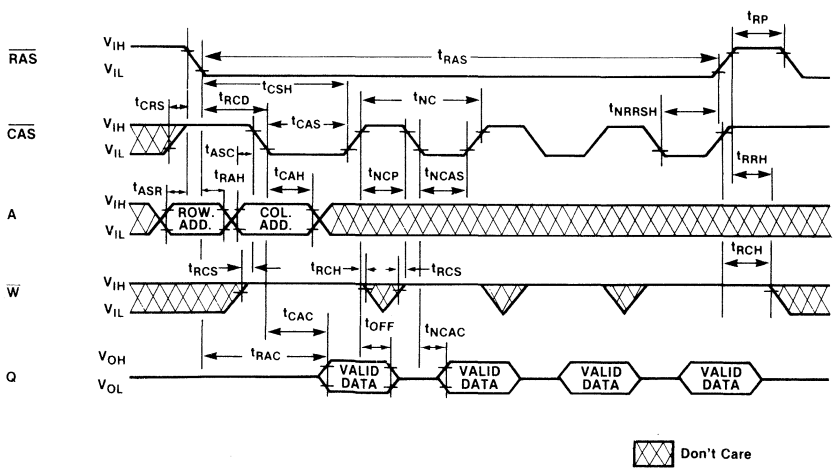
Timing Diagrams
(Continued)

Nibble Mode (continued)

2) EACH NIBBLE BIT

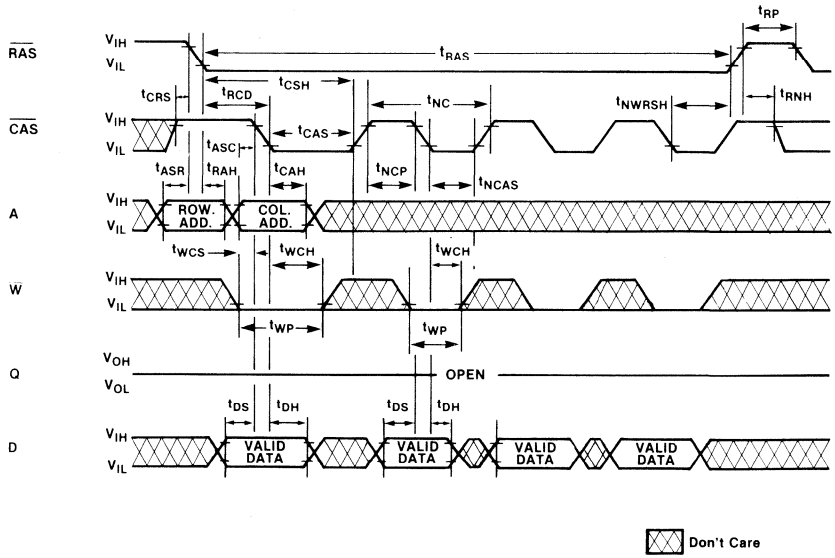


Nibble Mode Read Cycle



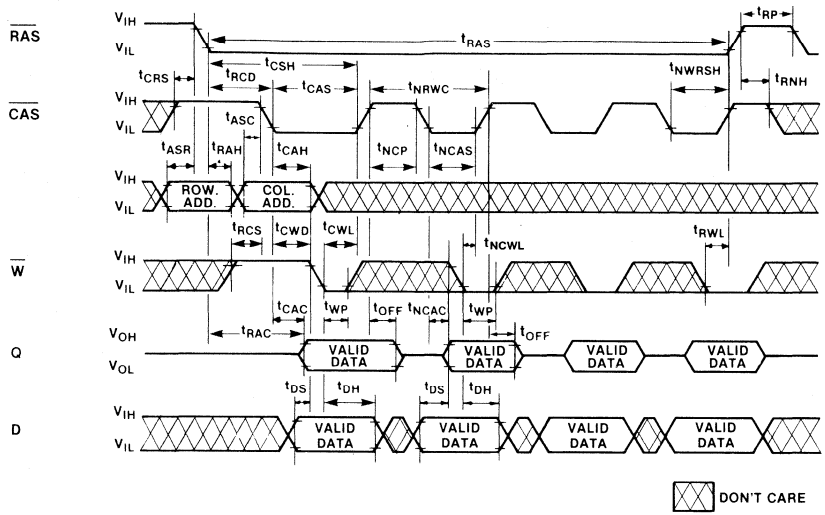
Timing Diagrams
(Continued)

Nibble Mode Write Cycle



Timing Diagrams
(Continued)

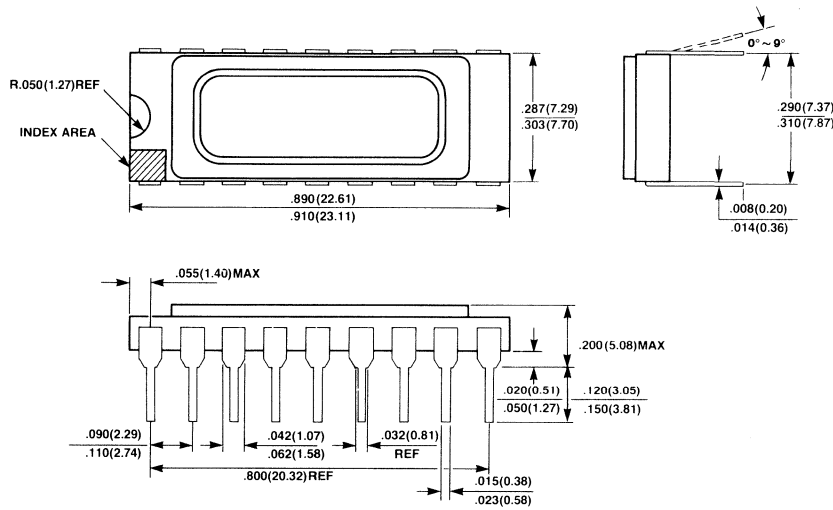
Nibble Mode Read-Write Cycle



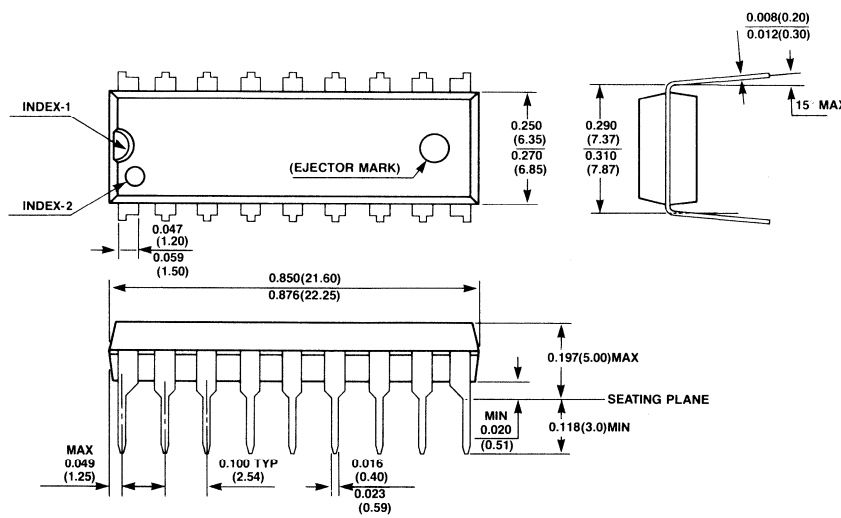
Package Dimensions

Dimensions in inches
(millimeters)

Ceramic Seam Weld Package (DIP-18C-A01)

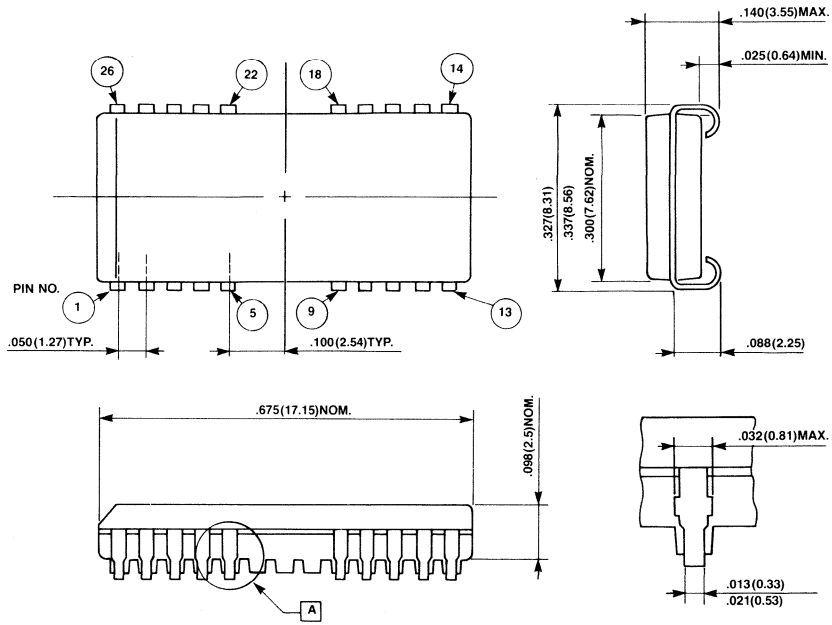


18 Lead Plastic Dual-In-Line Package (DIP-18P-M03)



Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

26 Lead SOJ Package



FUJITSU

MOS 65536-BIT DYNAMIC RANDOM ACCESS MEMORY

MB 8264A-10
MB 8264A-12
MB 8264A-15

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

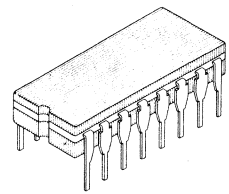
The Fujitsu MB 8264A is a fully decoded, dynamic random access memory organized as 65,536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MB 8264A to be housed in a standard 16 pin DIP and 18 pad LCC. Pin-outs conform to the JEDEC approved pin out.

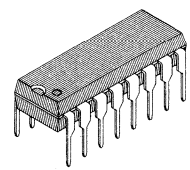
The MB 8264A is fabricated using silicon gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are non-critical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

- 65,536 x 1 RAM, 16 pin DIP/18 pad LCC
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  100 ns max (MB 8264A-10)
  120 ns max (MB 8264A-12)
  150 ns max (MB 8264A-15)
- Cycle time,
  190 ns min (MB 8264A-10)
  230 ns min (MB 8264A-12)
  260 ns min (MB 8264A-15)
- Single +5V Supply, ±10% tolerance
- Low power (active)
  275 mW max (MB 8264A-10)
  248 mW max (MB 8264A-12)
  220 mW max (MB 8264A-15)
  22 mW Standby (max)
- 2ms/128 refresh cycles
- $\overline{RAS}$-only and Hidden refresh capability
- Read-Modify-Write and Page-Mode capability
- Common I/O capability using Early Write operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- On-chip latches for Addresses and Data-in
- t_{AR}, t_{WCR}, t_{DHR} are eliminated
- Standard 16-pin Ceramic (Cerdip) DIP: Surfix-Z
  Standard 16-pin Plastic DIP: Surfix-P
  Standard 18-pad Ceramic LCC: Surfix-TV



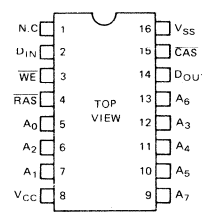
CERAMIC PACKAGE
(CERDIP)
DIP-16C-C04

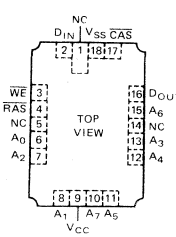


PLASTIC PACKAGE
DIP-16P-M03

LCC-18C-F02 : See Page 1-191

PIN ASSIGNMENT





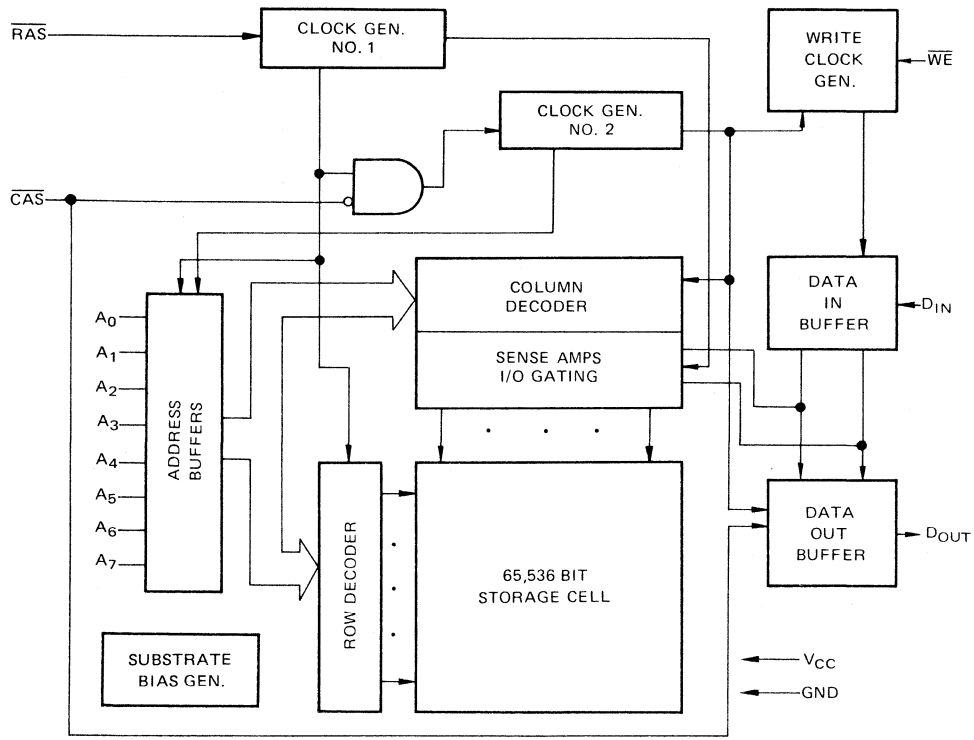
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	−1 to +7	V
Storage temperature	Ceramic	T_{STG}	−55 to +150	°C
	Pastic		−55 to +125	
Power dissipation		P_D	1.0	W
Short circuit output current			50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB 8264A BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance A_0~A_7, D_{IN}	C_{IN1}		5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}		8	pF
Output Capacitance D_{OUT}	C_{OUT}		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V	0°C to +70°C
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL} *	-1.0		0.8	V	

Note * : The device can withstand undershoots to the −2V level with a pulse width of 20 ns.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
OPERATING CURRENT * Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 8264A-10	I_{CC1}		50	mA
	MB 8264A-12			45	
	MB 8264A-15			40	
STANDBY CURRENT Standby Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}		4	mA
REFRESH CURRENT * Average power supply current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	MB 8264A-10	I_{CC3}		38	mA
	MB 8264A-12			35	
	MB 8264A-15			31	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min)	MB 8264A-10	I_{CC4}		35	mA
	MB 8264A-12			32	
	MB 8264A-15			28	
INPUT LEAKAGE CURRENT Input leakage current, any input ($0V \leq V_{IN} \leq 5.5V$, V_{CC}=5.5V, V_{SS}=0V, all other pins not test=0V)		$I_{I(L)}$	-10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \leq V_{OUT} \leq 5.5$)		$I_{O(L)}$	-10	10	μA
OUTPUT LEVELS Output high voltage (I_{OH} = -5mA) Output low voltage (I_{OL} = 4.2mA)		V_{OH} V_{OL}	2.4	 0.4	V V

Note * : I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS

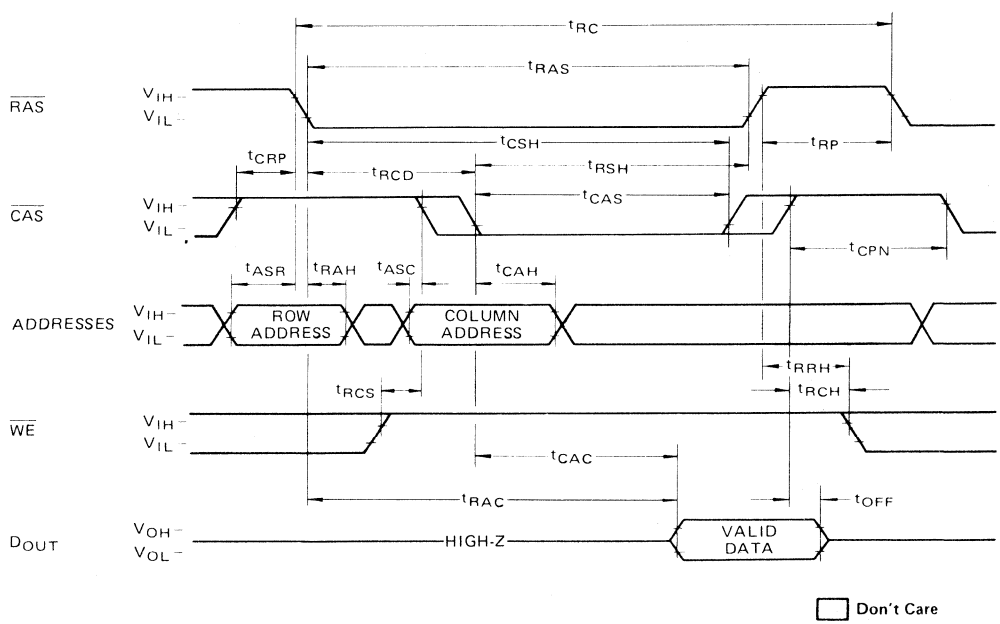
(Recommended operating conditions unless otherwise noted.) NOTES 1,2,3

Parameter	NOTES	Symbol	M8 8264A-10		MB 8264A-12		MB 8264A-15		Unit
			Min	Max	Min	Max	Min	Max	
Time between Refresh		t_{REF}		2		2		2	ms
Random Read/Write Cycle Time		t_{RC}	190		230		260		ns
Read-Write Cycle Time		t_{RWC}	230		265		280		ns
Page Mode Cycle Time		t_{PC}	105		120		145		ns
Page Mode Read-Write Cycle Time		t_{PRWC}	135		155		180		ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}		100		120		150	ns
Access Time from $\overline{CAS}$	5 6	t_{CAC}		50		60		75	ns
Output Buffer Turn Off Delay		t_{OFF}	0	30	0	35	0	40	ns
Transition Time		t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Tim		t_{RP}	80		100		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	100	10000	120	10000	150	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	50		60		75		ns
$\overline{CAS}$ Precharge Time (Page mode only)		t_{CP}	45		50		60		ns
$\overline{CAS}$ Precharge Time (All cycles except page mode)		t_{CPN}	20		20		25		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	50	10000	60	10000	75	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	100		120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Tim	7 8	t_{RCD}	20	50	20	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0		0		0		ns
Row Address Set Up Time		t_{ASR}	0		0		0		ns
Row Address Hold Time		t_{RAH}	10		10		15		ns
Column Address Set Up Time		t_{ASC}	0		0		0		ns
Column Address Hold Time		t_{CAH}	15		15		20		ns
Read Command Set Up Time		t_{RCS}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	10	t_{RCH}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	10	t_{RRH}	20		20		20		ns
Write Command Set Up Time	9	t_{WCS}	0		0		0		ns
Write Command Hold Time		t_{WCH}	20		25		30		ns
Write Command Pulse Width		t_{WP}	20		25		30		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	35		40		45		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	35		40		45		ns
Data In Set Up Time		t_{DS}	0		0		0		ns
Data In Hold Time		t_{DH}	20		25		30		ns
$\overline{CAS}$ to $\overline{WE}$ Delay	9	t_{CWD}	40		50		60		ns
$\overline{RAS}$ to $\overline{WE}$ Delay	9	t_{RWD}	90		110		120		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time ($\overline{RAS}$-only refresh)		t_{RPC}	20		20		20		ns

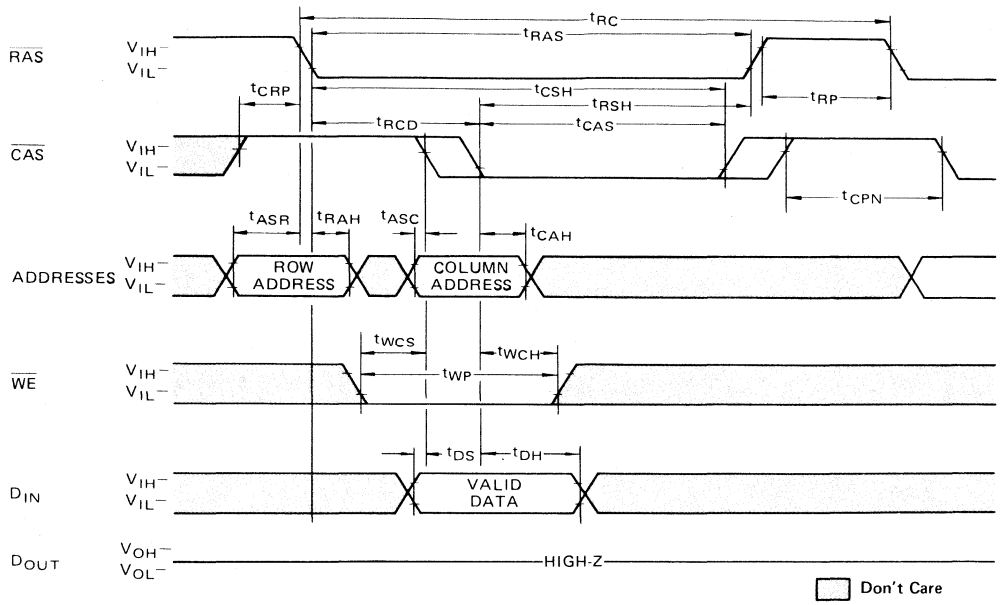
Notes:

1. An initial pause of 200 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2. AC characteristics assume t_T = 5ns.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
6. Measured with a load equivalent to 2 TTL loads and 100 pF.
7. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T=5ns) + t_{ASC} (min)
9. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min) the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.
   If $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

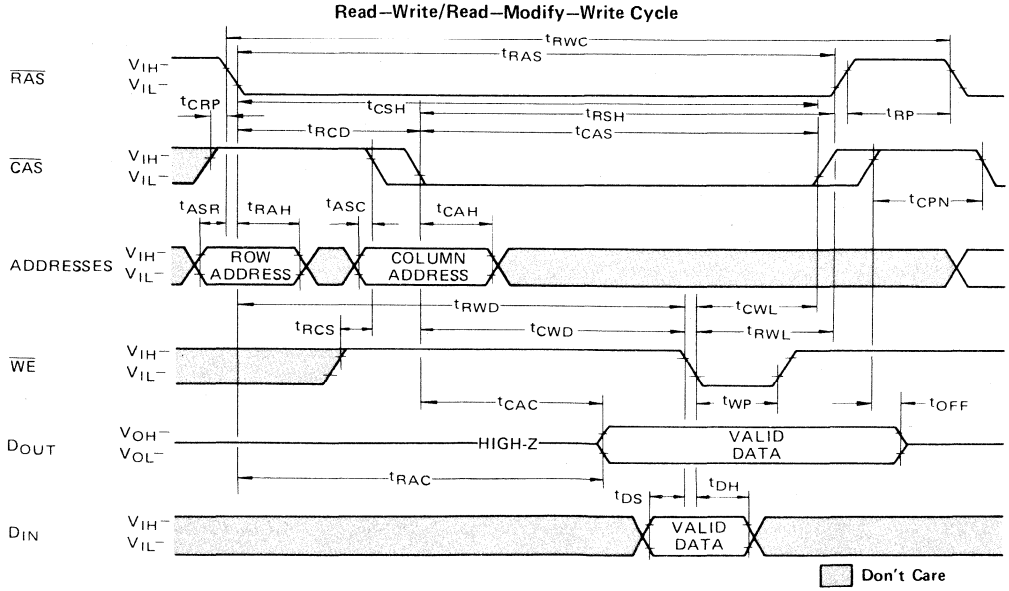
Read Cycle



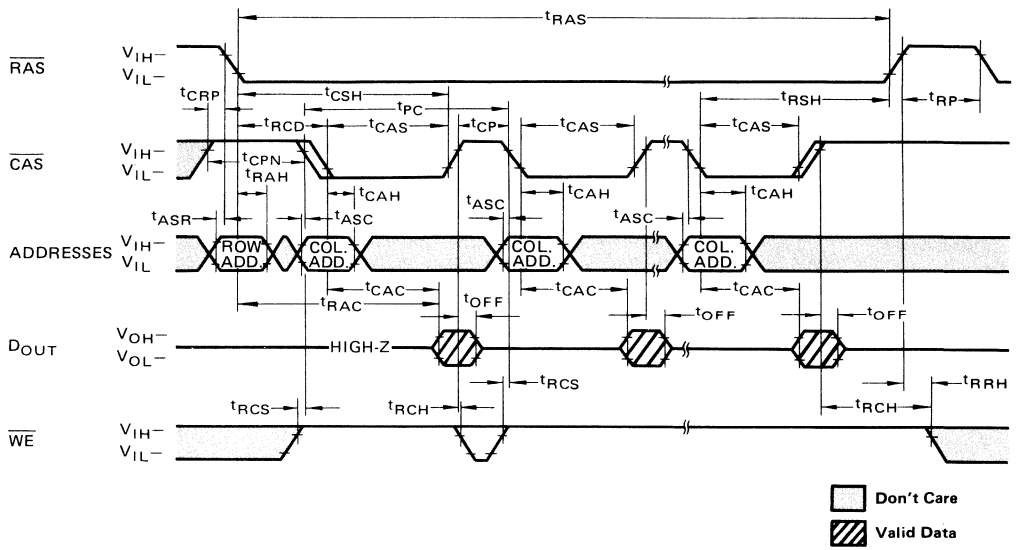
Write Cycle (Early Write)



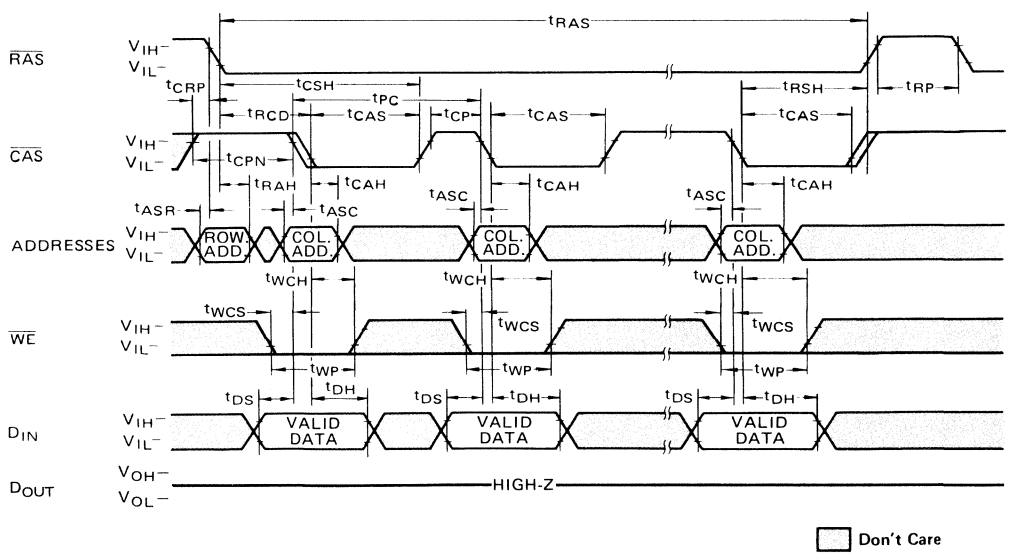
Read–Write/Read–Modify–Write Cycle



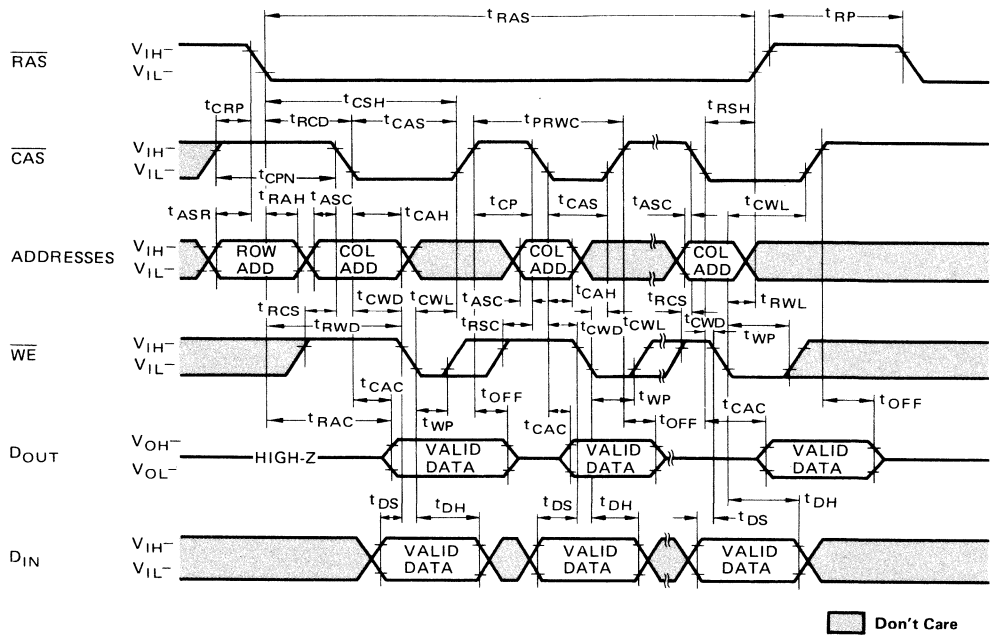
Page Mode Read Cycle



Page Mode Write Cycle

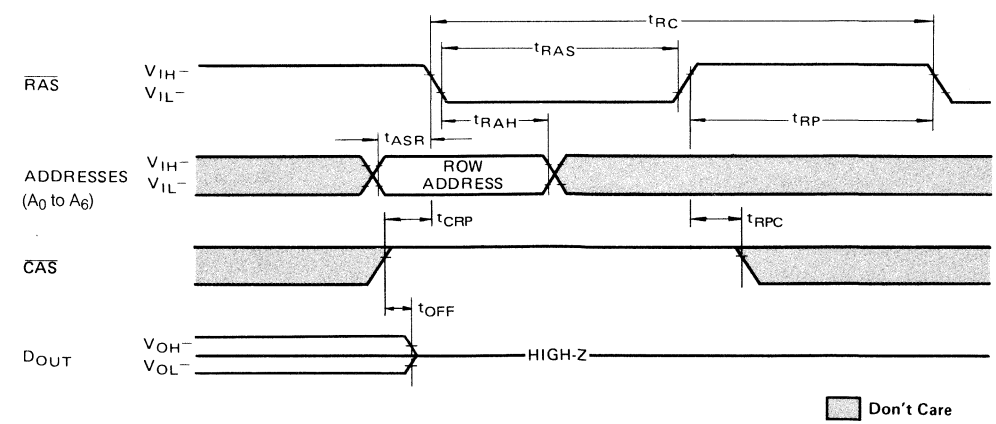


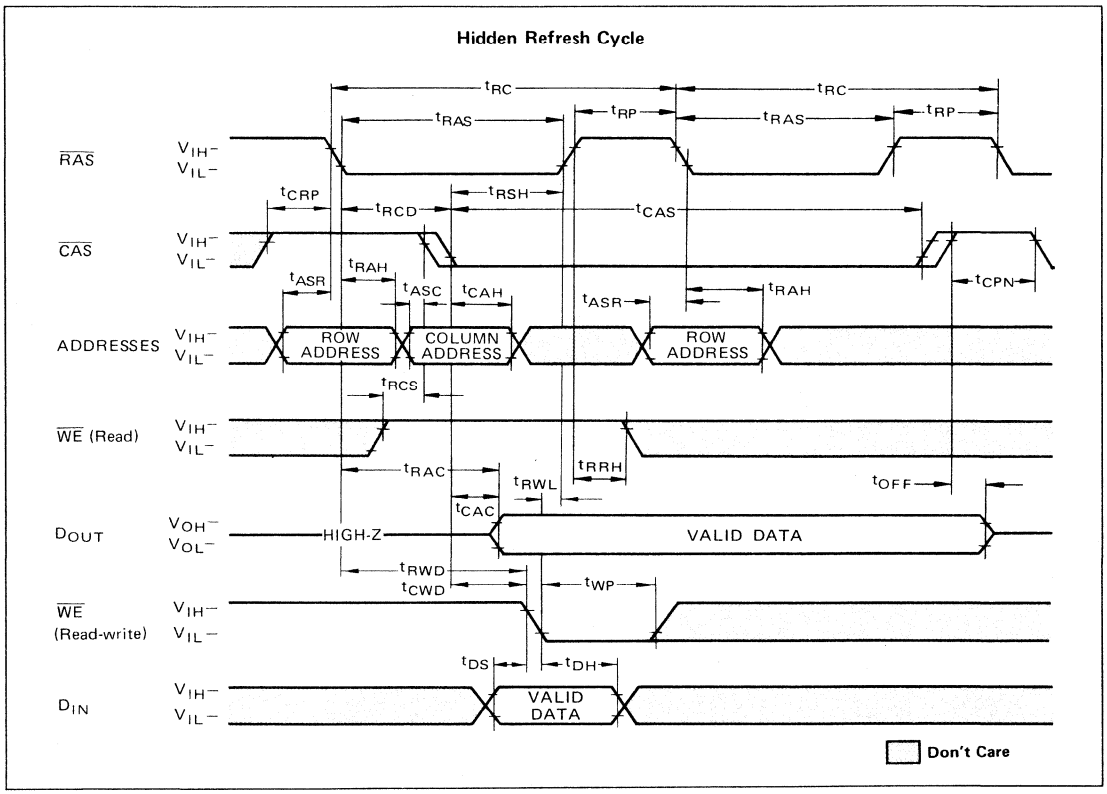
Page Mode Read-Write Cycle



$\overline{RAS}$-only Refresh Cycle

Note: $\overline{WE}$, D_{IN} = Don't care, $A_7 = V_{IH}$ or V_{IL}





DESCRIPTION

Address Inputs:
A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MB 8264A. Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permite triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:
The read mode or write mode is selected with the $\overline{WE}$ input. A high on $\overline{WE}$ selects read mode and low selects write mode. Data input is disabled when read mode is selected.

Data Input:
Data is written into the MB 8264A during a write or read-write cycle. The later falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ can be low after $\overline{CAS}$ has been low and $\overline{CAS}$ to $\overline{WE}$ Delay Time (t_{CWD}) has been satisfied. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:
The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a

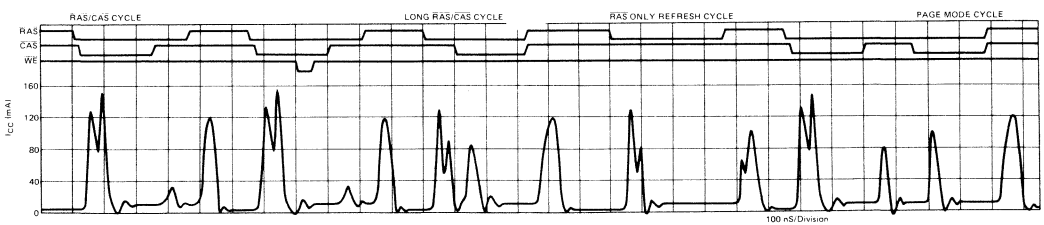
high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from the falling edge of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to a high. In a write cycle the indentical sequence occurs, but data is not valid.

Page Mode:
Page-mode operation permits strobing the row-address into the MB 8264A while maintaining $\overline{RAS}$ at a low throughout all successive memory operations in which the row addresses don't change. Thus the power dissipated by the falling edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row addresses are eliminated.

$\overline{RAS}$-only Refresh
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in a high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

Hidden Refresh:
$\overline{RAS}$-only refresh cycle may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.
Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

Fig. 2 – CURRENT WAVE FORM (V_{CC} = 5.5V, T_A = 25°C)



TYPICAL CHARACTERISTICS CURVES

Fig. 3 — NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

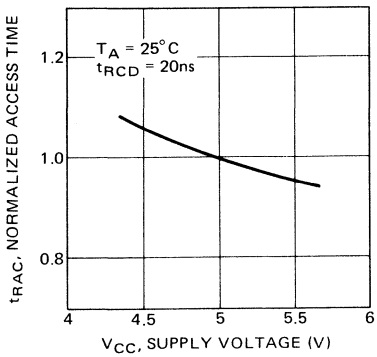


Fig. 4 — NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

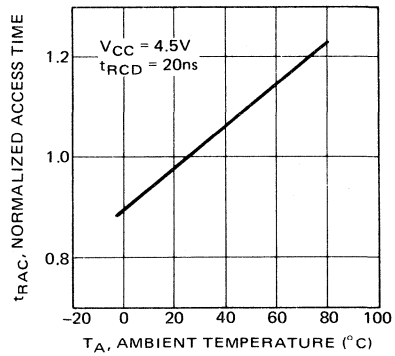


Fig. 5 — OPERATING CURRENT vs CYCLE RATE

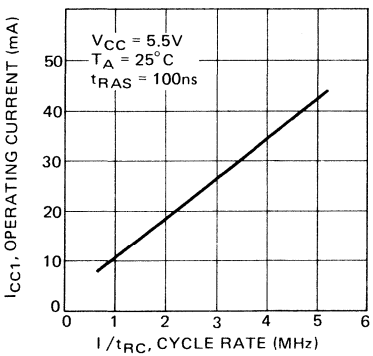


Fig. 6 — OPERATING CURRENT vs SUPPLY VOLTAGE

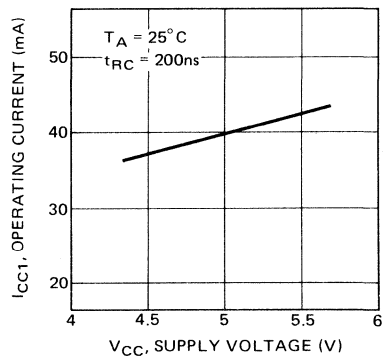


Fig. 7 — OPERATING CURRENT vs AMBIENT TEMPERATURE

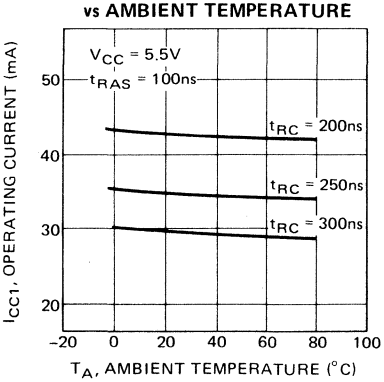


Fig. 8 — STANDBY CURRENT vs SUPPLY VOLTAGE

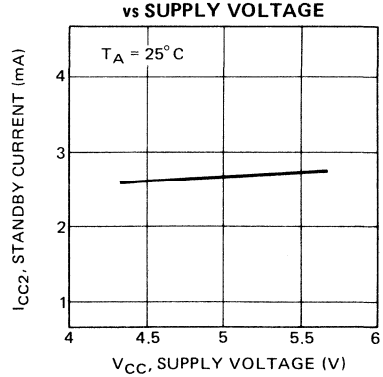


Fig. 9 — STANDBY CURRENT vs AMBIENT TEMPERATURE

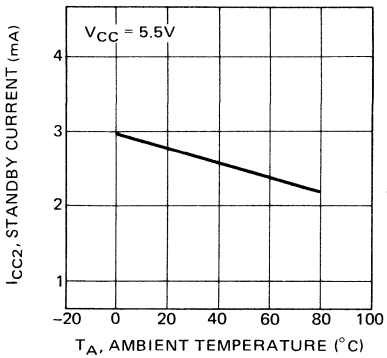


Fig. 10 — REFRESH CURRENT vs CYCLE RATE

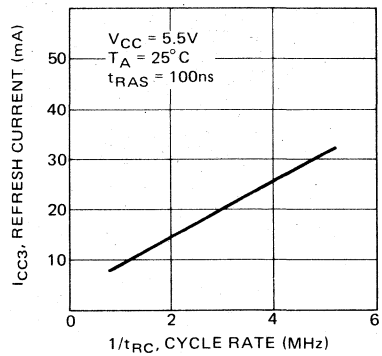


Fig. 11 — REFRESH CURRENT vs SUPPLY VOLTAGE

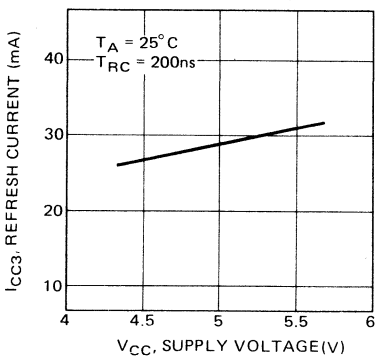


Fig. 12 — REFRESH CURRENT vs AMBIENT TEMPERATURE

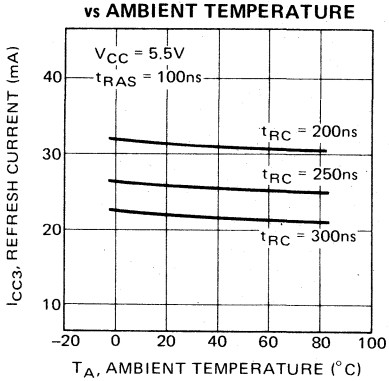


Fig. 13 — PAGE MODE CURRENT vs CYCLE RATE

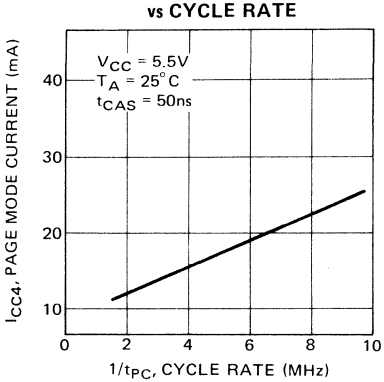


Fig. 14 — PAGE MODE CURRENT vs SUPPLY VOLTAGE

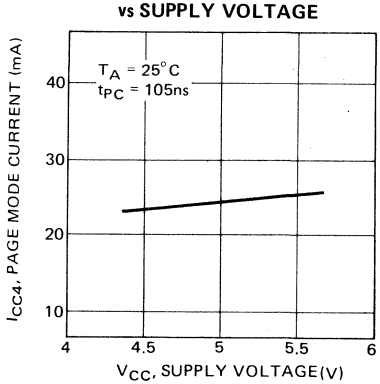


Fig. 15 — PAGE MODE CURRENT vs AMBIENT TEMPERATURE

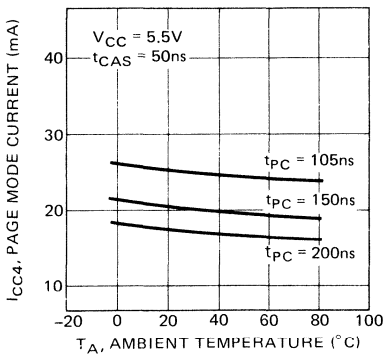


Fig. 16 — ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

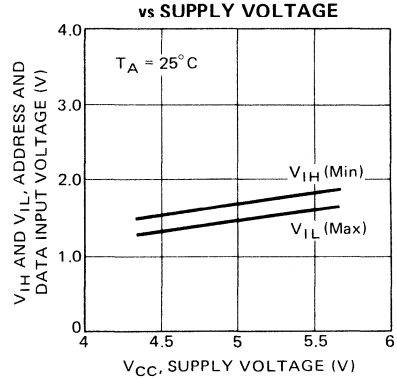


Fig. 17 — ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE

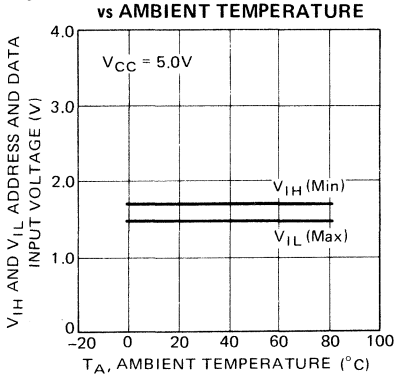


Fig. 18 — $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

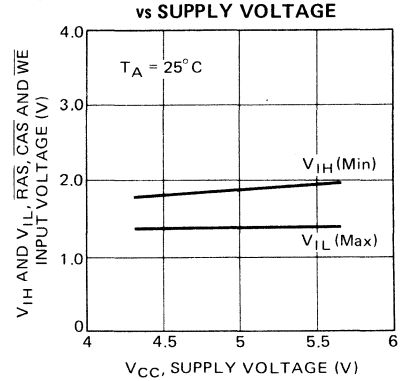


Fig. 19 — $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ VOLTAGE vs AMBIENT TEMPERATURE

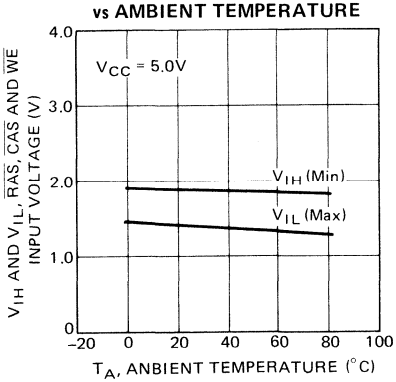


Fig. 20 – CURRENT WAVE FORM DURING POWER UP

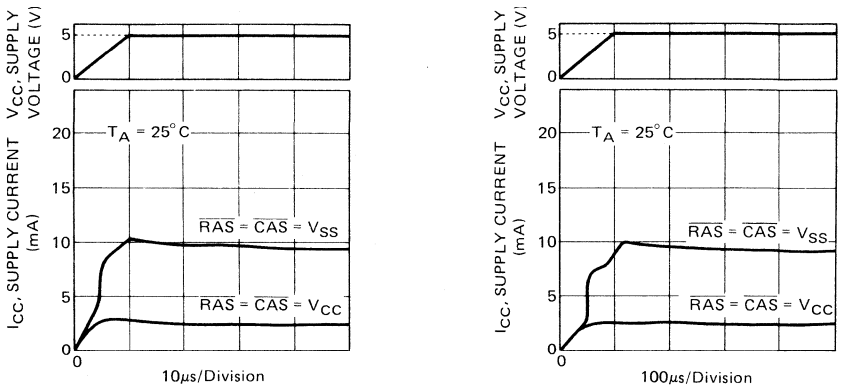


Fig. 21 – CURRENT WAVE FORM DURING POWER UP (ON MEMORY BOARD)

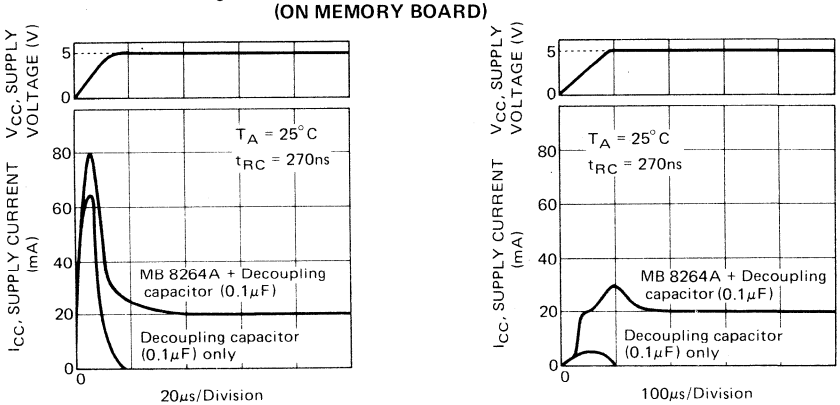
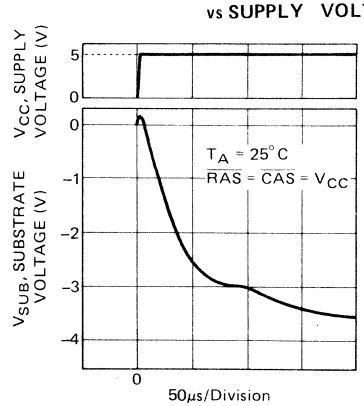
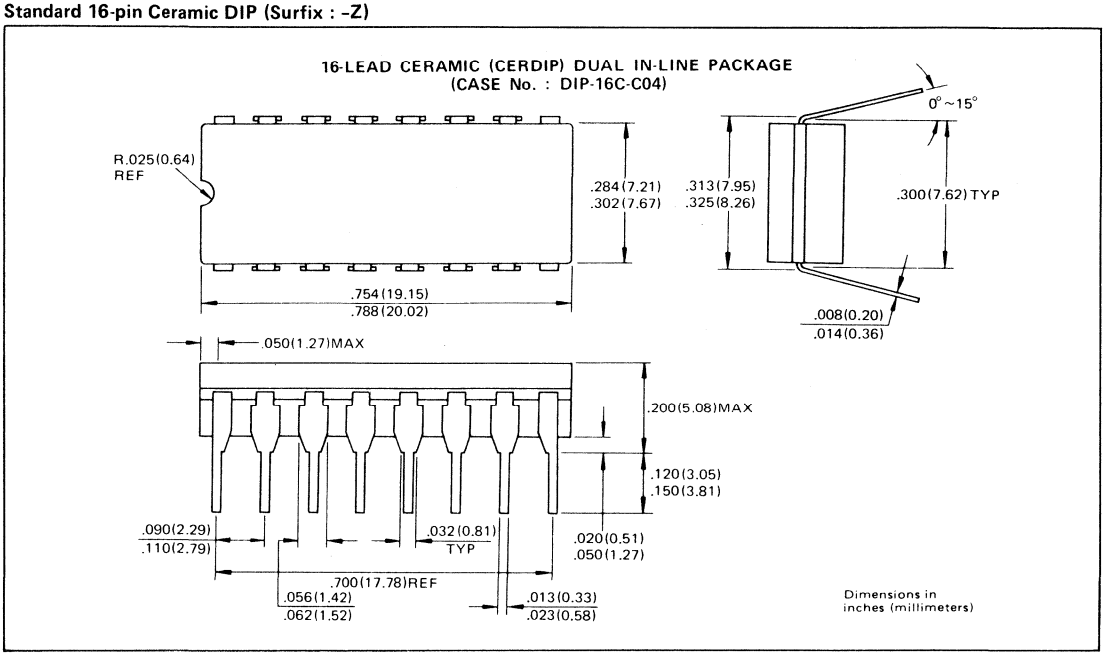


Fig. 22 – SUBSTRATE VOLTATE vs SUPPLY VOLTAGE (DURING POWER UP)

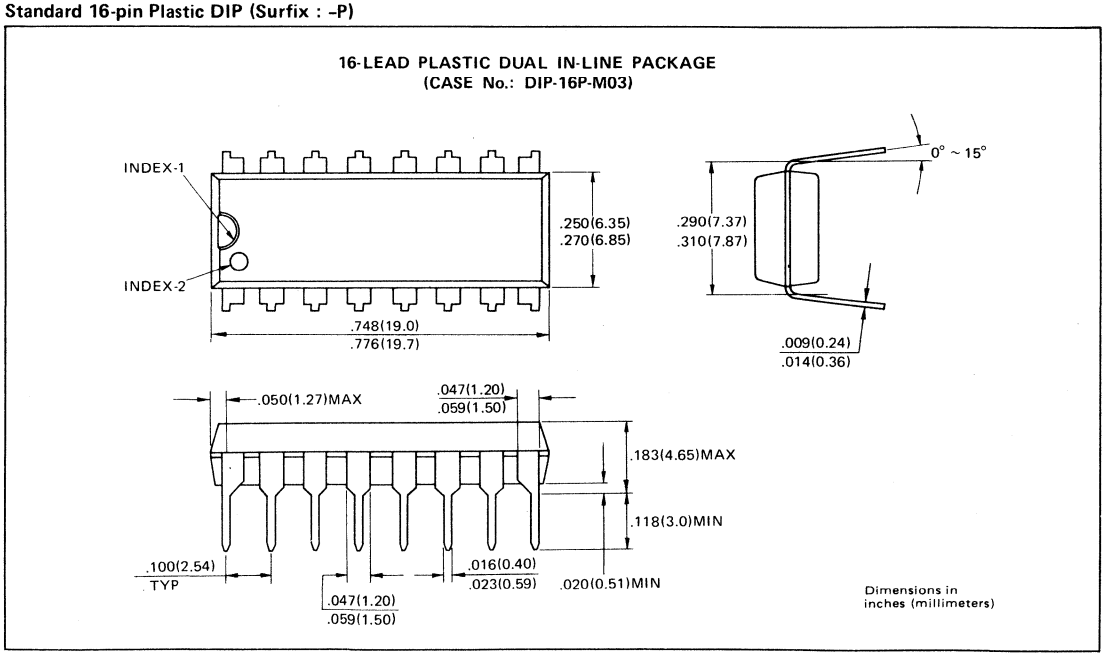


PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Surfix : -Z)

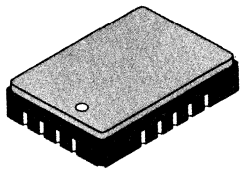


Standard 16-pin Plastic DIP (Surfix : -P)

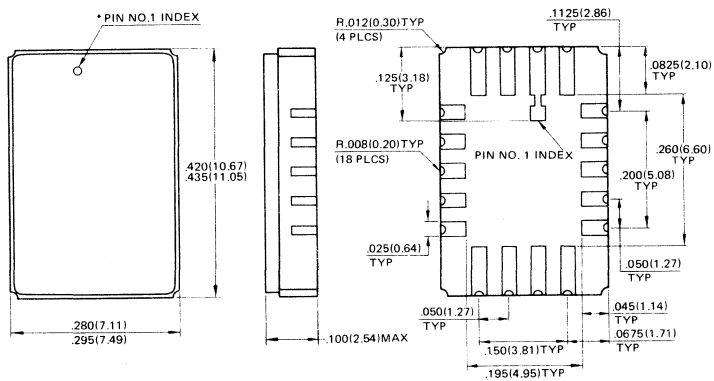


PACKAGE DIMENSIONS

Standard 18-pad Ceramic LCC (Surfix : -TV)



18-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-18C-F02)



*Shape of Pin 1 index: Subject to change without notice

Dimensions in inches
(millimeters)

Preliminary

MOS Memories

FUJITSU

■ MB8264A-12-W, MB8264A-15-W

NMOS 65,536-Bit Dynamic
Random Access Memory With
Wide Temperature Range

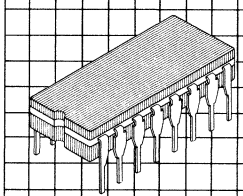
Description

The MB8264A-W is a 64K x 1 dynamic RAM intended for operation over the case temperature range −55°C to 110°C. The part is also available with Fujitsu's 883B high reliability screening.

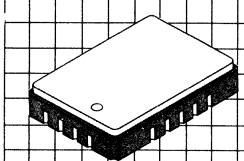
The MB8264A-W design has been optimized for high speed high performance applications such as mainframe memory, buffer memory, and peripheral storage where low power dissipation, compact layout, or wide temperature range operation are required.

The MB8264A-W has fully TTL compatible inputs and output. It operates on a single +5 V ± 10% power supply. An on chip substrate bias generator provides high performance operation. The MB8264A-W contains on-chip latches for the address inputs and for the data input.

The MB8264A-W is fabricated with Fujitsu's advanced silicon gate NMOS double layer polysilicon process. This process along with the use of single transistor storage cells permits maximum circuit density and minimum chip size. Multiplexed row and column addressing allows the MB8264A-W to be packaged in a standard 16-pin DIP.



Cerdip Package
DIP-16C-C04

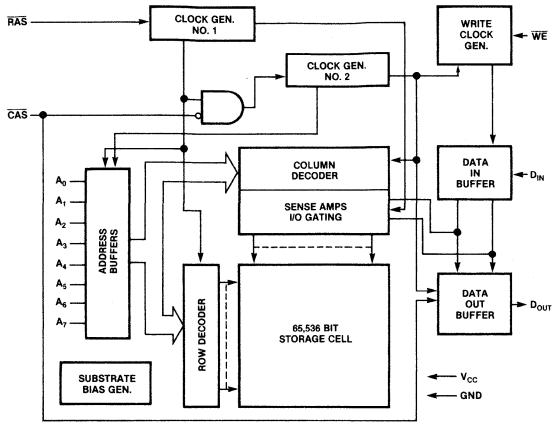


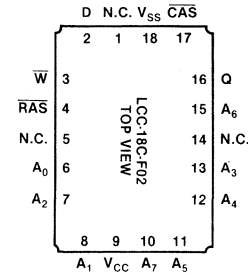
LCC-18C-F02

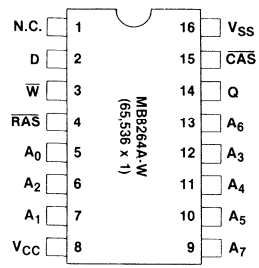
Features

- **Wide Temperature Range TC = −55°C to 110°C**
- **65,536 × 1 organization**
- **Row Access Time:**
  120 ns max. (MB8264A-12-W)
  150 ns max. (MB8264A-15-W)
- **Cycle Time:**
  230 ns min. (MB8264A-12-W)
  260 ns min. (MB8264A-15-W)
- **Low Power (Active)**
  305 mW max. (MB8264A-12-W)
  275 mW max. (MB8264A-15-W)
  33 mW max. (Standby)
- **1 ms/128 cycle refresh**
- **$\overline{RAS}$-Only and Hidden Refresh**
- **Read-Modify-Write capability**
- **Page Mode capability**
- **Common I/O capability using the early write operation**
- **Output unlatched at cycle end allows extended page boundary**
- **t_{AR}, t_{WCR}, t_{DHR} are eliminated**
- **883B processing available**

Block Diagram and Pin Assignments







Capacitance
($T_A = 25\,°C$)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance $A_0 \sim A_7$, D	C_{IN1}	—	5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$	C_{IN2}	—	8	pF
Output Capacitance D_{OUT}	C_{OUT}	—	7	pF

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature (case)
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	−55 °C to +110 °C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

AC Characteristics
(Recommended operating conditions unless otherwise noted.)
(Notes 1, 2, 3)

Parameter	Notes	Symbol	MB8264A -12-A Min	MB8264A -12-A Max	MB8264A -15-W Min	MB8264A -15-W Max	Unit
Time between Refresh		t_{REF}	—	1	—	1	ms
Random Read/Write Cycle Time		t_{RC}	230	—	260	—	ns
Read-Write Cycle Time		t_{RWC}	265	—	280	—	ns
Page Mode Cycle Time		t_{PC}	120	—	145	—	ns
Page Mode Read-Write Cycle Time		t_{PRWC}	155	—	180	—	ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}	—	120	—	150	ns
Access Time from $\overline{CAS}$	5 6	t_{CAC}	—	60	—	75	ns
Output Buffer Turn off Delay		t_{OFF}	0	35	0	40	ns
Transition Time		t_T	3	50	0	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	100	—	100	—	ns
$\overline{RAS}$ Pulse Width		t_{RAS}	120	10000	150	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	60	—	75	—	ns
$\overline{CAS}$ Precharge Time (Page mode only)		t_{CP}	50	—	60	—	ns
$\overline{CAS}$ Precharge Time (All cycles except page mode)		t_{CPN}	30	—	30	—	ns
$\overline{CAS}$ Pulse Width		t_{CAS}	60	10000	75	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	120	—	150	—	ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7 8	t_{RCD}	20	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0	—	0	—	ns
Row Address Set Up Time		t_{ASR}	0	—	0	—	ns
Row Address Hold Time		t_{RAH}	10	—	15	—	ns
Column Address Set Up Time		t_{ASC}	0	—	0	—	ns
Column Address Hold Time		t_{CAH}	15	—	20	—	ns
Read Command Set Up Time		t_{RCS}	0	—	0	—	ns
Read Command Hold Time Reference to $\overline{CAS}$	10	t_{RCH}	0	—	0	—	ns
Read Command Hold Time Referenced to $\overline{RAS}$	10	t_{RRH}	20	—	20	—	ns
Write Command Set Up Time	9	t_{WCS}	0	—	0	—	ns
Write Command Hold Time		t_{WCH}	25	—	30	—	ns
Write Command Pulse Width		t_{WP}	25	—	30	—	ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	40	—	45	—	ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	40	—	45	—	ns
Data In Set Up Time		t_{DS}	0	—	0	—	ns
Data In Hold Time		t_{DH}	25	—	30	—	ns
$\overline{CAS}$ to $\overline{WE}$ Delay	9	t_{CWD}	50	—	60	—	ns
$\overline{RAS}$ to $\overline{WE}$ Delay	9	t_{RWD}	110	—	120	—	ns

Notes:

1) An initial pause of 200 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved.
2) AC characteristics assume $t_T = 5$ ns.
3) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
4) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5) Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6) Measured with a load equivalent to 2 TTL loads and 100 pF.
7) Operation within the t_{RCD} (max) limit insures that t_{RAC} can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
8) t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T = 5 ns) + t_{ASC} (min).
9) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.
   If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
10) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
OPERATING CURRENT* Average Power Supply Current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB8264A-12-W MB8264A-15-W	I_{CC1}		55 50	mA
STANDBY CURRENT Standby Power Supply Current ($\overline{RAS} = \overline{CAS} = V_{IH}$)		I_{CC2}		6	mA
REFRESH CURRENT* Average Power Supply Current ($\overline{CAS} = V_{IH}$, $\overline{RAS}$ cycling; t_{RC} = min)	MB8264A-12-W MB8264A-15-W	I_{CC3}		40 35	mA
PAGE MODE CURRENT* Average Power Supply Current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; t_{PC} = min)	MB8264A-12-W MB8264A-15-W	I_{CC4}		40 35	mA
INPUT LEAKAGE CURRENT Input Leakage Current, any input ($0V \leq V_{IN} \leq 5.5V$, $V_{CC} = 5.5V$, $V_{SS} = 0V$, all other pins not under test = 0V)		$I_{I(L)}$	−10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0 \leq V_{OUT} \leq 5.5$)		$I_{O(L)}$	−10	10	μA
OUTPUT LEVELS Output High Voltage ($I_{OH} = -5mA$) Output Low Voltage ($I_{OL} = 4.2mA$)		V_{OH} V_{OL}	2.4	 0.4	V V

Note *: I_{CC} is dependent on output loading cycle rates. Specified values are obtained with the output open.

Description

Address Inputs

A total of sixteen binary input address bits are required to decode any 1 of 65,536 storage cell locations within the MB8264A-W. Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stabled on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high on $\overline{WE}$ dictates read mode; logic low dictates write mode. Data input is disabled when read mode is selected.

Data Input

Data is written into the MB8264A-W during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from the transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from the transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode

Page mode operation permits strobing the row-address into the MB8264A-W while maintaining $\overline{RAS}$ at a logic low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

RAS-Only Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

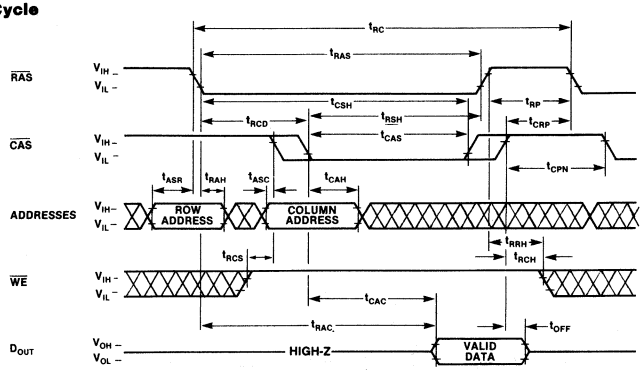
Hidden Refresh

$\overline{RAS}$-ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

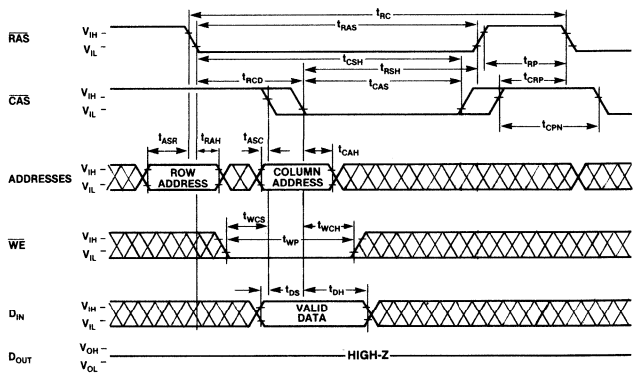
Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

Timing Diagrams

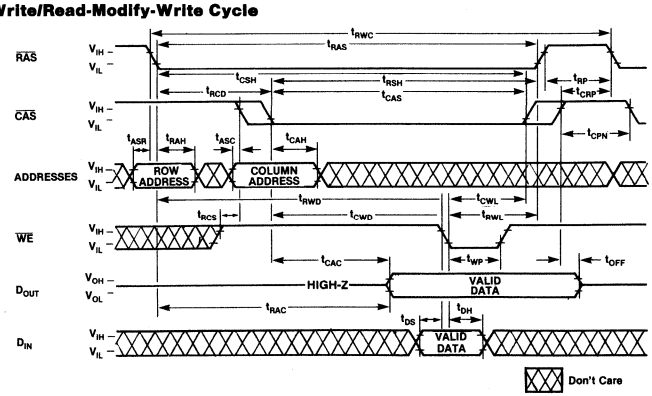
Read Cycle



Write Cycle (Early Write)

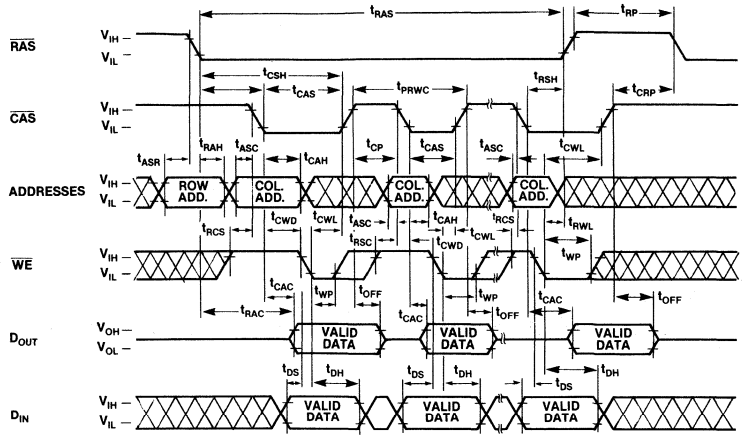


Read-Write/Read-Modify-Write Cycle



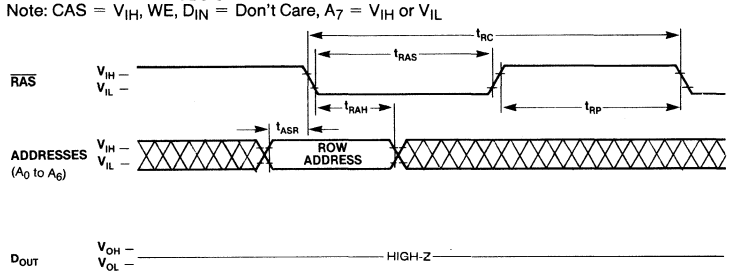
Timing Diagrams, Continued

Page Mode Read-Write Cycle

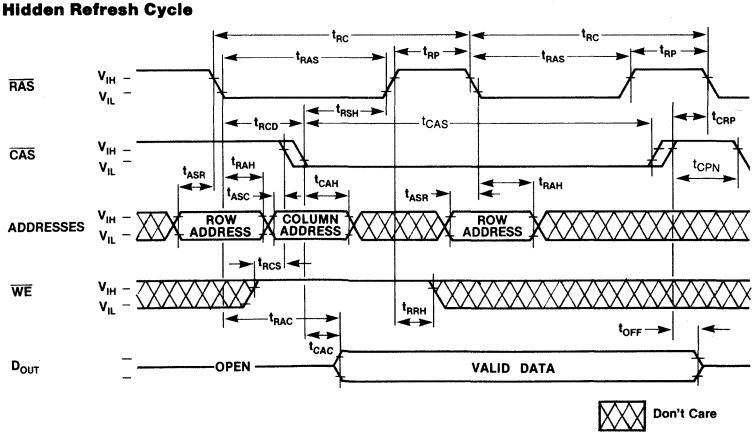


RAS-ONLY Refresh Cycle

Note: CAS = V_{IH}, WE, D_{IN} = Don't Care, A_7 = V_{IH} or V_{IL}

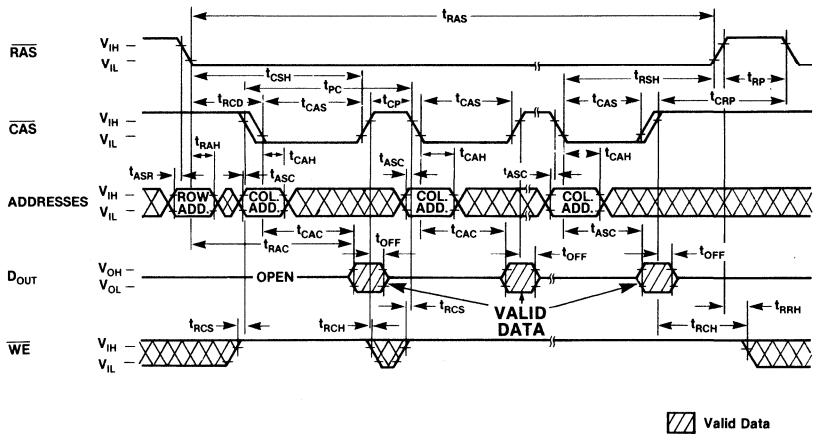


Hidden Refresh Cycle

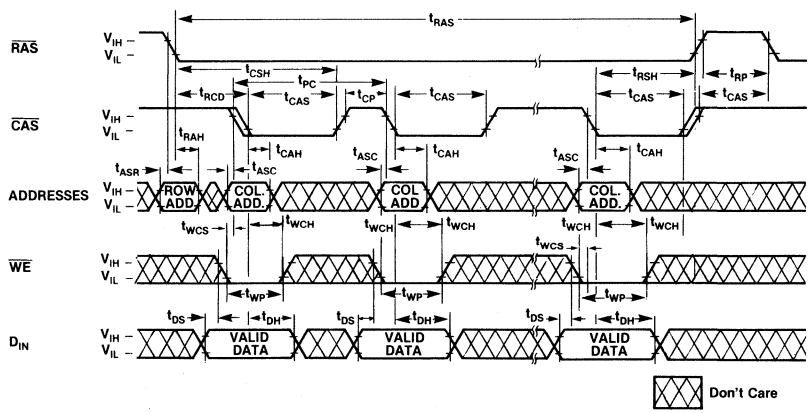


Timing Diagrams, Continued

Page Mode Read Cycle



Page Mode Write Cycle



FUJITSU

MOS 65536-BIT DYNAMIC RANDOM ACCESS MEMORY

MB 8265A-10
MB 8265A-12
MB 8265A-15

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

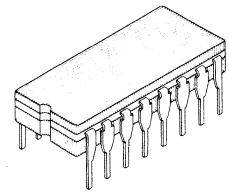
The Fujitsu MB 8265A is a fully decoded, dynamic random access memory organized as 65,536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MB 8265A to be housed in a standard 16 pin DIP and 18 pad LCC. Pin-outs conform to the JEDEC approved pin out.

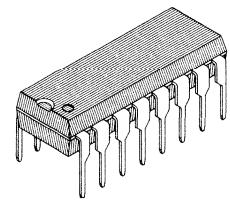
The MB 8265A is fabricated using silicon gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are non-critical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

- 65,536 x 1 RAM, 16 pin DIP/18 pad LCC
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  100 ns max (MB 8265A-10)
  120 ns max (MB 8265A-12)
  150 ns max (MB 8265A-15)
- Cycle time,
  190 ns min (MB 8265A-10)
  230 ns min (MB 8265A-12)
  260 ns min (MB 8265A-15)
- Single +5V Supply, ±10% tolerance
- Low power (active)
  275 mW max (MB 8265A-10)
  248 mW max (MB 8265A-12)
  220 mW max (MB 8265A-15)
  25mW standby (max)
- 2 ms/128 refresh cycle
- $\overline{RAS}$-only and $\overline{RFSH}$ (pin 1) refresh capability
- Offers two variations of Hidden refresh
- Read-Modify-Write, and Page-mode capability
- Common I/O capability using Early Write operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- On-chip latches for Addresses and Data-in
- t_{AR}, t_{WCR}, t_{DHR} are eliminated
- Standard 16-pin Ceramic (Cerdip) DIP: Suffix-Z
  Standard 16-pin Plastic DIP: Suffix-P
  Standard 18-pad Ceramic LCC: Suffix-TV



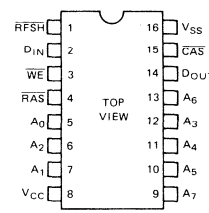
CERAMIC PACKAGE
CERDIP
DIP-16C-C04

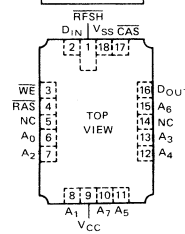


PLASTIC PACKAGE
DIP-16P-M03

LCC-18C-F02 : See Page 1-218

PIN ASSIGNMENT





LCC PAD CONFIGURATION : See Page 1-218

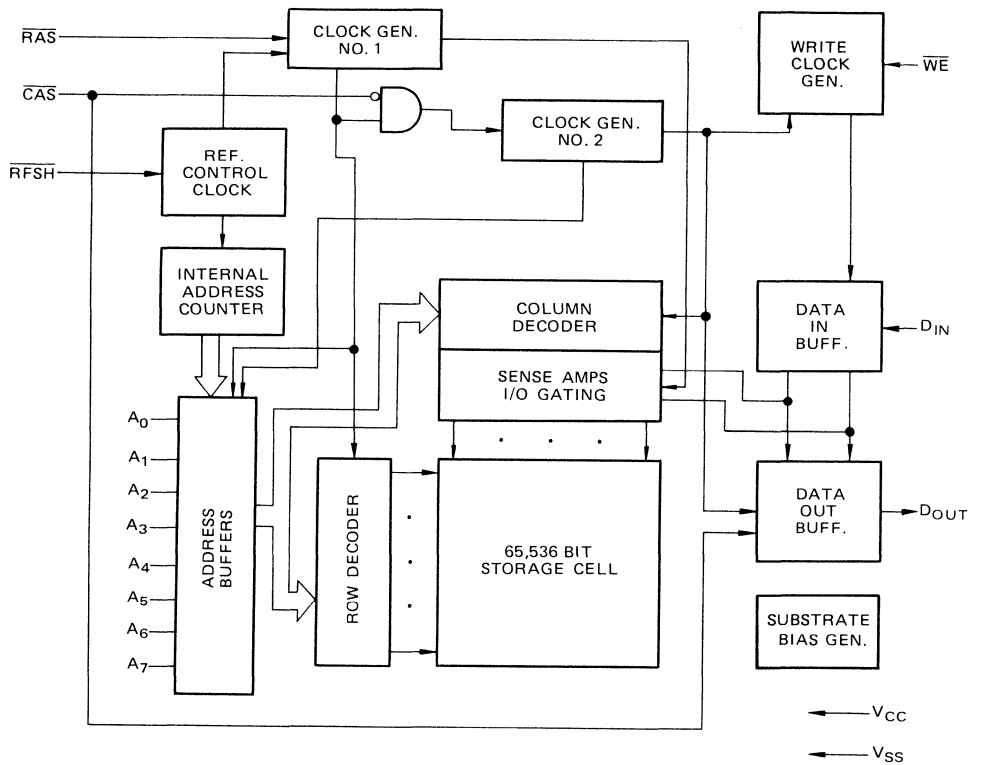
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	−1 to +7	V
Storage temperature	Ceramic	T_{STG}	−55 to +150	°C
	Pastic		−55 to +125	
Power dissipation		P_D	1.0	W
Short circuit output current			50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB 8265A BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance A_0 to A_7, D_{IN}	C_{IN1}		5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{RFSH}$	C_{IN2}		8	pF
Output Capacitance D_{OUT}	C_{OUT}		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V	0°C to +70°C
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}*	-1.0		0.8	V	

Note * : The device can withstand undershoots to the –2V level with a pulse width of 20 ns.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
OPERATING CURRENT* Average power supply current ($\overline{RFSH}$ = V_{IH}, $\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 8265A-10	I_{CC1}		50	mA
	MB 8265A-12			45	
	MB 8265A-15			40	
STANDBY CURRENT Standby power supply current ($\overline{RAS}$ = $\overline{CAS}$ = $\overline{RFSH}$ = V_{IH})		I_{CC2}		4.5	mA
REFRESH CURRENT 1* Average power supply current ($\overline{CAS}$ = $\overline{RFSH}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	MB 8265A-10	I_{CC3}		38	mA
	MB 8265A-12			35	
	MB 8265A-15			31	
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{RFSH}$ = V_{IH}, $\overline{CAS}$ cycling; t_{PC} = min)	MB 8265A-10	I_{CC4}		35	mA
	MB 8265A-12			32	
	MB 8265A-15			28	
REFRESH CURRENT 2* Average power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, $\overline{RFSH}$ cycling; t_{FC} = min)	MB 8265A-10	I_{CC5}		42	mA
	MB 8265A-12			38	
	MB 8265A-15			34	
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≦ V_{IN} ≦ 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not test = 0V)		$I_{I(L)}$	-10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≦ V_{OUT} ≦ 5.5V)		$I_{O(L)}$	-10	10	μA
OUTPUT LEVELS Output high voltage (I_{OH} = -5mA) Output low voltage (I_{OL} = 4.2mA)		V_{OH} V_{OL}	2.4	 0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1,2,3

Parameter	NOTES	Symbol	MB 8265A-10		MB 8265A-12		MB 8265A-15		Unit
			Min	Max	Min	Max	Min	Max	
Time between Refresh		t_{REF}		2		2		2	ms
Random Read/Write Cycle Time		t_{RC}	190		230		260		ns
Read-Write Cycle Time		t_{RWC}	230		265		280		ns
Page Mode Cycle Time		t_{PC}	105		120		145		ns
Page Mode Read-Write Cycle Time		t_{PRWC}	135		155		180		ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}		100		120		150	ns
Access Time from $\overline{CAS}$	5 6	t_{CAC}		50		60		75	ns
Output Buffer Turn Off Delay		t_{OFF}	0	30	0	35	0	40	ns
Transition Time		t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Tim		t_{RP}	80		100		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	100	10000	120	10000	150	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	50		60		75		ns
$\overline{CAS}$ Precharge Time (Page mode only)		t_{CP}	45		50		60		ns
$\overline{CAS}$ Precharge Time (All cycles except page mode)		t_{CPN}	20		20		25		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	50	10000	60	10000	75	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	100		120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7 8	t_{RCD}	20	50	20	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	0		0		0		ns
Row Address Set Up Time		t_{ASR}	0		0		0		ns
Row Address Hold Time		t_{RAH}	10		10		15		ns
Column Address Set Up Time		t_{ASC}	0		0		0		ns
Column Address Hold Time		t_{CAH}	15		15		20		ns
Read Command Set Up Time		t_{RCS}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{CAS}$	10	t_{RCH}	0		0		0		ns
Read Command Hold Time Referenced to $\overline{RAS}$	10	t_{RRH}	20		20		20		ns
Write Command Set Up Time	9	t_{WCS}	0		0		0		ns
Write Command Hold Time		t_{WCH}	20		25		30		ns
Write Command Pulse Width		t_{WP}	20		25		30		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	35		40		45		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	35		40		45		ns
Data In Set Up Time		t_{DS}	0		0		0		ns
Data In Hold Time		t_{DH}	20		25		30		ns
$\overline{CAS}$ to $\overline{WE}$ Delay	9	t_{CWD}	40		50		60		ns
$\overline{RAS}$ to $\overline{WE}$ Delay	9	t_{RWD}	90		110		120		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time ($\overline{RAS}$-only refresh)		t_{RPC}	20		20		20		ns

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1,2,3

Parameter	NOTES	Symbol	MB 8265A-10		MB 8265A-12		MB8265A-15		Unit
			Min	Max	Min	Max	Min	Max	
$\overline{RFSH}$ Set up Time Referenced to $\overline{RAS}$		t_{FSR}	90		100		100		ns
$\overline{RAS}$ to $\overline{RFSH}$ Delay ($\overline{RFSH}$ refresh)		t_{RFD}	90		100		100		ns
$\overline{RFSH}$ Cycle Time ($\overline{RFSH}$ refresh)		t_{FC}	200		230		260		ns
$\overline{RFSH}$ Pulse Width ($\overline{RFSH}$ refresh)		t_{FP}	100		120		150		ns
$\overline{RFSH}$ Inactive Time ($\overline{RFSH}$ refresh)		t_{FI}	90		100		100		ns
$\overline{RFSH}$ to $\overline{RAS}$ Delay	11	t_{FRD}	20		30		40		ns
$\overline{RFSH}$ Hold Time	11	t_{FSH}	30		40		50		ns

Notes:

1 An initial pause of 200 μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RFSH}$ cycles before proper device operation is achieved.
If internal refresh counter is to be effective, a minimum of 8 active $\overline{RFSH}$ initialization cycles is required. The internal refresh counter must be activated a minimum of 128 times every 2 ms if the $\overline{RFSH}$ refresh function is used.
If the $\overline{RFSH}$ refresh function is not used, $\overline{RFSH}$ (pin 1) pin can be open.

2 AC characteristics assume t_T = 5ns.

3 V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max.).

4 Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

5 Assumes that $t_{RCD} \geq t_{RCD}$ (max).

6 Measured with a load equivalent to 2 TTL loads and 100 pF.

7 Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

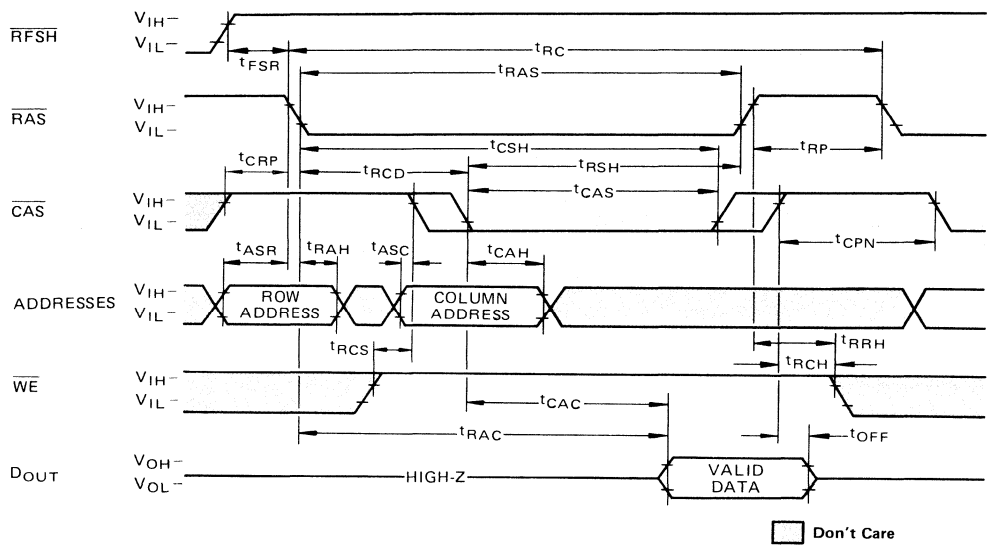
8 t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T=5ns) + t_{ASC} (min)

9 t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.
If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.

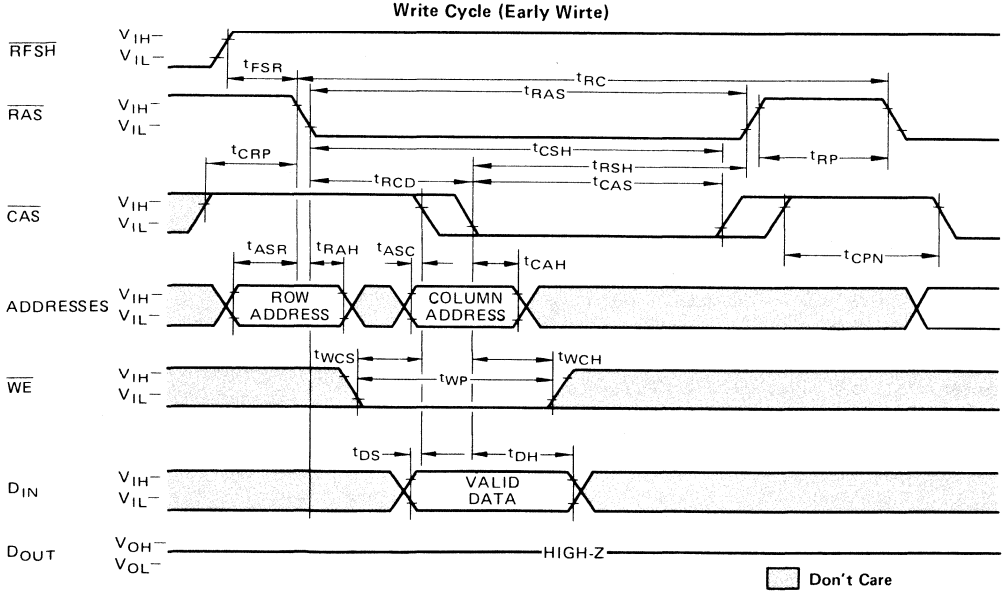
10 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

11 $\overline{RFSH}$ counter test read/write cycle only.

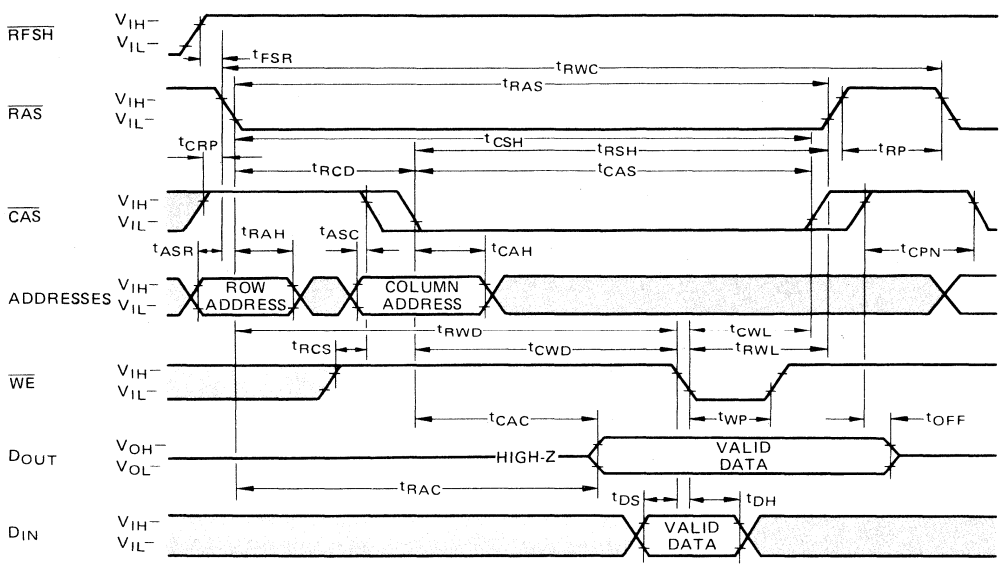
Read Cycle



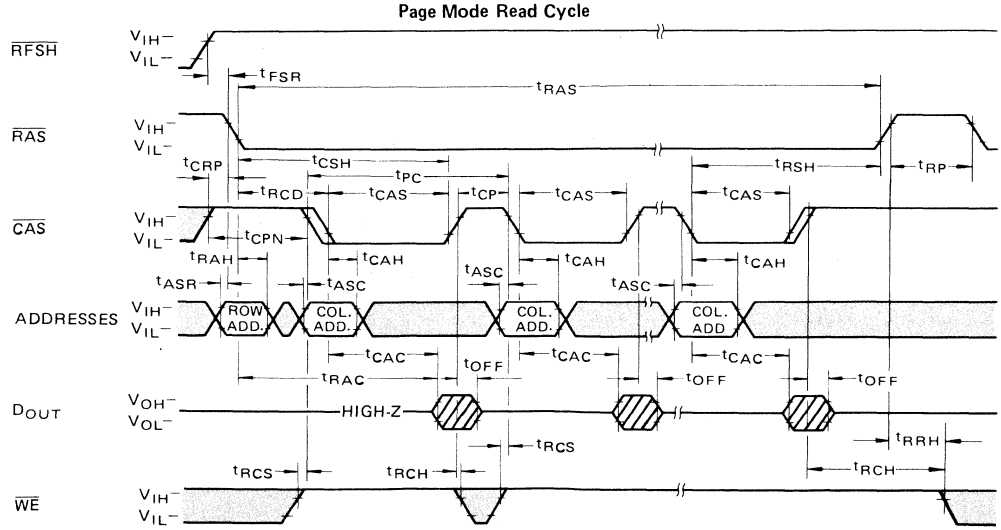
Write Cycle (Early Wirte)



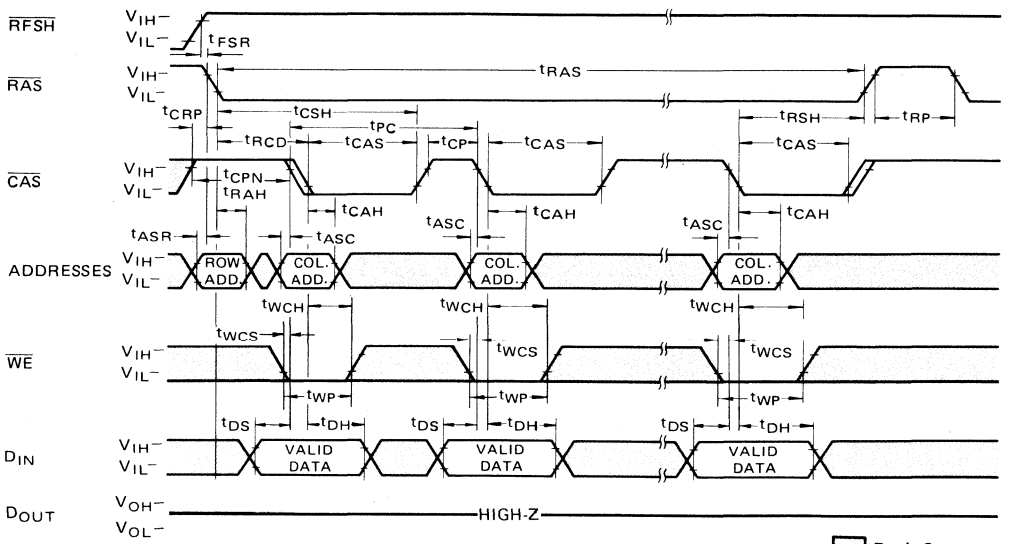
Read–Write/Read–Modify–Write Cycle



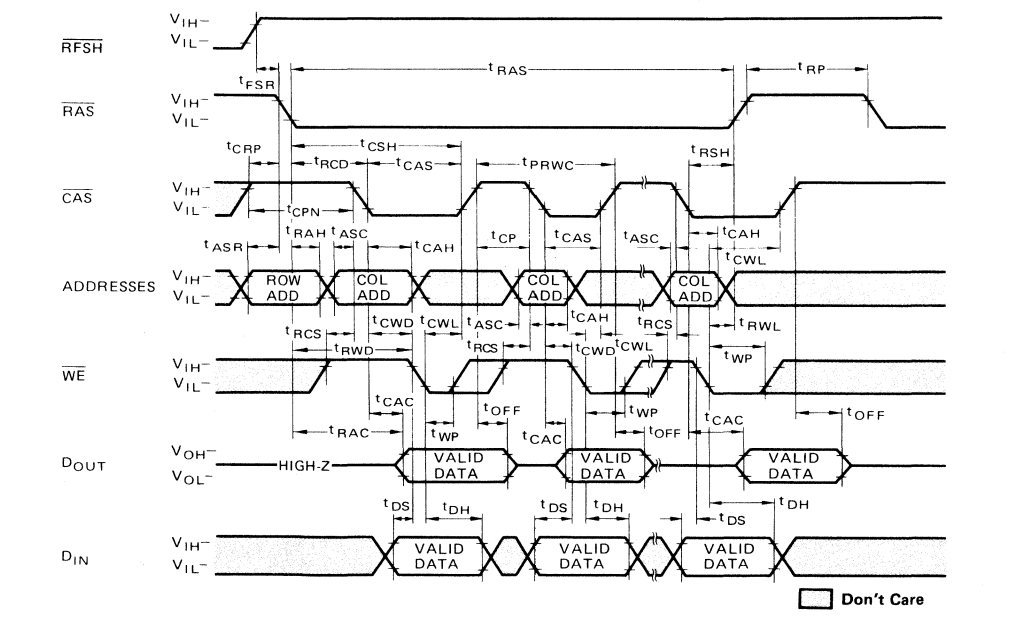
Page Mode Read Cycle



Page Mode Write Cycle

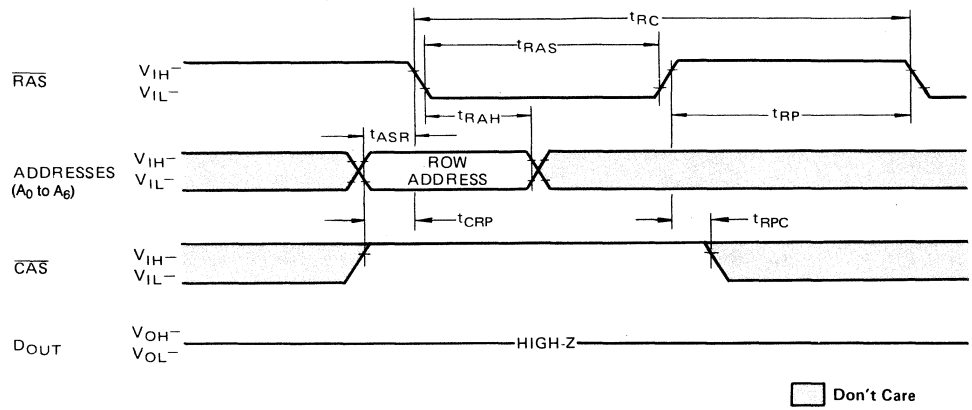


Page Mode Read-Write Cycle



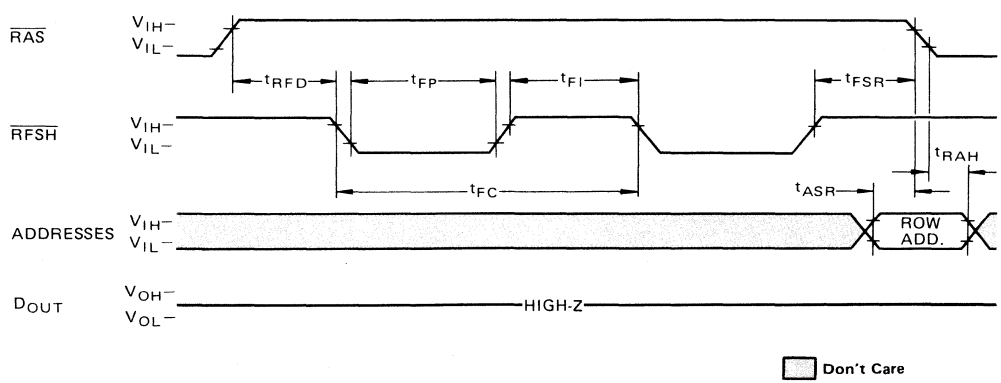
$\overline{RAS}$-only Refresh Cycle

Note: $\overline{RFSH} = V_{IH}$, $\overline{WE}$, D_{IN} = Don't care, $A_7 = V_{IH}$ or V_{IL}

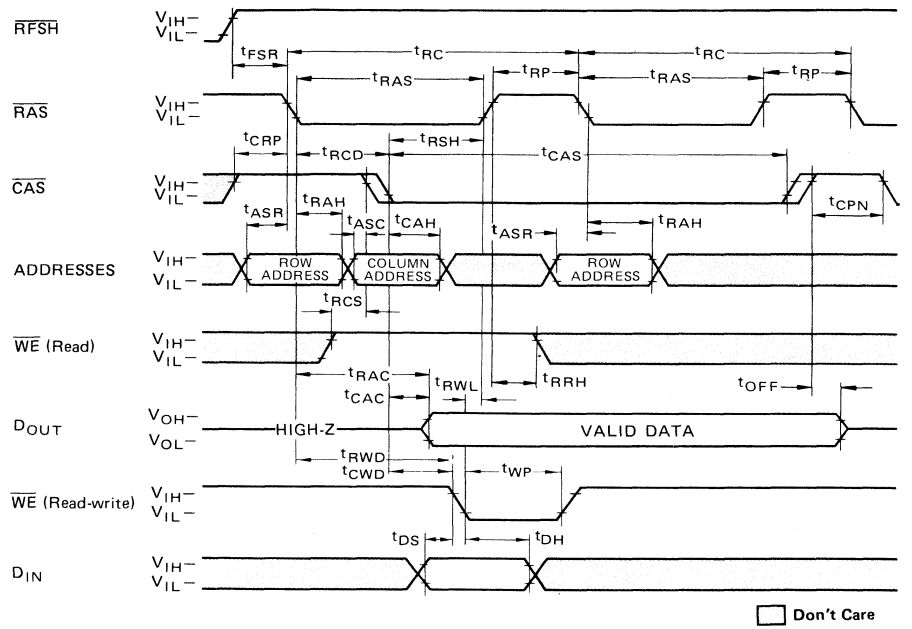


$\overline{RFSH}$ Refresh Cycle

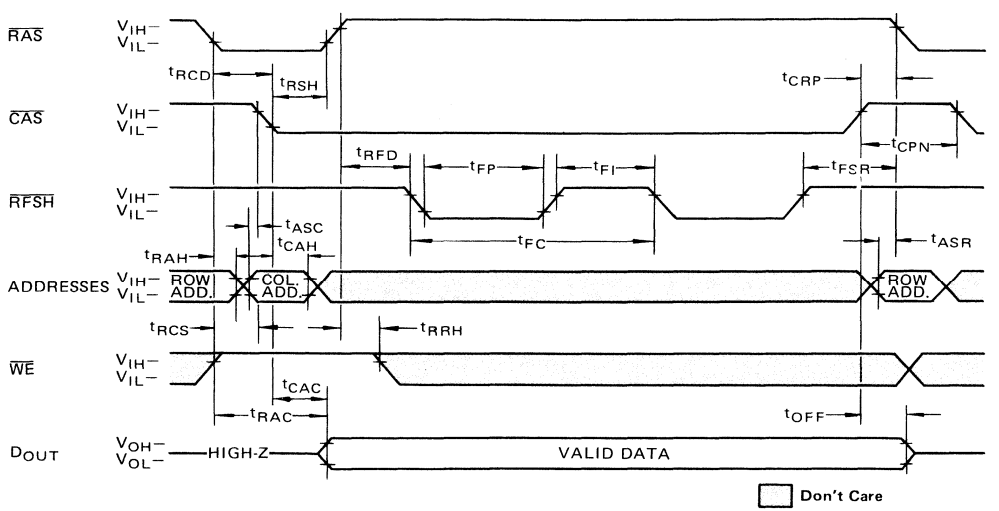
Note: $\overline{CAS} = V_{IH}$, $\overline{WE}$, D_{IN} = Don't care

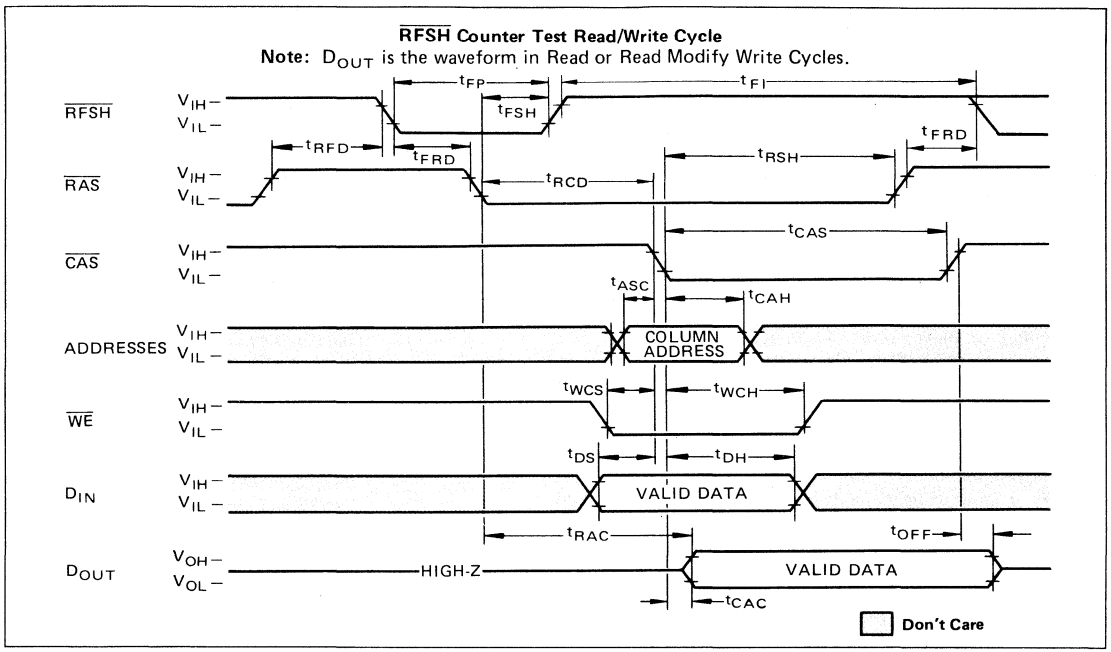


Hidden $\overline{RAS}$ only Refresh Cycle



Hidden $\overline{RFSH}$ Refresh Cycle





DESCRIPTION

Address Inputs:
A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MB 8265A. Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permite triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:
The read mode or write mode is selected with the $\overline{WE}$ input. A high on $\overline{WE}$ selects read mode and low selects write mode. Data input is disabled when read mode is selected.

Data Input:
Data is written into the MB 8265A during a write or read-write cycle. The later falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ can be low after $\overline{CAS}$ has been low and $\overline{CAS}$ to $\overline{WE}$ Delay Time (t_{CWD}) has been satisfied. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:
The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from the falling edge of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to a high. In a write cycle the indentical sequence occurs, but data is not valid.

Page Mode:
Page-mode operation permits strobing

the row-address into the MB 8265A while maintaining $\overline{RAS}$ at low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the falling edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. The MB 8265A offers the following three types of refresh.

1) $\overline{RAS}$-only Refresh;
$\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation. During $\overline{RAS}$ only refresh, either V_{IL} or V_{IH} is permitted for A_7.

2) $\overline{RFSH}$ Refresh;
$\overline{RFSH}$ type refreshing available on the MB 8265A offers an alternate refresh method: (1) When $\overline{RFSH}$ is brought low (active) during $\overline{RAS}$ is high (inactive), on-chip refresh control clock generators and a refresh address counter are enabled and an internal refresh operation takes place.
(2) When $\overline{RFSH}$ is brought high (inactive), the internal refresh address counter is automatically incremented in preparation for the next $\overline{RFSH}$ refresh cycle. Only $\overline{RFSH}$ activated cycles affect the internal address counter.
The use of $\overline{RFSH}$ type refreshing eliminates the need of providing any additional external devices to generate refresh addresses. Refer to the Fig. 2 for the example of $\overline{RFSH}$ refresh.

3) Hidden Refresh;
Hidden Refresh Cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time from the previous memory read or cycle or read-write.
The MB 8265A offers two types of Hidden Refresh. They are referred to as Hidden $\overline{RAS}$-only Refresh and Hidden $\overline{RFSH}$ Refresh.
A) Hidden $\overline{RAS}$-only Refresh
Hidden $\overline{RAS}$-only Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified percharge period (t_{RP}), executing "$\overline{RAS}$-only" refresh, but with $\overline{CAS}$ held low.
$\overline{RFSH}$ has to be held at V_{IH}.
B) Hidden $\overline{RFSH}$ Refresh
Hidden $\overline{RFSH}$ Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RFD}), executing $\overline{RFSH}$ refresh, but with $\overline{CAS}$ held low.
A specified precharge period (t_{CPN}) is required before normal memory Read, Write or Read-Modify-Write cycle after performing either type of Hidden Refresh.

Refresh Counter Test Cycle:
A special timing sequence provides a convenient method of verifying the functionality of the $\overline{RFSH}$ activated circuitry.

(A) $\overline{RFSH}$ Test Read/Write Cycle:
When $\overline{RFSH}$ is given a signal in timing as shown in timing diagram of $\overline{RFSH}$ counter Test Read/Write Cycle, Read/Write Operation is enabled. A memory cell address (consisting of a row address (8 bits) and a column address (8 bits)) to be accessed can be defined as follows:

*A ROW ADDRESS – Bits $A_0 \sim A_6$ are defined when contents of the internal address counter are latched. (The other bit A_7 is set low internally.)

*A COLUMN ADDRESS – All the bits $A_0 \sim A_7$ are defined by latching levels on $A_0 \sim A_7$ pins in a high-to-low transition of $\overline{CAS}$.

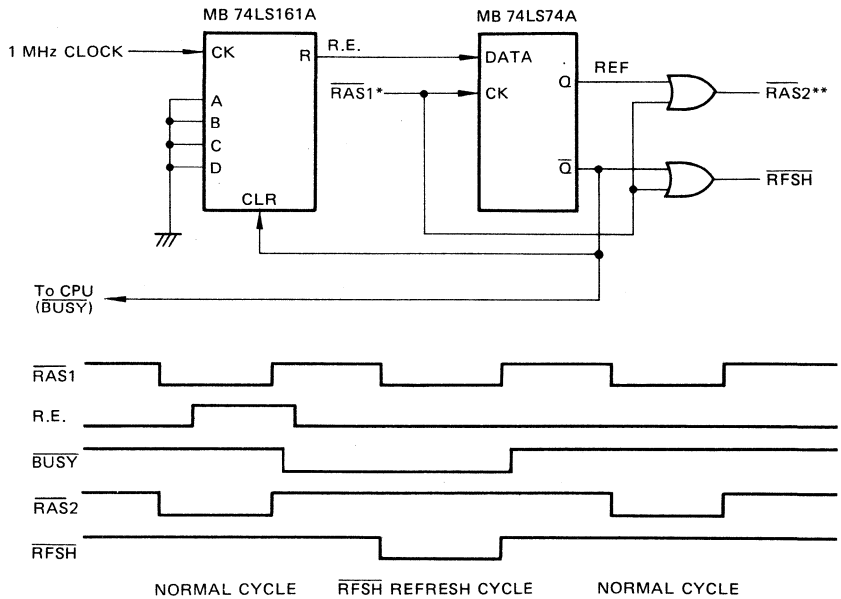
By using a 15-bit address latched into the on-chip address buffers by means of the above operation, any of 32K (in the fixed half cell array) memory cells can be read/written into/from.

(B) $\overline{RFSH}$ Test Read Modify Wirte Cycle:
Also, Read Modify Write Operation (not only the above normal Read/Write Operations) can be used in this $\overline{RFSH}$ Counter Test Cycle.

(C) Example of Refresh Counter Test Procedure:

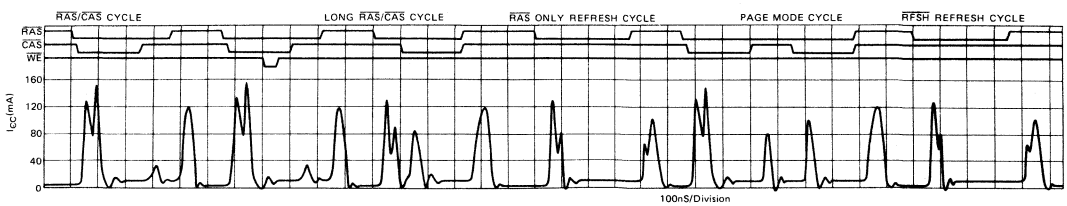
(1) Initialize the internal refresh counter. For this operation, 8 $\overline{RFSH}$ cycles are required.
(2) Write a test pattern of lows into memory cells at a single column address and 128 row addresses by using 128 $\overline{RFSH}$ Test Write Cycle or $\overline{RFSH}$ Test Read Modify Write Cycle.
(3) Verify the data written into the memory cells in the above step (2) by using the column address used in step (2) and sequence through 128 row address combinations ($A_0 \sim A_6$) by means of normal Read Cycle.
(4) Compliment the test pattern and repeat the steps (2) and (3).

Fig.2 — EXAMPLE OF $\overline{RFSH}$ REFRESH



**If $\overline{RFSH}$ refresh in not used, $\overline{RAS1}$ is connected to $\overline{RAS}$ input.
** $\overline{RAS2}$ should be connected $\overline{RAS}$ input.

Fig.3 — CURRENT WAVE FORM (V_{CC} = 5.5V, T_A = 25°C)



TYPICAL CHARACTERISTICS CURVES

Fig. 4 — NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

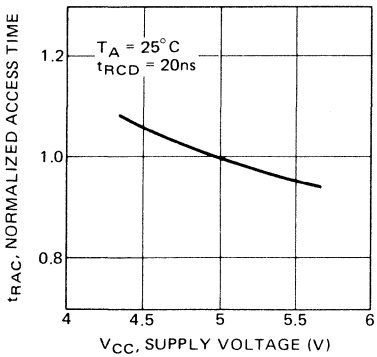


Fig. 5 — NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

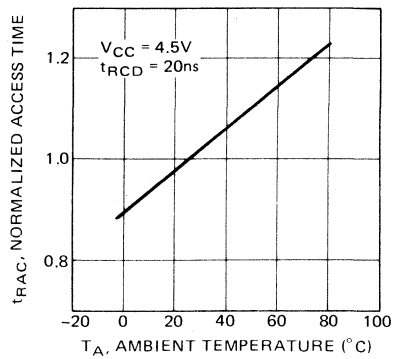


Fig. 6 — OPERATING CURRENT vs CYCLE RATE

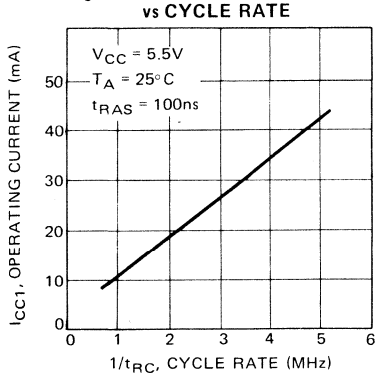
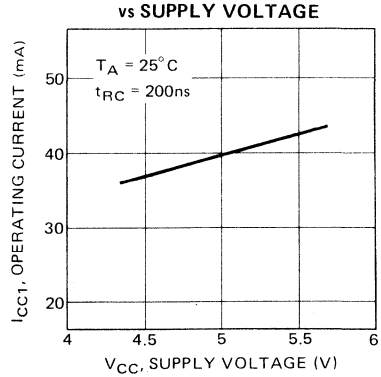


Fig. 7 — OPERATING CURRENT vs SUPPLY VOLTAGE



Fig, 8 — OPERATING CURRENT vs AMBIENT TEMPERATURE

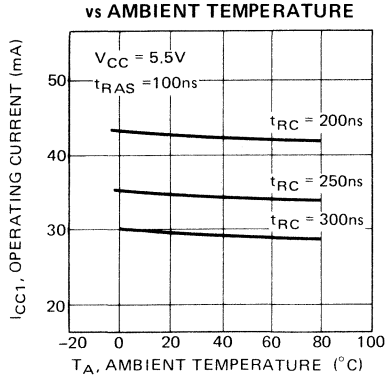


Fig. 9 — STANDBY CURRENT vs SUPPLY VOLTAGE

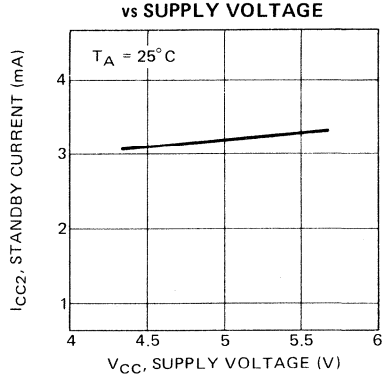


Fig. 10 — STANDBY CURRENT vs AMBIENT TEMPERATURE

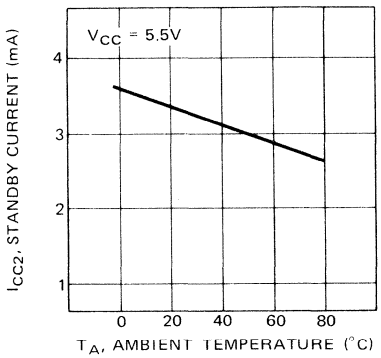


Fig. 11 — REFRESH CURRENT 1 vs CYCLE RATE

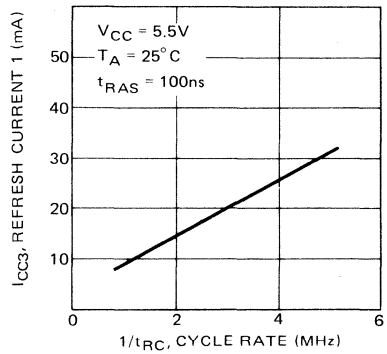


Fig. 12 — REFRESH CURRENT 1 vs SUPPLY VOLTAGE

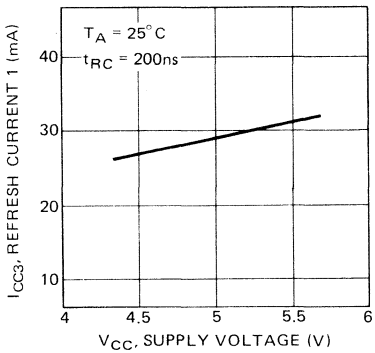


Fig. 13 — REFRESH CURRENT 1 vs AMBIENT TEMPERATURE

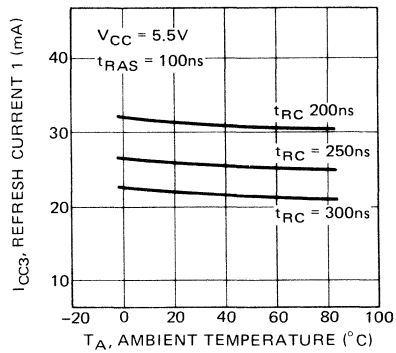


Fig. 14 — PAGE MODE CURRENT vs CYCLE RATE

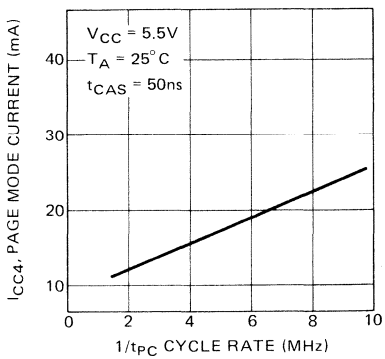


Fig. 15 — PAGE MODE CURRENT vs SUPPLY VOLTAGE

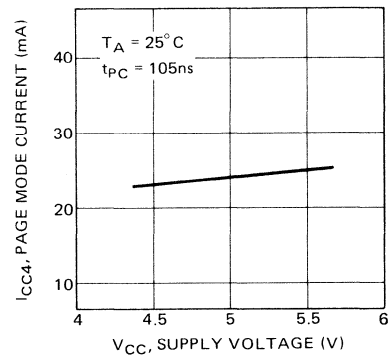


Fig. 16 — PAGE MODE CURRENT vs AMBIENT TEMPERATURE

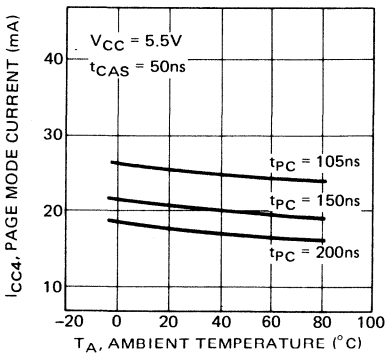


Fig. 17 — REFRESH CURRENT 2 vs CYCLE RATE

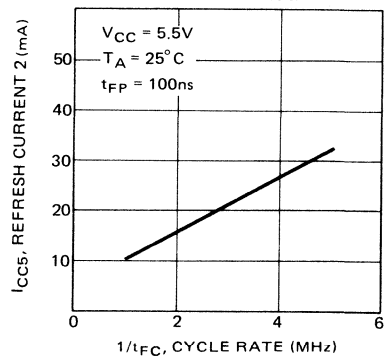


Fig. 18 — REFRESH CURRENT 2 vs SUPPLY VOLTAGE

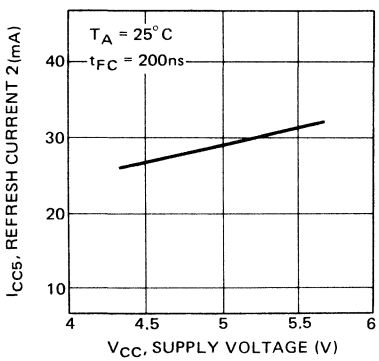


Fig. 19 — REFRESH CURRENT 2 vs AMBIENT TEMPERATURE

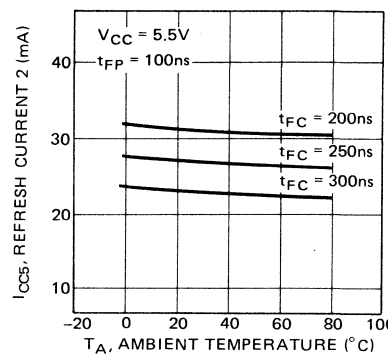


Fig. 20 — ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

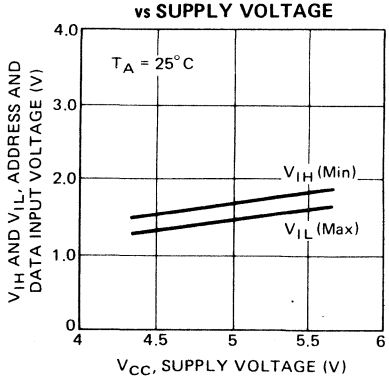


Fig. 21 — ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE

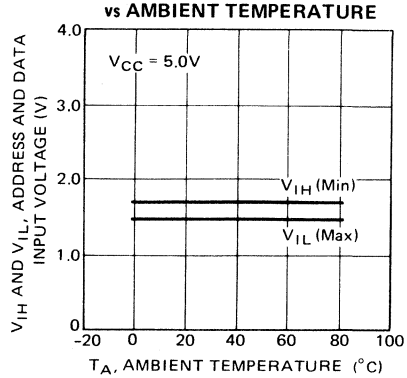


Fig. 22 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

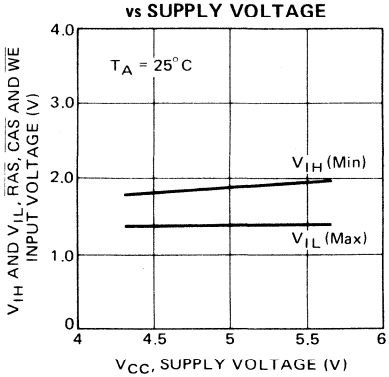


Fig. 23 – $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ VOLTAGE vs AMBIENT TEMPERATURE

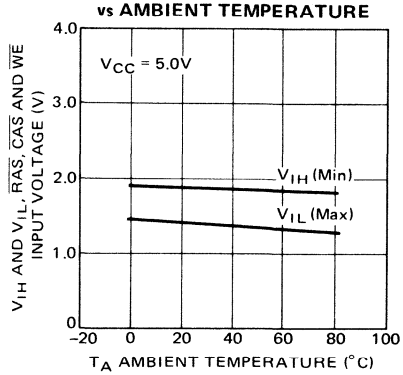
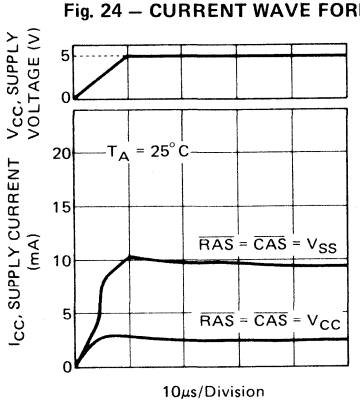


Fig. 24 – CURRENT WAVE FORM DURING POWER UP



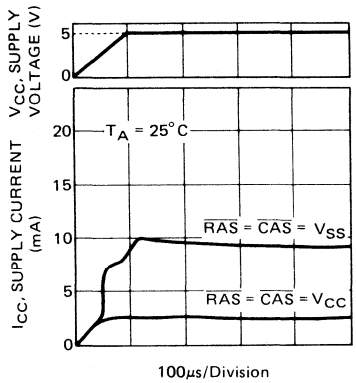
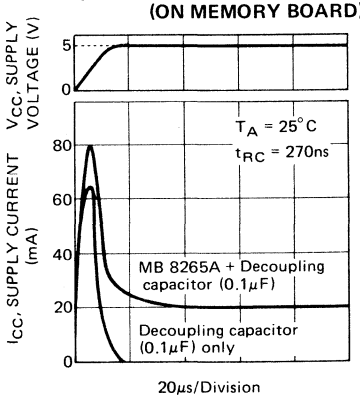


Fig. 25 – CURRENT WAVE FORM DURING POWER UP (ON MEMORY BOARD)



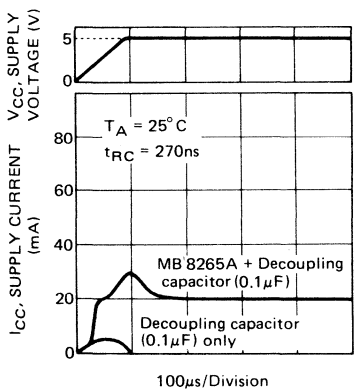
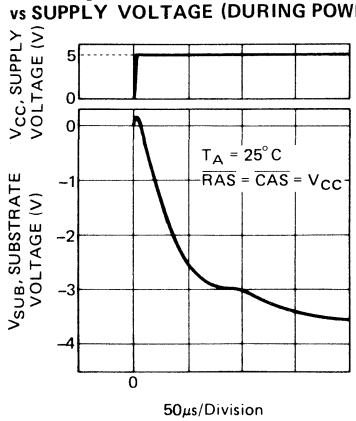
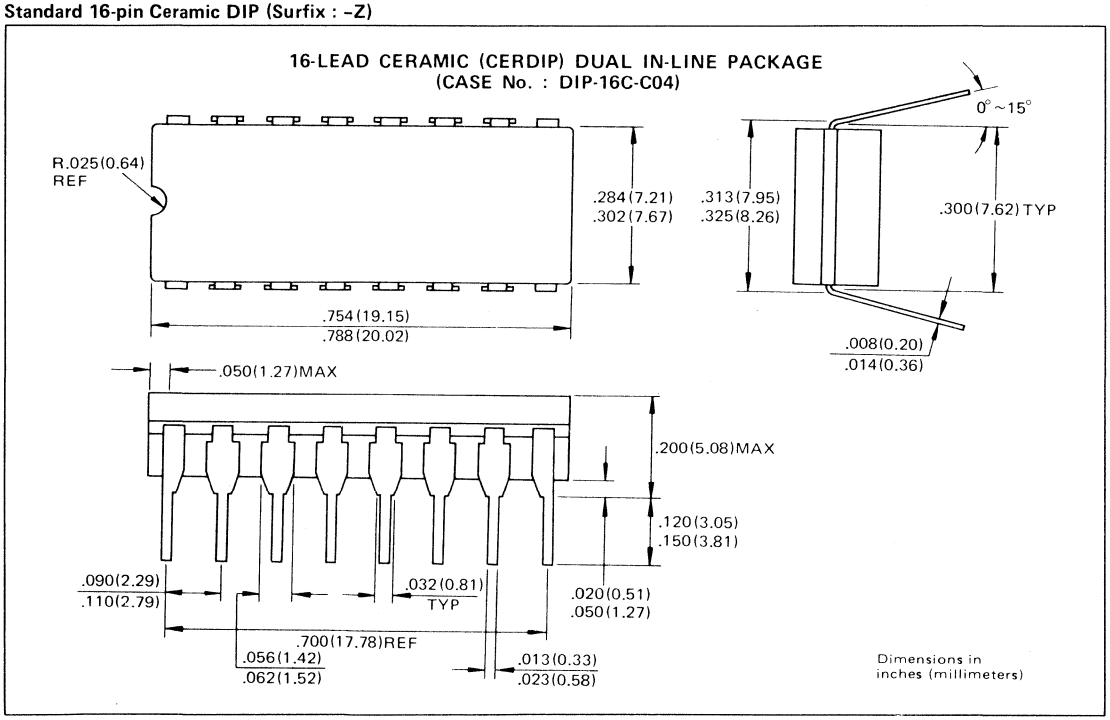


Fig. 26 – SUBSTRATE VOLTATE vs SUPPLY VOLTAGE (DURING POWER UP)



PACKAGE DIMENSIONS

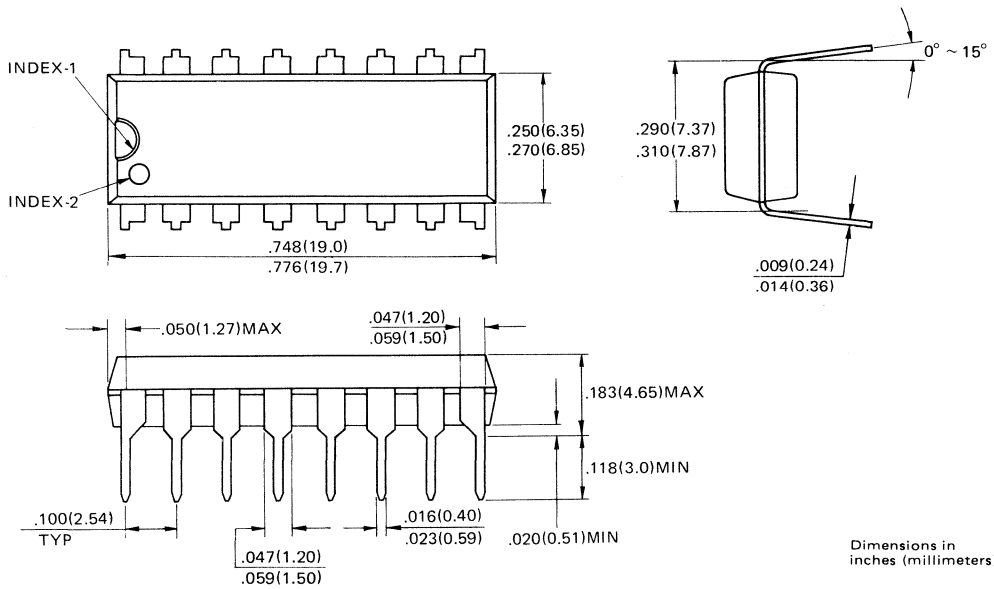
Standard 16-pin Ceramic DIP (Surfix : -Z)



PACKAGE DIMENSIONS

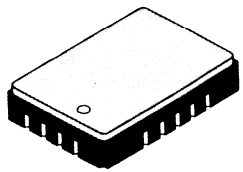
Standard 16-pin Plastic DIP (Surfix : -P)

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M03)

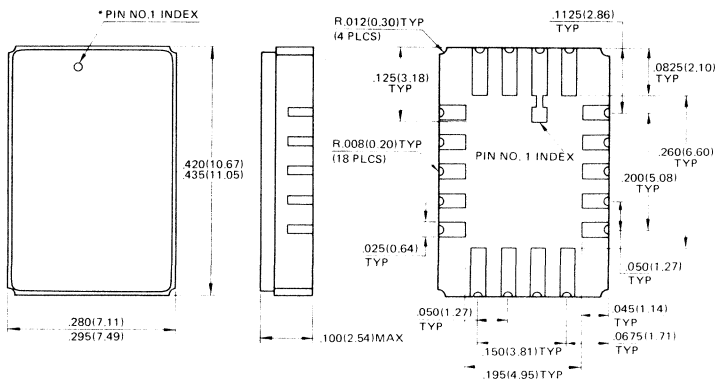


PACKAGE DIMENSIONS

Standard 18-pad Ceramic LCC (Surfix : -TV)



18-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-18C-F02)



*Shape of Pin 1 index: Subject to change without notice

Dimensions in inches
(millimeters)

FUJITSU

MOS 65536-BIT DYNAMIC RANDOM ACCESS MEMORY

MB 8266A-10
MB 8266A-12
MB 8266A-15

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

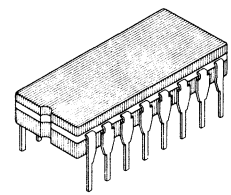
The Fujitsu MB 8266A is a fully decoded, dynamic random access memory organized as 65,536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MB 8266A to be housed in a standard 16 pin DIP and 18 pad LCC. Pin-outs conform to the JEDEC approved pin out. Additionally, the MB 8266A offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability that is acceptable upward to 256K dynamic RAMs, as pin 1 is left no-connect. The MB 8266A also features "Nibble Mode" which allows high speed serial access to up to 4 bits of data.

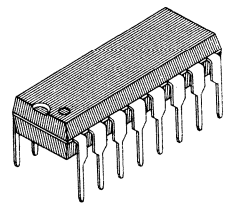
The MB 8266A is fabricated using silicon gate NMOS and Fujitsu's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimal chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are non-critical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

- 65,536 x 1 RAM, 16 pin DIP/18 pad LCC
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  100 ns max (MB 8266A-10)
  120 ns max (MB 8266A-12)
  150 ns max (MB 8266A-15)
- Cycle time,
  190 ns min (MB 8266A-10)
  230 ns min (MB 8266A-12)
  260 ns min (MB 8266A-15)
- Nibble cycle time,
  60 ns min (MB 8266A-10)
  70 ns min (MB 8266A-12)
  90 ns min (MB 8266A-15)
- Single +5V Supply, ±10% tolerance
- Low power (active)
  275 mW max (MB 8266A-10)
  248 mW max (MB 8266A-12)
  220 mW max (MB 8266A-15)
  25 mW standby (max)
- 2 ms/128 refresh cycles
- $\overline{CAS}$-before-$\overline{RAS}$, Hidden and $\overline{RAS}$-only refresh capability
- Common I/O capability using Early Write operation
- Output unlatched at cycle end allows two-dimensional chip
- Read-Modify-Write capability
- On-chip latches for Addresses and Data-in
- t_{AR}, t_{WCR}, t_{DHR} are eliminated
- Standard 16-pin Ceramic (Cerdip) DIP: Surfix-Z
  Standard 16-pin Plastic DIP: Surfix-P
  Standard 18-pad Ceramic LCC: Surfix-TV



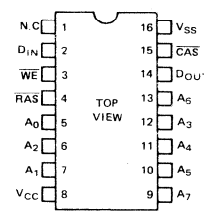
CERAMIC PACKAGE
DIP-16C-C04

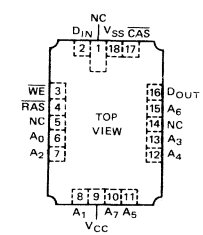


PLASTIC PACKAGE
DIP-16P-M03

LCC-18C-F02 : See Page 1-237

PIN ASSIGNMENT





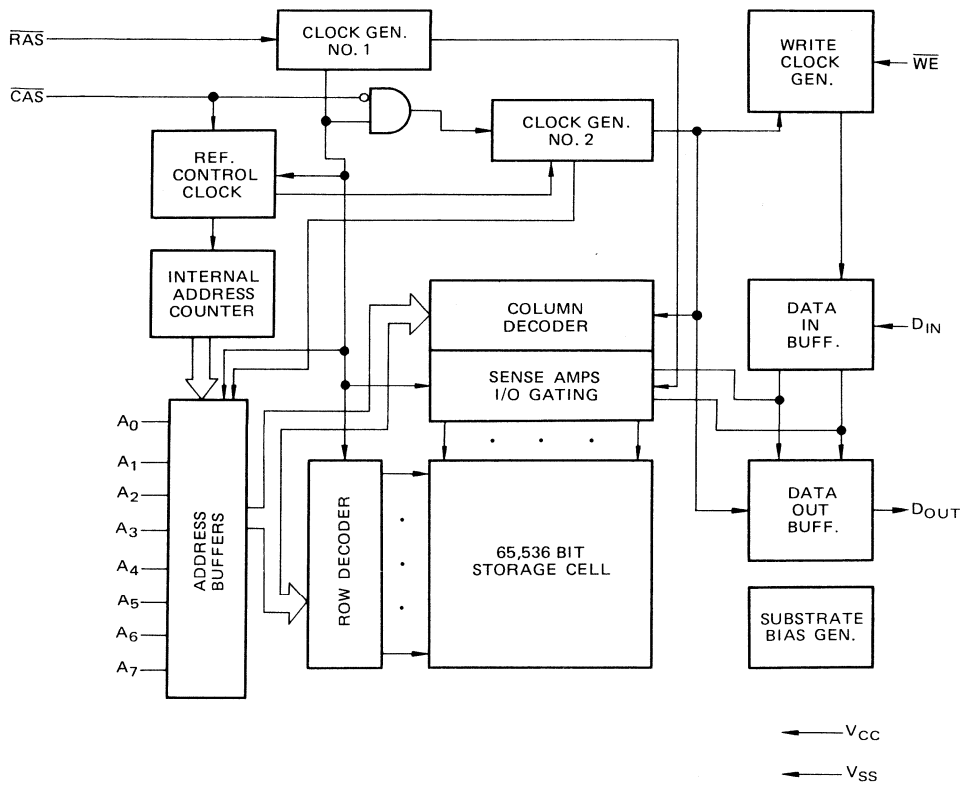
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}		V_{CC}	−1 to +7	V
Storage temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−55 to +125	
Power dissipation		P_D	1.0	W
Short circuit output current			50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 — MB 8266A BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance $A_0 \sim A_7$, D_{IN}	C_{IN1}		5	pF
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{IN2}		8	pF
Output Capacitance D_{OUT}	C_{OUT}		7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V	0°C to +70°C
Input High Voltage	V_{IH}	2.4		6.5	V	
Input Low Voltage	V_{IL}*	-1.0		0.8	V	

Note * : The device can withstand undershoots to the -2V level with a pulse width of 20 ns.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min)	MB 8266A-10	I_{CC1}		50	mA
	MB 8266A-12			45	
	MB 8266A-15			40	
STANDBY CURRENT Standby Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}		4.5	mA
REFRESH CURRENT 1* Average power supply current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ cycling; t_{RC} = min)	MB 8266A-10	I_{CC3}		38	mA
	MB 8266A-12			35	
	MB 8266A-15			31	
NIBBLE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{NC} = min)	MB 8266A-10	I_{CC4}		21	mA
	MB 8266A-12			21	
	MB 8266A-15			21	
REFRESH CURRENT 2* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$-before-$\overline{RAS}$)	MB 8266A-10	I_{CC5}		42	mA
	MB 8266A-12			38	
	MB 8266A-15			34	
INPUT LEAKAGE CURRENT Input leakage current, any input ($0 \leq V_{IN} \leq 5.5V$, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not test = 0 V)		$I_{I(L)}$	-10	10	μA
OUTPUT LEAKAGE CURRENT (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)		$I_{O(L)}$	-10	10	μA
OUTPUT LEVELS Output high voltage (I_{OH} = -5mA) Output low voltage (I_{OL} = 4.2mA)		V_{OH} V_{OL}	2.4	0.4	V

Note * : I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1,2,3

Parameter	NOTES	Symbol	MB 8266A-10		MB 8266A-12		MB 8266A-15		Unit
			Min	Max	Min	Max	Min	Max	
Time between Refresh		t_{REF}		2		2		2	ms
Random Read/Wire Cycle Time		t_{RC}	190		230		260		ns
Read-Write Cycle Time		t_{RWC}	230		265		280		ns
Access Time from $\overline{RAS}$	4 6	t_{RAC}		100		120		150	ns
Access Time from $\overline{CAS}$	5 6	t_{CAC}		50		60		75	ns
Output Buffer Turn Off Delay		t_{OFF}	0	30	0	35	0	40	ns
Transition Time		t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ Precharge Time		t_{RP}	90		100		100		ns
$\overline{RAS}$ Pulse Width		t_{RAS}	100	10000	120	10000	150	10000	ns
$\overline{RAS}$ Hold Time		t_{RSH}	50		60		75		ns
$\overline{CAS}$ Precharge Time		t_{CP}	40		50		60		ns
$\overline{CAS}$ Pulse Width		t_{CAS}	40	10000	60	10000	75	10000	ns
$\overline{CAS}$ Hold Time		t_{CSH}	100		120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	7 8	t_{RCD}	20	50	20	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ Set Up Time		t_{CRS}	30		30		30		ns
Row Address Set Up Time		t_{ASR}	0		0		0		ns
Row Address Hold Time		t_{RAH}	10		10		15		ns
Column Address Set Up Time		t_{ASC}	0		0		0		ns
Column Address Hold Time		t_{CAH}	15		15		20		ns
Read Command Set Up Time		t_{RCS}	0		0		0		ns
Read Command Hold Time Referenced To $\overline{CAS}$	10	t_{RCH}	0		0		0		ns
Read Command Hold Time Referenced To $\overline{RAS}$	10	t_{RRH}	20		20		20		ns
Write Command Set Up Time		t_{WCS}	0		0		0		ns
Write Command Hold Time		t_{WCH}	20		25		30		ns
Write Command Pulse Width		t_{WP}	20		25		30		ns
Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	35		40		45		ns
Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	35		40		45		ns
Data In Set Up Time		t_{DS}	0		0		0		ns
Data In Hold Time		t_{DH}	20		25		30		ns
$\overline{CAS}$ to $\overline{WE}$ Delay	9	t_{CWD}	40		50		60		ns
$\overline{RAS}$ to $\overline{WE}$ Delay	9	t_{RWD}	90		110		120		ns

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) NOTES 1,2,3

Parameter NOTES	Symbol	MB 8266A-10		MB 8266A-12		MB 8266A-15		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{CAS}$ Set Up Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)	t_{FCS}	20		25		30		ns
$\overline{CAS}$ Hold Time Referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)	t_{FCH}	20		25		30		ns
$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time (Refresh Cycles)	t_{RPC}	20		20		20		ns
Nibble Mode Read/Write Cycle Time	t_{NC}	60		70		90		ns
Nibble Mode Read-Write Cycle Time	t_{NRWC}	75		90		120		ns
Nibble Mode Access Time	t_{NCAC}		25		30		40	ns
Nibble Mode $\overline{CAS}$ Pulse Width	t_{NCAS}	25		30		40		ns
Nibble Mode $\overline{CAS}$ Precharge Time	t_{NCP}	25		30		40		ns
Nibble Mode Read $\overline{RAS}$ Hold Tim	t_{NRRSH}	25		30		40		ns
Nibble Mode Write $\overline{RAS}$ Hold Time	t_{NWRSH}	35		40		45		ns
Nipple Mode Write Command Set Up Tim	t_{NWCS}	0		0		0		ns
Nibble Mode Write Command to $\overline{CAS}$ Lead Time	t_{NCWL}	20		25		35		ns
Nibble Mode $\overline{CAS}$ to $\overline{WE}$ Delay	t_{NCWD}	15		20		30		ns
Refresh Counter Test Cycle Time 11	t_{RTC}	300		350		405		ns
Refresh Counter Test $\overline{RAS}$ Pulse Width 11	t_{TRAS}	200		240		295		ns

Notes:

1 An initial pause of 200 μs is required after power up. And then several cycles (to which any 8 cycles to perform refresh are adequate) are required before proper device operation is achieved.
If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

2 AC characteristics assume t_T = 5 ns.

3 V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max.).

4 Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

5 Assumes that $t_{RCD} \geq t_{RCD}$ (max).

6 Measured with a load equivalent to 2 TTL loads and 100 pF.

7 Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

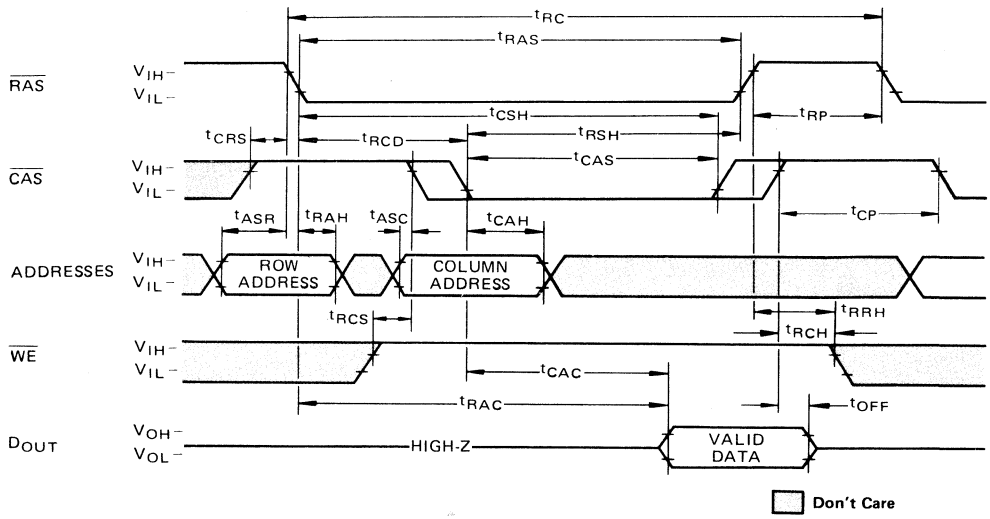
8 t_{RCD} (min) = t_{RAH} (min) + 2t_T (t_T=5ns) + t_{ASC} (min)

9 t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.
If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.

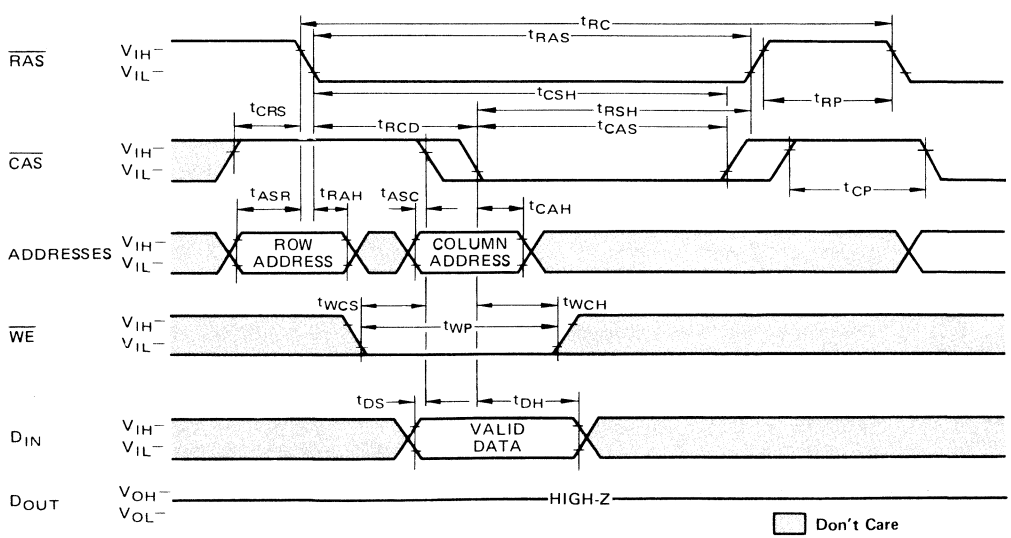
10 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

11 Refresh counter test cycle only.

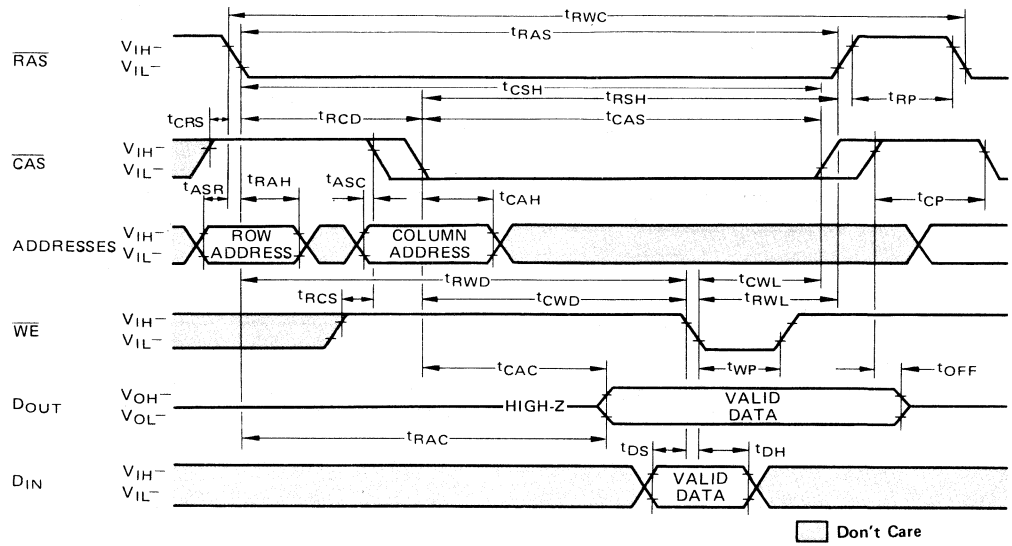
Read Cycle



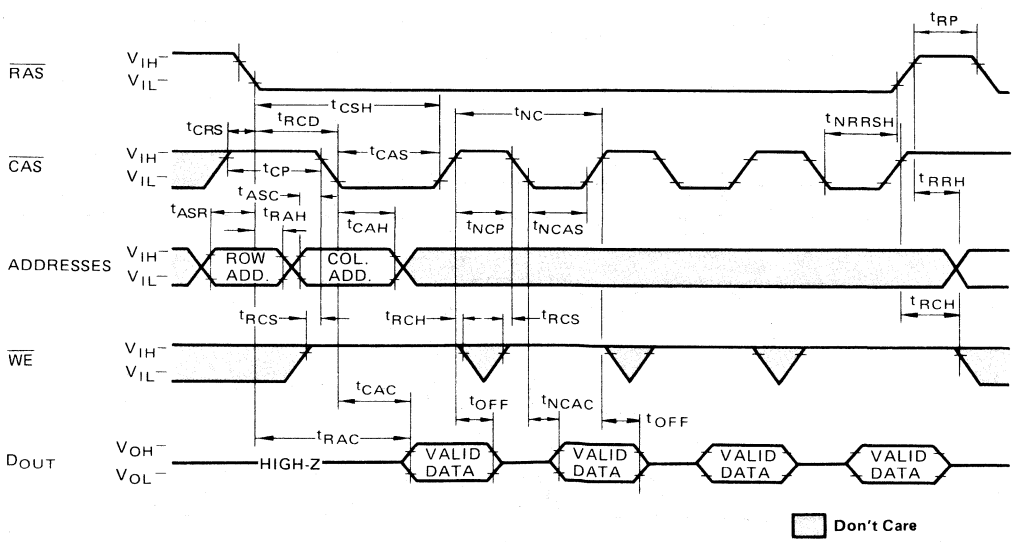
Write Cycle (Early Write)



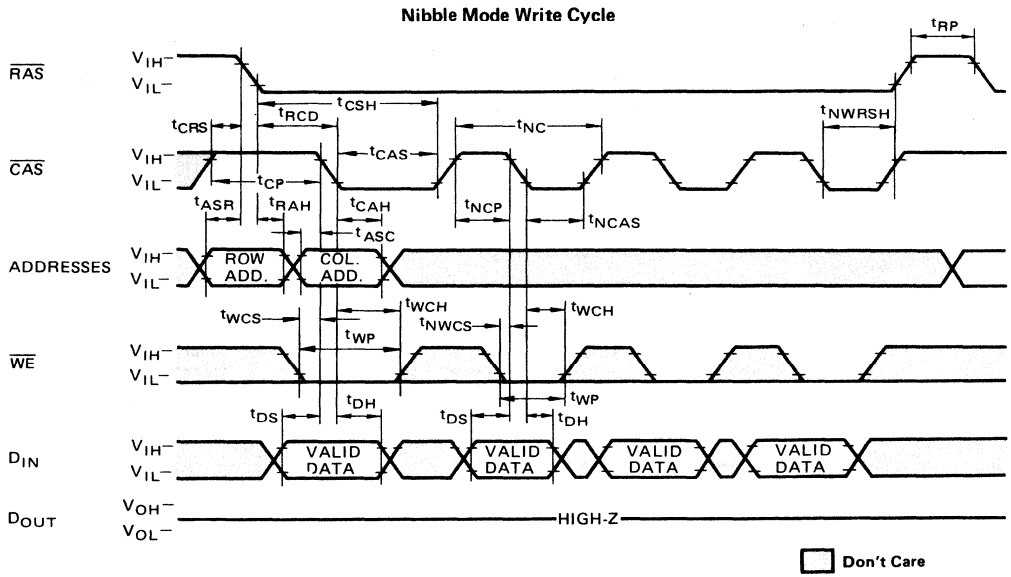
Read–Write/Read–Modify–Write Cycle



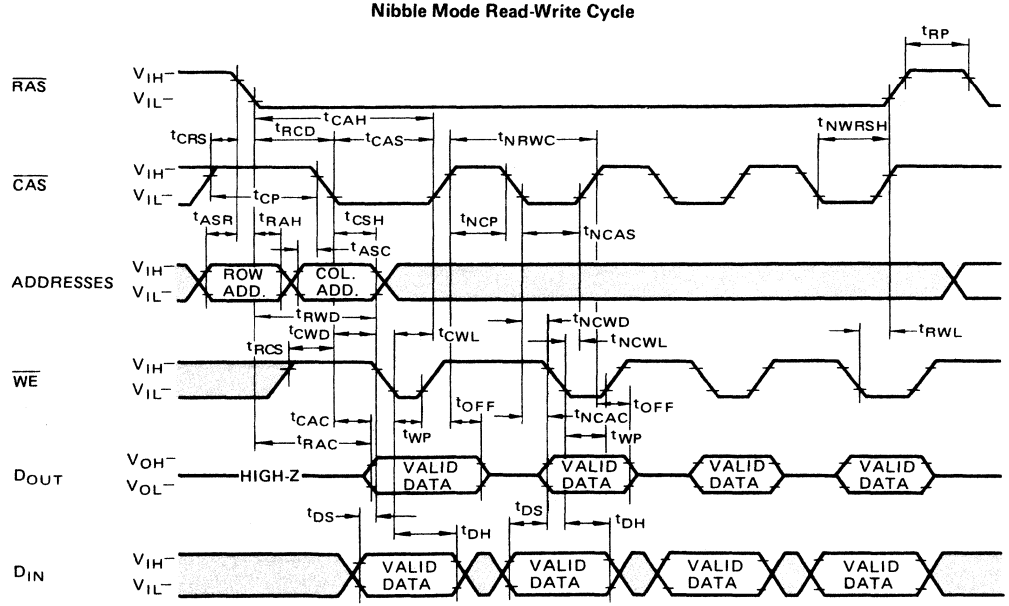
Nibble Mode Read Cycle



Nibble Mode Write Cycle

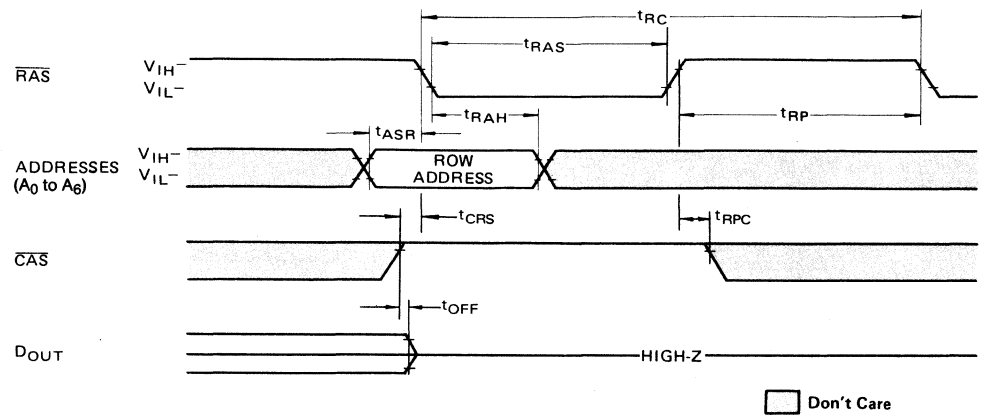


Nibble Mode Read-Write Cycle



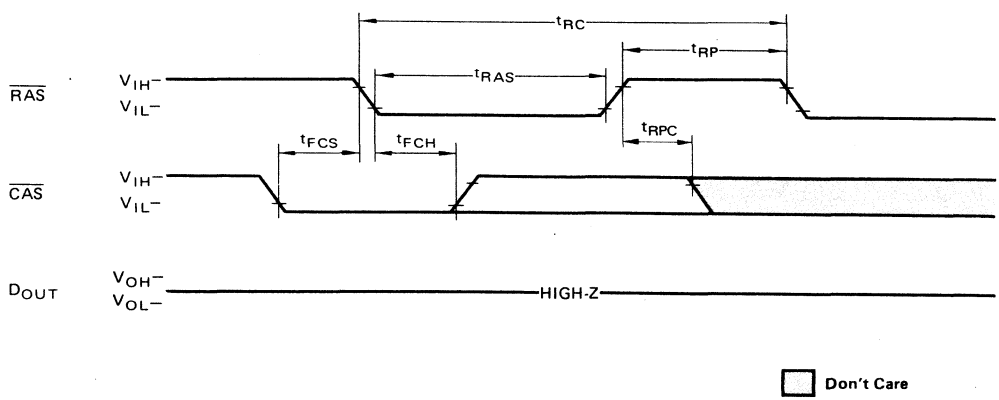
$\overline{RAS}$-only Refresh Cycle

Note: $\overline{WE}$, D_{IN} = Don't care, $A_7 = V_{IH}$ or V_{IL}

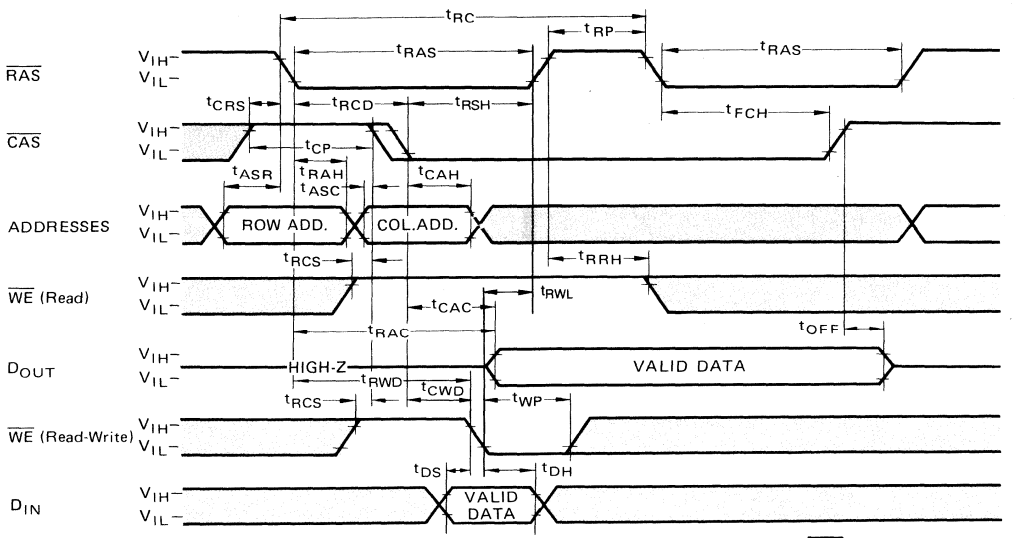


$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

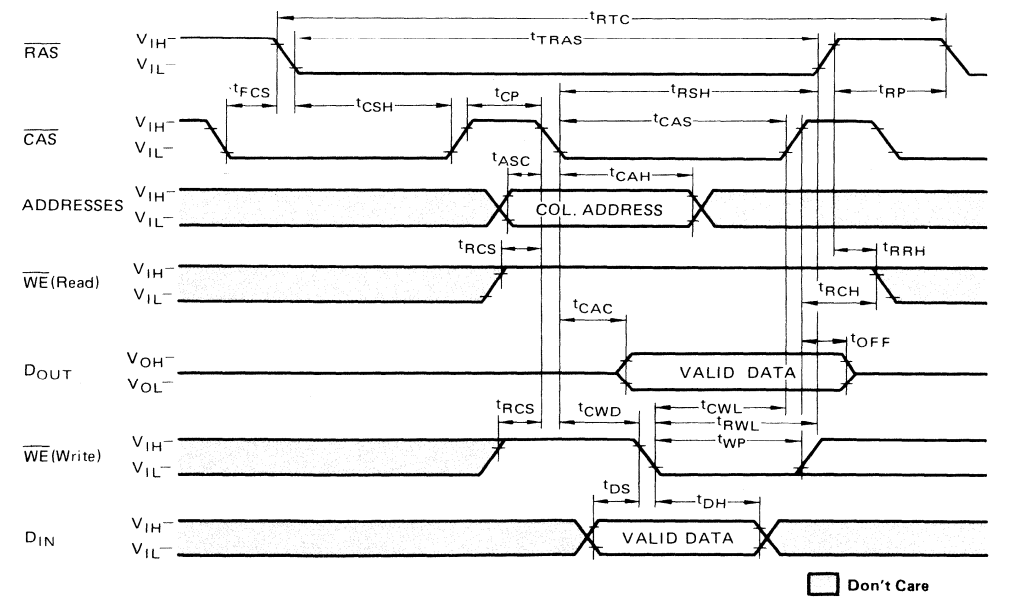
Note: Address, $\overline{WE}$, D_{IN} = Don't care



Hidden Refresh Cycle



CAS-before-RAS Refresh Counter Test Cycle



DESCRIPTION

Address Inputs:
A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MB 8266A. Eight row-address bits are established on the input pins (A_0 through A_7) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:
The read mode or write mode is selected with the $\overline{WE}$ input. A high on $\overline{WE}$ selectes read mode and low selectes write mode. Data input is disabled when read mode is selected.

Data Input:
Data is written into the MB 8266A during a write or read-write cycle. The later falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ can be low after $\overline{CAS}$ has been low and $\overline{CAS}$ to $\overline{WE}$ Delay Time (f_{CWD}) has been satisfied. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:
The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from the falling edge of $\overline{CAS}$ when the transistion occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Nibble Mode:
Nibble mode allows high speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 row addresses and the 6 column addresses. The 2 bits of column addresses (A_3, A_6) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by normal mode, the remaining nibble bits may be accessed by toggling $\overline{CAS}$ high then low while $\overline{RAS}$ remains low. Toggling $\overline{CAS}$ causes A_6 and A_3 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. (See Table 1).
If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent accesses. If the write operation is executed again on subsequent access, the new data will be written into the selected cell location. Using Fujitsu's nibble mode along with shift registers allows some interesting application possibilities. For instance it is possible to use an MB 8266A and a 4-bit universal shift register as a 16K x 4 dynamic RAM. This approach provides 16K granularity with the density and cost savings of 64K DRAMs. Refer to the Fig. 2 for example of 16K x 4 DRAM with MB 8266A.
Another application is to use Fujitsu's MB 8266As to generate a high speed serial bit stream for video display systems. In the example shown in Fig. 3 the eight MB 8266As are operating in nibble mode with each successive byte of data loaded into its appropriate shift register. The shift registers are then unloaded serially to form a data stream with rates for this example as fast as 12ns per bit. Only 220ns are required to load the four registers. While the 32 bits are being unloaded the MB 8266As are available to the system for other functions.

Refresh:
Refresh of the dynamic memory alls is accomplished by performing a memory cycle at each of the 128 row addresses ($A_0 \sim A_6$) at least every two milliseconds. The MB 8266A offers the following 3 types of refresh.

$\overline{RAS}$-only Refresh:
$\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation. During $\overline{RAS}$ only refresh cycle, either V_{IL} or V_{IH} is permitted to A_7.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh:
$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB 8266A offers an alternate refresh method. If $\overline{CAS}$ is held low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. The $\overline{CAS}$-before-$\overline{RAS}$ refresh mode eliminates the need to provide refresh address inputs.

Hidden Refresh:
Hidden refresh cycle may takes place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. In MB 8266A, hidden refresh means $\overline{CAS}$-before-$\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle:
A special timing sequence using $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. After the $\overline{CAS}$-

before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. A memory cell address (consisting of a row address (8 bits) and a column address (8 bits)) to be accessed, can be defined as follows:

*A ROW ADDRESS – Bits A_0 through A_6 are defined by the refresh counter. The other bit A_7 is set low internally.

*A COLUMN ADDRESS – All the bits A_0 through A_7 are defined by latching levels on A_0 through A_7 at the second falling edge of $\overline{CAS}$.

SUGGESTED $\overline{CAS}$-before-$\overline{RAS}$ REFRESH COUNTER TEST PROCEDURE

The timing, as shown in $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle, is used for all the operations described as follows:

(1) Initialize the internal refresh counter. For this operation, 8 cycles are required.

(2) Write a test pattern of lows into memory cells at a single column address and 128 row addresses.

(3) By using read-modify-write cycle, read the low written at the last operation (Step (2)) and write a new high in the same cycle. This cycle is repeated 128 times, and highs are written into the 128 memory cells.

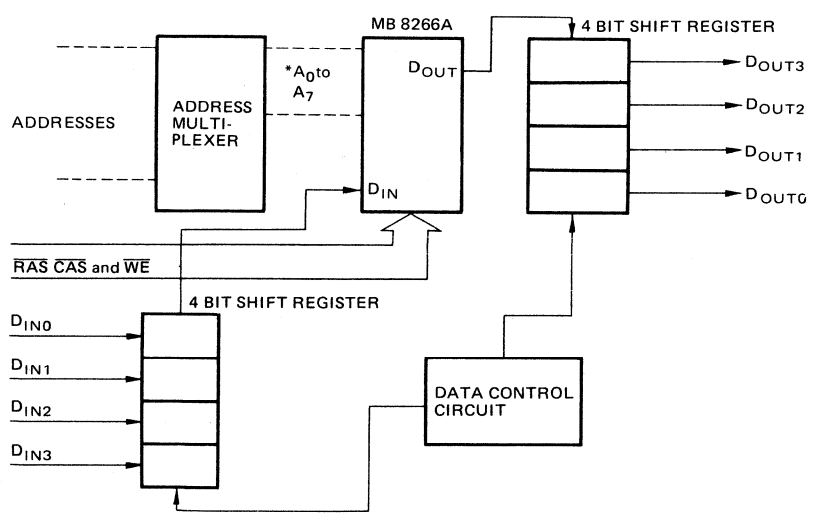
(4) Read the highs written at the last operation (Step (3)).

(5) Compliment the test pattern and repeat the steps (2), (3) and (4).

Table 1 – NIBBLE MODE ADDRESS SEQUENCE EXAMPLE

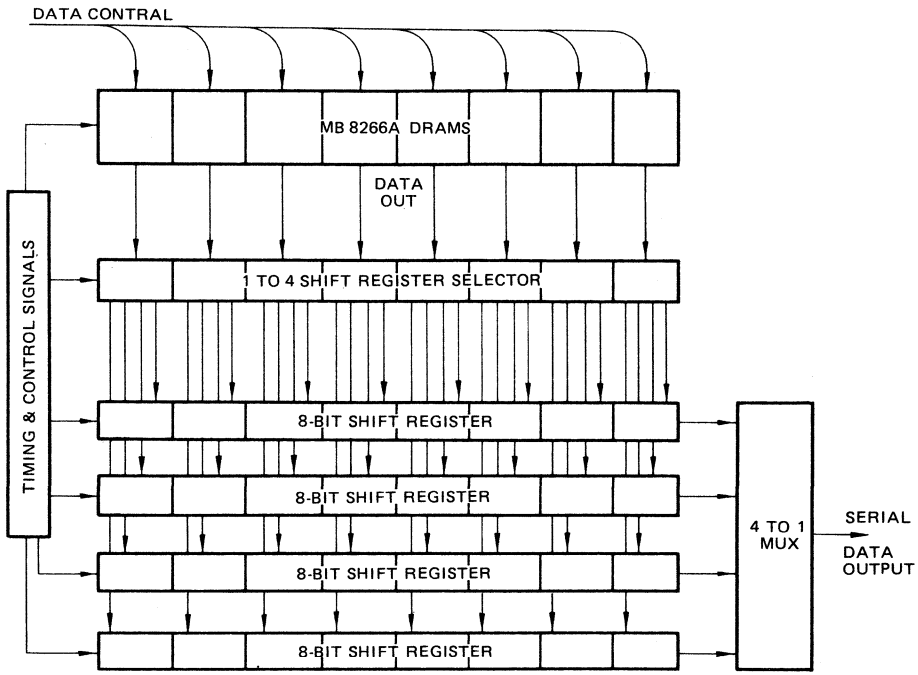
SEQUENCE	NIBBLE BIT	ROW ADDRESS	COLUMN ADDRESS			
				A_3	A_6	
$\overline{RAS}/\overline{CAS}$ (normal mode)	1	10101010	101010	1	0	input addresses
toggle $\overline{CAS}$ (nibble mode)	2	10101010	101010	1	1	generated internally
toggle $\overline{CAS}$ (nibble mode)	3	10101010	101010	0	0	generated internally
toggle $\overline{CAS}$ (nibble mode)	4	10101010	101010	0	1	generated internally
toggle $\overline{CAS}$ (nibble mode)	1	10101010	101010	1	0	sequence repeats

Fig. 2 – EXAMPLE OF 16K x 4 DRAM WITH MB 8266A



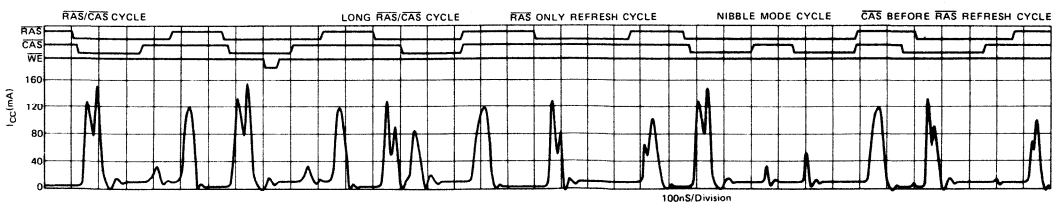
* The column address inputs for A_3 and A_6 should be Low because these addresses are used for nibble address.

Fig. 3 — VIDEO DISPLAY SYSTEM EXAMPLE



MB 8266A's operating in nibble mode provide a high speed serial output for video display system.

Fig. 4 — CURRENT WAVE FORM (V_{CC} = 5.5V, T_A = 25°C)



TYPICAL CHARACTERISTICS CURVES

Fig. 5 — NORMALIZED ACCESS TIME vs SUPPLY VOLTAGE

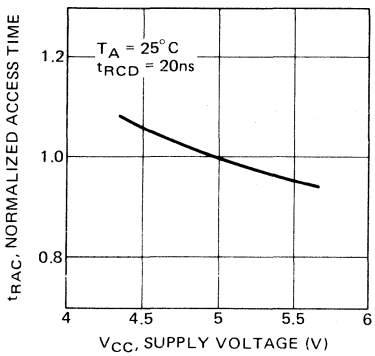


Fig. 6 — NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

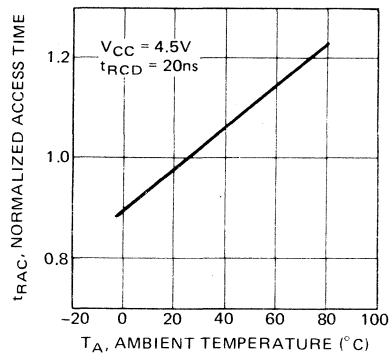


Fig. 7 — NORMALIZED NIBBLE ACCESS TIME vs SUPPLY VOLTAGE

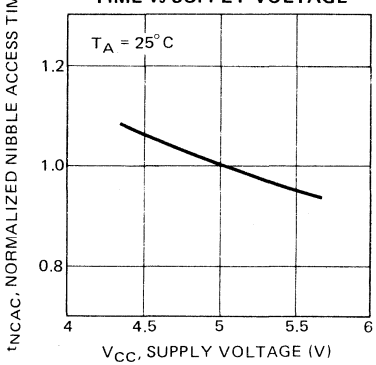


Fig. 8 — NORMALIZED NIBBLE ACCESS TIME vs AMBIENT TEMPERATURE

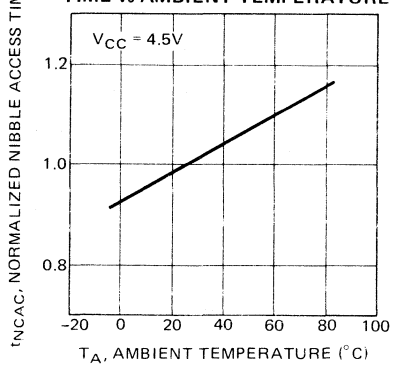


Fig. 9 — OPERATING CURRENT vs CYCLE RATE

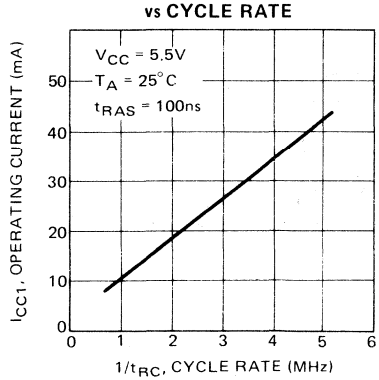


Fig. 10 — OPERATING CURRENT vs SUPPLY VOLTAGE

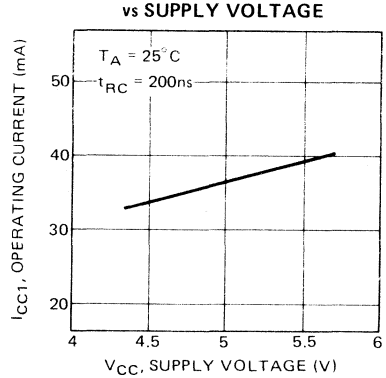


Fig. 11 — OPERATING CURRENT vs AMBIENT TEMPERATURE

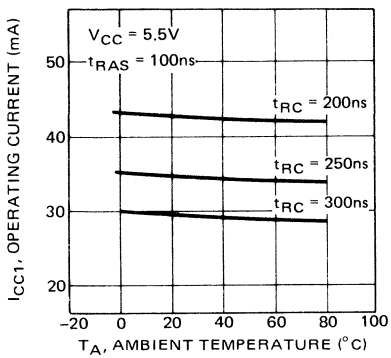


Fig. 12 — STANDBY CURRENT vs SUPPLY VOLTAGE

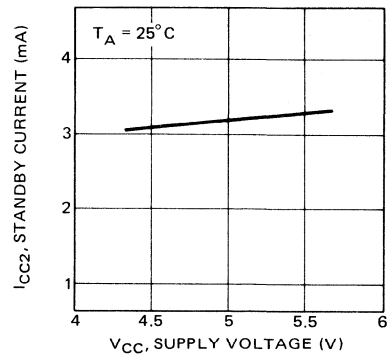


Fig. 13 — STANDBY CURRENT vs AMBIENT TEMPERATURE

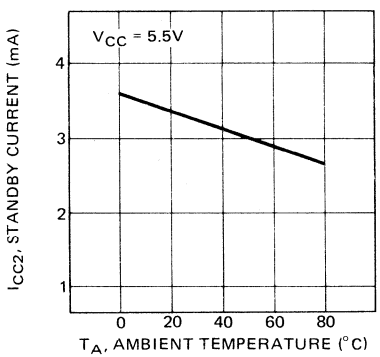


Fig. 14 — REFRESH CURRENT 1 vs CYCLE RATE

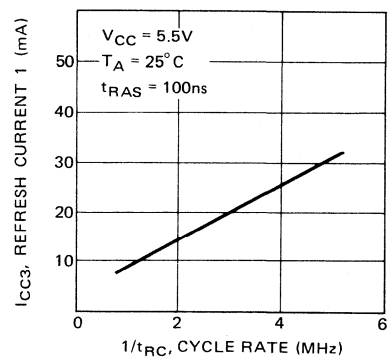


Fig. 15 — REFRESH CURRENT 1 vs SUPPLY VOLTAGE

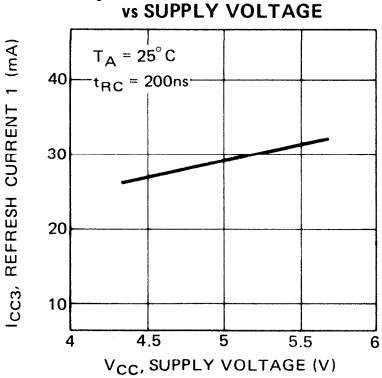


Fig. 16 — REFRESH CURRENT 1 vs AMBIENT TEMPERATURE

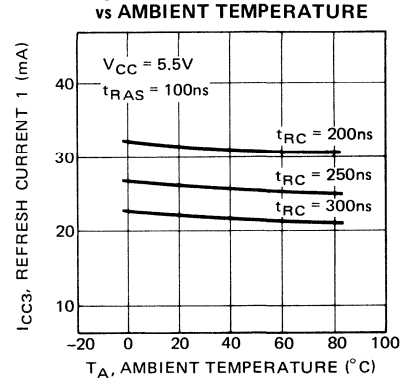


Fig. 15 – NIBBLE MODE CURRENT vs CYCLE RATE

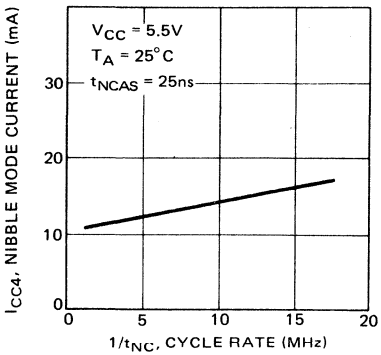


Fig. 16 – NIBBLE MODE CURRENT vs SUPPLY CURRENT

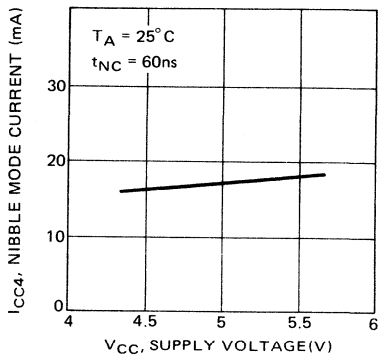


Fig. 17 – NIBBLE MODE CURRENT vs AMBIENT TEMPERATURE

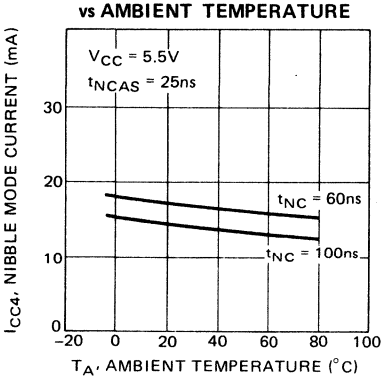


Fig. 18 – REFRESH CURRENT 2 vs CYCLE RATE

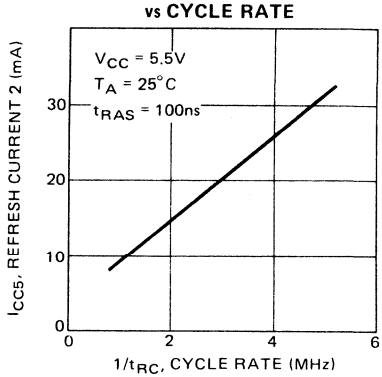


Fig. 19 – REFRESH CURRENT 2 vs SUPPLY VOLTAGE

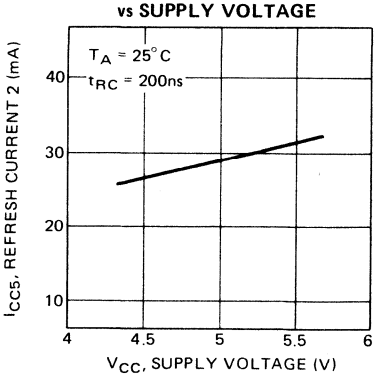


Fig. 20 – REFRESH CURRENT 2 vs AMBIENT TEMPERATURE

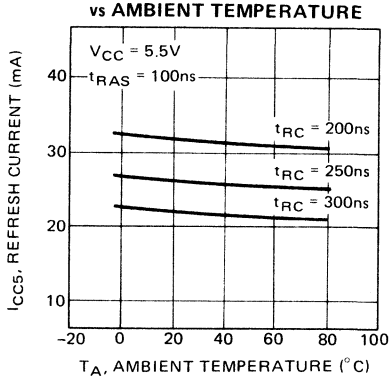


Fig. 21 — ADDRESS AND DATA INPUT VOLTAGE vs SUPPLY VOLTAGE

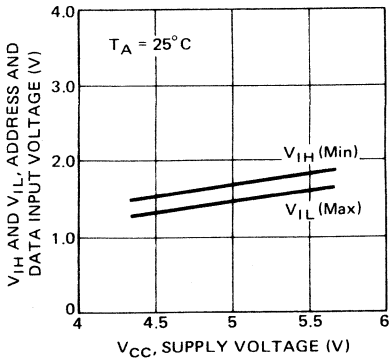


Fig. 22 — ADDRESS AND DATA INPUT VOLTAGE vs AMBIENT TEMPERATURE

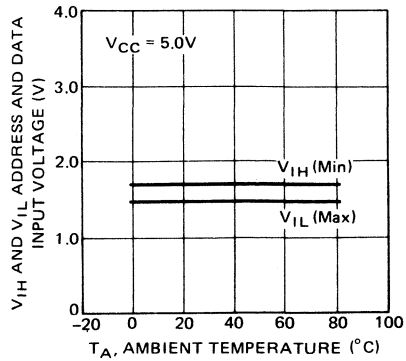


Fig. 23 — $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ INPUT VOLTAGE vs SUPPLY VOLTAGE

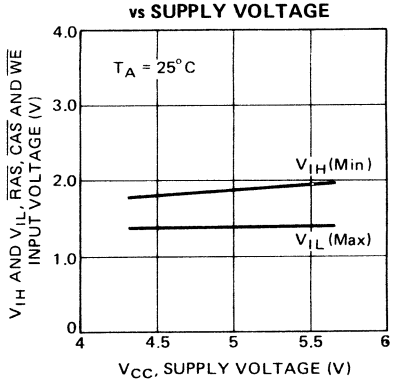


Fig. 24 — $\overline{RAS}$, $\overline{CAS}$ AND $\overline{WE}$ VOLTAGE vs AMBIENT TEMPERATURE

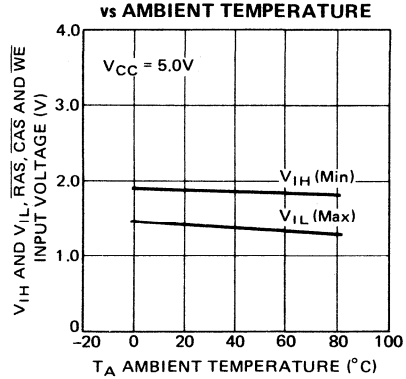


Fig. 27 — CURRENT WAVE FORM DURING POWER UP

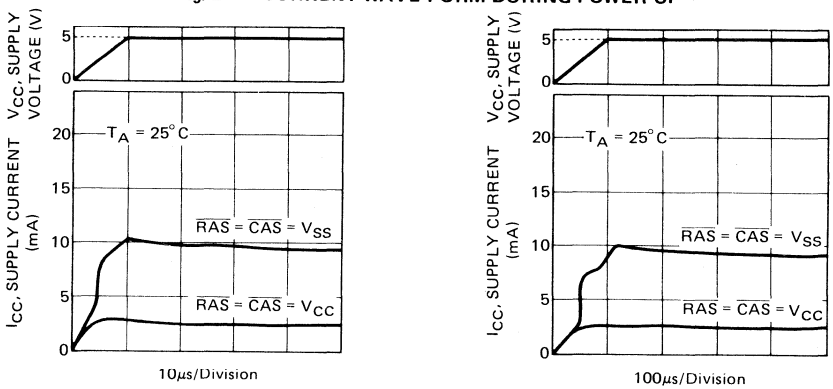


Fig. 28 — CURRENT WAVE FORM DURING POWER UP (ON MEMORY BOARD)

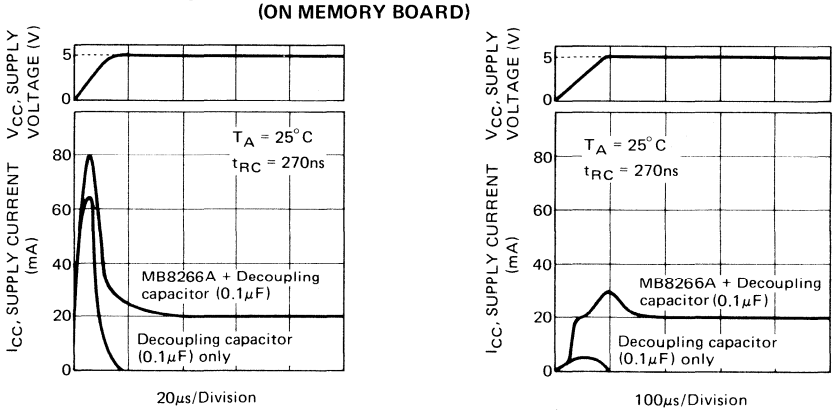
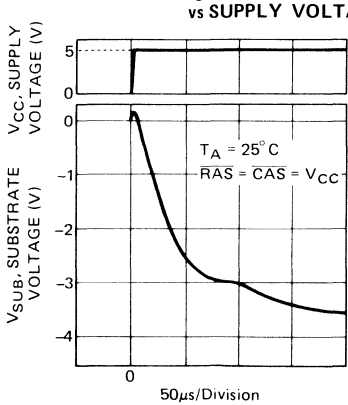
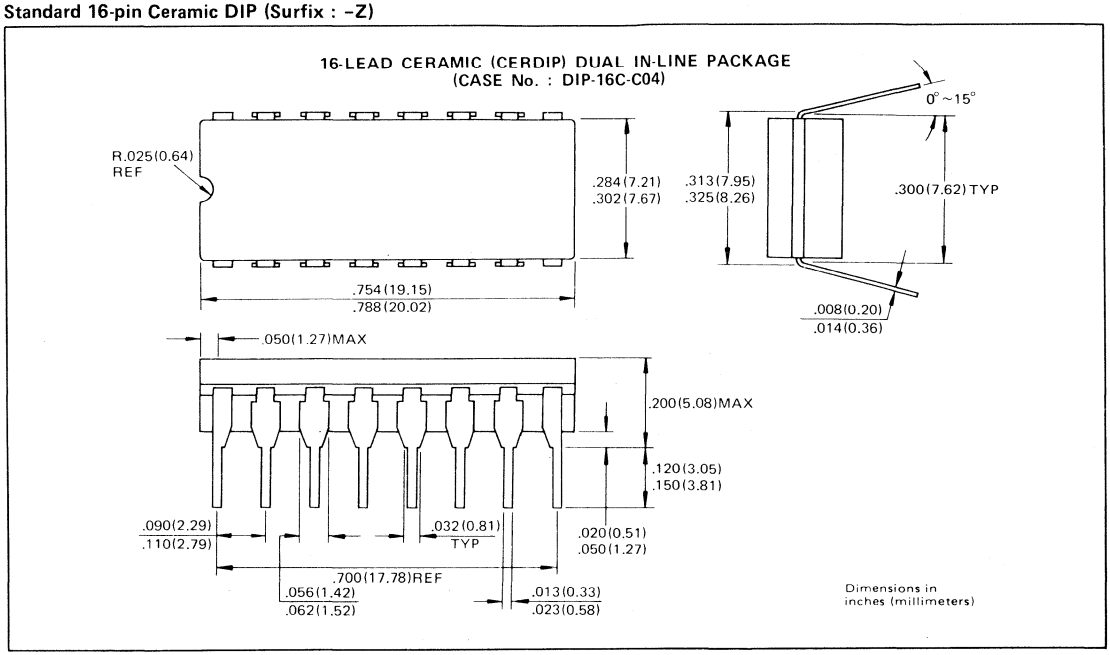


Fig. 29 — SUBSTRATE VOLTATE vs SUPPLY VOLTAGE (DURING POWER UP)

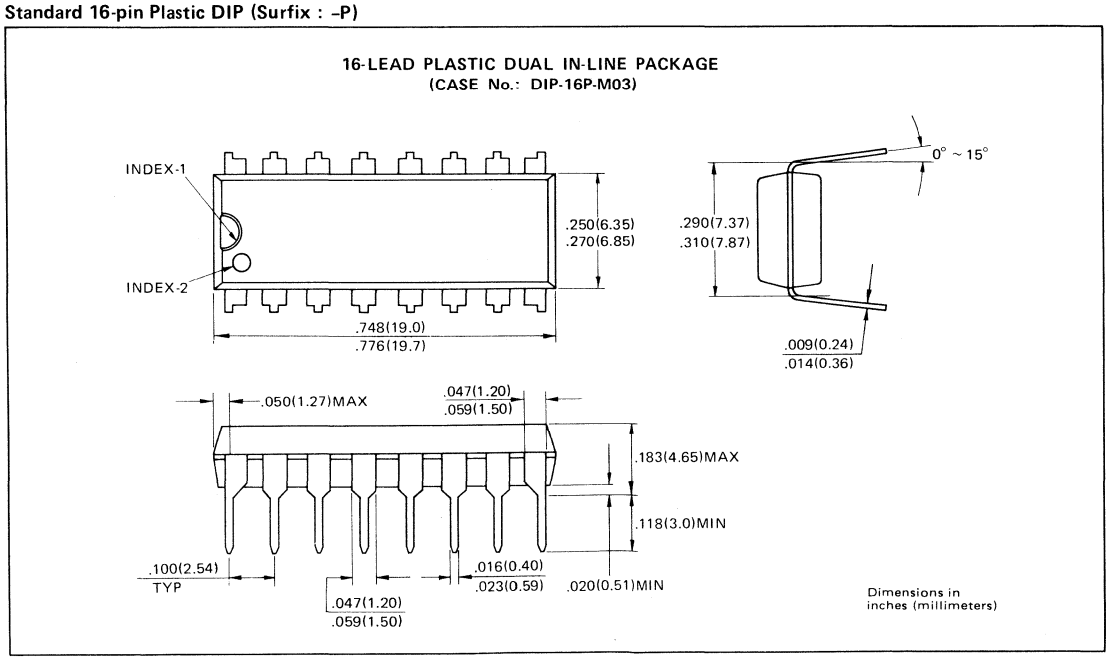


PACKAGE DIMENSIONS

Standard 16-pin Ceramic DIP (Surfix : -Z)

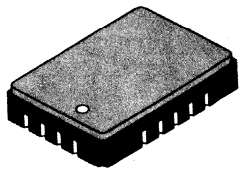


Standard 16-pin Plastic DIP (Surfix : -P)

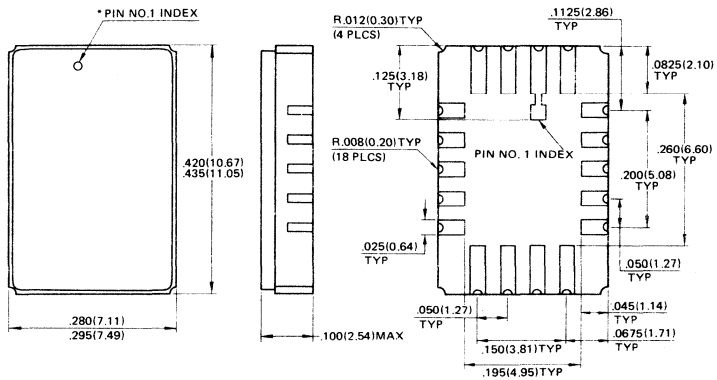


PACKAGE DIMENSIONS

Standard 18-pad Ceramic LCC (Surfix : -TV)



18-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-18C-F02)



*Shape of Pin 1 index: Subject to change without notice

Dimensions in inches
(millimeters)

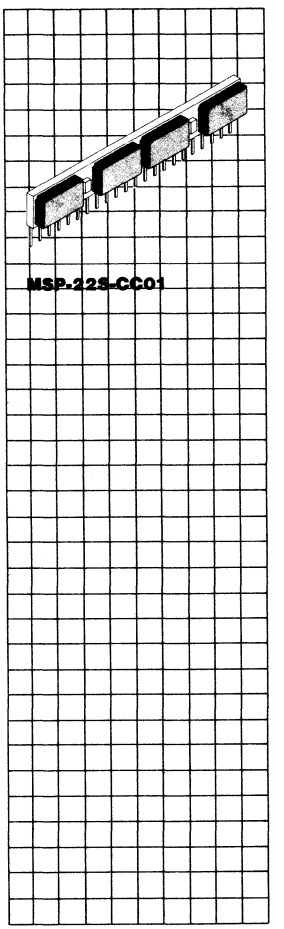
FUJITSU

MB85101A-10, MB85101A-12, MB85101A-15
MOS 65,536 x 4-Bit Dynamic RAM Module

Description

The Fujitsu MB85101A is a 64K x 4 dynamic RAM high density memory module. It consists of four MB8264A DRAMs in 18-pad LCC packages mounted on a 22-pin multilayer ceramic substrate.

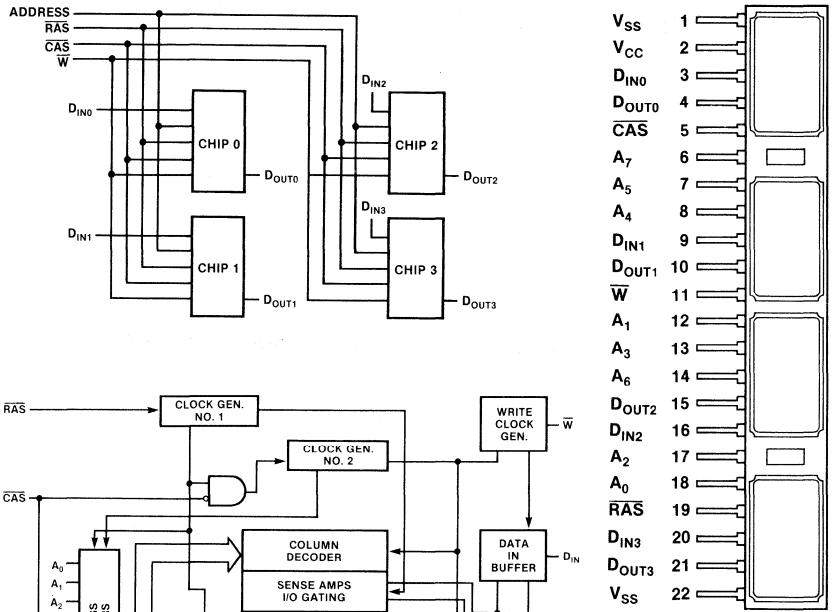
The MB85101A is intended for use in memory applications in which large amounts of memory are required in a compact space or in which board space is limited. Significant size reduction can be realized in applications such as mainframe memory, buffer memory, desktop computers and peripheral storage.



Features

- 65,536 x 4-bit DRAM module
- Row Access Time
  - 100 ns max. (MB85101A-10)
  - 120 ns max. (MB85101A-12)
  - 150 ns max. (MB85101A-15)
- Cycle Time
  - 200 ns min. (MB85101A-10)
  - 230 ns min. (MB85101A-12)
  - 260 ns min. (MB85101A-15)
- Single +5 V supply, ±10% tolerance
- Low power (active)
  - 1100 mW max. (MB85101A-10)
  - 990 mW max. (MB85101A-12)
  - 880 mW max. (MB85101A-15)
  - 88 mW max. (standby)
- 2 ms/128 cycle refresh
- $\overline{RAS}$-only and Hidden refresh capability
- Read-Modify-Write and Page Mode capability
- Common I/O capability using Early Write operation
- Output unlatched at cycle end allows extended page boundary and two dimentional chip selects.
- On-chip latches for Addresses and Data-in

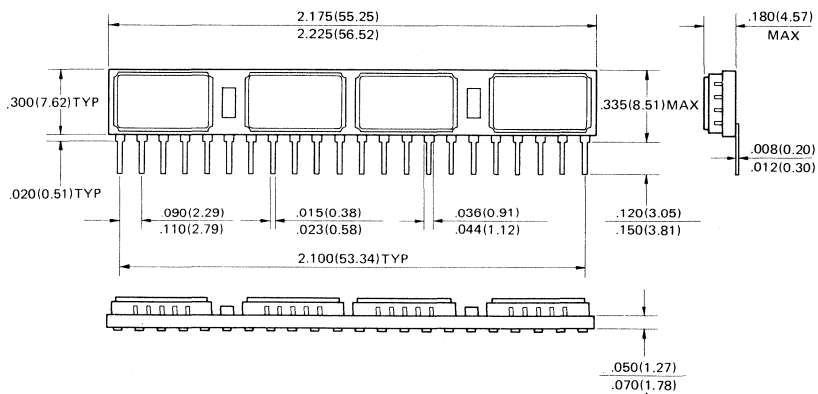
MB85101 Block Diagram and Pin Assignment



Block Diagram for Each Chip

Package Dimensions
Dimensions in inches (millimeters)

22-Lead Single In-Line Package
(Module MSP-22S-CC01)



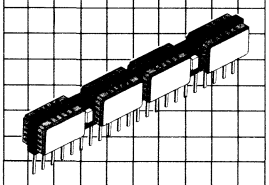
FUJITSU

MB85103A-12, MB85103A-15
MOS 65,536 x 8-Bit Dynamic RAM Module

Description

The Fujitsu MB85103A is a 64K x 8 dynamic RAM high density memory module. It consists of eight MB8264A DRAMs in 18-pad LCC packages mounted on a 22-pin multilayer ceramic substrate.

The MB85103A is intended for use in memory applications in which large amounts of memory are required in a compact space or in which board space is limited. Significant size reduction can be realized in applications such as mainframe memory, buffer memory, desktop computers and peripheral storage.

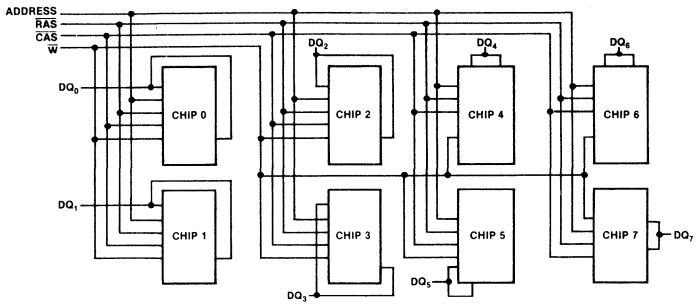


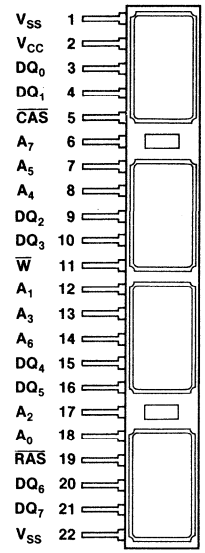
MSP-22S-CC02

Features

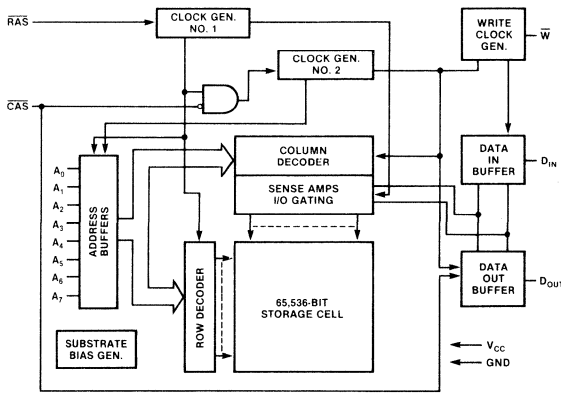
- 65,536 x 8-bit DRAM module
- Row Access Time
  - 120 ns max. (MB85103A-12)
  - 150 ns max. (MB85103A-15)
- Cycle Time
  - 230 ns min. (MB85103A-12)
  - 260 ns min. (MB85103A-15)
- Single +5 V supply, ±10% tolerance
- Low power (active)
  - 1980 mW max. (MB85103A-12)
  - 1760 mW max. (MB85103A-15)
  - 176 mW max. (standby)
- 2 ms/128 cycle refresh
- $\overline{\text{RAS}}$-only and Hidden refresh capability
- Page Mode capability
- Common I/O
- Output unlatched at cycle end allows extended page boundary and two dimentional chip selects.
- On-chip latches for Addresses and Data-in

MB85103 Block Diagram and Pin Assignment





Block Diagram for Each Chip

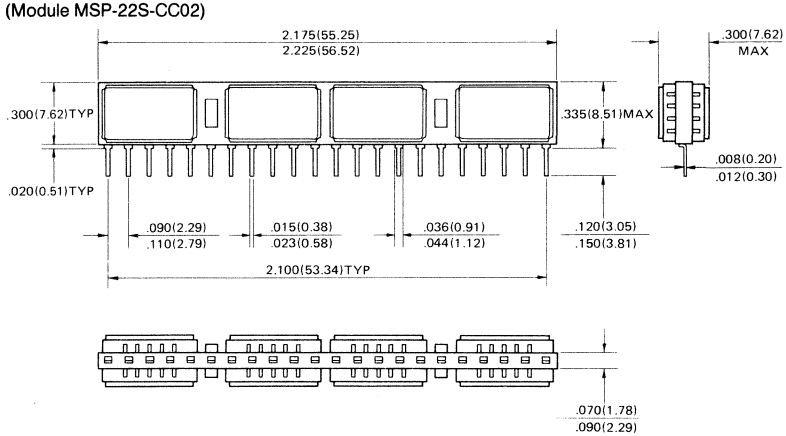


Package Dimensions

Dimensions in inches (millimeters)

22-Lead Single In-Line Package

(Module MSP-22S-CC02)



FUJITSU

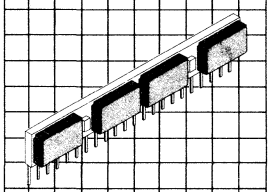
■ MB85108A-12, MB85108A-15
MOS 262,144 x 1-Bit Dynamic RAM Module

Description

The Fujitsu MB85108A is a 256K x 1 dynamic RAM high density memory module. It consists of four MB8266A DRAMs in 18-pad LCC packages mounted on a 22-pin multilayer ceramic substrate.

The MB85108A is intended for use in memory applications in which large amounts of memory are required in a compact space or in which board space is limited. Significant size reduction can be realized in applications such as mainframe memory, buffer memory, desktop computers, and peripheral storage.

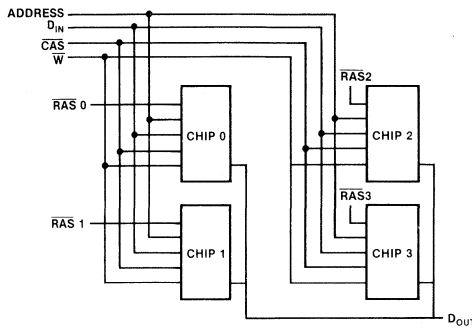
The MB85108A features two new functional enhancements that make it more versatile than previous dynamic RAM's. The $\overline{CAS}$-before-$\overline{RAS}$ refresh mode provides an on-chip refresh capability. The nibble mode function allows high speed serial access to up to 4 bits of data.

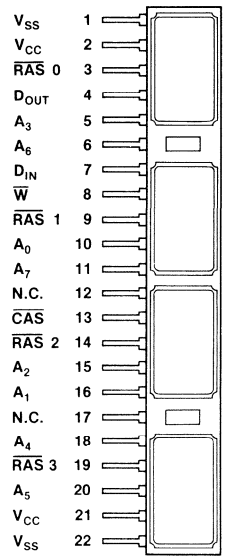


Features

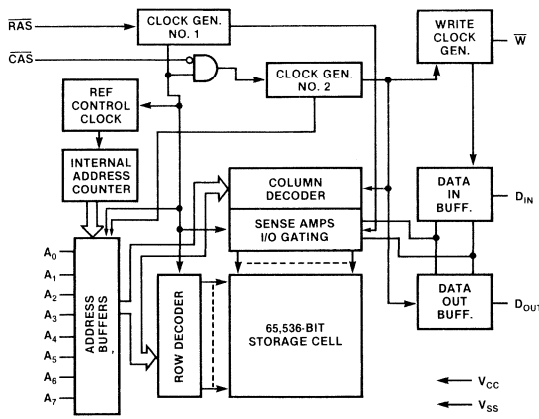
- 262,144 x 1-bit DRAM module
- Row Access Time
  120 ns max. (MB85108A-12)
  150 ns max. (MB85108A-15)
- Cycle Time
  230 ns min. (MB85108A-12)
  260 ns min. (MB85108A-15)
- Nibble Cycle Time
  70 ns min. (MB85108A-12)
  90 ns min. (MB85108A-15)
- Single +5 V supply, ±10% tolerance
- Low power (active)
  341 mW max. (MB85108A-12)
  303 mW max. (MB85108A-15)
  99 mW max. (standby)
- 2 ms/128 cycle refresh
- $\overline{RAS}$-only, Hidden and $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- Read-Modify-Write capability
- Nibble Mode capability
- Common I/O capability using Early Write
- On-chip Address and Data-in latches
- Output unlatched at cycle end allows extended page boundary and two dimentional chip selects.

MB85108 Block Diagram and Pin Assignment



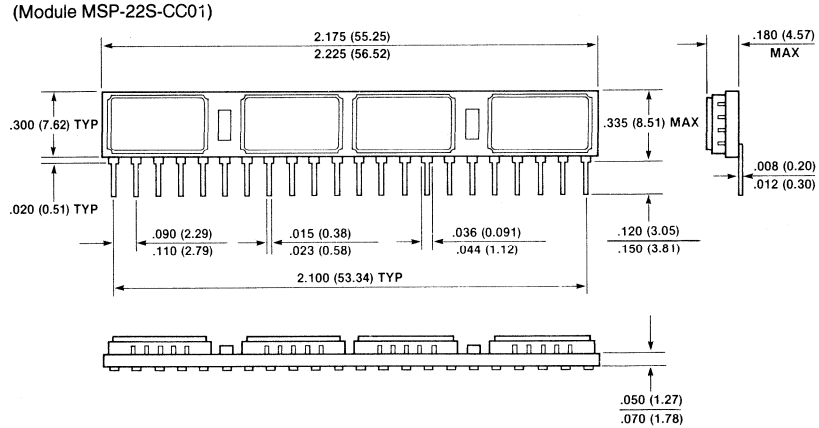


Block Diagram for Each Chip



Package Dimensions
Dimensions in inches
(millimeters)

22-Lead Single In-Line Package
(Module MSP-22S-CC01)



FUJITSU

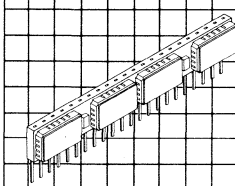
MB85201-12, MB85201-15

1,048,576 x 1-Bit Dynamic Random Access Memory SIP Module

Description

The Fujitsu MB85201 is a fully decoded, 1,048,576 word x 1-bit NMOS dynamic random access memory module consisting of four MB81256 DRAMs in 18-pad LCC packages mounted on a 22-pin multilayer ceramic substrate.

The MB85201 is intended for use in memory applications where large memory capacity is required within limited physical volume. Significant size reduction can be realized in applications such as mainframe memory, buffer memory, desk top computers and peripheral storage.



MSP-22S-CC04

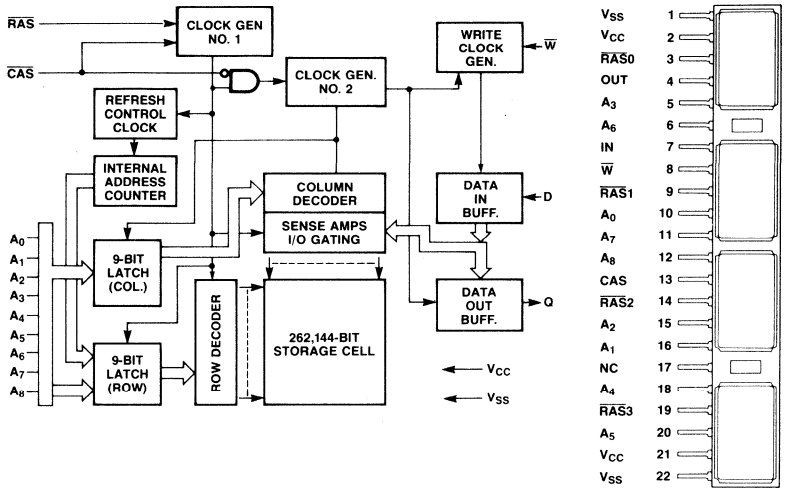
Features

- **1,048,576 x 1-Bit DRAM 22-pin SIP (MB81256x4)**
- **Row access time 120 ns max. (MB85201-12) 150 ns max. (MB85201-15)**
- **Cycle time 230 ns min. (MB85201-12) 260 ns min. (MB85201-15)**
- **Page cycle time 120 ns min. (MB85201-12) 150 ns min. (MB85201-15)**
- **Single + 5V supply, ±10% tolerance**
- **Low power (active) 435 mW max. (MB85201-12) 390 mW max. (MB85201-15) 100 mW max. (standby)**
- **4 ms/256 refresh cycles capability**
- **$\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$ and Hidden refresh capability**
- **Read-Modify-Write and Page Mode capability**
- **Common I/O capability using Early Write operation**
- **On-chip latches for Addresses and Data-in**
- **All inputs and outputs are TTL compatible**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB85201 Block Diagrams and Pin Assignment

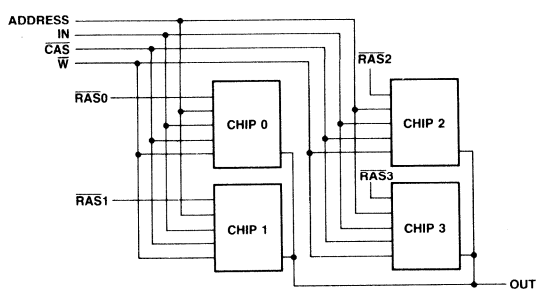
Block Diagram For Each Chip



FUNCTIONAL TRUTH TABLE FOR EACH CHIP

$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	IN	OUT	Read	Write	Refresh	Note
H	H	Don't Care	Don't Care	High-Z	No	No	No	Standby
L	L	H	Don't Care	Valid Data	Yes	No	Yes	Read
L	L	L	Valid Data	High-Z	No	Yes	Yes	Early Write $t_{WCS} \geq t_{WCS}$ (min)
L	L	L	Valid Data	Valid Data	Yes	Yes	Yes	Delayed Write or Read-Write $t_{CWD} \geq t_{CWD}$ (min)
L	H	Don't Care	Don't Care	High-Z	No	No	Yes	$\overline{RAS}$-only Refresh
L	L	Don't Care	Don't Care	Valid Data	No	No	Yes	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Valid data selected at previous Read or Read-Write cycle is held
H	L	Don't Care	Don't Care	High-Z	No	No	No	$\overline{CAS}$ disturb

Functional Block Diagram



MB85201 Block Diagrams and Pin Assignments
(Continued)

FUNCTIONAL TRUTH TABLE FOR MODULE

$\overline{RAS0}$ to $\overline{RAS3}$	$\overline{CAS}$	$\overline{W}$	IN	OUT	Function
H	H	Don't Care	Don't Care	High-Z	Standby
L*1	L	H	Don't Care	Valid Data	Read cycle
L*1	L	L	Valid Data	High-Z	Write cycle
L*1	L	H→L*2	Valid Data	Valid Data	Read-write cycle
H→L*3	H→L*3	Don't Care	Don't Care	High-Z	$\overline{CAS}$-before-$\overline{RAS}$ Refresh cycle
L	H	Don't Care	Don't Care	High-Z	$\overline{RAS}$-only Refresh cycle

NOTES: *1 For the selected $\overline{RAS}$, and the other $\overline{RAS}$ inputs are high.
*2 $t_{CWD} \geq t_{CWD}$ (min).
*3 $t_{FCS} \geq t_{FCS}$ (min).

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	2.4	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Description

Simple Timing Requirement

The MB85201 has improved circuitry that eases timing requirements for high speed access operations. The MB85201 can operate under the condition of t_{RCD} (max) = t_{CAC} thus providing optimal timing for address multiplexing. In addition, the MB85201 has the minimal hold times of address (t_{CAH}), $\overline{W}$ (t_{WCH}) and IN (t_{DH}). Fujitsu has made timing requirements that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the column address, IN and $\overline{W}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{W}$ Delay) are not restricted by t_{RCD}.

Address Inputs

A total of eighteen binary input address bits are required to decode any one of 1,048,576 locations within the MB85201. Nine row address bits are established on the input pins (A_0 through A_8) and latched with the $\overline{RAS}$ (one of $\overline{RAS0}$ to $\overline{RAS3}$) of the selected chip. Nine column address bits are established on the input pins and latched with $\overline{CAS}$. All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

$\overline{RAS0}$ to $\overline{RAS3}$

The MB85201 has four $\overline{RAS}$ inputs in order to select a chip within the MB85201. Other $\overline{RAS}$s except for one $\overline{RAS}$ to be selected must be high in order to avoid data conflict during read, delayed write or read-write cycles.

Write Enable

The read mode or write mode is selected with the $\overline{W}$ input. A high on the $\overline{W}$ selects read mode, a low selects write mode. Data input is disabled when read mode is selected.

Description
(Continued)

Data Input

Data is written into the chip selected by $\overline{RAS}$ (one of $\overline{RAS0}$ to $\overline{RAS3}$) of MB85201 during a write or read-write cycle. The later falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the IN register. In a write cycle, if $\overline{W}$ is brought low before the falling edge of $\overline{CAS}$, the set-up and hold times are referenced to $\overline{CAS}$. In a delayed write or read-write cycle, $\overline{W}$ can be low after $\overline{CAS}$ has already been low and $\overline{CAS}$ to $\overline{W}$ Delay time (t_{CWD}) has been satisfied (read-write cycle). Thus IN is strobed by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$.

Data Output

The output buffer of each chip is three-state TTL compatible with a fan-out of two standard TTL loads. OUT is the same polarity as IN. The output is in high impedance state until $\overline{CAS}$ is brought low. In a read or read-write cycle, the output is valid after t_{RAC} from negative transition of the $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from negative transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to a high level. In a write cycle, the identical sequence occurs but data is not valid.

Fast Read-While-Write Cycle

The MB85201 has a fast read-while-write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{W}$ when $\overline{CAS}$ goes low. When $\overline{W}$ is low during $\overline{CAS}$ transition to low, the MB85201 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. Whereas, when $\overline{W}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MB85201 goes into the delayed write mode. The output then contains the data from the cell selected and the data from IN are written into the cell selected. Therefore, a very fast read write cycle ($t_{RC} = t_{RWC}$) is possible with the MB85201.

Page-Mode

Page-mode operation permits strobing the row-address into the MB85201 while maintaining $\overline{RAS}$ (one of $\overline{RAS0}$ to $\overline{RAS3}$) at a logic low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row address (A_0 through A_7) for each chip at least every 4 ms. During refresh, either V_{IL} or V_{IH} is permitted for A_8 and any combinations of $\overline{RAS0}$ to $\overline{RAS3}$ are allowed. When all chips are refreshed simultaneously, the average power dissipation of the module must be less than 640 mW at any 100 ms interval.
The MB85201 offers the following three types of refresh.

1) $\overline{RAS}$-Only Refresh;
   $\overline{RAS}$ Only refresh avoids any output during refresh because the output buffer is in high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 row addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed.
2) $\overline{CAS}$-before-$\overline{RAS}$ Refresh;
   $\overline{CAS}$-before-$\overline{RAS}$ refresh available on the MB85201 offers an alternate refresh method. If $\overline{CAS}$ is held low for the specified period, $\overline{CAS}$ Set Up Time Referenced to $\overline{RAS}$ (t_{FCS})has been satisfied before the falling edge of $\overline{RAS}$, on chip refresh control clock generators and the refresh address counter for each chip are enabled, and an internal refresh operation takes place. After the refresh operation has been executed the refresh address counter is automatically incremented for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.
3) Hidden Refresh;
   Hidden refresh may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. In the MB85201, hidden refresh means $\overline{CAS}$-before-$\overline{RAS}$ refresh and the internal refresh address is used, that is, no external refresh address is needed.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes into high and goes into low again while $\overline{RAS}$ is held low, the read and write operation are enabled. This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell address (consisting of a row address (9-bits) and a column address (9-bits)) to be accessed, can be defined as follows:

1) A ROW ADDRESS—Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set high internally.
2) A COLUMN ADDRESS—All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of $\overline{CAS}$.

Description
(Continued)

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

The timing, as shown in $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle, is used for all operations described as follows:

1) Initialize the internal refresh address counter. For this operation, the 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
2) Write a test pattern of lows into memory cells at a single column address and 256 row addresses.
3) By using read-modify-write cycle, read the lows written at the last step and write a new high in the same cycle. This cycle is repeated 256 times, and highs are written into the 256 memory cells.
4) Read the high written at the last step.
5) Compliment the test pattern and repeat the steps 2, 3 and 4.
6) Repeat the steps 2 through 5 for another 3 chips.

Decoupling and Noise Reduction Recommendations for MB85201

To minimize noise induction between signal lines as well as between signal and power supply lines, good board design practice requires consideration of the following.

1) Provide a capacitor of approx. a few μF for each module, even though the MB85201 has two decoupling capacitors of 0.15μF on each module.
2) Remove noise, ringing, overshoot and undershoot from the address, control and data-input lines, so that the MB85201 won't latch spurious signals due to the noise induction between signal lines, and between signal and power supply lines.
3) Maintain sufficient timing margins and remove critical timing in the board design to avoid the problem mentioned in Item 2.
4) In order to avoid noise induction on the IN line at the falling edge of $\overline{W}$ when the delayed write or read-modify-write cycle is used, the falling edge of $\overline{W}$ signal should not coincide with the transition point of address and OUT signals. Since decoupling capacitors on the module board can't smooth the output current at the OUT pin, noise is introduced on the power supply buss (V_{CC} or V_{SS}) and also on the IN line at t_{RAC} or t_{CAC} in the read cycle.
5) Provide appropriate damping if necessary, to avoid excessive overshoot or undershoot on the TTL input waveform.

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.4		6.5	V	
Input low voltage	V_{IL}	−1.0		0.8	V	

Capacitance
(T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input capcitance A_0 through A_8, IN, $\overline{W}$	C_{IN1}		50	pF
Input capacitance $\overline{RAS}$0 through $\overline{RAS}$3	C_{IN2}		15	pF
Input capacitance $\overline{CAS}$	C_{IN3}		65	pF
Output capacitance OUT	C_{OUT}		55	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB85201-12 Min	MB85201-12 Max	MB85201-15 Min	MB85201-15 Max	Unit
Operating current*1 Average power supply current (one $\overline{RAS}$*2, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		79		71	mA
Standby current Standby power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		18		18	mA
Refresh current 1*1,4 Average power supply current ($\overline{CAS}$ = V_{IH}, all $\overline{RAS}$ cycling; t_{RC} = min)	I_{CC3}		220		200	mA
Page mode current*1 Average power supply current (one $\overline{RAS}$*3 = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min)	I_{CC4}		44		39	mA
Refresh current 2*4 Average power supply current (all $\overline{RAS}$ cycling, $\overline{CAS}$-before-$\overline{RAS}$)	I_{CC5}		240		220	mA
Input leakage current Any input (0 ≤ V_{IN} ≤ 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)	$I_{I(L)}$	−40	40	−40	40	μA
Output leakage current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	$I_{O(L)}$	−40	40	−40	40	μA
Output levels Output high voltage (I_{OH} = −5 mA) Output low voltage (I_{OL} = 4.2 mA)	V_{OH} V_{OL}			2.4	0.4	V

Notes: *1 I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
*2 The selected $\overline{RAS}$ is cycling and other $\overline{RAS}$s are in V_{IH}.
*3 The selected $\overline{RAS}$ is in V_{IL} and other $\overline{RAS}$s are in V_{IH}.
*4 When all chips are refreshed simultaneously, the average power dissipation of the module must be less than 640 mW at any 100 ms interval.

AC Characteristics *1,2,3
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB85201-12 Min	MB85201-12 Max	MB85201-15 Min	MB85201-15 Max	Unit
Time between refresh	t_{REF}		4		4	ns
Random read/write cycle time	t_{RC}	230		260		ns
Read-write-cycle time	t_{RWC}	230		260		ns
Access time from $\overline{RAS}$*4,6	t_{RAC}		120		150	ns
Access time from $\overline{CAS}$*5,6	t_{CAC}		60		75	ns
Output buffer turn off delay	t_{OFF}	0	25	0	30	ns
Transition time	t_T	3	50	3	50	ns

Notes: *1 An initial pause of 200 μs is required after power-up. And then several cycles of all $\overline{RAS}$'s (to which any 8 cycles to perform refresh are adequate) are required before proper device operation is achieved.
If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
*2 AC characteristics assume t_T = 5 ns.
*3 V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
*4 Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
*5 Assumes that $t_{RCD} \geq t_{RCD}$ (max).
*6 Measured with a load equivalent to 2 TTL loads and 100 pF.

AC Characteristics *1,2,3
(Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB85201-12 Min	MB85201-12 Max	MB85201-15 Min	MB85201-15 Max	Unit
$\overline{RAS}$ precharge time	t_{RP}	100		100		ns
$\overline{RAS}$ pulse width	t_{RAS}	120	10000	150	10000	ns
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns
$\overline{CAS}$ pulse width	t_{CAS}	60	10000	75	10000	ns
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ delay time*7,8	t_{RCD}	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ set up time	t_{CRS}	20		20		ns
Row address set up time	t_{ASR}	0		0		ns
Row address hold time	t_{RAH}	12		15		ns
Column address set up time	t_{ASC}	0		0		ns
Column address hold time	t_{CAH}	20		25		ns
Read command set up time	t_{RCS}	0		0		ns
Read command hold time referenced to $\overline{CAS}$*10	t_{RCH}	0		0		ns
Read command hold time referenced to $\overline{RAS}$*10	t_{RRH}	20		20		ns
Write command set up time	t_{WCS}	0		0		ns
Write command hold time	t_{WCH}	20		25		ns
Write command pulse width	t_{WP}	20		25		ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	50		60		ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	50		60		ns
Data in set up time	t_{DS}	0		0		ns
Data in hold time	t_{DH}	20		25		ns
$\overline{CAS}$ to $\overline{W}$ delay*9	t_{CWD}	20		25		ns
$\overline{CAS}$ set up time referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)	t_{FCS}	25		30		ns
$\overline{CAS}$ hold time referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)	t_{FCH}	25		30		ns
$\overline{RAS}$ precharge to $\overline{CAS}$ active time ($\overline{CAS}$-before-$\overline{RAS}$)	t_{RPC}	20		20		ns

Notes:
*1 An initial pause of 200 μs is required after power-up. And then several cycles of all $\overline{RAS}$'s (to which any 8 cycles to perform refresh are adequate) are required before proper device operation is achieved.
If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

*2 AC characteristics assume t_T = 5 ns.

*3 V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).

*7 Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

*8 t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T = 5 ns) + t_{ASC} (min).

*9 t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.

*10 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

AC Characteristics *1,2,3
(Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB85201-12 Min	MB85201-12 Max	MB85201-15 Min	MB85201-15 Max	Unit
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CPR}	25		30		ns
Page mode read/write cycle time	t_{PC}	120		150		ns
Page mode read-write cycle time	t_{PRWC}	120		150		ns
Page mode $\overline{CAS}$ precharge time	t_{CP}	50		65		ns
Refresh counter test cycle time*11	t_{RTC}	375		430		ns
Refresh counter test $\overline{RAS}$ pulse width*11	t_{TRAS}	265	1000	320	1000	ns
Refresh counter test $\overline{CAS}$ precharge time*11	t_{CPT}	60		70		ns
$\overline{RAS}$ to $\overline{RAS}$ precharge time	t_{RRP}	0		0		ns

Notes: *1 An initial pause of 200 μs is required after power-up. And then several cycles of all $\overline{RAS}$'s (to which any 8 cycles to perform refresh are adequate) are required before proper device operation is achieved.
If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

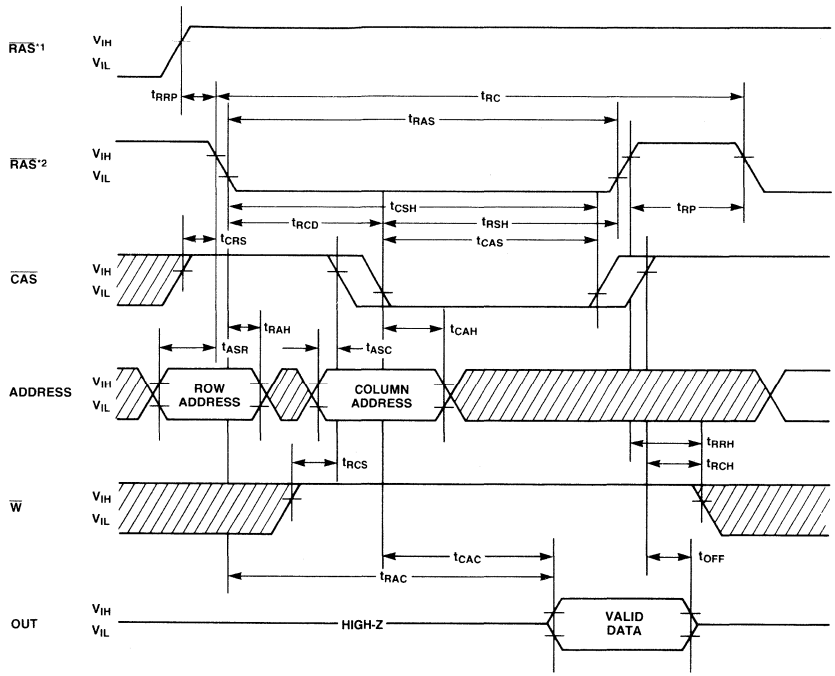
*2 AC characteristics assume t_T = 5 ns.

*3 V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).

*11 Refresh counter test cycle only.

Timing Diagrams

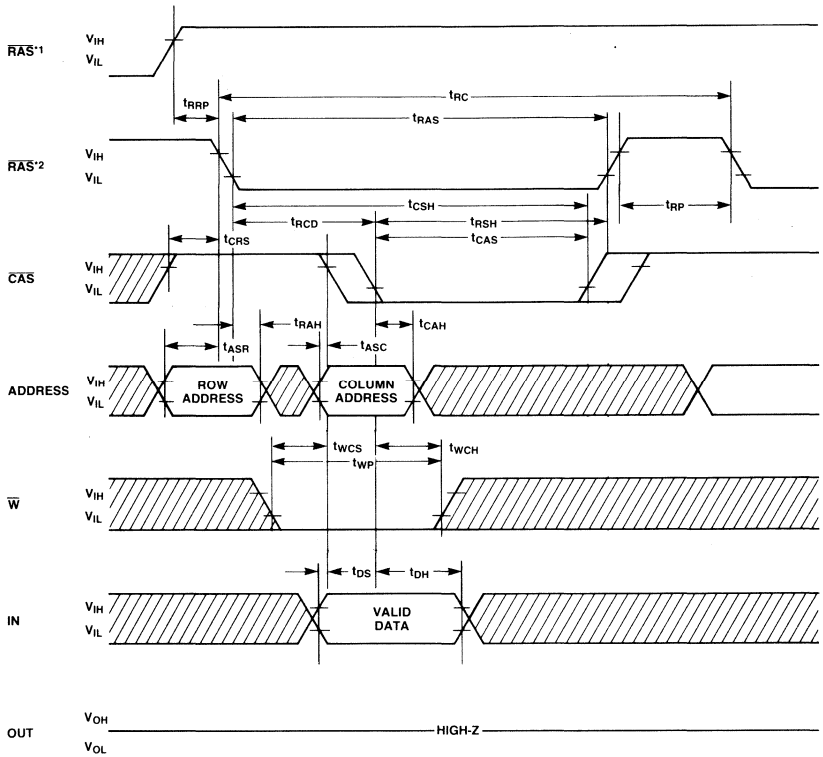
Read Cycle



NOTES: *1 IT IS FOR UNSELECTED $\overline{RAS}$.
*2 IT IS FOR THE SELECTED $\overline{RAS}$.

Timing Diagrams
(Continued)

Write Cycle (Early Write)

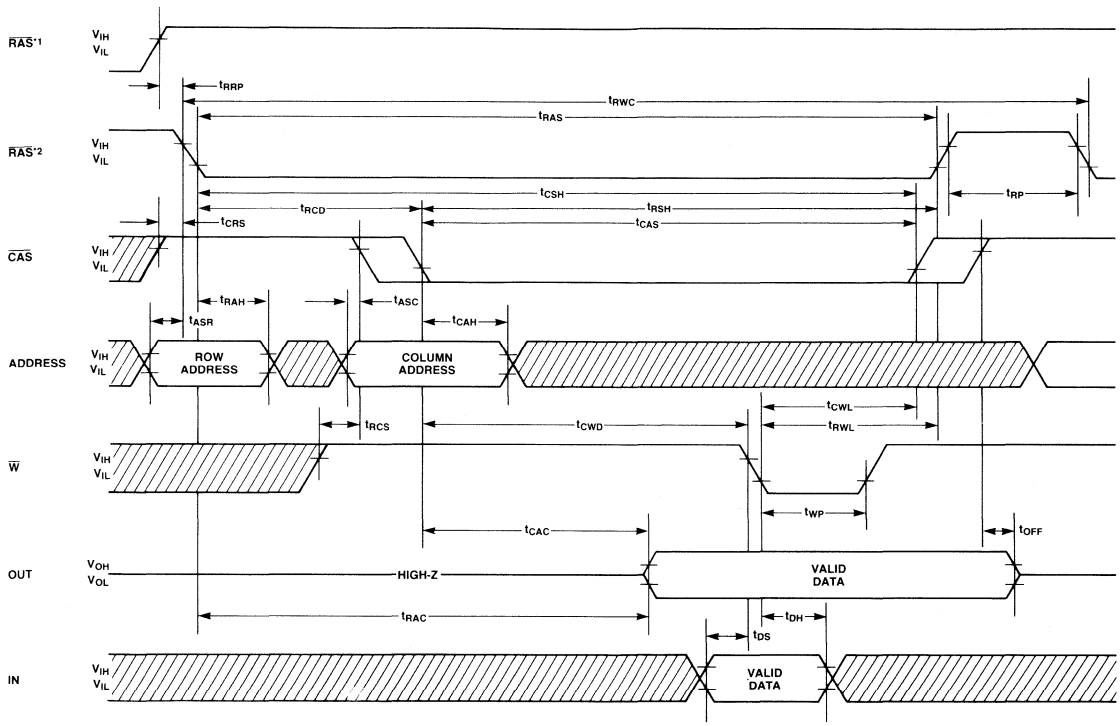


NOTES: *1 IT IS FOR UNSELECTED $\overline{RAS}$.
*2 IT IS FOR THE SELECTED $\overline{RAS}$.

DON'T CARE

Timing Diagrams
(Continued)

Read-Write/Read-Modify-Write Cycle

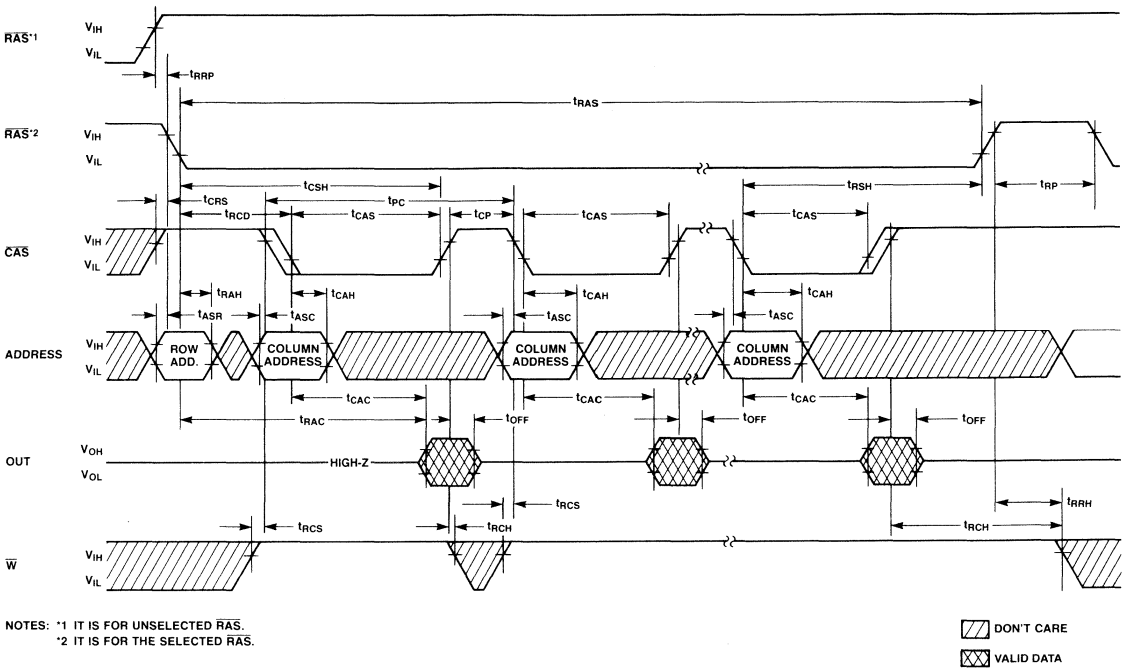


NOTES: *1 IT IS FOR UNSELECTED $\overline{RAS}$.
*2 IT IS FOR THE SELECTED $\overline{RAS}$.

DON'T CARE

Timing Diagrams
(Continued)

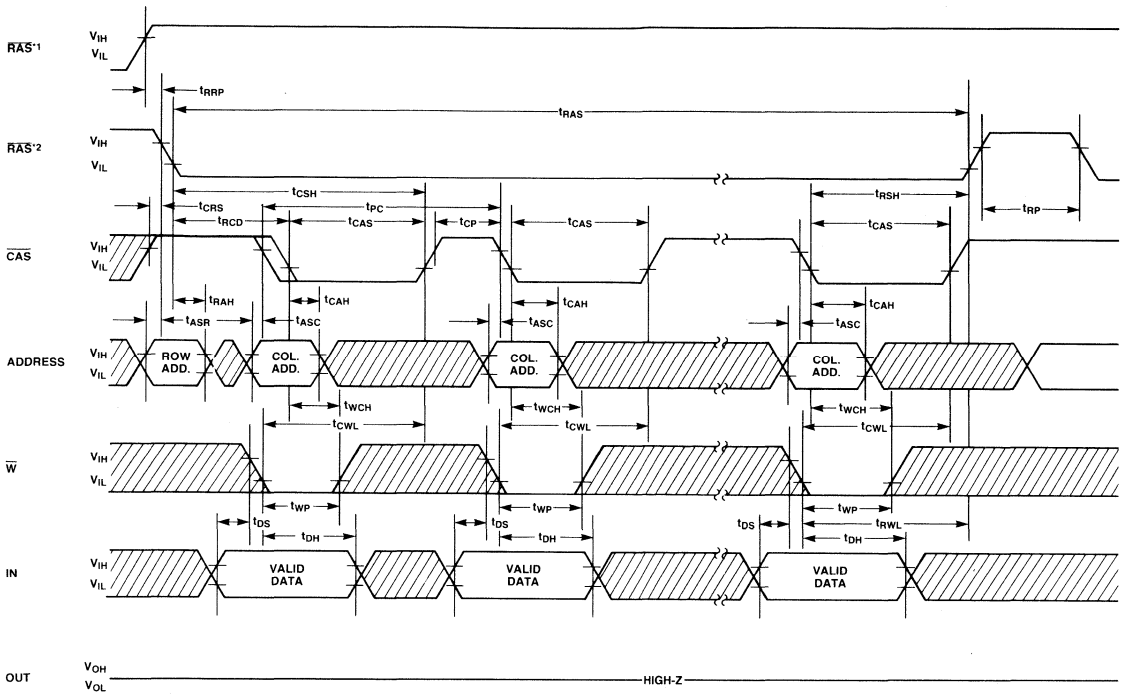
Page Mode Read Cycle



NOTES: *1 IT IS FOR UNSELECTED $\overline{RAS}$.
*2 IT IS FOR THE SELECTED $\overline{RAS}$.

Timing Diagrams
(Continued)

Page Mode Write Cycle

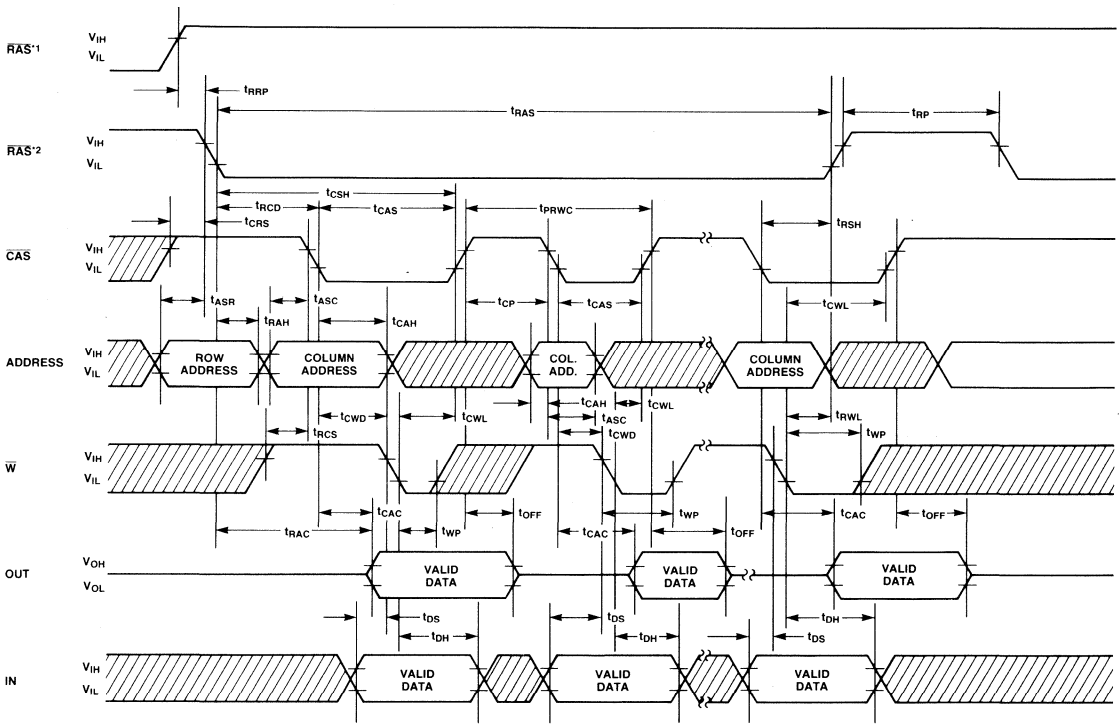


NOTES: *1 IT IS FOR UNSELECTED $\overline{RAS}$.
*2 IT IS FOR THE SELECTED $\overline{RAS}$.

DON'T CARE

Timing Diagrams
(Continued)

Page Mode Read-Write Cycle



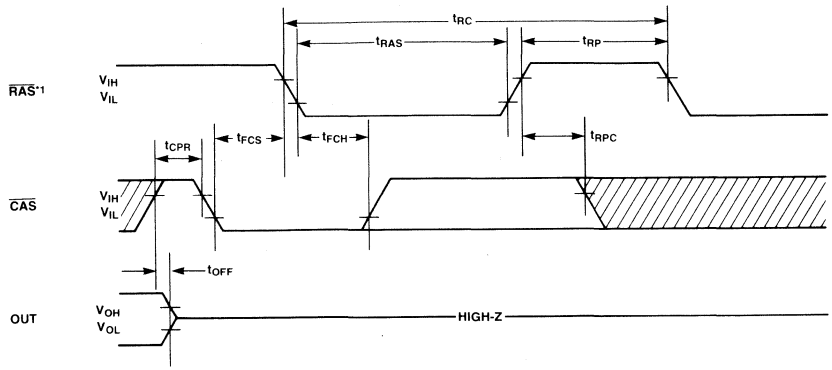
NOTES: *1 IT IS FOR UNSELECTED $\overline{RAS}$.
*2 IT IS FOR THE SELECTED $\overline{RAS}$.

DON'T CARE

Timing Diagrams
(Continued)

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

Note: Address, $\overline{W}$, IN = Don't care

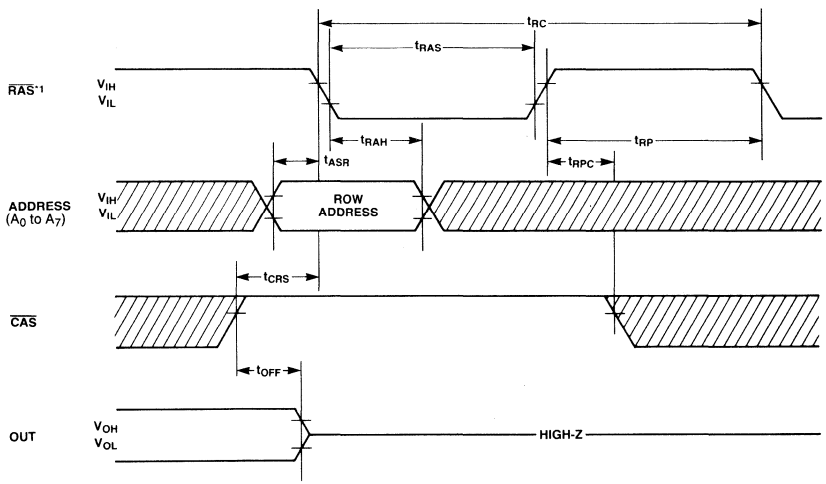


NOTE: *1 ANY COMBINATIONS OF $\overline{RAS}$0 TO $\overline{RAS}$3 ARE ALLOWED AND $\overline{RAS}$'s TO BE NOT REFRESHED ARE IN V_{IH}.

DON'T CARE

$\overline{RAS}$-only Refresh Cycle

Note: WE, D_{IN} = Don't Care, $A_8 = V_{IH}$ or V_{IL}

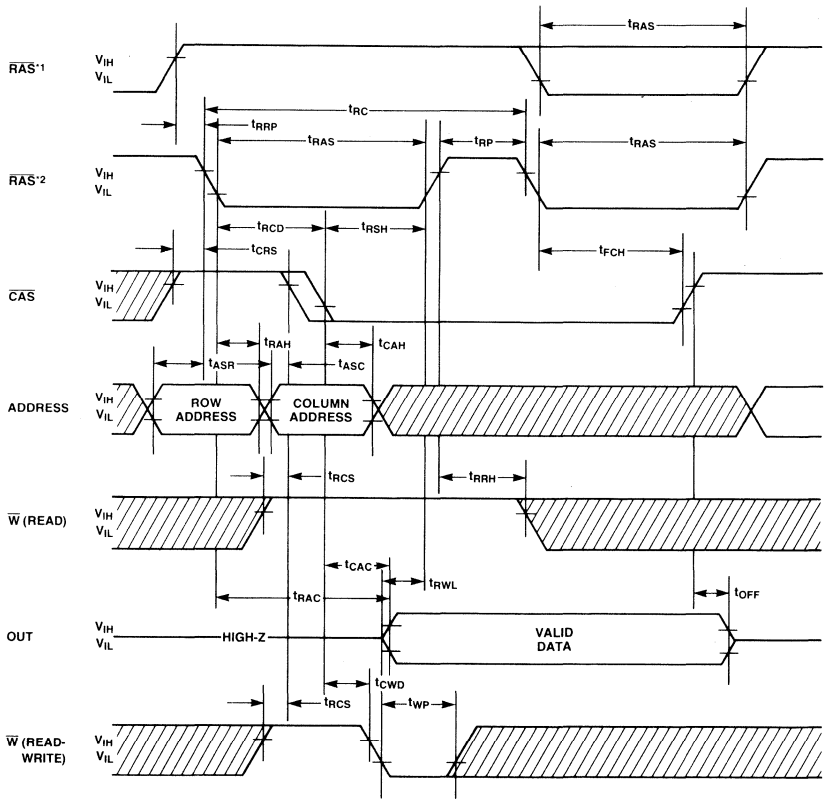


NOTE: *1 ANY COMBINATIONS OF $\overline{RAS}$0 TO $\overline{RAS}$3 ARE ALLOWED AND $\overline{RAS}$'s TO BE NOT REFRESHED ARE IN V_{IH}.

DON'T CARE

Timing Diagrams
(Continued)

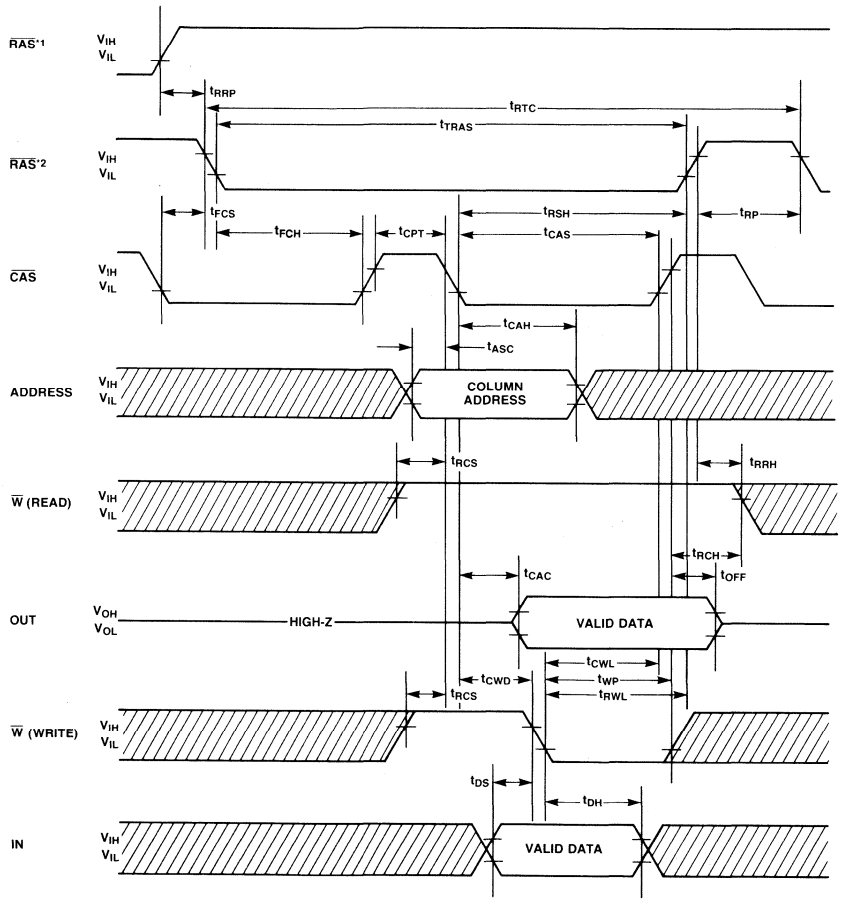
Hidden Refresh Cycle



NOTES: *1 IT IS FOR UNSELECTED $\overline{RAS}$.
*2 IT IS FOR THE SELECTED $\overline{RAS}$.

Timing Diagrams
(Continued)

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

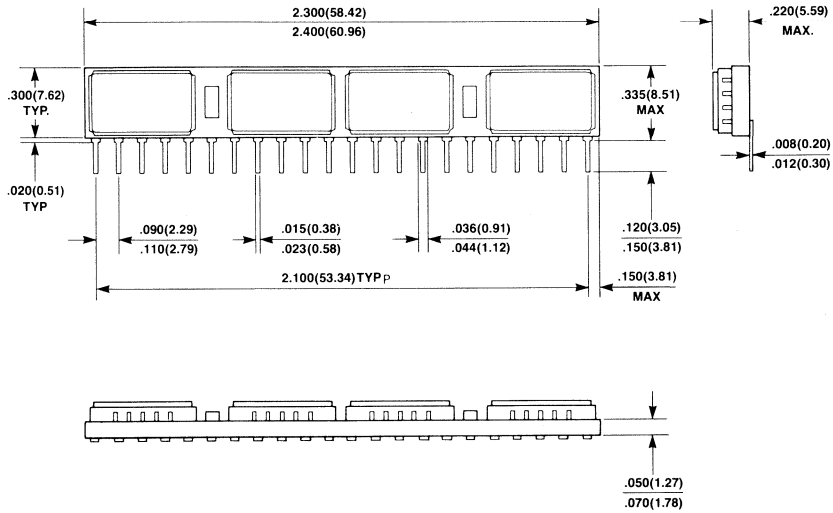


NOTES: *1 IT IS FOR UNSELECTED $\overline{RAS}$.
*2 IT IS FOR THE SELECTED $\overline{RAS}$.

Package Dimensions

Dimensions in inches
(millimeters)

22-Lead Single In-Line Package Module
(Module No.: MSP-22S-CC04)



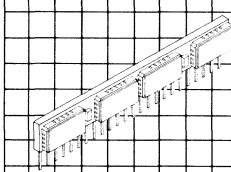
MB85203-10,MB85203-12,MB85203-15

MOS 262,144 x 4-Bit Dynamic RAM Module

Description

The Fujitsu MB85203 is a fully decoded, 262,144 words x 4-bit NMOS dynamic random access memory module consisting of four MB81257 DRAMs in 18-pad LCC packages mounted on a 24-pin multilayer ceramic substrate.

The MB85203 is intended for use in memory applications where large memory capacity is required within limited physical volume. Significant size reduction can be realized in applications such as mainframe memory, buffer memory, desk top computer and peripheral storage.



MSP-24S-CC04

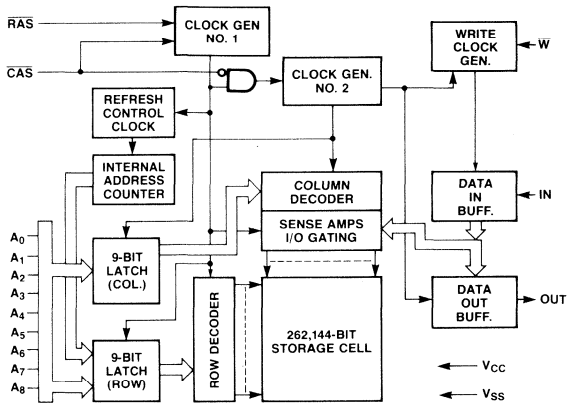
Features

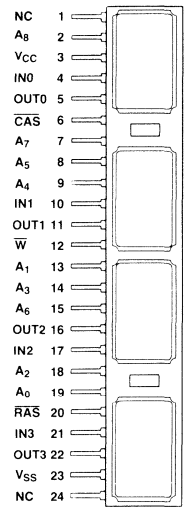
- **262,144 x 4 DRAM 24-pin SIP (MB81257 x 4)**
- **Row access time**
  100 ns max. (MB85203-10)
  120 ns max. (MB85203-12)
  150 ns max. (MB85203-15)
- **Cycle time**
  210 ns min. (MB85203-10)
  230 ns min. (MB85203-12)
  260 ns min. (MB85203-15)
- **Nibble cycle mode**
  50 ns min. (MB85203-10)
  65 ns min. (MB85203-12)
  80 ns min. (MB85203-15)
- **Single +5V supply, ±10° tolerance**
- **Low power (active)**
  1540 mW max. (MB85203-10)
  1430 mW max. (MB85203-12)
  1254 mW max. (MB85203-15)
  100 mW max. (Standby)
- **4 ms/256 refresh cycles capability**
- **$\overline{RAS}$-only, CAS-before-$\overline{RAS}$ and Hidden refresh capability**
- **Read-Modify-Write and Nibble mode capability**
- **Common I/O capability using Early Write operation**
- **On-chip latches for Addresses and Data-in**
- **All inputs and outputs are TTL compatible**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

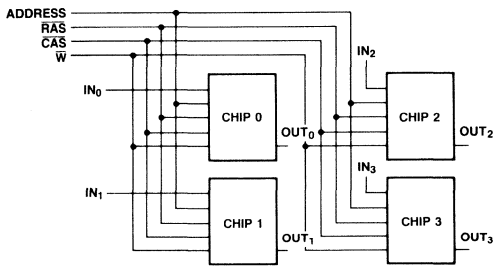
MB85203 Block Diagrams and Pin Assignment

Block Diagram for Each Chip





Functional Block Diagram



Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Storage temperature	T_{STG}	−55 to +150	°C
Power dissipation	P_D	2.4	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Description

Simple Timing Requirement

The MB85203 has improved circuitry that eases timing requirements for high speed access operations. The MB85203 can operate under the condition of t_{RCD} (max) = t_{CAC} thus providing optimal timing for address multiplexing. In addition; the MB85203 has the minimal hold times of address (t_{CAH}), $\overline{W}$ (t_{WCH}) and IN (t_{DH}). The MB85203 provides higher throughout in interleaved memory system applications. Fujitsu has made timing requirements that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the column address, IN and $\overline{W}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{W}$ Delay) are not restricted by t_{RCD}.

Address Inputs

A total of eighteen binary input address bits are required to decode any 4-bits of data in 1,048,576 cell locatons within the MB85203.

Nine row address bits are established on the input pins (A_0 through A_8) and latched with $\overline{RAS}$.

Nine column address bits are established on the input pins and latched with $\overline{CAS}$. All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

Write Enable

The read mode or write mode is selected with the $\overline{W}$ input. A logic high on the $\overline{W}$ dictates read mode, logic low dictates write mode. Data inputs are disabled when read mode is selected.

Data Inputs

The 4-bit data is written into the MB85203 during a write or read-write cycle. The latter falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the Data In (IN) register. In a write cycle, if $\overline{W}$ is brought low before $\overline{CAS}$, IN are strobed by $\overline{CAS}$ and the set-up and hold times are referenced to $\overline{CAS}$. In a delayed write or read-write cycle, $\overline{W}$ can be delayed after $\overline{CAS}$ has already gone low and $\overline{CAS}$ to $\overline{W}$ Delay Time (t_{CWD}) has been satisfied.

Thus IN0 to IN3 are strobed by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$.

Data Outputs

The output buffers of each chip are three-state TTL compatible with a fan-out of two standard TTL loads. OUT are the same polarity as IN. The output is in high impedance state until $\overline{CAS}$ is brought low. In a read or read-write cycle, the output is valid after t_{RAC} from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from the falling edge of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle, the identical sequence occurs but data are not valid.

Fast Read-While-Write-Cycle

The MB85203 has a fast read-while-write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{W}$ when $\overline{CAS}$ goes low. When $\overline{W}$ is low during $\overline{CAS}$ transition to low, the MB85203 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. Whereas, when $\overline{W}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MB85203 goes into the delayed write mode. The output then contains the data from the cell selected and the data from IN are written into the cell selected. Therefore, a very fast read write cycle (t_{RC} = t_{RWC}) is possible with the MB85203.

Nibble Mode

Nibble mode allows high speed serial read, write or read-modify-write access of 2, 3 or 4-bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 row addresses and 8 column addresses.

The 2-bits of addresses (CA_8, RA_8) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by normal mode, the remaining nibble bits may be accessed by toggling $\overline{CAS}$ "high" then "low" while $\overline{RAS}$ remains low. Toggling $\overline{CAS}$ causes RA_8 and CA_8 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. (See Table 1). If more than 4-bits are accessed during nibble mode, the address sequence will begin to repeat.

Description
(Continued)

If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on subsequent access, the new data will be written into the selected cell location.

In nibble mode, the three-state control of the OUT pin is determined by the first normal access cycle.

The data output is controlled only by the $\overline{W}$ state referenced at the $\overline{CAS}$ negative transition of the normal cycle (first nibble bit). That is, when $t_{WCS} > t_{WCS}$ (min) is met, the data output will remain high impedance state throughout the succeeding nibble cycle regardless of the $\overline{W}$ state. When $t_{CWD} > t_{CWD}$ (min) is met, the data output will contain data from the cell selected during the succeeding nibble cycle regardless of the $\overline{W}$ state. The write operation is done during the period in which the $\overline{W}$ and $\overline{CAS}$ clocks are low.

Therefore, the write operation can be performed bit by bit during each nibble operation regardless of timing conditions of $\overline{W}$ (t_{WCS} and t_{CWD}) during the normal cycle (first nibble bit). See Fig. 3.

Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row address (A_0 through A_7) at least every 4 ms. During refresh,either V_{IL} or V_{IH} is permitted for A_8.

The MB85203 offers the following three types of refresh.

1) $\overline{RAS}$ Only refresh avoids any output during refresh because the output buffer is in high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 row addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed.
2) $\overline{CAS}$-before-$\overline{RAS}$ Refresh: $\overline{CAS}$-before $\overline{RAS}$ refresh available on the MB85203 offers an alternate refresh method. If $\overline{CAS}$ is held low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter for each chip are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.
3) Hidden Refresh: Hidden refresh may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. In MB85203, hidden refresh means $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The internal refresh address counter provides the refresh addresses as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to high and then goes low again while $\overline{RAS}$ is held low, the read and write operation is enabled. This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with x row address bits to be defined as follows:

1) A ROW ADDRESS-Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set "high" internally.
2) A COLUMN ADDRESS-All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

1) Initialize the internal refresh address counter by using eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Throughout the test, use the same column address, and keep RA_8 high.
3) Write "low" to all 256 row address on the same column address by using normal early write cycles.
4) Read "low" written in step 3 and check, and simultaneously write "high" to the same address by using internal refresh counter test read-write cycles. This step is repeated 256 times, with the addresses being generated by the internal refresh address counter.
5) Read "high" written in step 4) and check by using normal read cycle for all 256 locations.
6) Complement the test pattern and repeat step 3), 4) and 5).

NIBBLE MODE ADDRESS SEQUENCE EXAMPLE

Sequence	Nibble Bit	RA_8	Row Address	CA_8	Column Address	
$\overline{RAS}$/$\overline{CAS}$ (normal mode)	1	0	10101010	0	10101010	input addresses
toggle $\overline{CAS}$ (nibble mode)	2	1	10101010	0	10101010	
toggle $\overline{CAS}$ (nibble mode)	3	0	10101010	1	10101010	generated internally
toggle $\overline{CAS}$ (nibble mode)	4	1	10101010	1	10101010	
toggle $\overline{CAS}$ (nibble mode)	1	0	10101010	0	10101010	sequence repeats

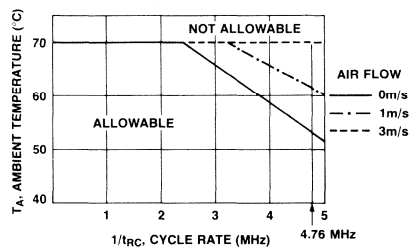
Description
(Continued)

Decoupling and Noise Reduction Recommendations for MB85203

To minimize noise induction between signal lines as well as between signal and power supply lines, good board design practice requires consideration of the following:

1. Provide a capacitor of appox. a few μF for each module, though the MB85203 has two decoupling capacitors of 0.15 μF on the each module.
2. Remove noise, riging, overshoot and undershoot from the address, control and data input lines, so that the MB85203 won't latch wrong signals due to the noise induction between signal lines and between signal and power supply lines.
3. Keep enough timing margin and remove critical timing in the board design, to avoid the problem mentioned in the above item 2.
4. In order to avoid noise induction on the IN line at the falling edge of $\overline{W}$ when the delayed write or read-modify-write cycle is used, the falling edge of $\overline{W}$ signal should not coincide with the transition point of address and OUT signal.(Since decoupling capacitors on the module board can't smooth the output current at the OUT pin, noise is inducted on the power supply line (V_{CC} or V_{SS}) and also on the IN line at t_{RAC} or t_{CAC} in the read cycle).
5. Provide an appropriate damping if necessary, to avoid excessive overshoot or undershoot on the TTL input waveforms.

MB85203 Derating Curve



Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V	0°C to +70°C*1
Input high voltage	V_{IH}	2.4		6.5	V	
Input low voltage	V_{IL}	−2.0		0.8	V	

Note: *1 Maximum ambient temperature is permissable under certain conditions. See derating curve.

Capacitance
(T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input capacitance A_0 to A_8	C_{IN1}		40	pF
Input capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$	C_{IN2}		50	pF
Input capacitance IN	C_{IN3}		15	pF
Output capacitance OUT	C_{OUT}		15	pF

DC Characteristics

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
Operating current*1 average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	MB85203-10	I_{CC1}		280	mA
	MB85203-12			260	
	MB85203-15			228	
Standby current standby power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}		18	mA
Refresh current 1*1 average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	MB85203-10	I_{CC3}		240	mA
	MB85203-12			220	
	MB85203-15			200	
Nibble mode current*1 average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{NC} = min.)	MB85203-10	I_{CC4}		88	mA
	MB85203-12			80	
	MB85203-15			72	
Refresh current 2*1 average power supply current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min.)	MB85203-10	I_{CC5}		260	mA
	MB85203-12			240	
	MB85203-15			220	
Input leakage current any input ($0 \leqslant V_{IN} \leqslant 5.5V$, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)		$I_{I(L)}$	−40	40	μA
Output leakage current (data out is disabled, $0V \leqslant V_{OUT} \leqslant 5.5V$)		$I_{O(L)}$	−10	10	μA
Output levels output high voltage (I_{OH} = −5 mA) output low voltage (I_{OL} = 4.2 mA)		V_{OH} V_{OL}	2.4	 0.4	V

Note: *1 I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC Characteristics *1,2,3
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB85203-10 Min	MB85203-10 Max	MB85203-12 Min	MB85203-12 Max	MB85203-15 Min	MB85203-15 Max	Unit
Time between refresh	t_{REF}		4		4		4	ms
Random read/write cycle time*12	t_{RC}	210		230		260		ns
Read-write cycle time*12	t_{RWC}	210		230		260		ns
Access time from $\overline{RAS}$*4,6	t_{RAC}		100		120		150	ns
Access time from $\overline{CAS}$*5,6	t_{CAC}		50		60		75	ns
Output buffer turn off delay	t_{OFF}	0	25	0	25	0	30	ns
Transition time	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	90		100		100		ns
$\overline{RAS}$ pulse width	t_{RAS}	110	100000	120	100000	150	100000	ns
$\overline{RAS}$ hold time	t_{RSH}	60		60		75		ns
$\overline{CAS}$ pulse width	t_{CAS}	60	100000	60	100000	75	100000	ns
$\overline{CAS}$ hold time	t_{CSH}	110		120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ delay time*7,8	t_{RCD}	20	50	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ set up time	t_{CRS}	15		20		20		ns
Row-address set up time	t_{ASR}	0		0		0		ns
Row-address hold time	t_{RAH}	10		12		15		ns
Column address set up time	t_{ASC}	0		0		0		ns
Column address hold time	t_{CAH}	15		20		25		ns
Read command set up time	t_{RCS}	0		0		0		ns
Read command hold time referenced to $\overline{CAS}$*11	t_{RCH}	0		0		0		ns
Read command hold time referenced to $\overline{RAS}$*11	t_{RRH}	20		20		20		ns

Notes:
*1 An initial pause of 200 μs is required after power-up. And then several cycles (to which any 8 cycle to perform refresh are adequate) are required before proper device operation is achieved. If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.
*2 AC characteristics assume t_T = 5 ns.
*3 V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
*4 Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
*5 Assumes that $t_{RCD} \geq t_{RCD}$ (max).
*6 Measured with a load equivalent to 2 TTL loads and 100 pF.
*7 Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
*8 t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T = 5 ns) + t_{ASC} (min).
*11 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
*12 The minimum cycle time is dependent on the ambient temperature and cooling conditions. See Fig. 4 for derating curve.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

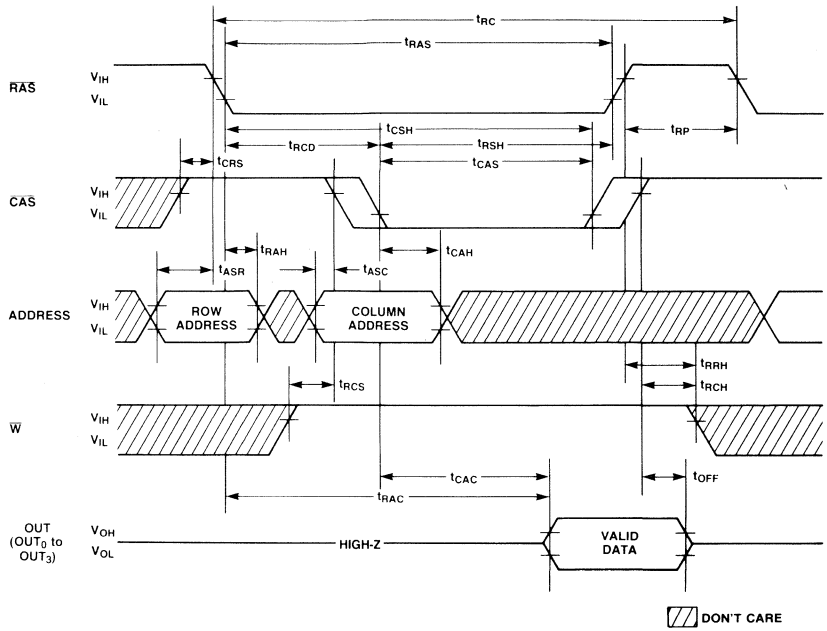
Parameter	Symbol	MB85203-10 Min	MB85203-10 Max	MB85203-12 Min	MB85203-12 Max	MB85203-15 Min	MB85203-15 Max	Unit
Write command set up time*9	t_{WCS}	0		0		0		ns
Write command pulse width	t_{WP}	15		20		25		ns
Write command hold time	t_{WCH}	15		20		25		ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		50		60		ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		30		40		ns
Data in set up time	t_{DS}	0		0		0		ns
Data in hold time	t_{DH}	15		20		25		ns
$\overline{CAS}$ to $\overline{W}$ delay*9	t_{CWD}	15		20		25		ns
Refresh set up time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCS}	20		25		30		ns
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCH}	20		25		30		ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CPR}	20		25		30		ns
$\overline{RAS}$ precharge to $\overline{CAS}$ active time (refresh cycles)	t_{RPC}	20		20		20		ns
Nibble mode read/write cycle time	t_{NC}	50		65		80		ns
Nibble mode read-write cycle time	t_{NRWC}	50		65		80		ns
Nibble mode access time	t_{NCAC}		20		30		40	ns
Nibble mode $\overline{CAS}$ pulse width	t_{NCAS}	20		30		40		ns
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	20		25		30		ns
Nibble mode read $\overline{RAS}$ hold time	t_{NRRSH}	20		30		40		ns
Nibble mode write $\overline{RAS}$ hold time	t_{NWRSH}	40		50		60		ns
Nibble mode $\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{RNH}	20		20		20		ns
Refresh counter test cycle time*10	t_{RTC}	330		375		430		ns
Refresh counter test $\overline{RAS}$ pulse width*10	t_{TRAS}	230	10000	265	10000	320	10000	ns
Refresh counter test $\overline{CAS}$ precharge time*10	t_{CPT}	50		60		70		ns

Notes: *9 t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.

*10 Test mode write cycle only.

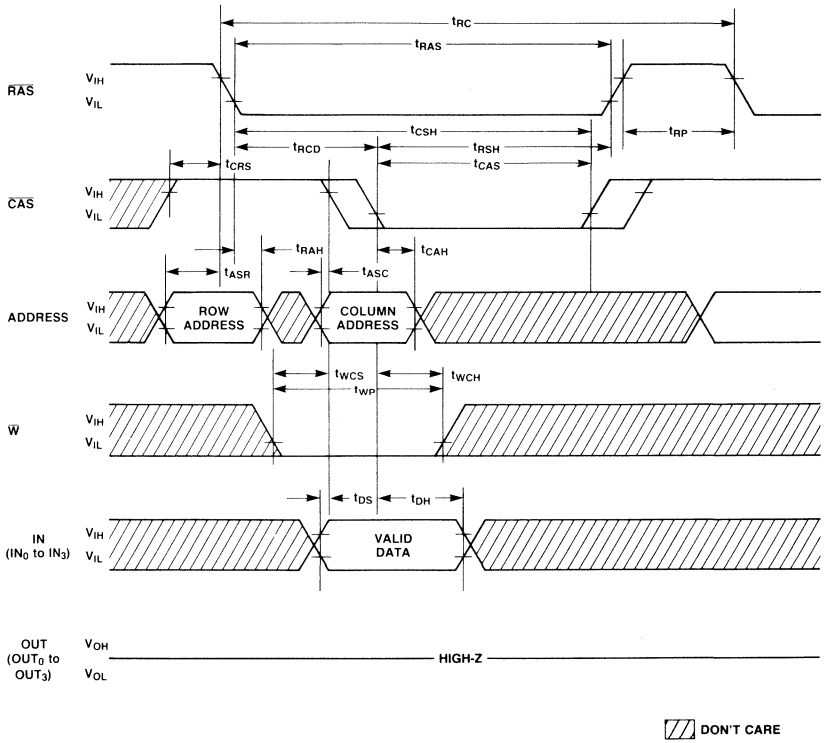
Timing Diagrams

Read Cycle



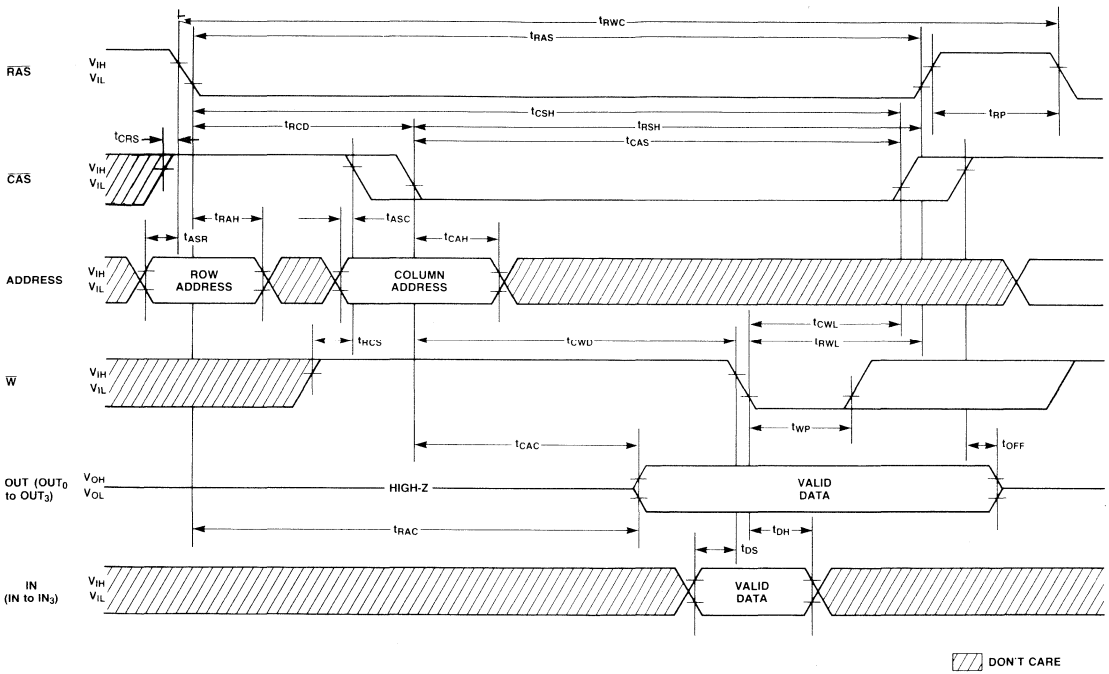
Timing Diagrams
(Continued)

Write Cycle (Early Write)



Timing Diagrams
(Continued)

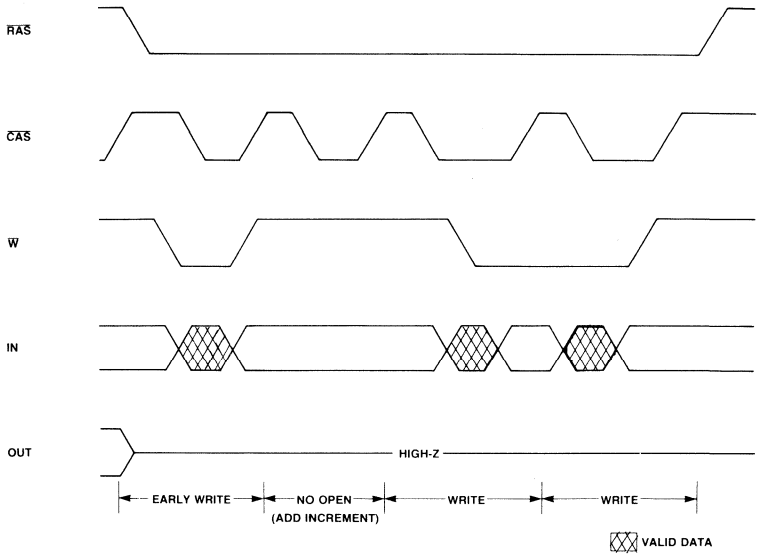
Read-Write/Read-Modify-Write Cycle



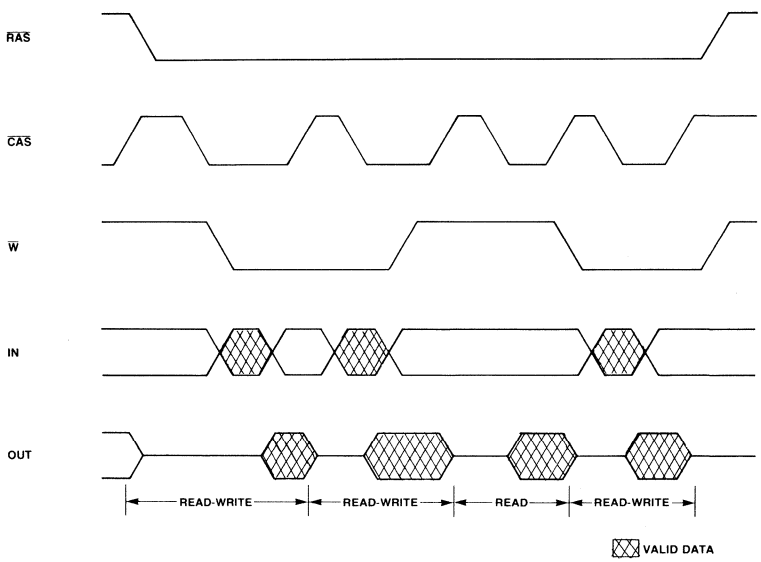
Timing Diagrams
(Continued)

Nibble Mode

*1 THE CASE OF FIRST NIBBLE CYCLE IS EARLY WRITE

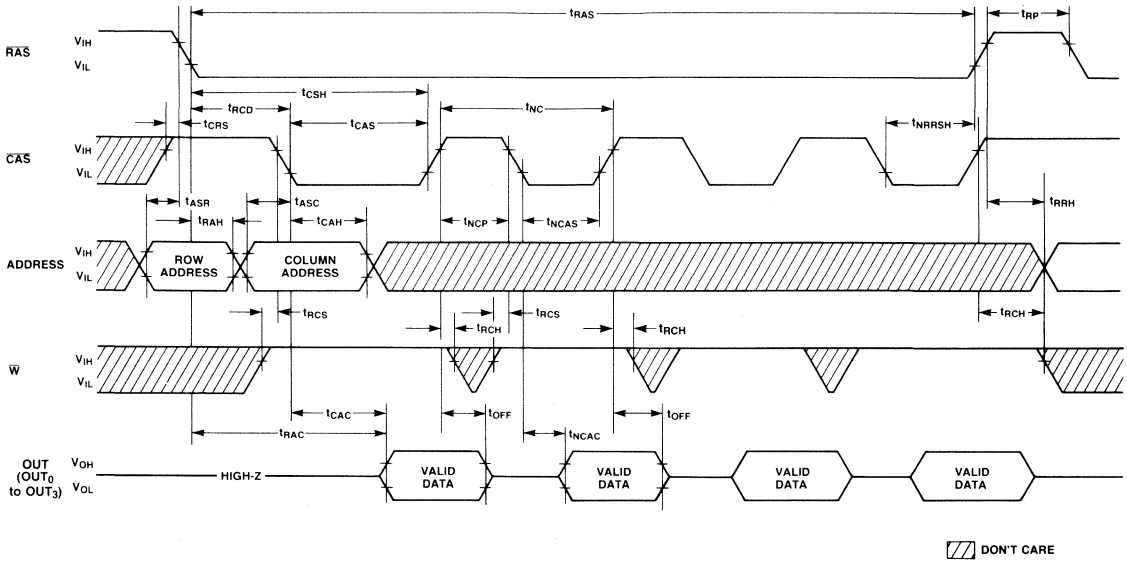


*2 THE CASE OF FIRST NIBBLE CYCLE IS DELAYED WRITE (READ-WRITE)



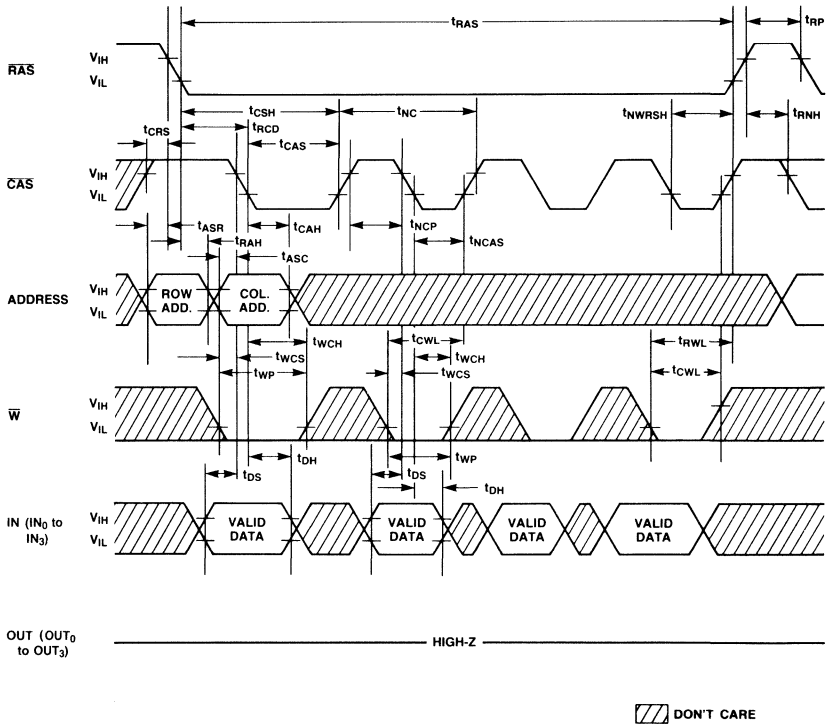
Timing Diagrams
(Continued)

Nibble Mode Read Cycle



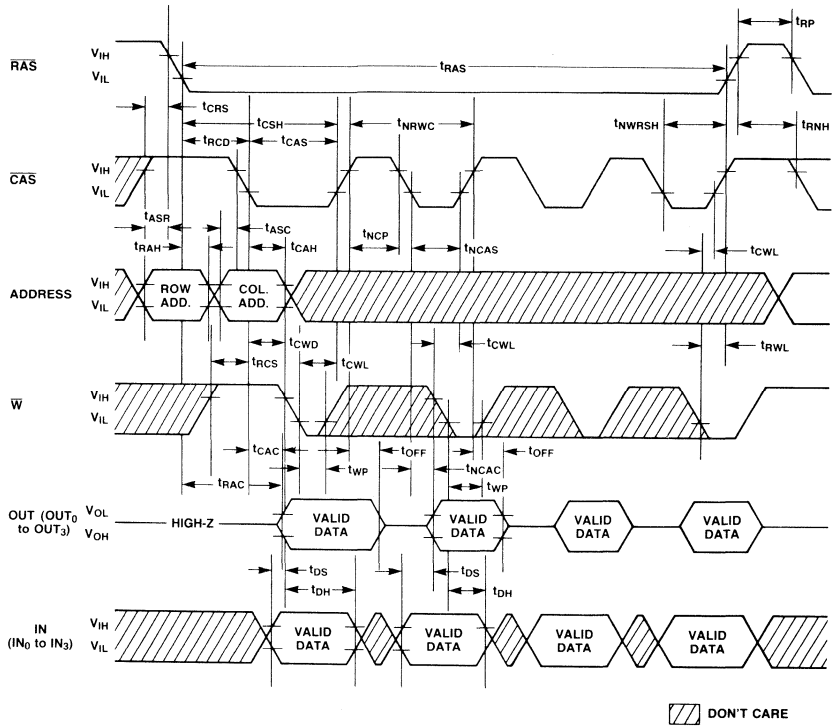
Timing Diagrams
(Continued)

Nibble Mode Write Cycle



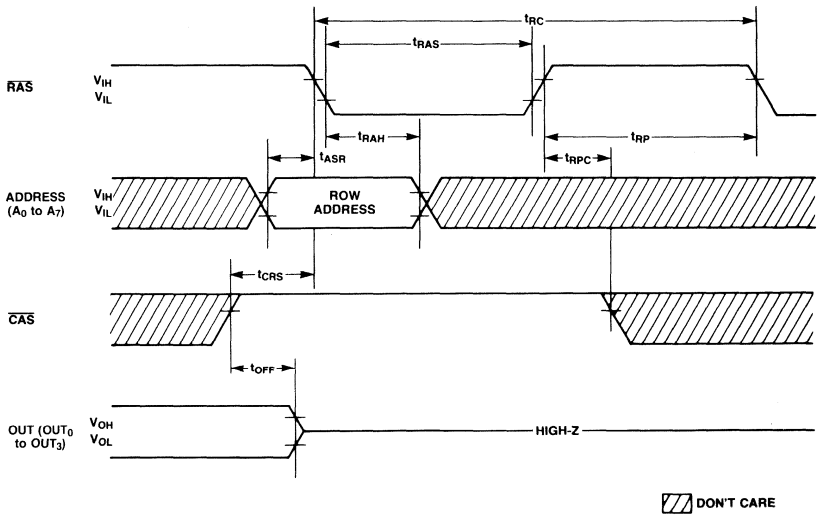
Timing Diagrams
(Continued)

Nibble Mode Read-Write Cycle

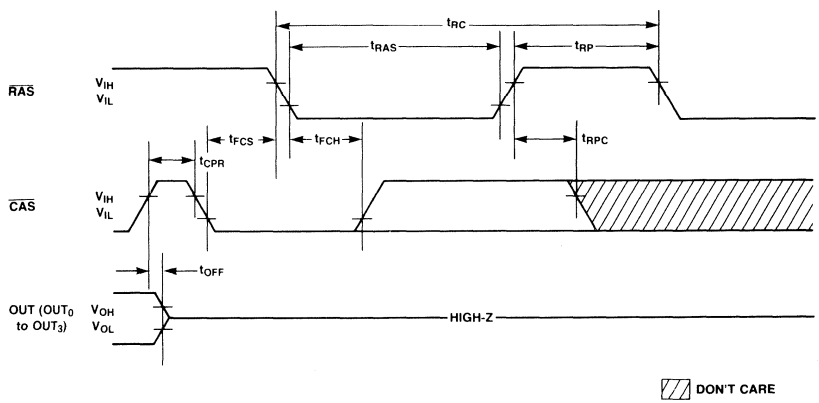


Timing Diagrams
(Continued)

$\overline{RAS}$-only Refresh Cycle
Note: $\overline{W}$, IN = Don't Care, A_8 = V_{IH} or V_{IL}

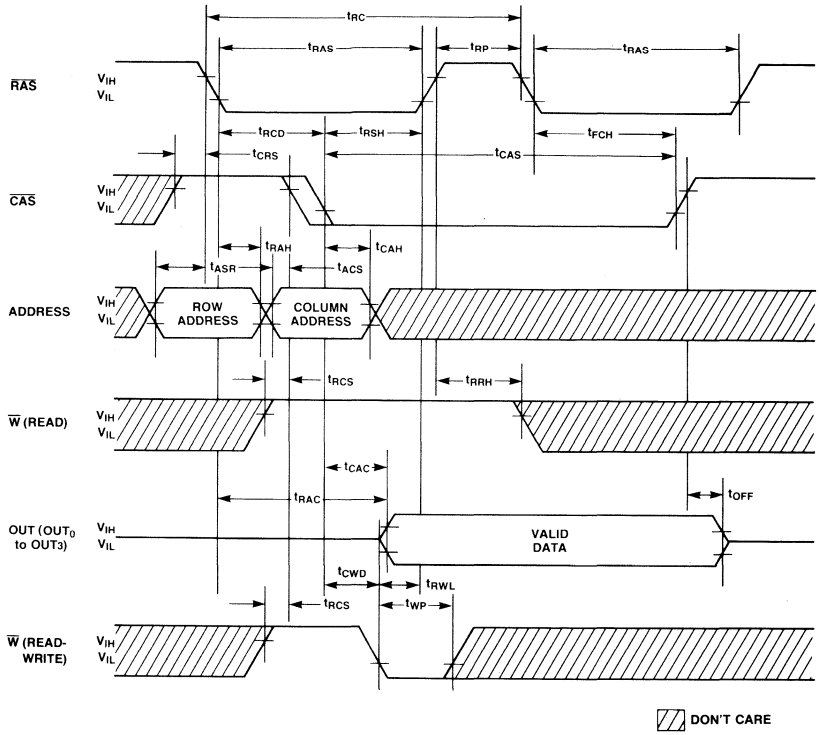


$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle
Note: Address, W, IN = Don't Care



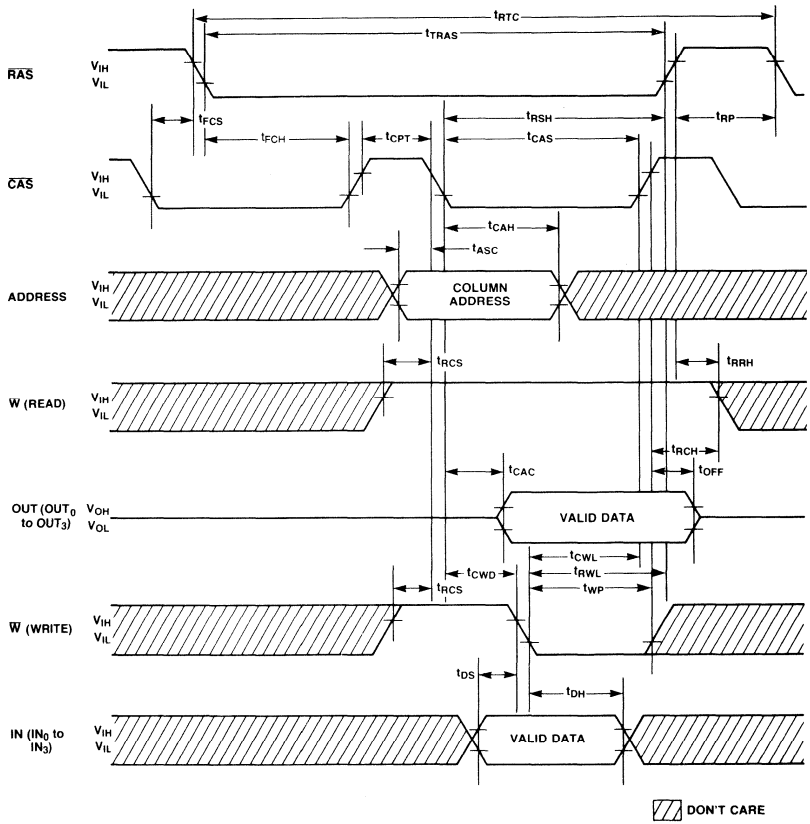
Timing Diagrams
(Continued)

Hidden Refresh Cycle



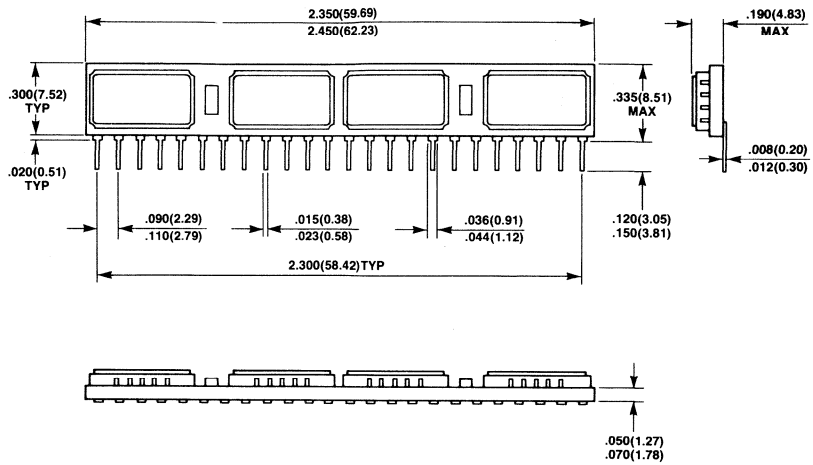
Timing Diagrams
(Continued)

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



Package Dimensions
(Continued)

24-Lead Single In-Line Package Module
(Module No.: MSP-24S-CC04)



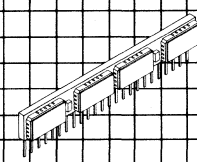
MB85204-10, MB85204-12, MB85204-15

262,144 x 4-Bit Dynamic Random Access Memory SIP Module

Description

The Fujitsu MB85204 is a fully decoded, 262,144 word x 4-bit NMOS dynamic random access memory module consisting of four MB81256 DRAMs in 18-pad LCC packages mounted on a 24-pin multilayer ceramic substrate.

The MB85204 is intended for use in memory applications where large memory capacity is required within limited physical volume. Significant size reduction can be realized in applications such as mainframe memory, buffer memory, desk top computers and peripheral storage.



MSP-24S-C04

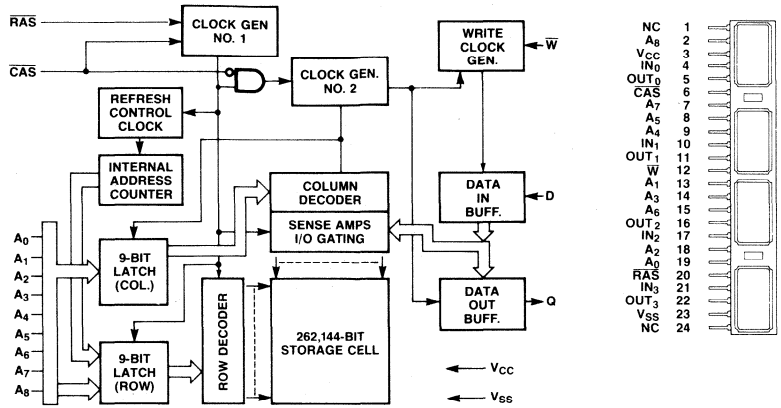
Features

- **262,144 x 4 DRAM 24-pin SIP (MB81256x4)**
- **Row access time**
  100 ns max. (MB85204-10)
  120 ns max. (MB85204-12)
  150 ns max. (MB85204-15)
- **Cycle time**
  210 ns min. (MB85204-10)
  230 ns min. (MB85204-12)
  260 ns min. (MB85204-15)
- **Page cycle time**
  100 ns min. (MB85204-10)
  120 ns min. (MB85204-12)
  150 ns m'n. (MB85204-15)
- **Single + 5V supply, ±10% tolerance**
- **Low power (active)**
  1540 mW max. (MB85204-10)
  1430 mW max. (MB85204-12)
  1254 mW max. (MB85204-15)
  100 mW max. (standby)
- **4 ms/256 refresh cycles capability**
- **$\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$ and Hidden refresh capability**
- **Read-Modify-Write and Page Mode Capability**
- **Common I/O capability using Early Write operation**
- **On-chip latches for Addresses and Data-in**
- **All inputs and outputs are TTL compatible.**

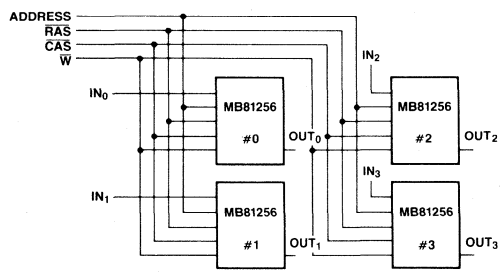
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB85204 Block Diagrams and Pin Assignment

Block Diagram for Each Chip



Functional Block Diagram



Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	2.4	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Description

Simple Timing Requirements

The MB85204 has improved circuitry that eases timing requirements for high speed access operations. The MB85204 can operate under the condition of $t_{RCD}(max) = t_{CAC}$ thus providing optimal timing for address multiplexing. In addition, the MB85204 has minimal hold times of address (t_{CAH}), $\overline{W}$ (t_{WCH}) and IN (t_{DH}). Fujitsu has made timing requirements that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the column address, IN and $\overline{W}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{W}$ Delay) are not restricted by t_{RCD}.

Address Inputs

A total of eighteen binary input address bits are required to decode any 4 bits of data in 1,048,576 storage cells within the MB85204. Nine row address bits are established on the input pins (A_0 through A_8) and latched with $\overline{RAS}$. Nine column address bits are established on the input pins and latched with $\overline{CAS}$. All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

Write Enable

The read mode or write mode is selected with the $\overline{W}$ input. A logic high on the $\overline{W}$ dictates read mode, logic low dictates write mode. Data inputs are disabled when read mode is selected.

Data Inputs

The 4-bit data is written into the MB85204 during a write or read-write cycle. The latter falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the IN register. In a write cycle, if $\overline{W}$ is brought low before the negative transition of $\overline{CAS}$, the set-up and hold times are referenced to $\overline{CAS}$. In a delayed write or read-write cycle, $\overline{W}$ will be low after $\overline{CAS}$ has already been low. Thus IN_0 to IN_3 are strobed by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$.

Data Outputs

The output buffers of each chip are three-state TTL compatible with a fan-out of two standard TTL loads. OUT is the same polarity as IN. The output is in high impedance state until $\overline{CAS}$ is brought low. In a read or read-write cycle, the output is valid after t_{RAC} from negative transition of the $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from negative transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to a high level. In a write cycle, the identical sequence occurs but data is not valid.

Fast Read-While-Write Cycle

The MB85204 has a fast read-while-write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{W}$ when $\overline{CAS}$ goes low. When $\overline{W}$ is low during $\overline{CAS}$ transition to low, the MB85204 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. Whereas, when $\overline{W}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MB85204 goes into the delayed write mode. The output then contains the data from the cell selected and the data from IN are written into the cell selected. Therefore, a very fast read-write cycle ($t_{RC} = t_{RWC}$) is possible with the MB85204.

Page-Mode

Page-mode operation permits strobing the row-address into the MB85204 while maintaining $\overline{RAS}$ at low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row addresses (A_0 through A_7) at least every 4 ms. During refresh, either V_{IL} or V_{IH} is permitted for A_8. Then MB85204 offers the following three types of refresh.

1) $\overline{RAS}$-Only Refresh;
   $\overline{RAS}$ Only refresh avoids any output during refresh because the output buffer is in high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 row addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed.
2) $\overline{CAS}$-before-$\overline{RAS}$ Refresh;
   $\overline{CAS}$-before-$\overline{RAS}$ refresh available on the MB85204 offers an alternate refresh method. If $\overline{CAS}$ is held low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter for each chip are enabled, and an internal refresh operation takes place. After the refresh operation has been executed the refresh address counter is automatically incremented for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.
3) Hidden Refresh;
   Hidden refresh may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. In the MB85204, hidden refresh means $\overline{CAS}$-before-$\overline{RAS}$ refresh and the internal refresh address is used; that is, no external refresh address is needed.

Description
(Continued)

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using $\overline{CAS}$-before-$\overline{RAS}$ counter test cyclo provides a convenient method of verifying the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes into high and goes into low again while $\overline{RAS}$ is held low, the read and write operations are enabled. This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell address (consisting of a row address (9 bits) and a column address (9 bits)) to be accessed, can be defined as follows:

1) A ROW ADDRESS—Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set high internally.
2) A COLUMN ADDRESS—All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

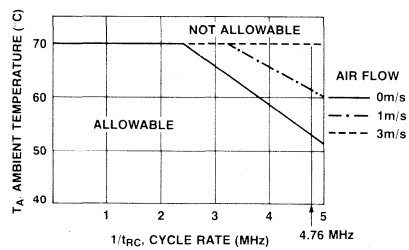
1) Initialize the internal refresh address counter by using eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Throughout the test, use the same column address, and keep RA8 high.
3) Write "low" to all 256 row address on the same column address by using normal early write cycles.
4) Read "low" written in step (3) and check, and simultaneously write "high" to the same address by using internal refresh counter test read-write cycles. This spec is repeated 256 times, with the addresses being generated by internal refresh address counter.
5) Read "high" written in step (4) and check by using normal read cycle for all 256 locations.
6) Complement the test pattern and repeat step (3), (4) and (5).

Decoupling and Noise Reduction Recommendations for MB85204

To minimize noise induction between signal lines as well as between signal and power supply lines, good board design practice requires consideration of the following:

1) Provide a capacitor of approx. a few μF for each module—even though the MB85204 has two or four decoupling capacitors of 0.1 μF on each module.
2) Remove noise, overshoot and undershoot from the address, control and data-input lines, so that the MB85204 won't latch wrong signals due to the noise induction between signal lines, and between signal and power supply lines.
3) Keep enough timing margin and remove critical timing in the board design to avoid the problem mentioned in Item 2 above.
4) In order to avoid noise induction on the IN line at the falling edge of $\overline{W}$ when the delayed write or read-modify-write cycle is used, the falling edge of $\overline{W}$ signal should not coincide with the transition point of address and OUT signals. (Since decoupling capacitors on the module board can't smooth the output current at the OUT pin, noise is inducted on the power supply line (V_{CC} or V_{SS}) and also on the IN line at t_{RAC} or t_{CAC} in the read cycle.)
5) Provide an appropriate damping if necessary, to avoid excessive overshoot or undershoot on the TTL input waveform.

MB85204 Derating Curve



Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V V	
Input high voltage	V_{IH}	2.4		6.5	V	0°C to +70°C*1
Input low voltage	V_{IL}	−2.0		0.8	V	

Note: 1* Maximum ambient temperature is permissible under certain conditions. See derating curve.

Capacitance
(T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input capcitance A_0 to A_8	C_{IN1}		40	pF
Input capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$	C_{IN2}		50	pF
Input capacitance IN	C_{IN3}		15	pF
Output capacitance OUT	C_{OUT}		15	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB85204-10 Min	MB85204-10 Max	MB85204-12 Min	MB85204-12 Max	MB85204-15 Min	MB85204-15 Max	Unit
Operating current Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = Min.)	I_{CC1}	280		260		228		mA
Standby current Standby power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		18		18		18	mA
Refresh current 1*1 Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = Min.)	I_{CC3}		240		220		200	mA
Page mode current Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = Min.)	I_{CC4}		140		120		100	mA
Refresh current 2*1 Average power supply current ($\overline{CAS}$-before-RAS; t_{RC} = Min.)	I_{CC5}		260		240		220	mA
Input leakage current, any input (0 ≤ V_{IN} ≤ 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)	$I_{I(L)}$	−40	40	−40	40	−40	40	μA
Output leakage current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	$I_{O(L)}$	−10	10	−10	10	−10	10	μA
Output levels Output high voltage (I_{OH} = −5 mA) Output low voltage (I_{OL} = 4.2 mA)	V_{OH} V_{OL}	2.4	 0.4	2.4	 0.4	2.4	 0.4	V

Notes: *1 I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC Characteristics[*1,2,3]
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB85204-10 Min	MB85204-10 Max	MB85204-12 Min	MB85204-12 Max	MB85204-15 Min	MB85204-15 Max	Unit
Time between refresh	t_{REF}		4		4		4	ms
Random read/write cycle time[*12]	t_{RC}	210		230		260		ns
Read-write-cycle time[*12]	t_{RWC}	210		230		260		ns
Access time from $\overline{RAS}$[*4,5]	t_{RAC}		100		120		150	ns
Access time from $\overline{CAS}$[*5,6]	t_{CAC}		50		60		75	ns
Output buffer turn off delay	t_{OFF}	0	25	0	25	0	30	ns
Transition time	t_T	3	50	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	90		100		100		ns
$\overline{RAS}$ pulse width	t_{RAS}	110	100000	120	100000	150	100000	ns
$\overline{RAS}$ hold time	t_{RSH}	60		60		75		ns
$\overline{CAS}$ pulse width	t_{CAS}	60	100000	60	100000	75	100000	ns
$\overline{CAS}$ hold time	t_{CSH}	110		120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ delay time[*7,8]	t_{RCD}	20	50	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ set up time	t_{CRS}	15		20		20		ns
Row address set up time	t_{ASR}	0		0		0		ns
Row address hold time	t_{RAH}	10		12		15		ns
Column address set up time	t_{ASC}	0		0		0		ns
Column address hold time	t_{CAH}	15		20		25		ns
Read command set up time	t_{RCS}	0		0		0		ns
Read command hold time referenced to $\overline{CAS}$[*11]	t_{RCH}	0		0		0		ns
Read command hold time referenced to $\overline{RAS}$[*11]	t_{RRH}	20		20		20		ns
Write command set up time[*9]	t_{WCS}	0		0		0		ns
Write command pulse width	t_{WP}	15		20		25		ns
Write command hold time	t_{WCH}	15		20		25		ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	40		50		60		ns

Notes:
- *1 An initial pause of 200 μs is required after power-up. And then several cycle (to which any 8 cycle to perform refresh are adequate) are required before proper device operation is achieved.
  If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.
- *2 AC characteristics assume t_T = 5 ns.
- *3 V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
- *4 Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
- *5 Assumes that $t_{RCD} \geq t_{RCD}$ (max).
- *6 Measured with a load equivalent to 2 TTL loads and 100 pF.
- *7 Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
- *8 t_{RCD} (min) = t_{RAH} (min) + 2t_T (t_T = 5 ns) + t_{ASC} (min).
- *9 t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
- *11 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
- *12 The minimum cycle time is dependent on the ambient temperature and cooling conditions.
  See derating curve.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

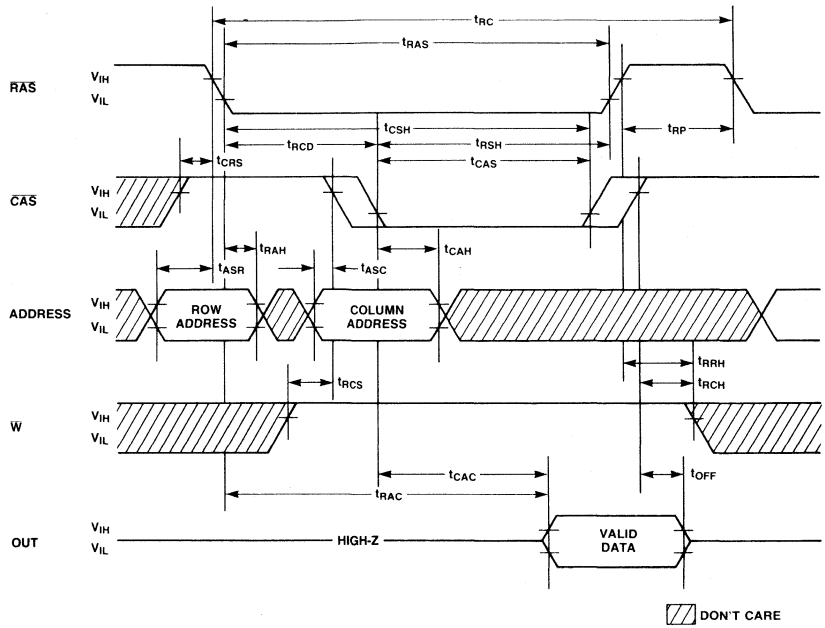
Parameter	Symbol	MB85204-10 Min	MB85204-10 Max	MB85204-12 Min	MB85204-12 Max	MB85204-15 Min	MB85204-15 Max	Unit
Write command to $\overline{CAS}$ lead time	t_{CWL}	40		50		60		ns
Data in set up time	t_{DS}	0		0		0		ns
Data in hold time	t_{DH}	15		20		25		ns
$\overline{CAS}$ to $\overline{W}$ delay*9	t_{CWD}	15		20		25		ns
Refresh set up time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCS}	20		25		30		ns
Refresh hold time for $\overline{CAS}$ Referenced to $\overline{RAS}$	t_{FCH}	20		25		30		ns
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	20		20		20		ns
Page mode read/write cycle time	t_{PC}	100		120		150		ns
Page mode read/write cycle time	t_{PRWC}	100		120		150		ns
Page mode $\overline{CAS}$ precharge time	t_{CP}	40		50		65		ns
Refresh counter test cycle time*10	t_{RTC}	330		375		430		ns
Refresh counter test $\overline{RAS}$ pulse width*10	t_{TRAS}	230	10000	265	10000	320	10000	ns
Refresh counter test $\overline{CAS}$ precharge time*10	t_{CPT}	50		60		70		ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CPR}	20		25		30		ns

Notes: *9 t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.

*10 Test mode write cycle only.

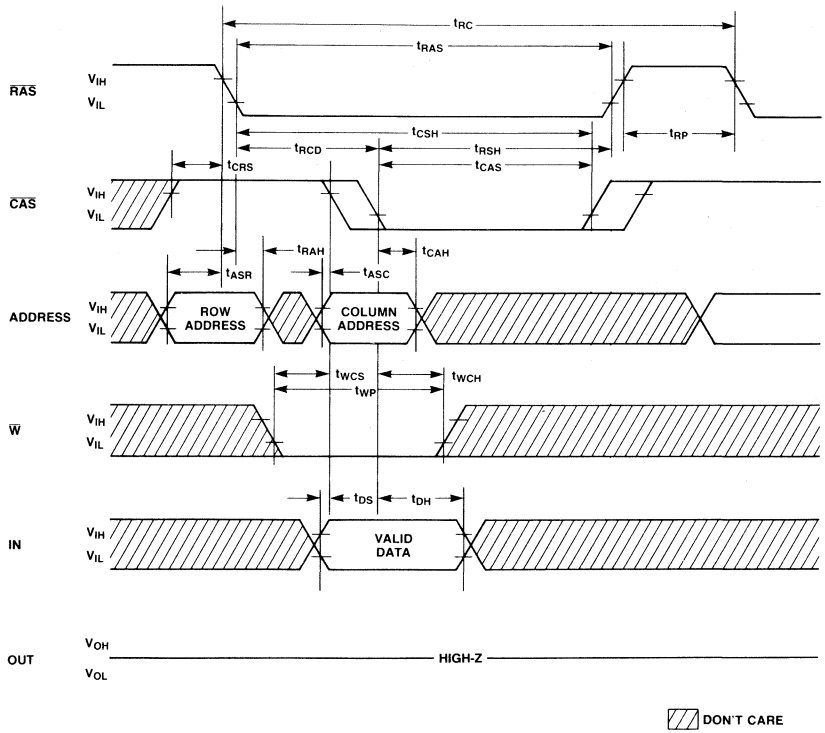
Timing Diagrams

Read Cycle



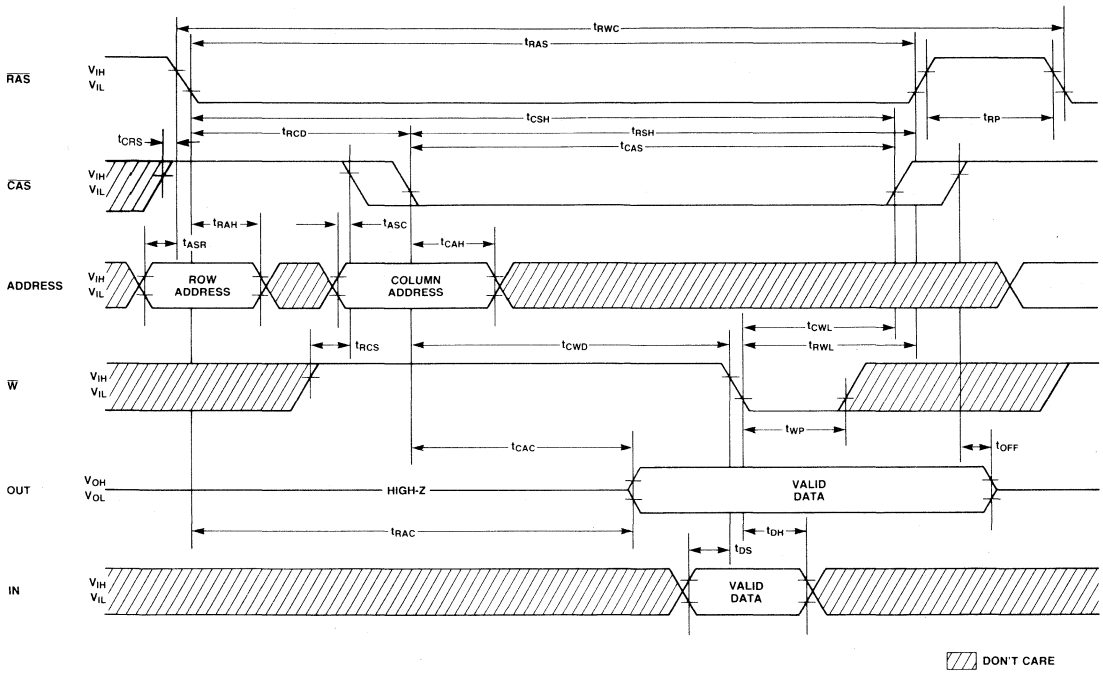
Timing Diagrams
(Continued)

Write Cycle (Early Write)



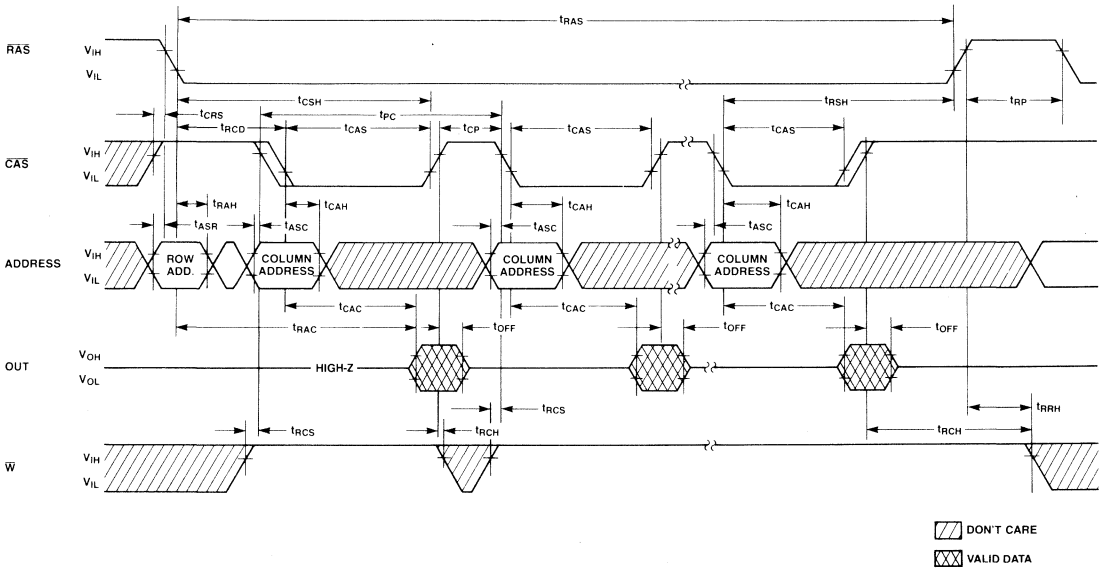
Timing Diagrams
(Continued)

Read-Write/Read-Modify-Write Cycle



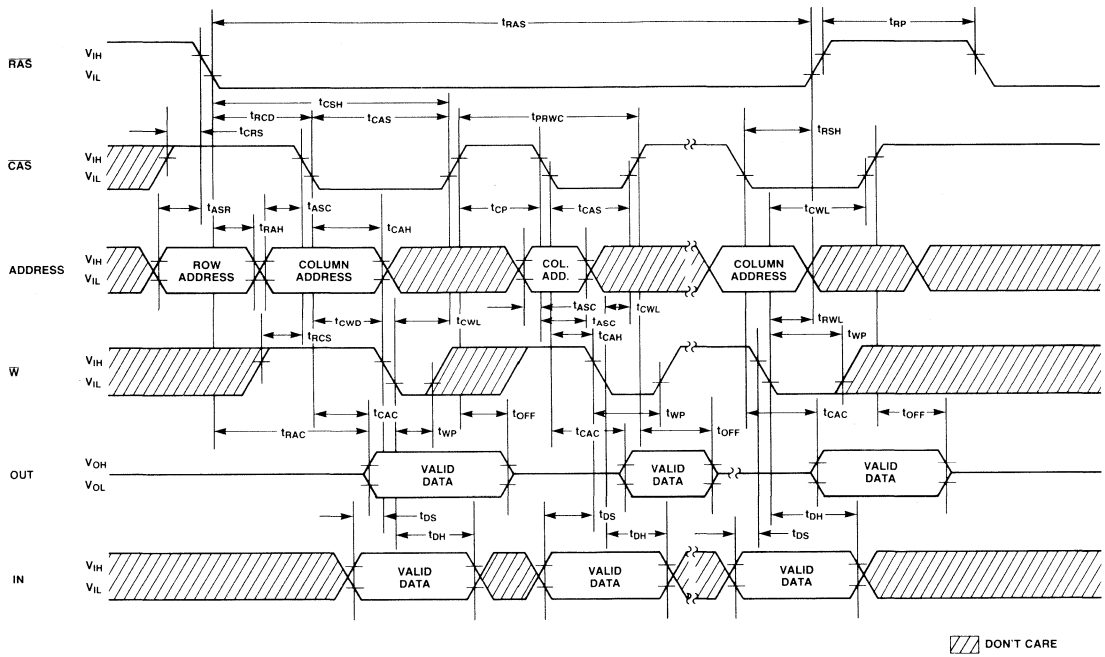
Timing Diagrams
(Continued)

Page Mode Read Cycle



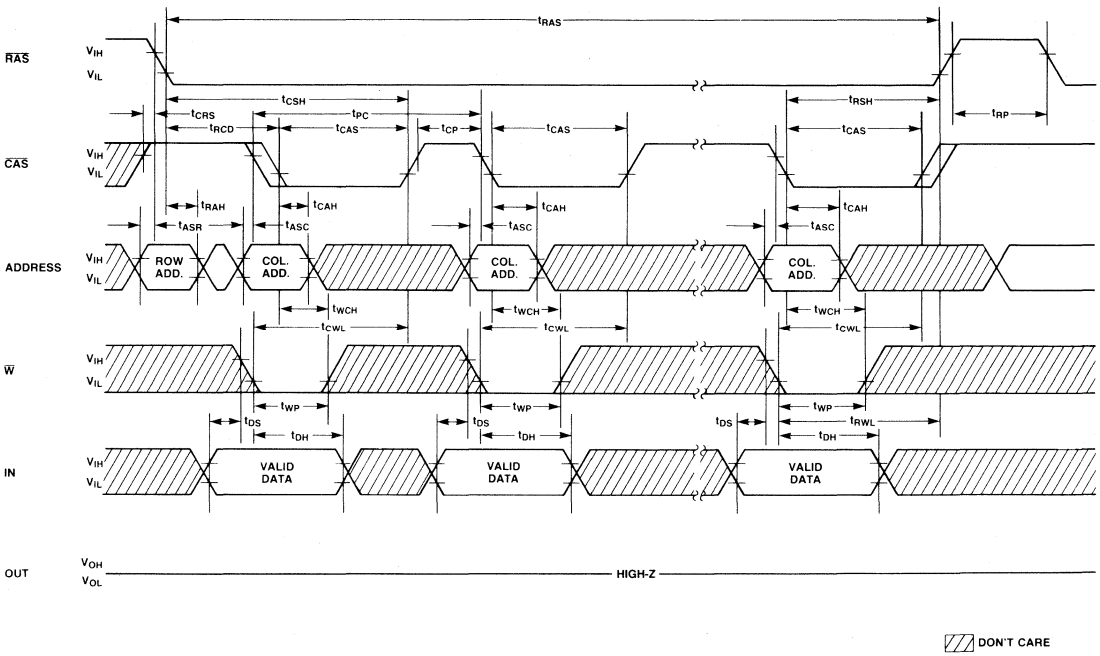
Timing Diagrams
(Continued)

Page Mode Read-Write Cycle



Timing Diagrams
(Continued)

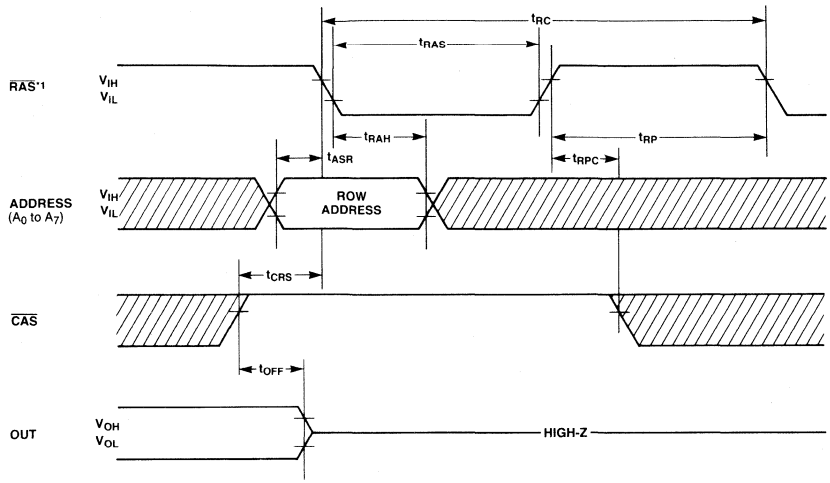
Page Mode Write Cycle



Timing Diagrams
(Continued)

$\overline{RAS}$-only Refresh Cycle

Note: $\overline{CAS}$ = V_{IH}, W, IN = Don't Care, A_8 = V_{IH} or V_{IL}

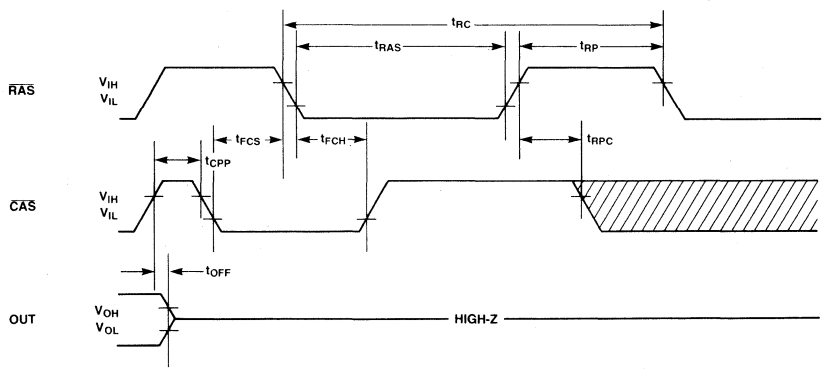


NOTE: *1 ANY COMBINATIONS OF $\overline{RAS}$0 TO $\overline{RAS}$3 ARE ALLOWED AND $\overline{RAS}$'s TO BE NOT REFRESHED ARE IN V_{IH}.

DON'T CARE

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

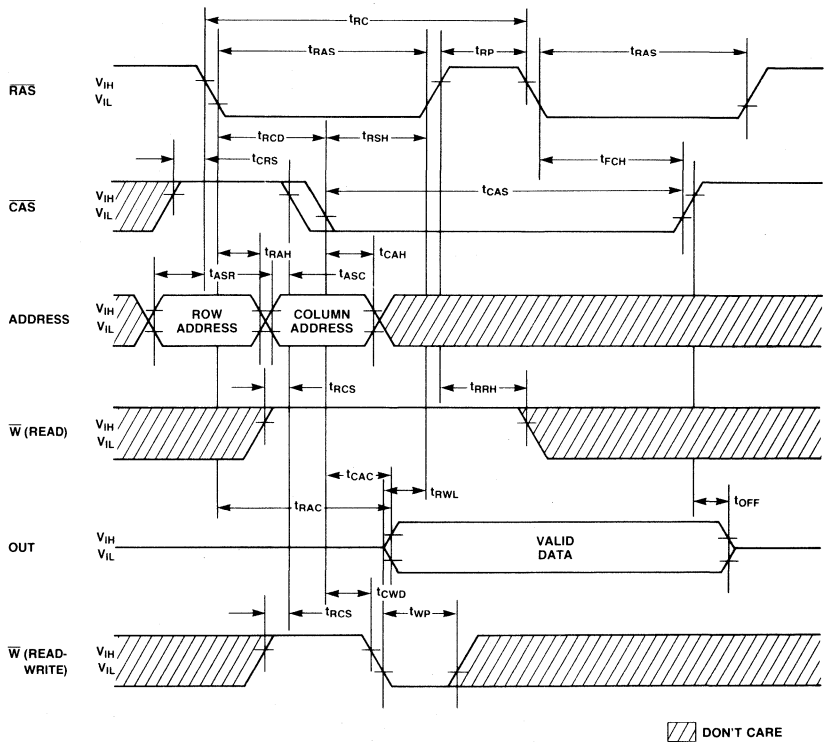
Note: Address, W, IN = Don't care



DON'T CARE

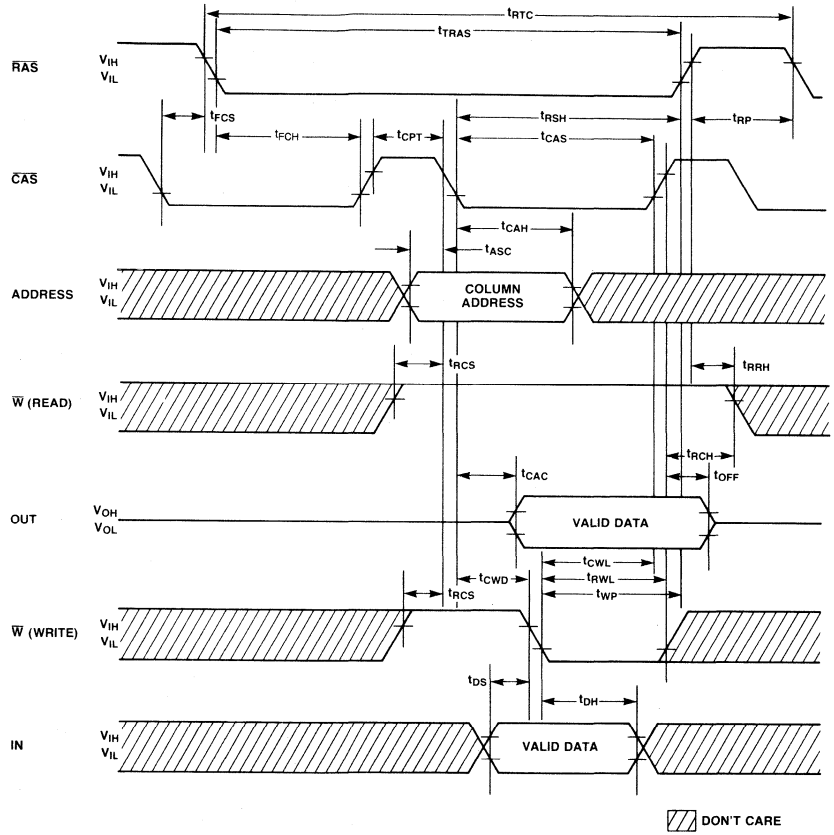
Timing Diagrams
(Continued)

Hidden Refresh Cycle



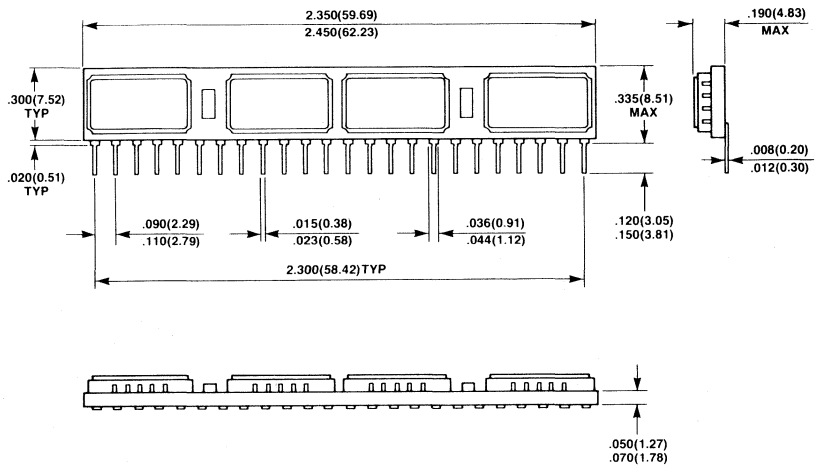
Timing Diagrams
(Continued)

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



Package Dimensions
Dimensions in inches
(millimeters)

24-Lead Single In-Line Package Module
(Module No.: MSP-24S-CC04)



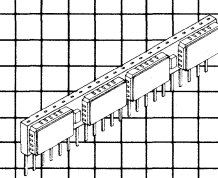
MB85208-12, MB85208-15

1,048,576 x 1-Bit Dynamic Random Access Memory SIP Module

Description

The Fujitsu MB85208 is a fully decoded, 1,048,576 word x 1-bit NMOS dynamic random access memory module consisting of four MB81257 DRAMs in 18-pad LCC packages mounted on a 22-pin multilayer ceramic substrate.

The MB85208 is intended for use in memory applications where large memory capacity is required within limited physical volume. Significant size reduction can be realized in applications such as mainframe memory, buffer memory, desk top computers and peripheral storage.



MSP-22S-CC03

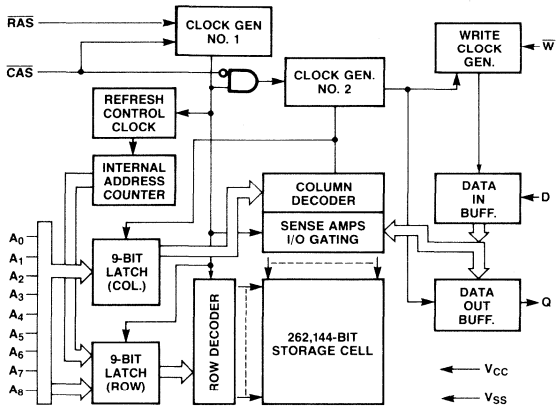
Features

- **1,048,576 x 1 DRAM 22-pin SIP (MB81257x4)**
- **Row access time 120 ns max. (MB85208-12) 150 ns max. (MB85208-15)**
- **Cycle time 230 ns min. (MB85208-12) 260 ns min. (MB85208-15)**
- **Nibble cycle time 65 ns min. (MB85208-12) 50 ns min. (MB85208-15)**
- **Single + 5V supply, ±10% tolerance**
- **Low power (active) 435 mW max. (MB85208-12) 390 mW max. (MB85208-15) 100 mW max. (standby)**
- **4 ms/256 refresh cycles capability**
- **$\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$ and Hidden refresh capability**
- **Read-Modify-Write and Nibble Mode Capability**
- **Common I/O capability using Early Write operation**
- **On-chip latches for Addresses and Data-in**
- **All inputs and outputs are TTL compatible.**

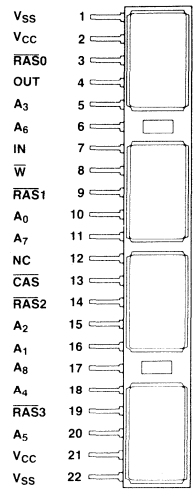
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB85208 Block Diagrams and Pin Assignments

Block Diagram for Each Chip



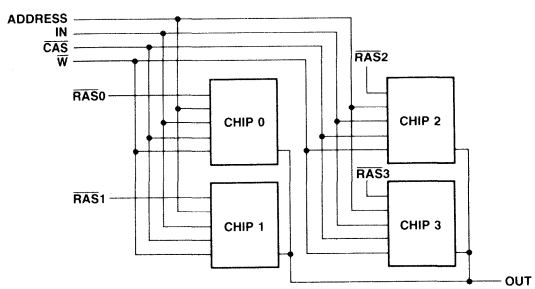
Pin Diagram



FUNCTIONAL TRUTH TABLE FOR EACH CHIP

RAS	CAS	W	IN	OUT	Read	Write	Refresh	Note
H	H	Don't Care	Don't Care	High-Z	No	No	No	Standby
L	L	H	Don't Care	Valid Data	Yes	No	Yes	Read
L	L	L	Valid Data	High-Z	No	Yes	Yes	Early Write $t_{WCS} \geq t_{WCS}$ (min)
L	L	L	Valid Data	Valid Data	Yes	Yes	Yes	Delayed Write or Read-Write $t_{CWD} \geq t_{CWD}$ (min)
L	H	Don't Care	Don't Care	High-Z	No	No	Yes	RAS-only Refresh
L	L	Don't Care	Don't Care	Valid Data	No	No	Yes	CAS-before-RAS Refresh Valid data selected at previous Read or Read-Write cycle is held
H	L	Don't Care	Don't Care	High-Z	No	No	No	CAS disturb

Functional Block Diagram



MB85208 Block Diagrams and Pin Assignments
(Continued)

FUNCTIONAL TRUTH TABLE FOR MODULE

$\overline{RAS0}$ to $\overline{RAS3}$	$\overline{CAS}$	$\overline{W}$	IN	OUT	Function
H	H	Don't Care	Don't Care	High-Z	Standby
L*1	L	H	Don't Care	Valid Data	Read cycle
L*1	L	L	Valid Data	High-Z	Write cycle
L*1	L	H→L*2	Valid Data	Valid Data	Read-write cycle
H→L*3	H→L*3	Don't Care	Don't Care	High-Z	$\overline{CAS}$-before-$\overline{RAS}$ Refresh cycle
L	H	Don't Care	Don't Care	High-Z	$\overline{RAS}$-only Refresh cycle

Notes: *1 It is for the selected $\overline{RAS}$, and other $\overline{RAS}$s are high.
*2 $t_{CWD} \geq t_{CWD}$ (min).
*3 $t_{FCS} \geq t_{FCS}$ (min).

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	2.4	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Description

Simple Timing Requirement

The MB85208 has improved circuitry that eases timing requirements for high speed access operations. The MB85208 can operate under the condition of t_{RCD} (max) = t_{CAC} thus providing optimal timing for address multiplexing. In addition, the MB85208 has the minimal hold times of address (t_{CAH}), W (t_{WCH}) and IN (t_{DH}). Fujitsu has made timing requirements that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the column address, IN and $\overline{W}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{W}$ Delay) are not restricted by t_{RCD}.

Address Inputs

A total of eighteen binary input address bits and four $\overline{RAS}$ clocks are required to decode any 1 of 1,048,576 locations within the MB85208. Nine row address bits are established on the input pins (A_0 through A_8) and latched with the $\overline{RAS}$ (one of $\overline{RAS0}$ to $\overline{RAS3}$) of the selected chip. Nine column address bits are established on the input pins and latched with $\overline{CAS}$. All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

$\overline{RAS0}$ to $\overline{RAS3}$

The MB85208 has four $\overline{RAS}$ inputs in order to select a chip within the MB85208. Other $\overline{RAS}$s except for one $\overline{RAS}$ to be selected must be high to avoid data conflict during read, delayed write or read-write cycles.

Write Enable

The read mode or write mode is selected with the $\overline{W}$ input. A high on the $\overline{W}$ selects read mode, a low selects write mode. Data input is disabled when read mode is selected.

Data Input

Data is written into the chip selected by $\overline{RAS}$ (one of $\overline{RAS0}$ to $\overline{RAS3}$) of MB85208 during a write or read-write cycle. The latter falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the IN register. In a write cycle, if $\overline{W}$ is brought low before the falling edge of $\overline{CAS}$, the set-up and hold times are referenced to $\overline{CAS}$. In a delayed write or read-write cycle, $\overline{W}$ can be low after $\overline{CAS}$ has already been low and $\overline{CAS}$ to $\overline{W}$ Delay time (t_{CWD}) has been satisfied (read-write cycle). Thus IN is strobed by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$.

Description
(Continued)

Data Output

The output buffer of each chip is three-state TTL compatible with a fan-out of two standard TTL loads. OUT is the same polarity as IN. The output is in high impedance state until $\overline{CAS}$ is brought low. In a read or read-write cycle, the output is valid after t_{RAC} from the falling edge of the selected $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from negative transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remains valid until $\overline{CAS}$ is returned to a high. In a write cycle, the identical sequence occurs but data is not valid.

Fast Read-While-Write Cycle

The MB85208 has a fast read-while-write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{W}$ when $\overline{CAS}$ goes low. When $\overline{W}$ is low during $\overline{CAS}$ transition to low, the MB85208 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. Whereas, when $\overline{W}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MB85208 goes into the delayed write mode. The output then contains the data from the cell selected and the data from IN are written into the cell selected. Therefore, a very fast read-write cycle ($t_{RC} = t_{RWC}$) is possible with the MB85208.

Nibble Mode

Nibble Mode allows high speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The data that will be accessed during nibble mode are determined by the 8 row and 8 column addresses. The 2 addresses (CA_8 and RA_8) are used to select 1 of 4 nibble bits for initial access. After the first bit is accessed by normal mode, the followed nibble bits will be accessed by toggling $\overline{CAS}$ high then low while $\overline{RAS}$ remains low. Toggling $\overline{CAS}$ causes RA_8 and CA_8 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on subsequent access, the new data will be written into the selected cells. In nibble mode, three-state control of OUT pin is determined by the first normal access cycle. The OUT is controlled only by the state of $\overline{W}$ strobed by the falling edge of $\overline{CAS}$ on the first nibble bit. That is when $t_{WCS} \geqslant t_{WCS}$ (min) is met, the OUT will remain high impedance throughout the succeeding nibble cycle regardless of $\overline{W}$ state. Whereas, when $t_{CWD} \geqslant t_{CWD}$ (min) is met the OUT will contain the accessed data during the succeeding nibble cycle regardless of $\overline{W}$ state. The write operation is done during $\overline{CAS}$ and $\overline{W}$ are low. Therefore, the write operation can be done bit by bit during each nibble operation regardless of the timing conditions of $\overline{W}$ (t_{WCS} and t_{CWD}) during the first nibble bit.

Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row addresses (A_0 through A_7) at least every 4 ms. During refresh, either V_{IL} or V_{IH} is permitted for A_8 and any combinations of $\overline{RAS0}$ to $\overline{RAS3}$ are allowed. When all chips are refreshed simultaneously, the average power dissipation of the module must be less than 640 mW at any 100 ms interval.

The MB85208 offers the following three types of refresh.

1) $\overline{RAS}$-Only Refresh;
$\overline{RAS}$-only refresh avoids any output data during refresh because the output buffer is in high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 row addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed.
2) $\overline{CAS}$-before-$\overline{RAS}$ Refresh;
$\overline{CAS}$-before-$\overline{RAS}$ refresh available on the MB85208 offers an alternate refresh method. If $\overline{CAS}$ is brought low before the specified period, $\overline{CAS}$ Set Up Time Referenced to $\overline{RAS}$ (t_{FCS}) has been satisfied before the falling edge of $\overline{RAS}$, on chip refresh control clock generators and the refresh address counter for each chip are enabled, and an internal refresh operation take place. After the refresh operation has been executed the refresh address counter is automatically incremented for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.
3) Hidden Refresh;
Hidden refresh may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. In the MB85208, hidden refresh means $\overline{CAS}$-before-$\overline{RAS}$ refresh and the internal refresh address is used; that is, no refresh address is needed.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes into high and goes into low again while $\overline{RAS}$ is held low, the read and write operation are enabled. This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell address (consisting of a row address (9 bits) and a column address (9 bits)) to be accessed, can be defined as follows:

1) A ROW ADDRESS—Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set high internally.
2) A COLUMN ADDRESS—All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of $\overline{CAS}$.

Description
(Continued)

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

1) Initialize the internal refresh counter. For this operation, the 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
2) Write a test pattern of lows into memory cells at a single column address and 256 row addresses.
3) By using read-modify-write cycle, read the lows written at the last step and write a new high in the same cycle. This cycle is repeated 256 times, and highs are written into the 256 memory cells.
4) Read the high written at the last step.
5) Compliment the test pattern and repeat the steps 2, 3 and 4.
6) Repeat steps 2 through 5 for another 3 chips.

Nibble Mode Address Sequence Example

SEQUENCE	NIBBLE BIT	RA_S	ROW ADDRESS	CA_S	COLUMN ADDRESS	
$\overline{RAS}$/$\overline{CAS}$ (normal mode)	1	0	10101010	0	10101010	input address
toggle $\overline{CAS}$ (nibble mode)	2	1	10101010	0	10101010	
toggle $\overline{CAS}$ (nibble mode)	3	0	10101010	1	10101010	generated internally
toggle $\overline{CAS}$ (nibble mode)	4	1	10101010	1	10101010	
toggle $\overline{CAS}$ (nibble mode)	1	0	10101010	0	10101010	sequence repeats

Decoupling and Noise Reduction Recommendations for MB85208

To minimize noise induction between signal lines as well as between signal and power supply lines, good board design practice requires consideration of the following:

1) Provide a capacitor of approx. a few μF for each module—even though the MB85208 has two or four decoupling capacitors of 0.5 μF on each module.
2) Remove noise, overshoot and undershoot from the address, control and data-input lines, so that the MB85208 won't latch wrong signals due to the noise induction between signal lines, and between signal and power supply lines.
3) Keep enough timing margin and remove critical timing in the board design to avoid the problem mentioned in Item 2 above.
4) In order to avoid noise induction on the IN line at the falling edge of $\overline{W}$ when the delayed write or read-modify-write cycle is used, the falling edge of $\overline{W}$ signal should not coincide with the transition point of address and OUT signals. Since decoupling capacitors on the module board can't smooth the output current at the OUT pin, noise is introduced on the power supply line (V_{CC} or V_{SS}) and also on the IN line at t_{RAC} or t_{CAC} in the read cycle.
5) Provide an appropriate damping if necessary, to avoid excessive overshoot or undershoot on the TTL input waveform.

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.4		6.5	V	0°C to +70°C
Input low voltage	V_{IL}	−2.0		0.8	V	

Capacitance
(T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input capacitance A_0 through A_8, IN, $\overline{W}$	C_{IN1}		50	pF
Input capacitance $\overline{RAS}$0 through $\overline{RAS}$3	C_{IN2}		15	pF
Input capacitance $\overline{CAS}$	C_{IN3}		65	pF
Output capacitance OUT	C_{OUT}		55	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB85208-12 Min	MB85208-12 Max	MB85208-15 Min	MB85208-15 Max	Unit
Operating current*1 Average power supply current (one $\overline{RAS}$*2, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		79		71	mA
Standby current Standby power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		18		18	mA
Refresh current 1*1,4 Average power supply current ($\overline{CAS}$ = V_{IH}, all $\overline{RAS}$ cycling; t_{RC} = min)	I_{CC3}		220		200	mA
Nibble mode current*1 Average power supply current (one $\overline{RAS}$*3 = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min)	I_{CC4}		34		32	mA
Refresh current 2*4 Average power supply current (all $\overline{RAS}$ cycling, $\overline{CAS}$-before-$\overline{RAS}$)	I_{CC5}		240		220	mA
Input leakage current Any input (0 ≤ V_{IN} ≤ 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)	$I_{I(L)}$	−40	40	−40	40	μA
Output leakage current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	$I_{O(L)}$	−40	40	−40	40	μA
Output levels Output high voltage (I_{OH} = −5 mA) Output low voltage (I_{OL} = 4.2 mA)	V_{OH} V_{OL}	2.4	 0.4	2.4	 0.4	V

Notes: *1 I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
*2 The selected $\overline{RAS}$ is cycling and other $\overline{RAS}$s are in V_{IH}.
*3 The selected $\overline{RAS}$ is in V_{IL} and other $\overline{RAS}$s are in V_{IH}.
*4 When all chips are refreshed simultaneously, the average power dissipation of the module must be less than 640 mW at any 100 ms interval.

AC Characteristics[*1,2,3]
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB85208-12 Min	MB85208-12 Max	MB85208-15 Min	MB85208-15 Max	Unit
Time between refresh	t_{REF}		4		4	ns
Random read/write cycle time	t_{RC}	230		260		ns
Read-write-cycle time	t_{RWC}	230		260		ns
Access time from $\overline{RAS}$[*4,6]	t_{RAC}		120		150	ns
Access time from $\overline{CAS}$[*5,6]	t_{CAC}		60		75	ns
Output buffer turn off delay	t_{OFF}	0	25	0	30	ns
Transition time	t_T	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	100		100		ns
$\overline{RAS}$ pulse width	t_{RAS}	120	10000	150	10000	ns
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns
$\overline{CAS}$ pulse width	t_{CAS}	60	10000	75	10000	ns
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ delay time[*7,8]	t_{RCD}	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ set up time	t_{CRS}	20		20		ns
Row address set up time	t_{ASR}	0		0		ns
Row address hold time	t_{RAH}	12		15		ns
Column address set up time	t_{ASC}	0		0		ns
Column address hold time	t_{CAH}	20		25		ns
Read command set up time	t_{RCS}	0		0		ns
Read command hold time referenced to $\overline{CAS}$[*10]	t_{RCH}	0		0		ns
Read command hold time referenced to $\overline{RAS}$[*10]	t_{RRH}	20		20		ns
Write command set up time	t_{WCS}	0		0		ns
Write command hold time	t_{WCH}	20		25		ns
Write command pulse width	t_{WP}	20		25		ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	50		60		ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	30		40		ns
Data in set up time	t_{DS}	0		0		ns
Data in hold time	t_{DH}	20		25		ns

Notes:
- *1 An initial pause of 200 μs is required after power-up. And then several cycles of all $\overline{RAS}$'s (to which any 8 cycles to perform refresh are adequate) are required before proper device operation is achieved. If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
- *2 AC characteristics assume t_T = 5 ns.
- *3 V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
- *4 Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
- *5 Assumes that $t_{RCD} \geq t_{RCD}$ (max).
- *6 Measured with a load equivalent to 2 TTL loads and 100 pF.
- *7 Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
- *8 t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T = 5 ns) + t_{ASC} (min).
- *10 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

AC Characteristics[*1,2,3] (Continued) (Recommended operating conditions unless otherwise noted.)

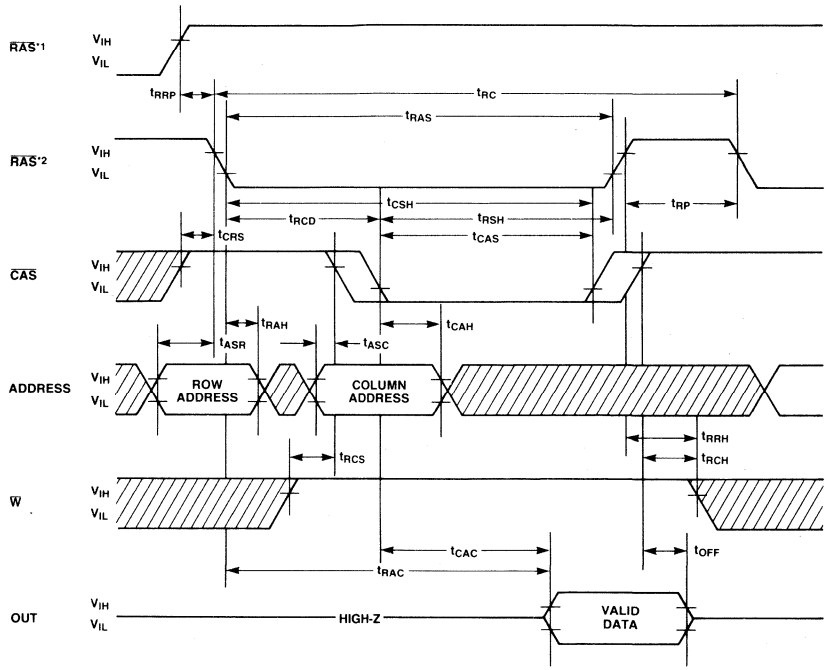
Parameter	Symbol	MB85208-12 Min	MB85208-12 Max	MB85208-15 Min	MB85208-15 Max	Unit
$\overline{CAS}$ to $\overline{W}$ delay[*9]	t_{CWD}	20		25		ns
$\overline{CAS}$ set up time referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)	t_{FCS}	25		30		ns
$\overline{CAS}$ hold time referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)	t_{FCH}	25		30		ns
$\overline{RAS}$ precharge to $\overline{CAS}$ active time ($\overline{CAS}$-before-$\overline{RAS}$)	t_{RPC}	20		20		ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CPR}	25		30		ns
Nibble mode read/write cycle time	t_{NC}	65		80		ns
Nibble mode read-write cycle time	t_{NRWC}	65		80		ns
Nibble mode access time	t_{NCAC}		30		40	ns
Nibble mode $\overline{CAS}$ pulse width	t_{NCAS}	30		40		ns
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	25		30		ns
Nibble mode read $\overline{RAS}$ hold time	t_{NRRSH}	30		40		ns
Nibble mode write $\overline{RAS}$ hold time	t_{NWRSH}	60		60		ns
Refresh counter test cycle time[*11]	t_{RTC}	375		430		ns
Refresh counter test $\overline{RAS}$ pulse width[*11]	t_{TRAS}	265	10000	320	10000	ns
Refresh counter test $\overline{CAS}$ precharge time[*11]	t_{CPT}	60		70		ns
Nibble mode $\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{RNH}	20		20		ns
$\overline{RAS}$ to $\overline{RAS}$ precharge time	t_{RRP}	0		0		ns

Notes: *9 t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.

*11 Refresh counter test cycle only.

Timing Diagrams

Read Cycle

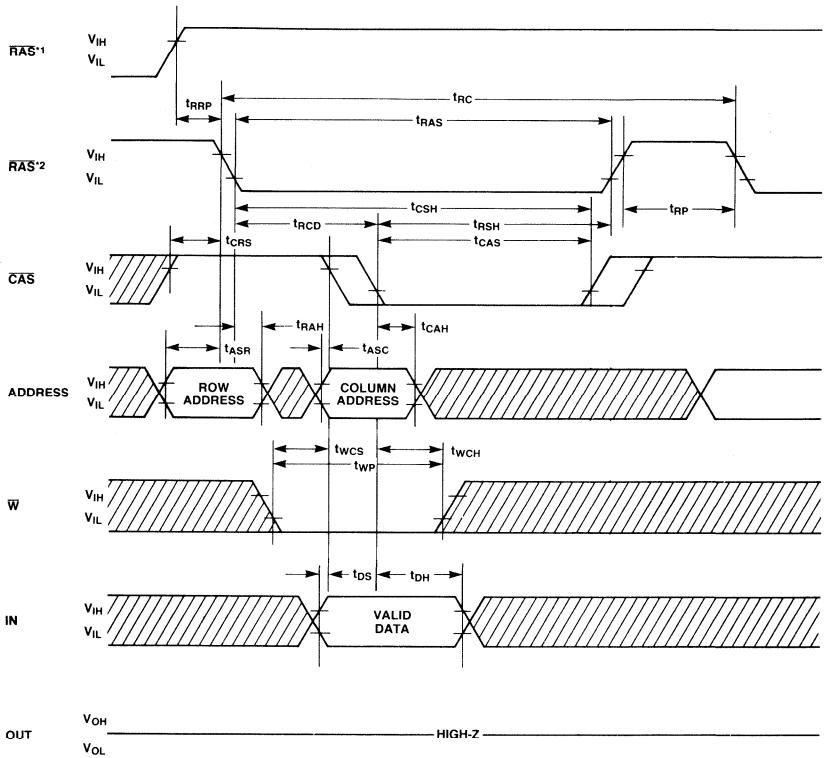


NOTES: *1 IT IS FOR UNSELECTED $\overline{RAS}$.
*2 IT IS FOR THE SELECTED $\overline{RAS}$.

DON'T CARE

Timing Diagrams
(Continued)

Write Cycle (Early Write)

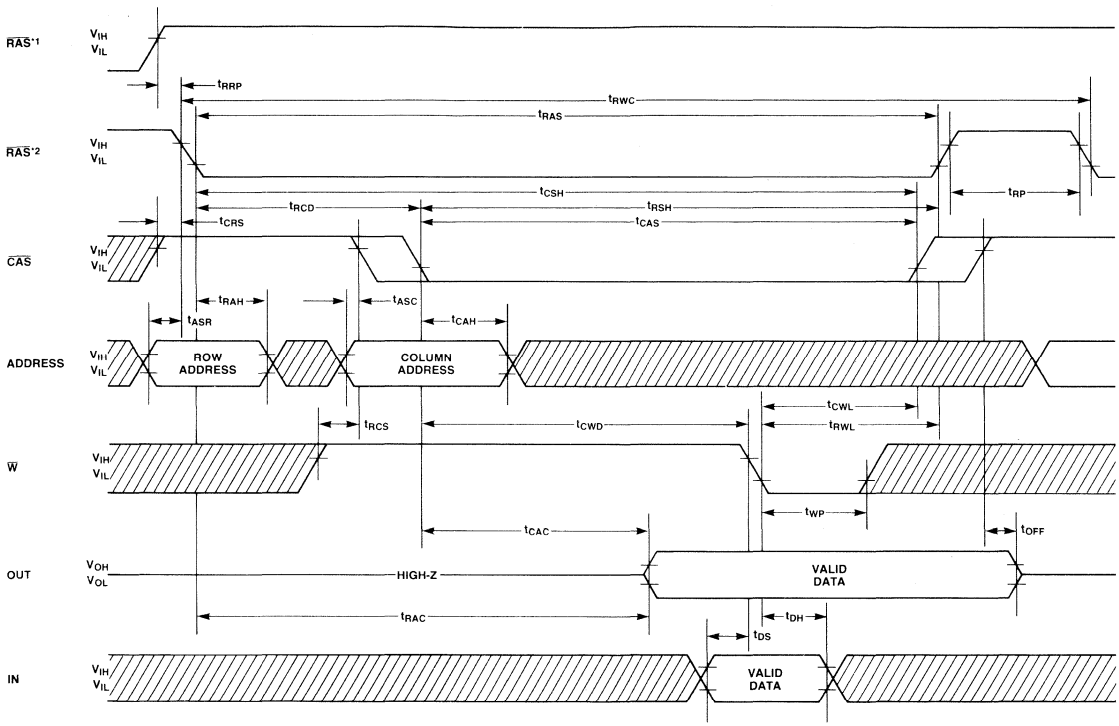


NOTES: *1 IT IS FOR UNSELECTED $\overline{RAS}$.
*2 IT IS FOR THE SELECTED $\overline{RAS}$.

DON'T CARE

Timing Diagrams
(Continued)

Read-Write/Read-Modify-Write Cycle



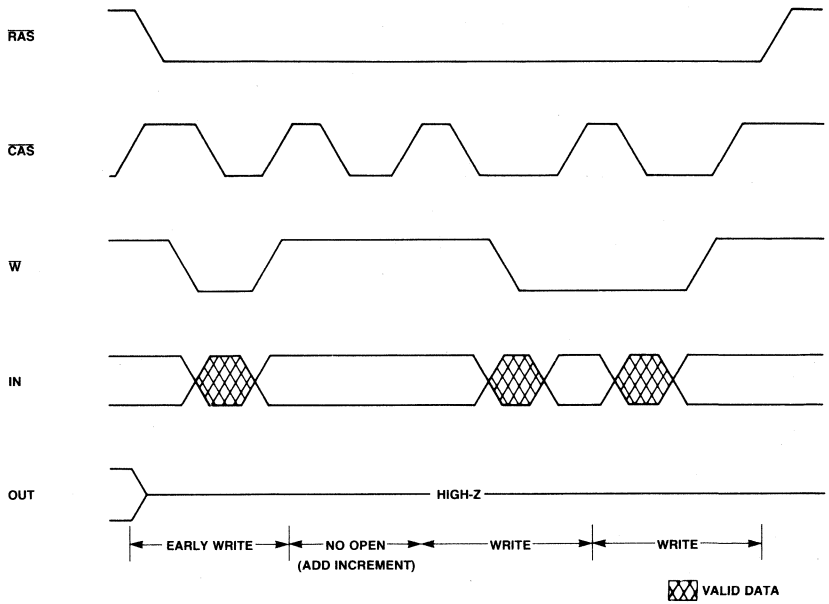
NOTES: *1 IT IS FOR UNSELECTED $\overline{RAS}$.
*2 IT IS FOR THE SELECTED $\overline{RAS}$.

DON'T CARE

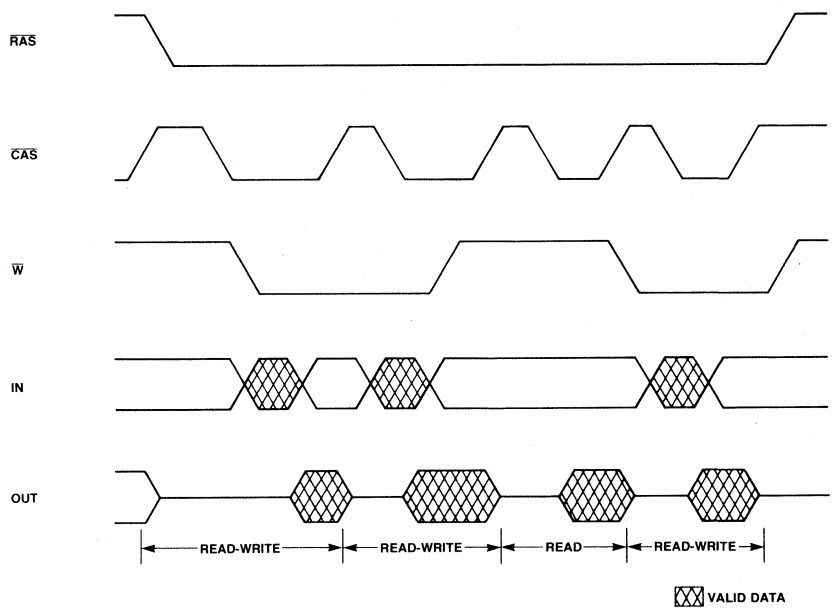
Timing Diagrams
(Continued)

Nibble Mode

*1 THE CASE OF FIRST NIBBLE CYCLE IS EARLY WRITE

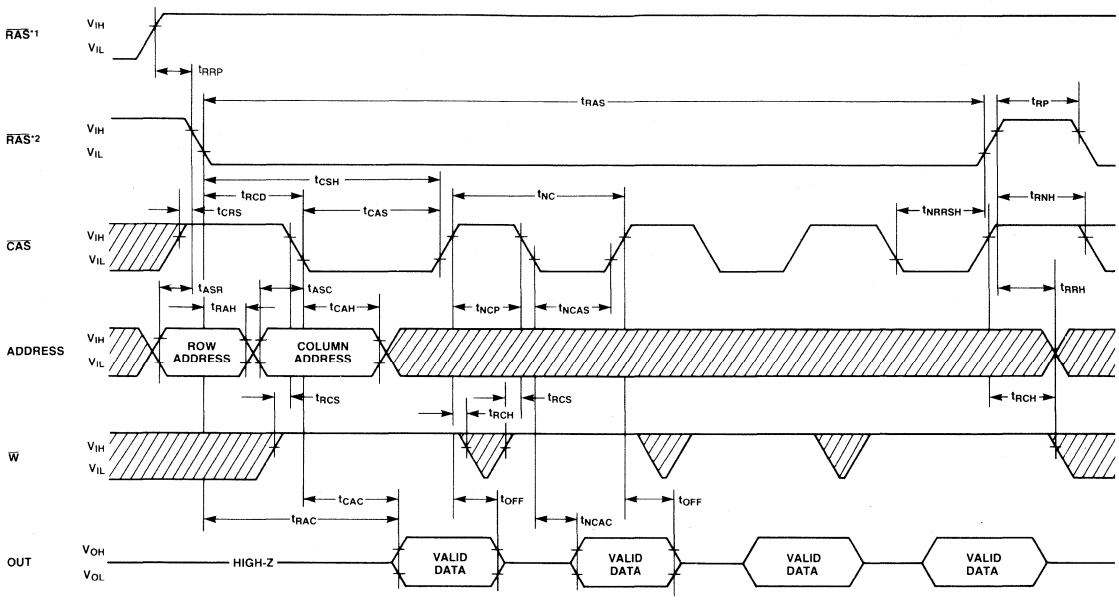


*2 THE CASE OF FIRST NIBBLE CYCLE IS DELAYED WRITE (READ-WRITE)



Timing Diagrams
(Continued)

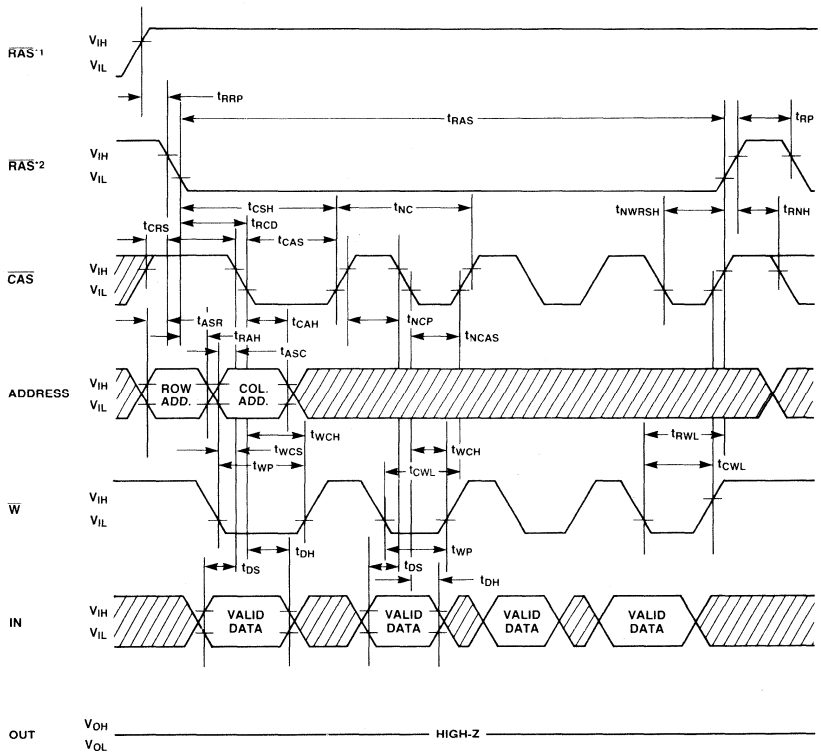
Nibble Mode Read Cycle



NOTES: *1 IT IS FOR UNSELECTED $\overline{RAS}$.
*2 IT IS FOR THE SELECTED $\overline{RAS}$.

Timing Diagrams
(Continued)

Nibble Mode Write Cycle

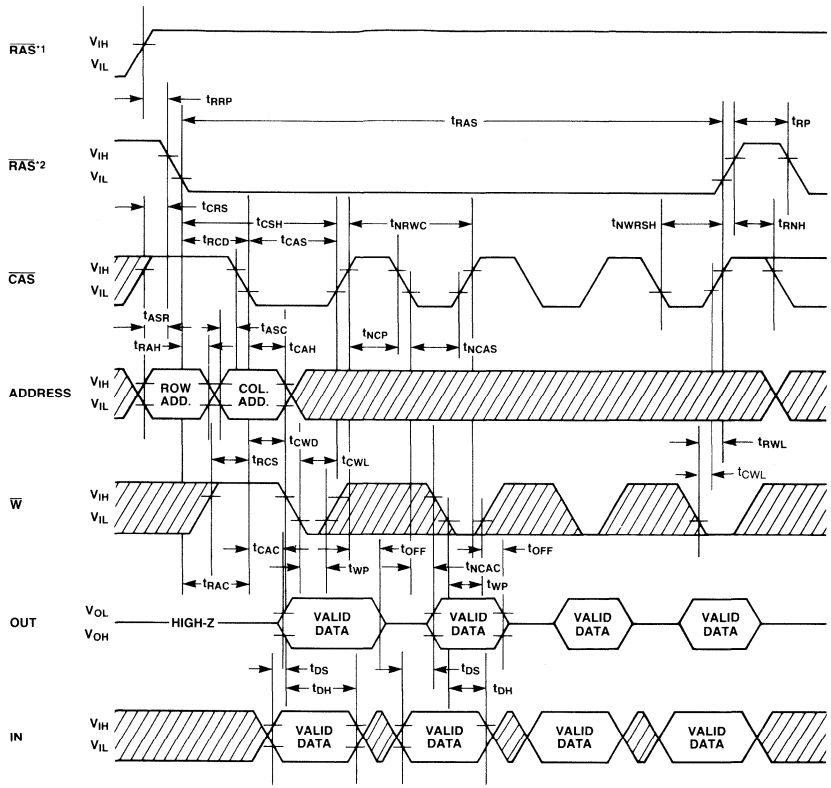


NOTES: *1 IT IS FOR UNSELECTED $\overline{RAS}$.
*2 IT IS FOR THE SELECTED $\overline{RAS}$.

DON'T CARE

Timing Diagrams
(Continued)

Nibble Mode Read-Write Cycle

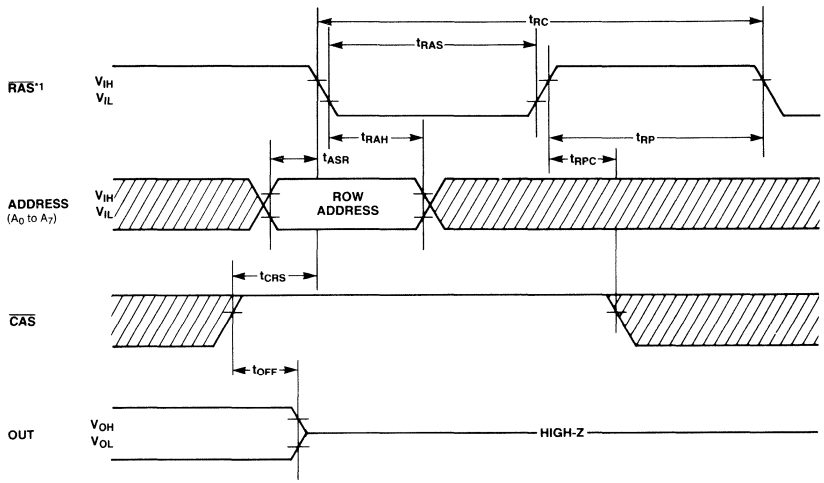


NOTES: *1 IT IS FOR UNSELECTED $\overline{RAS}$.
*2 IT IS FOR THE SELECTED $\overline{RAS}$.

Timing Diagrams
(Continued)

$\overline{RAS}$-only Refresh Cycle

Note: A_8 = V_{IH} or V_{IL}, $\overline{W}$, IN = Don't care

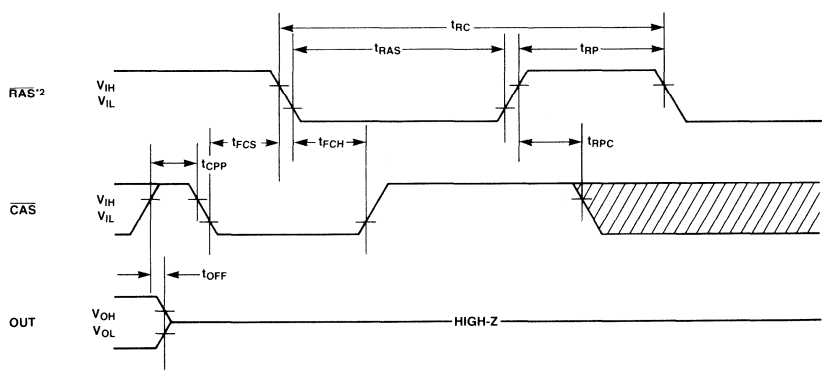


NOTE: *1 ANY COMBINATIONS OF $\overline{RAS}$0 TO $\overline{RAS}$3 ARE ALLOWED AND $\overline{RAS}$'s TO BE NOT REFRESHED ARE IN V_{IH}.

DON'T CARE

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

Note: Address, $\overline{W}$, IN = Don't care

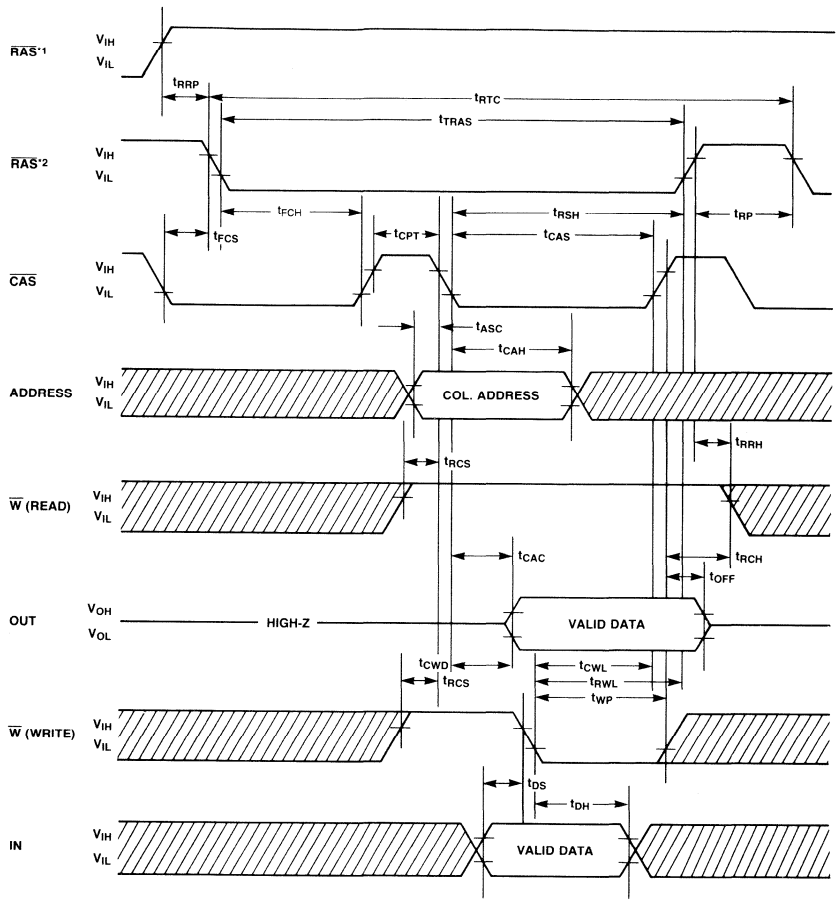


NOTE: *1 ANY COMBINATIONS OF $\overline{RAS}$0 TO $\overline{RAS}$3 ARE ALLOWED AND $\overline{RAS}$'s TO BE NOT REFRESHED ARE IN V_{IH}.

DON'T CARE

Timing Diagrams
(Continued)

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

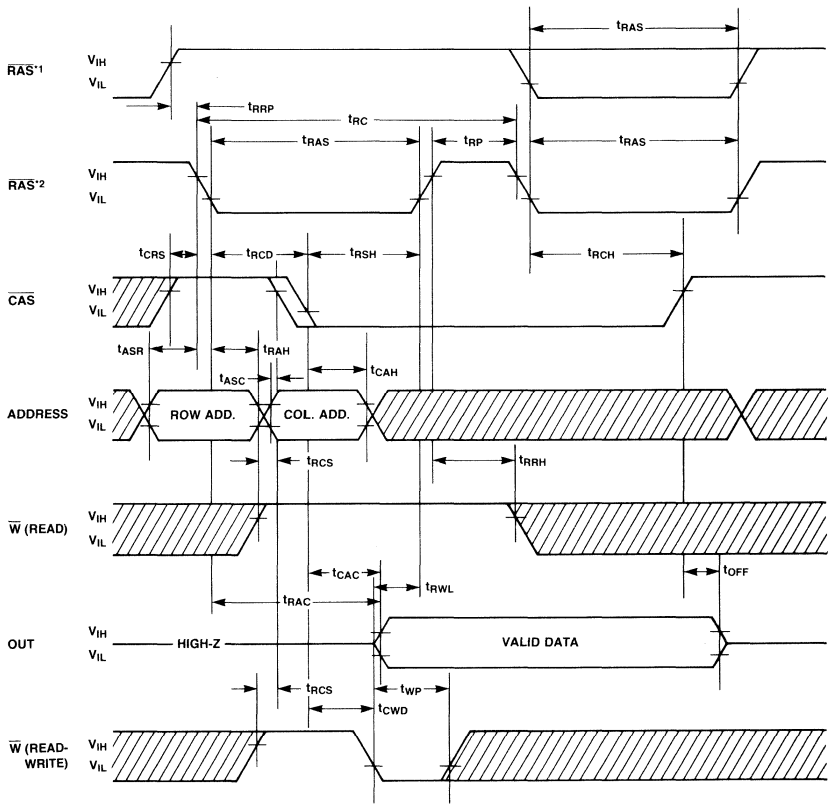


NOTES: *1 IT IS FOR UNSELECTED $\overline{RAS}$.
*2 IT IS FOR THE SELECTED $\overline{RAS}$.

DON'T CARE

Timing Diagrams
(Continued)

Hidden Refresh Cycle

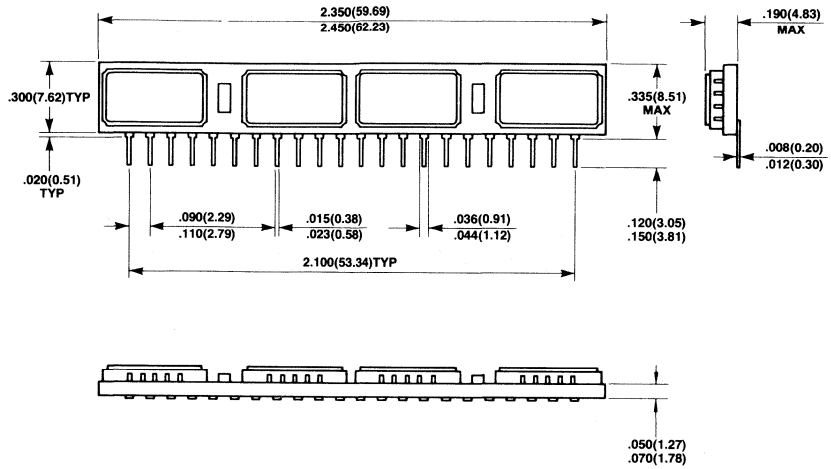


NOTES: *1 IT IS FOR UNSELECTED $\overline{RAS}$.
*2 IT IS FOR THE SELECTED $\overline{RAS}$.

DON'T CARE

Package Dimensions
Dimensions in Inches
(millimeters)

22-Lead Single In-Line Package Module
(Module No.: MSP-22S-CC03)



Preliminary

MOS Memories

FUJITSU

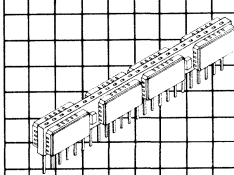
■ MB85210-12, MB85210-15

524,288 x 4-Bit Dynamic
Random Access Memory
SIP Module

Description

The Fujitsu MB85210 is a fully decoded, 524,288 word x 4-bit NMOS dynamic random access memory module consisting of eight MB81257 DRAMs in 18-pad LCC packages mounted on a 24-pin multilayer ceramic substrate.

The MB85210 is intended for use in memory applications where large memory capacity is required within limited physical volume. Significant size reduction can be realized in applications such as mainframe memory, buffer memory, desk top computers and peripheral storage.



MSP-24S-CC02

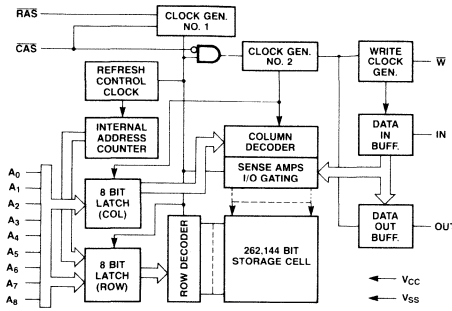
Features

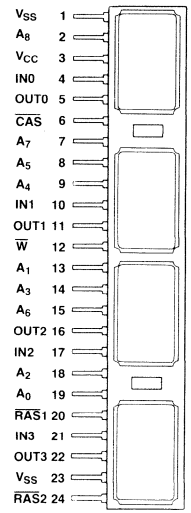
- **524,288 x 4 DRAM, 24 pin SIP (MB81257x8)**
- **Row access time**
  120 ns max. (MB85210-12)
  150 ns max. (MB85210-15)
- **Cycle time**
  230 ns min. (MB85210-12)
  260 ns min. (MB85210-15)
- **Nibble cycle time**
  65 ns min. (MB85210-12)
  80 ns min. (MB85210-15)
- **Single + 5V supply, ±10% tolerance**
- **Low power (active)**
  1529 mW max. (MB85210-12)
  1353 mW max. (MB85210-15)
  198 mW max. (standby)
- **256/4 ms refresh cycles capability**
- **$\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$ and Hidden refresh capability**
- **Read-Modify-Write and Nibble Mode capability**
- **Common I/O capability using Early Write operation**
- **On-chip latches for Addresses and Data-in**
- **All inputs and outputs are TTL compatible**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

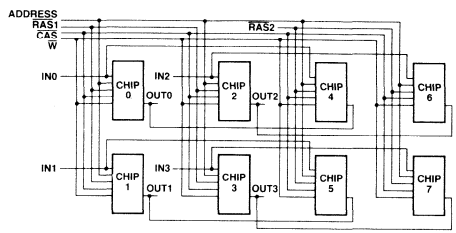
MB85210 Block Diagrams and Pin Assignment

Block Diagram for Each Chip





Functional Block Diagram



FUNCTIONAL TRUTH TABLE FOR EACH CHIP

RAS	CAS	W	IN	OUT	Read	Write	Refresh	Note
H	H	Don't Care	Don't Care	High-Z	No	No	No	Standby
L	L	H	Don't Care	Valid Data	Yes	No	Yes	Read
L	L	L	Valid Data	High-Z	No	Yes	Yes	Early Write $t_{WCS} \geq t_{WCS}$ (min)
L	L	L	Valid Data	Valid Data	Yes	Yes	Yes	Delayed Write or Read-Write $t_{CWD} \geq t_{CWD}$ (min)
L	H	Don't Care	Don't Care	High-Z	No	No	Yes	RAS-only Refresh
L	L	Don't Care	Don't Care	Valid Data	No	No	Yes	CAS-before-RAS Refresh Valid data selected at previous Read or Read-Write cycle is held
H	L	Don't Care	Don't Care	High-Z	No	No	No	CAS disturb

FUNCTIONAL TRUTH TABLE FOR MODULE

RAS1 and RAS2	CAS	WE	D_{IN1} to D_{IN3}	D_{OUT1} to D_{OUT3}	Function
H	H	Don't Care	Don't Care	High-Z	Standby
L[1)]	L	H	Don't Care	Valid Data	Read Cycle
L[1)]	L	L[2)]	Valid Data	High-Z	Write Cycle
L[1)]	L	H → L[3)]	Valid Data	Valid Data	Read-Write Cycle
L	H	Don't Care	Don't Care	High-Z	RAS-Only Refresh
L	L[4)]	Don't Care	Don't Care	High-Z	CAS-before-RAS Refresh

Notes 1): It is for the selected RAS, and other RAS is high.
2): $t_{WCS} \geq t_{WCS}$ (min).
3): $t_{CWD} \geq t_{CWD}$ (min).
4): $t_{FCS} \geq t_{FCS}$ (min).

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	8.0	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Description

Simple Timing Requirement

The MB85210 has improved circuitry that eases timing requirements for high speed access operations. The MB85210 can operate under the condition of t_{RCD} (max) = t_{CAC} thus providing optimal timing for address multiplexing. In addition, the MB85210 has the minimal hold times of address (t_{CAH}), $\overline{W}$ (t_{WCH}) and IN (t_{DH}). Fujitsu has made timing requirements that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the column address, IN and $\overline{W}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{W}$ Delay) are not restricted by t_{RCD}.

Address Inputs

A total of eighteen binary input address bits are required to decode any 4-bits of data in 524,288 locations within the MB85210. Nine row address bits are established on the input pins (A_0 through A_8) and latched with the Row Address Strobe ($\overline{RAS1}$ or $\overline{RAS2}$). $\overline{RAS1}$ and $\overline{RAS2}$ are respectively applied to the lower 262,144 addresses and the upper 262,144 addresses. Nine column address bits are established on the input pins and latched with $\overline{CAS}$. All input addresses must be stable on or before the falling edge of $\overline{RAS}$. If the lower 262,144 addresses are used, it is applied to $\overline{RAS1}$ and if the upper 262,144 addresses are used, it is applied to $\overline{RAS2}$. $\overline{CAS}$ is internally inhibited by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

$\overline{RAS1}$ and $\overline{RAS2}$

The MB85210 has $\overline{RAS1}$ and $\overline{RAS2}$ inputs in order to select all 524,288 x 4 locations using eighteen address inputs. $\overline{RAS1}$ is used to select the lower 262,144 x 4 locations and $\overline{RAS2}$ is used to select the upper 252,144 x 4 locations. In the read, delayed write or read-write cycle, $\overline{RAS1}$ and $\overline{RAS2}$ must not be low simultaneously in order to avoid data conflict.

Write Enable

The read mode or write mode is selected with the $\overline{W}$ input. A high on the $\overline{W}$ selects read mode, low selects write mode. Data inputs are disabled when read mode is selected.

Data Inputs

The 4-bit data is written into the MB85210 during a write or read-write cycle. The latter falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the IN register. In a write cycle, if $\overline{W}$ is brought low before the negative transition of $\overline{CAS}$, the set-up and hold times are referenced to $\overline{CAS}$. In a delayed write or read-write cycle, $\overline{W}$ will be low after $\overline{CAS}$ has already gone low. Thus IN0 to IN3 are strobed by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$.

Data Outputs

The output buffers of each chip are three-state TTL compatible with a fan-out of two standard TTL loads. OUT is the same polarity as IN. The output is in high impedance state until $\overline{CAS}$ is brought low. In a read or read-write cycle, the output is valid after t_{RAC} from negative transition of the $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from negative transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to a high. In a write cycle, the identical sequence occurs but data is not valid.

Fast Read-While-Write Cycle

The MB85210 has a fast read-while-write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{W}$ when $\overline{CAS}$ goes low. When $\overline{W}$ is low during $\overline{CAS}$ transition to low, the MB85210 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. Whereas, when $\overline{W}$ goes low after T_{CWD} following $\overline{CAS}$ transition to low, the MB85210 goes into the delayed write mode. The output then contains the data from the cell selected and the data from IN is written into the cell selected. Therefore, a very fast read write cycle (t_{RC} = t_{RWC}) is possible with the MB85210.

Description
(Continued)

Nibble Mode

Nibble Mode allows high speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The data that will be accessed during nibble mode is determined by the 8 row and 8 column addresses. The 2 addresses (CA_8, RA_8) are used to select 1 of 4 nibble bits for initial access. After the first bit is accessed by normal mode, the following nibble bits can be accessed by toggling $\overline{CAS}$ high then low while $\overline{RAS}$ remains low. Toggling $\overline{CAS}$ causes RA_8 and CA_8 to be incremented internally while all other address bits are held constant. This accesses the next nibble bit in sequence. If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on subsequent access, the new data will be written into the selected cells. In the nibble mode, three-state control of OUT pin is determined by the first normal access cycle. The OUT is controlled only by the state of $\overline{W}$ referenced at negative transition of $\overline{CAS}$ on the first nibble bit. That is, when $t_{WCS} \geq t_{WCS}$ (min) is met, the OUT will remain open throughout the succeeding nibble cycle regardless of $\overline{W}$ state. Whereas, when $t_{CWD} \geq t_{CWD}$ (min) is met the OUT will contain the accessed data during the succeeding nibble cycle regardless of $\overline{W}$ state. The write operation is done during the time $\overline{CAS}$ and $\overline{W}$ are low. Therefore, the write operation can be done bit by bit during each nibble operation regardless of the timing conditions of $\overline{W}$ (t_{WCS} and t_{CWD}) during the first nibble bit.

Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row addresses (A_0 through A_7) for each chip at least every 4 ms. During refresh, either V_{IL} or V_{IH} is permitted for A_8 and any combinations of $\overline{RAS}1$ and $\overline{RAS}2$ are allowed. When all chips are refreshed simultaneously, the average power dissipation of the module must be less than 640 mW at any 100 ms interval.

The MB85210 offers the following three types of refresh.

1) $\overline{RAS}$-Only Refresh;
   $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 row addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Both $\overline{RAS}1$ and $\overline{RAS}2$ can be refreshed simultaneously under the specified power dissipation limit.
2) $\overline{CAS}$-before-$\overline{RAS}$ Refresh;
   $\overline{CAS}$-before-$\overline{RAS}$ refresh available on the MB85210 offers an alternate refresh method. If $\overline{CAS}$ is held low for the specified period (t_{FCS}) before $\overline{RAS}$ goes low, on chip refresh control clock generators and the refresh address counter for each chip are enabled, and an internal refresh operation takes place. After the refresh operation has been executed the refresh address counter is automatically incremented for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.
3) Hidden Refresh;
   Hidden refresh may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. In MB85210, hidden refresh means $\overline{CAS}$-before-$\overline{RAS}$ refresh and the internal refresh addresses are used, that is, no external refresh address is needed. In hidden refresh, $\overline{RAS}1$ and $\overline{RAS}2$ cannot be refreshed at the same time because of data conflict.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then goes low again while $\overline{RAS}$ is held low, the read and write operations are enabled. This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell address (consisting of a row address (9 bits) and a column address (9 bits)) to be accessed can be defined as follows:

1) A ROW ADDRESS—Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set high internally.
2) A COLUMN ADDRESS—All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Procedure

The timing, as shown in $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle, is used for all operations described as follows:

1) Initialize the internal refresh counter. For this operation, the 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
2) Write a test pattern of lows into memory cells at a single column address and 256 row addresses.
3) By using read-modify-write cycle, read the lows written at the last step and write a new high in the same cycle. This cycle is repeated 256 times, and highs are written into the 256 memory cells.
4) Read the high written at the last step.
5) Compliment the test pattern and repeat the steps 2, 3 and 4.

Description
(Continued)

Nibble Mode Address Sequence Example

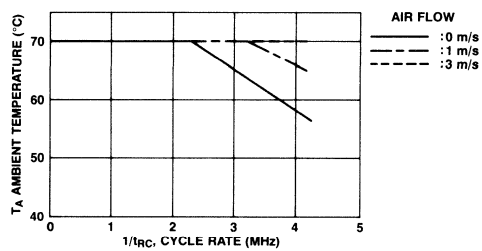
SEQUENCE	NIBBLE BIT	RA_8	ROW ADDRESS	CA_8	COLUMN ADDRESS	
$\overline{RAS}$/$\overline{CAS}$ (normal mode)	1	0	10101010	0	10101010	input address
toggle $\overline{CAS}$ (nibble mode)	2	1	10101010	0	10101010	
toggle $\overline{CAS}$ (nibble mode)	3	0	10101010	1	10101010	generated internally
toggle $\overline{CAS}$ (nibble mode)	4	1	10101010	1	10101010	
toggle $\overline{CAS}$ (nibble mode)	1	0	10101010	0	10101010	sequence repeats

Decoupling and Noise Reduction Recommendations for MB85210

To minimize noise induction between signal lines as well as between signal and power supply lines, good board design practice requires consideration of the following:

1) Provide a capacitor of approx. a few μF for each module—even though the MB85210 has two or four decoupling capacitors of 0.15 μF on each module.
2) Remove noise, overshoot and undershoot from the address, control and data-input lines, so that the MB85210 won't latch wrong signals due to the noise induction between signal lines, and between signal and power supply lines.
3) Keep enough timing margin and remove critical timing in the board design to avoid the problem mentioned in Item 2 above.
4) In order to avoid a noise induction on the IN line at the falling edge of $\overline{W}$ when the delayed write or read-modify-write cycle is used, the falling edge of $\overline{W}$ signal should not coincide with the transition point of address and OUT signals. Since decoupling capacitors on the module board can't smooth the output current at the OUT pin, noise is introduced on the power supply line (V_{CC} or V_{SS}) and also on the IN line at t_{RAC} or t_{CAC} in the read cycle.
5) Provide an appropriate damping if necessary, to avoid excessive overshoot or undershoot on the TTL input waveform.

MB85210 Derating Curve



Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.4		6.5	V	0°C to +70°C*1
Input low voltage	V_{IL}	−2.0		0.8	V	

Note: *1 Maximum ambient temperature is permissible under certain conditions.

Capacitance
(T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance A_0 to A_8	C_{IN1}		70	pF
Input Capacitance $\overline{RAS}1$ and $\overline{RAS}2$	C_{IN2}		50	pF
Input Capacitance $\overline{CAS}$	C_{IN3}		90	pF
Input Capacitance $\overline{WE}$	C_{IN4}		60	pF
Input Capacitance D_{IN0} to D_{IN3}	C_{IN5}		19	pF
Output Capacitance D_{OUT0} to D_{OUT3}	C_{OUT}		21	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB85210-12 Min	MB85210-12 Max	MB85210-15 Min	MB85210-15 Max	Unit
Operating current*1 Average power supply current (one $\overline{RAS}$*2, $\overline{CAS}$ cycling; t_{RC} = min)	I_{CC1}		278		246	mA
Standby current Standby power supply current ($\overline{RAS}1 = \overline{RAS}2 = \overline{CAS} = V_{IH}$)	I_{CC2}		36		36	mA
Refresh current 1*1 Average power supply current ($\overline{CAS}$ = V_{IH}, all $\overline{RAS}$ cycling; t_{RC} = min)	I_{CC3}		440		400	mA
Nibble mode current*1 Average power supply current (one $\overline{RAS}$*3 = V_{IL}, $\overline{CAS}$ cycling; t_{NC} = min)	I_{CC4}		98		90	mA
Refresh current*2 Average power supply current (all $\overline{RAS}$ cycling, $\overline{CAS}$-before-$\overline{RAS}$)	I_{CC5}		480		440	mA
Input leakage current Input leakage current, any input ($0 \leqslant V_{IN} \leqslant 5.5V$, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)	$I_{I(L)}$	−80	80	−80	80	μA
Output leakage current (Data out is disabled, $0V \leqslant V_{OUT} \leqslant 5.5V$)	$I_{O(L)}$	−80	80	−80	80	μA
Output levels Output high voltage (I_{OH} = −5 mA) Output low voltage (I_{OL} = 4.2 mA)	V_{OH} V_{OL}	2.4	 0.4	2.4	 0.4	V

Notes: *1 I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
*2 $\overline{RAS}$ of the selected chip is cycling and another $\overline{RAS}$ is in V_{IH}.
*3 $\overline{RAS}$ of the selected chip is in V_{IL} and another $\overline{RAS}$ is in V_{IH}.

AC Characteristics*1,2,3
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB85210-12 Min	MB85210-12 Max	MB85210-15 Min	MB85210-15 Max	Unit
Time between refresh	t_{REF}		4		4	ms
Random read/write cycle time*12	t_{RC}	230		260		ns
Read-write cycle time*12	t_{RWC}	230		260		ns

Notes: *1 An initial pause of 200 μs is required after power up. And then several cycles (any 8 cycles to perform refresh are adequate) are required before proper device operation is achieved. If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
*2 AC characteristics assume t_T = 5 ns.
*3 V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
*12 The minimum cycle time is dependent on the ambient temperature and cooling conditions.

AC Characteristics[*1,2,3] (Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB85210-12 Min	MB85210-12 Max	MB85210-15 Min	MB85210-15 Max	Unit
Access time from $\overline{RAS}$[*4,6]	t_{RAC}		120		150	ns
Access time from $\overline{CAS}$[*5,6]	t_{CAC}		60		75	ns
Output buffer turn off delay	t_{OFF}	0	25	0	30	ns
Transition time	t_T	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	100		100		ns
$\overline{RAS}$ pulse width	t_{RAS}	120	100000	150	100000	ns
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns
$\overline{CAS}$ pulse width	t_{CAS}	60	100000	75	100000	ns
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ delay time[*7,8]	t_{RCD}	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ set up time	t_{CRS}	20		20		ns
Row address set up time	t_{ASR}	0		0		ns
Row address hold time	t_{RAH}	12		15		ns
Column address set up time	t_{ASC}	0		0		ns
Column address hold time	t_{CAH}	20		25		ns
Read command set up time	t_{RCS}	0		0		ns
Read command hold time referenced to $\overline{CAS}$[*11]	t_{RCH}	0		0		ns
Read command hold time referenced to $\overline{RAS}$[*11]	t_{RRH}	20		20		ns
Write command set up time[*9]	t_{WCS}	0		0		ns
Write command hold time	t_{WCH}	20		25		ns
Write command pulse width	t_{WP}	20		25		ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	50		60		ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	30		40		ns
Data in set up time	t_{DS}	0		0		ns
Data in hold time	t_{DH}	20		25		ns
$\overline{CAS}$ to $\overline{W}$ Delay[*9]	t_{CWD}	20		25		ns

Notes:
*4 Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
*5 Assumes that $t_{RCD} \geq t_{RCD}$ (max).
*6 Measured with a load equivalent to 2 TTL loads and 100 pF.
*7 Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
*8 t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T = 5 ns) + t_{ASC} (min).
*9 t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle. If $t_{CWC} \geq t_{CWC}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.
*11 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

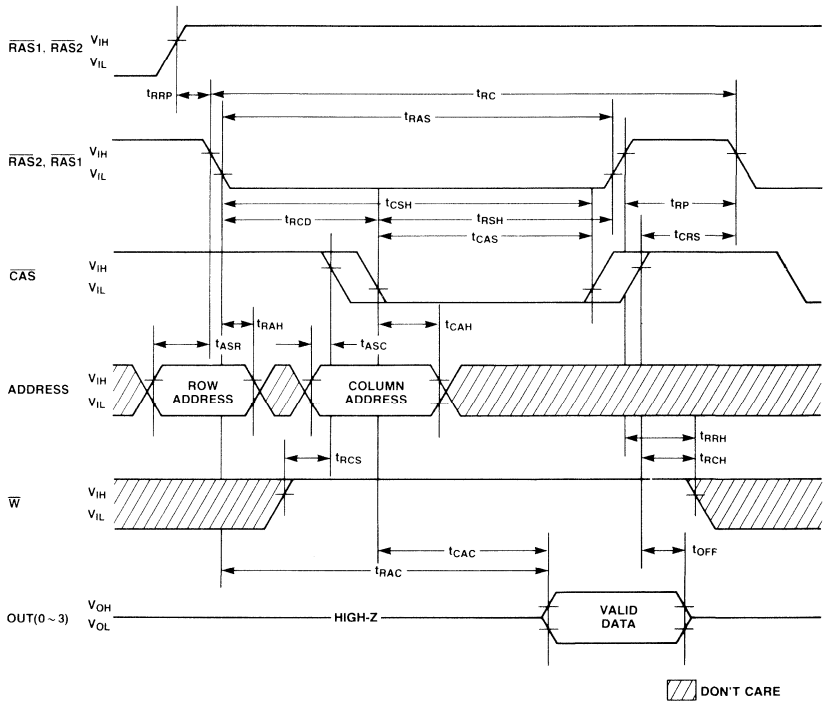
AC Characteristics[*1,2,3] (Continued) (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB85210-12 Min	MB85210-12 Max	MB85210-15 Min	MB85210-15 Max	Unit
Refresh set up time for $\overline{CAS}$ referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)	t_{FCS}	25		30		ns
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)	t_{FCH}	25		30		ns
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	20		20		ns
Nibble mode read/write cycle time	t_{NC}	65		80		ns
Nibble mode read-write cycle time	t_{NRWC}	65		80		ns
Nibble mode access time	t_{NCAC}		30		40	ns
Nibble mode $\overline{CAS}$ pulse width	t_{NCAS}	30		40		ns
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	25		30		ns
Nibble mode read $\overline{RAS}$ hold time	t_{NRRSH}	30		40		ns
Nibble mode write $\overline{RAS}$ hold time	t_{NWRSH}	50		60		ns
Nibble mode $\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{RNH}	20		20		ns
Refresh counter test $\overline{CAS}$ precharge time[*10]	t_{CPT}	60		70		ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CPR}	25		30		ns
Refresh counter test cycle time	t_{RTC}	350		405		ns
Refresh counter test $\overline{RAS}$ pulse width	t_{TRAS}	240		295		ns
$\overline{RAS}$1 to $\overline{RAS}$2 precharge time	t_{RRP}	0		0		ns

Notes: *10 Test mode write cycle only.

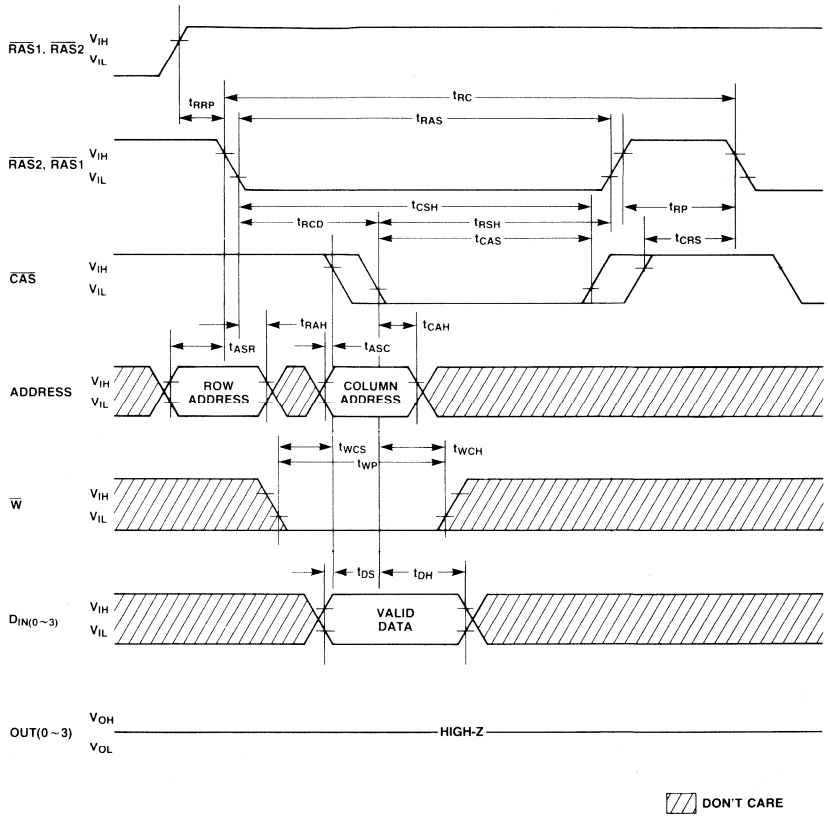
Timing Diagrams

Read Cycle



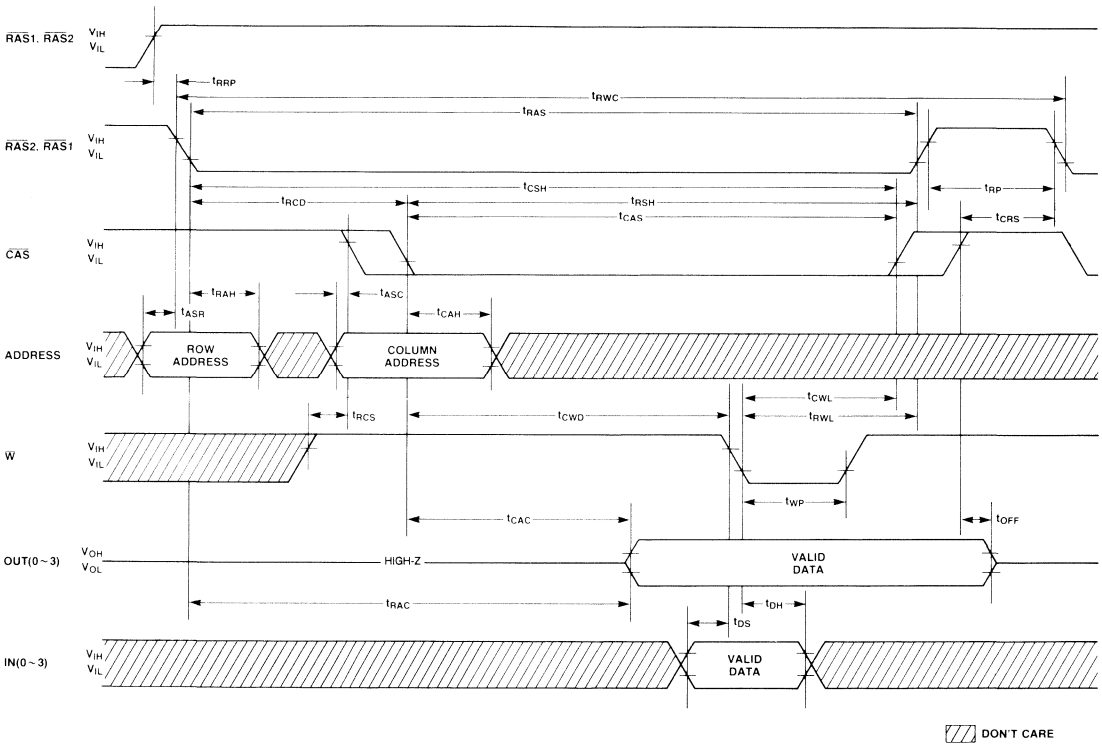
Timing Diagrams
(Continued)

Write Cycle (Early Write)



Timing Diagrams
(Continued)

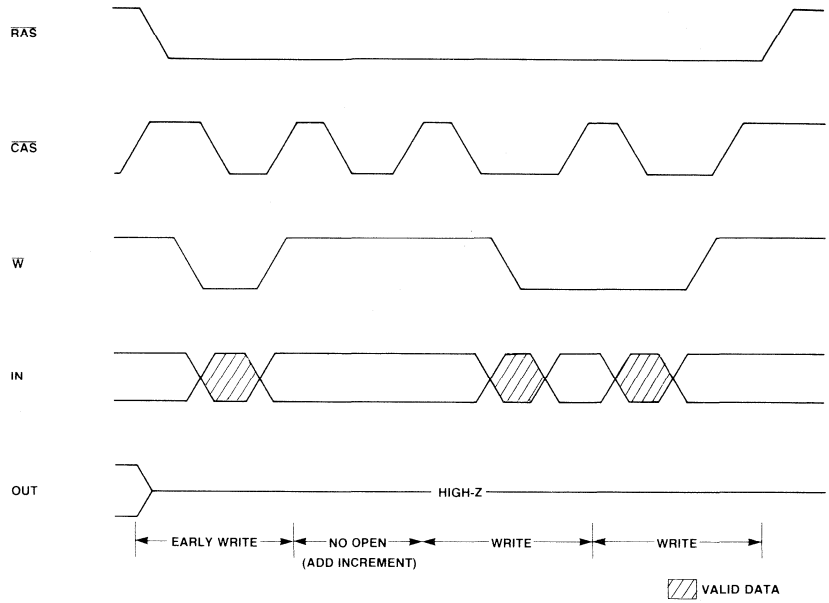
Read-Write/Read-Modify-Write Cycle



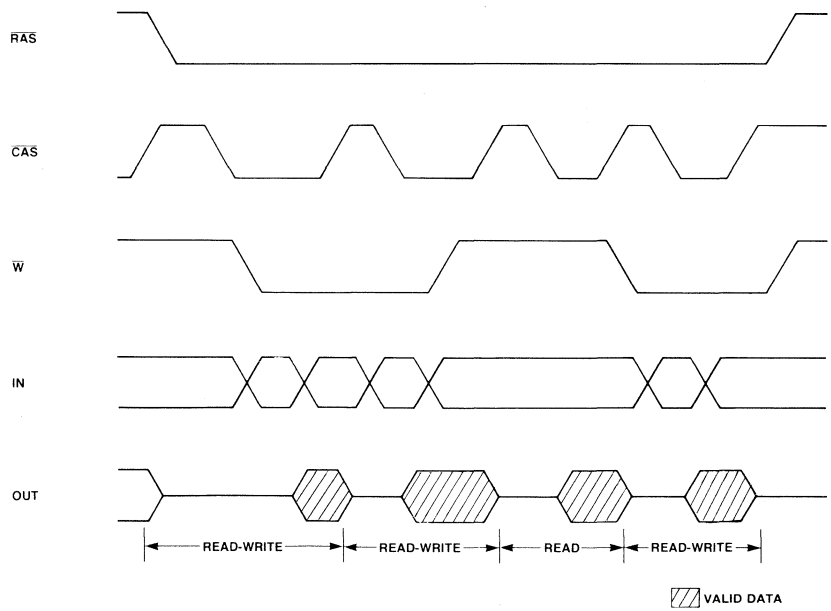
Timing Diagrams
(Continued)

Nibble Mode

*1 THE CASE OF FIRST NIBBLE CYCLE IS EARLY WRITE

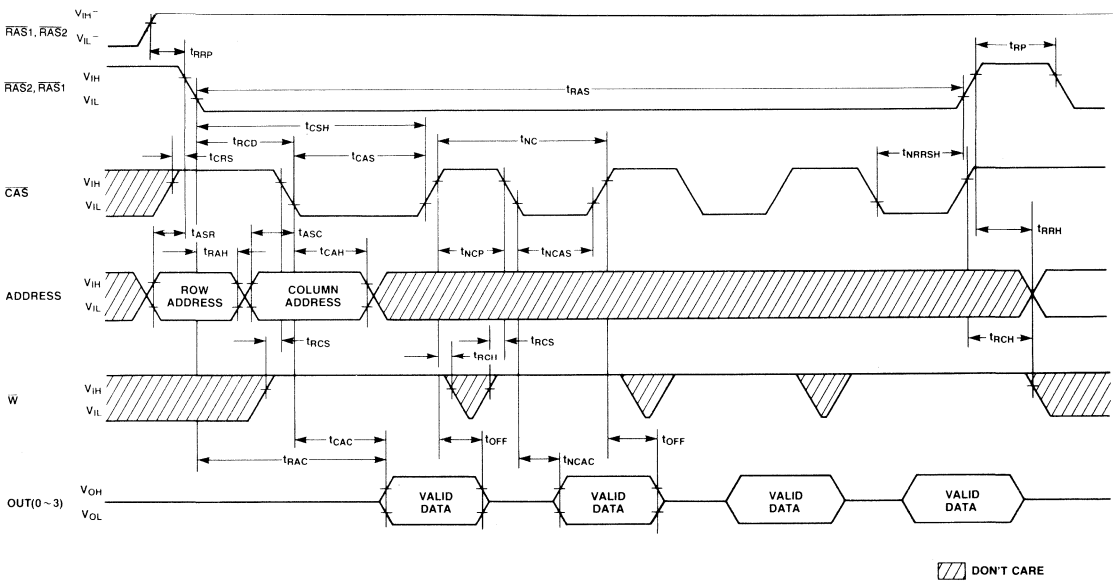


*2 THE CASE OF FIRST NIBBLE CYCLE IS DELAYED WRITE (READ-WRITE)



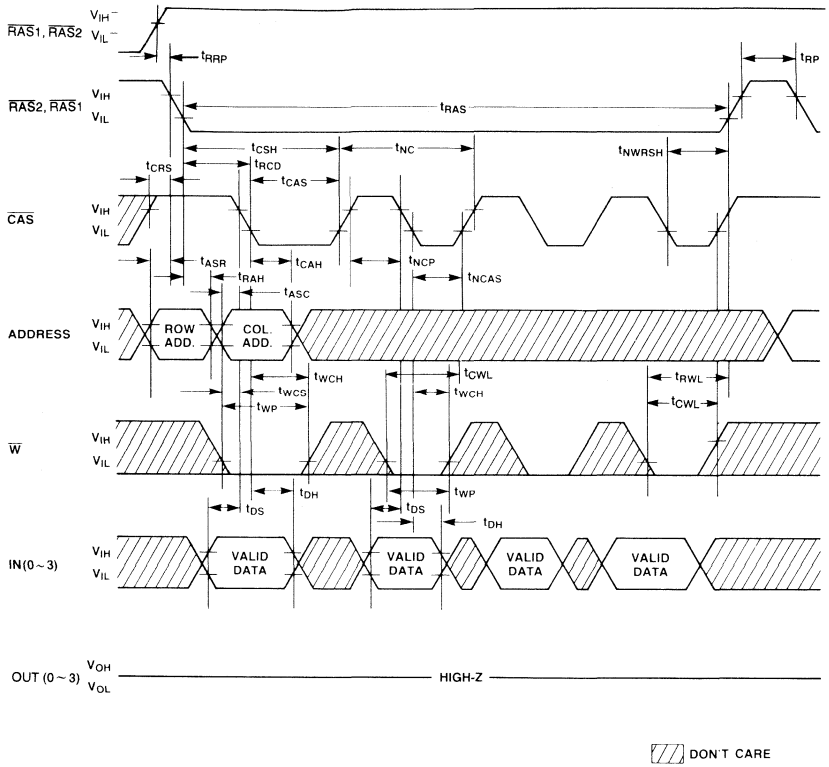
Timing Diagrams
(Continued)

Nibble Mode Read Cycle



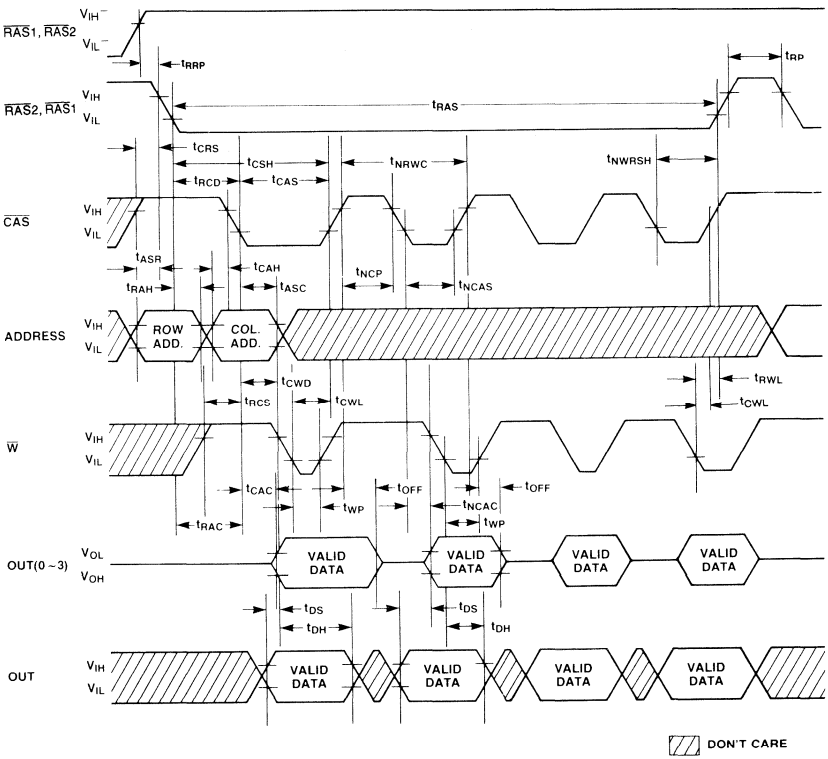
Timing Diagrams
(Continued)

Nibble Mode Write Cycle



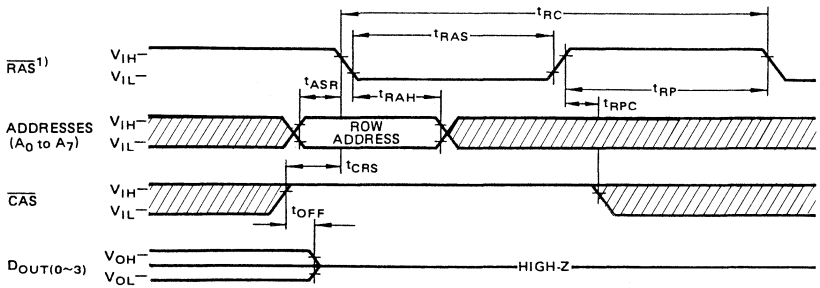
Timing Diagrams
(Continued)

Nibble Mode Read-Write Cycle



Timing Diagrams
(Continued)

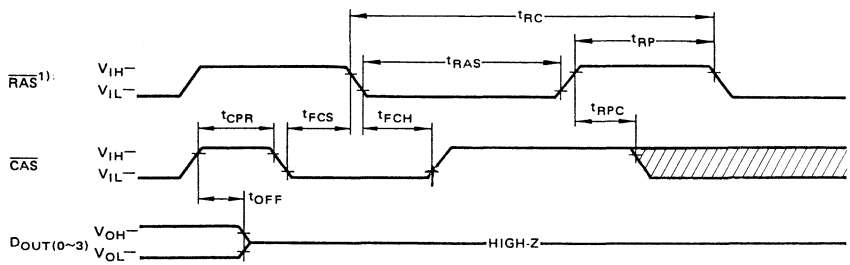
$\overline{RAS}$-Only Refresh Cycle
Note: $\overline{WE}$, $D_{IN(0\sim3)}$ = Don't care, $A_8 = V_{IH}$ or V_{IL}



NOTE: BOTH $\overline{RAS}$1 AND $\overline{RAS}$2 CAN BE ACTIVATED SIMULTANEOUSLY.

DON'T CARE

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle
Note: Address, $\overline{WE}$, $D_{IN(0\sim3)}$ = Don't care

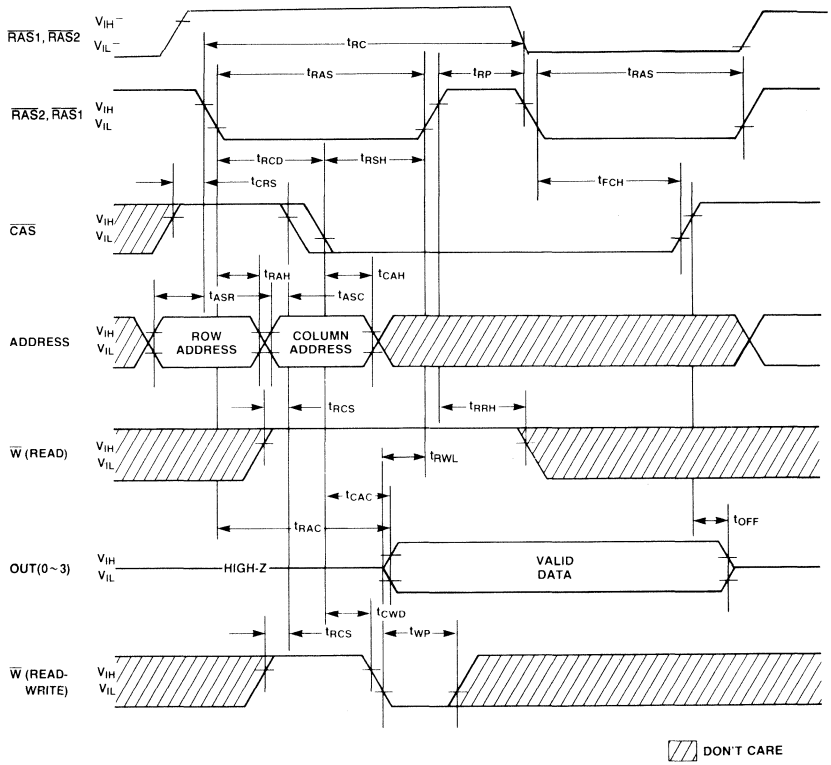


NOTE: BOTH $\overline{RAS}$1 AND $\overline{RAS}$2 CAN BE ACTIVATED SIMULTANEOUSLY.

DON'T CARE

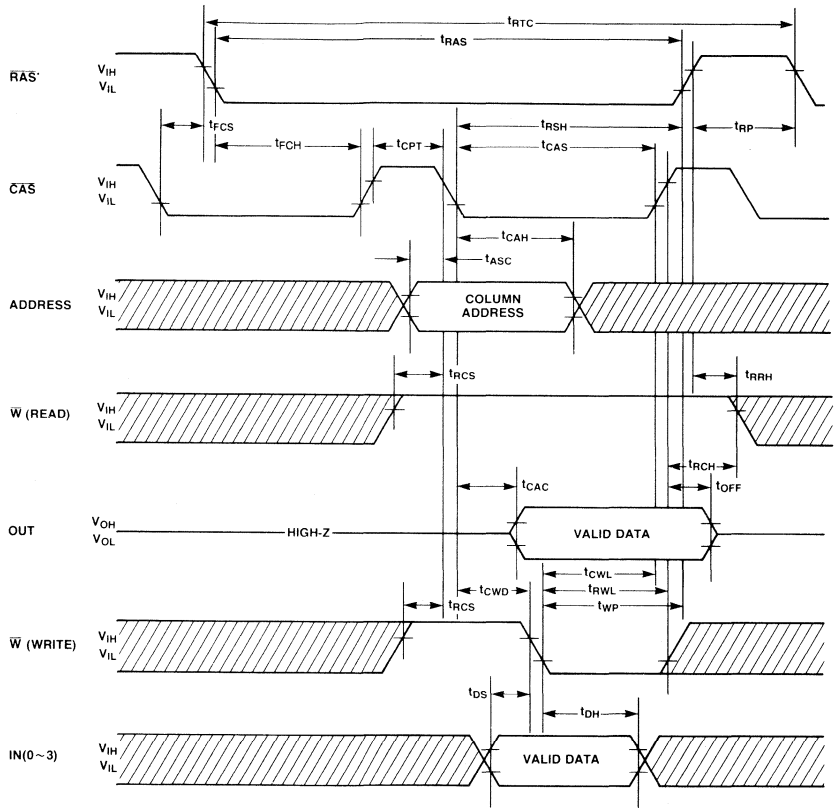
Timing Diagrams
(Continued)

Hidden Refresh Cycle



Timing Diagrams
(Continued)

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

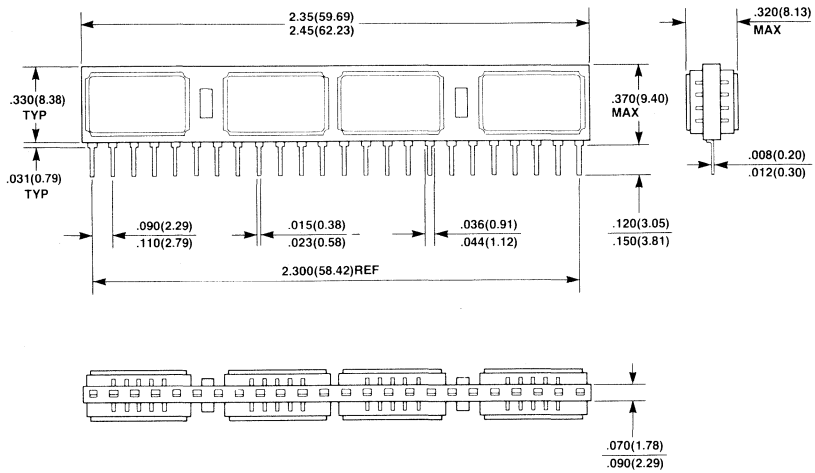


NOTE: *IT IS FOR SELECTED CHIP, OTHER $\overline{RAS}$ IS IN V_{IH}.

DON'T CARE

Package Dimensions
Dimensions in Inches
(millimeters)

24-Lead Single In-Line Package Module
(Module No.: MSP-24S-CC02)



Preliminary

MOS Memories

FUJITSU

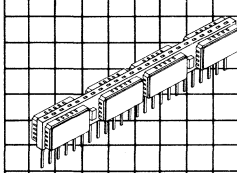
■ MB85211-12, MB85211-15

524,288 x 4-Bit Dynamic
Random Access Memory
SIP Module

Description

The Fujitsu MB85211 is a fully decoded, 524,288 word x 4-bit NMOS dynamic random access memory module consisting of eight MB81256 DRAMs in 18-pad LCC packages mounted on a 24-pin multilayer ceramic substrate.

The MB85211 is intended for use in memory applications where large memory capacity is required within limited physical volume. Significant size reduction can be realized in applications such as mainframe memory, buffer memory, desk top computers and peripheral storage.



MSP-24S-C003

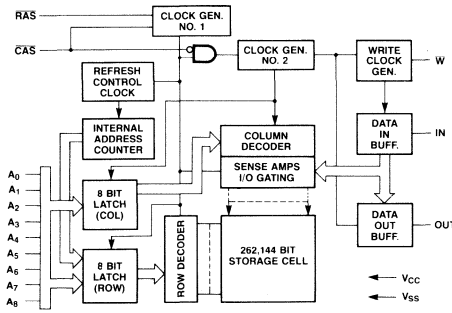
Features

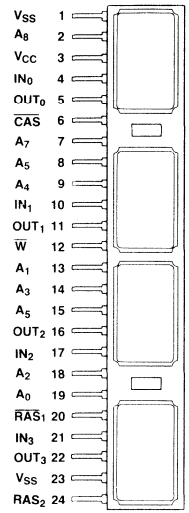
- **524,288 x 4 DRAM 24-pin SIP (MB81256x8)**
- **Row access time**
  120 ns max. (MB85211-12)
  150 ns max. (MB85211-15)
- **Cycle time**
  230 ns min. (MB85211-12)
  260 ns min. (MB85211-15)
- **Page cycle time**
  120 ns min. (MB85211-12)
  150 ns min. (MB85211-15)
- **Single + 5V supply, ±10% tolerance**
- **Low power (active)**
  1529 mW max. (MB85211-12)
  1353 mW max. (MB85211-15)
  198 mW max. (standby)
- **256/4 ms refresh cycles capability**
- **$\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$ and Hidden refresh capability**
- **Read-Modify-Write and Page Mode Capability**
- **Common I/O capability using Early Write operation**
- **On-chip latches for Addresses and Data-in**
- **All inputs and outputs are TTL compatible**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

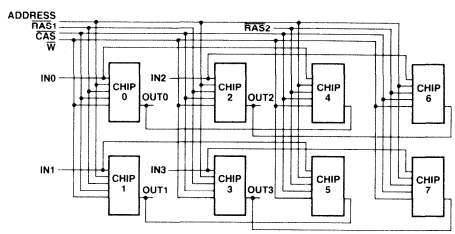
MB85211 Block Diagrams and Pin Assignment

Block Diagram for Each Chip





Functional Block Diagram



FUNCTIONAL TRUTH TABLE

RAS	CAS	W	IN	OUT	Read	Write	Refresh	Note
H	H	Don't Care	Don't Care	High-Z	No	No	No	Standby
L	L	H	Don't Care	Valid Data	Yes	No	Yes	Read
L	L	L	Valid Data	High-Z	No	Yes	Yes	Early Write $t_{WCS} \geq t_{WCS}$ (min.)
L	L	L	Valid Data	Valid Data	Yes	Yes	Yes	Delayed Write or Read-Write $t_{CWD} \geq t_{CWD}$ (min.)
L	H	Don't Care	Don't Care	High-Z	No	No	Yes	RAS-only Refresh
L	L	Don't Care	Don't Care	Valid Data	No	No	Yes	CAS-before-RAS Refresh Valid data selected at previous Read or Read-Write cycle is held
H	L	Don't Care	Don't Care	High-Z	No	No	No	CAS disturb

FUNCTIONAL TRUTH TABLE FOR MODULE

RAS1 and RAS2	CAS	WE	D_{IN1} to D_{IN3}	D_{OUT1} to D_{OUT3}	Function
H	H	Don't Care	Don't Care	High-Z	Standby
L1)	L	H	Don't Care	Valid Data	Read Cycle
L1)	L	L2)	Valid Data	High-Z	Write Cycle
L1)	L	H → L3)	Valid Data	Valid Data	Read-Write Cycle
L	H	Don't Care	Don't Care	High-Z	RAS-Only Refresh
L	L4)	Don't Care	Don't Care	High-Z	CAS-before-RAS Refresh

Notes 1): It is for the selected RAS, and other RAS is high.
2): $t_{WCS} \geq t_{WCS}$ (min).
3): $t_{CWD} \geq t_{CWD}$ (min).
4): $t_{FCS} \geq t_{FCS}$ (min).

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Storage temperature	T_{STG}	−55 to +150	°C
Power dissipation	P_D	8.0	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Description

Simple Timing Requirement

The MB85211 has improved circuitry that eases timing requirements for high speed access operations. The MB85211 can operate under the condition of t_{RCD} (max) = t_{CAC} thus providing optimal timing for address multiplexing. In addition, the MB85211 has the minimal hold times of address (t_{CAH}), $\overline{W}$ (t_{WCH}) and IN (t_{DH}). Fujitsu has made timing requirements that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. As a result, the hold times of the column address, IN and $\overline{W}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{W}$ Delay) are not restricted by t_{RCD}.

Address Inputs

A total of eighteen binary input address-bits are required to decode any 4-bits of data in 524,288 locations within the MB85211. Nine row address bits are established on the input pins (A_0 through A_8) and latched with the Row Address Strobe ($\overline{RAS}$1 or $\overline{RAS}$2). $\overline{RAS}$1 and $\overline{RAS}$2 are respectively applied to the lower 262,144 addresses and the upper 262,144 addresses. Nine column address bits are established on the input pins and latched with $\overline{CAS}$. All input addresses must be stable on or before the falling edge of $\overline{RAS}$. If the lower 262,144 addresses are used, it is applied to $\overline{RAS}$1 and if the upper 262,144 addresses are used, it is applied to $\overline{RAS}$2. $\overline{CAS}$ is internally inhibited by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

$\overline{RAS}$1 and $\overline{RAS}$2

The MB85211 has two $\overline{RAS}$ inputs in order to select all 524,288x4 locations using eighteen address inputs. $\overline{RAS}$1 is used to select the lower 262,144x4 locations and $\overline{RAS}$2 is used to select the upper 252,144x4 locations. In the read, delayed write or read-write cycle, both $\overline{RAS}$1 and $\overline{RAS}$2 must not be low simultaneously in order to avoid data conflict.

Write Enable

The read mode or write mode is selected with the $\overline{W}$ input. A high on the $\overline{W}$ selects read mode, a low selects write mode. Data input is disabled when read mode is selected.

Data Inputs

The 4-bit data is written into the MB85211 during a write or read-write cycle. The latter falling edge of $\overline{W}$ or $\overline{CAS}$ is a strobe for the IN register. In a write cycle, if $\overline{W}$ is brought low before the negative transition of $\overline{CAS}$, the set-up and hold times are referenced to $\overline{CAS}$. In a delayed write or read-write cycle, $\overline{W}$ can be low after $\overline{CAS}$ has already gone low. Thus IN_0 to IN_3 are strobed by $\overline{W}$, and set-up and hold times are referenced to $\overline{W}$.

Data Outputs

The output buffers of each chip are three-state TTL compatible with a fan-out of two standard TTL loads. OUT is the same polarity as IN. The output is in high impedance state until $\overline{CAS}$ is brought low. In a read or read-write cycle, the output is valid after t_{RAC} from negative transition of the RAS when t_{RCD} (max) is satisfied, or after t_{CAC} from negative transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid untiil $\overline{CAS}$ is returned to a high. In a write cycle, the identical sequence occurs but data is not valid.

Fast Read-While-Write Cycle

The MB85211 has a fast read-while-write cycle which is achieved by precise control of the three-state output buffer as well as by the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{W}$ when $\overline{CAS}$ goes low. When $\overline{W}$ is low during $\overline{CAS}$ transition to low, the MB85211 goes into the early write mode in which the output floats and the common I/O bus can be used on the system level. Whereas, when $\overline{W}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MB85211 goes into the delayed write mode. The output then contains the data from the cell selected and the data from IN is written into the cell selected. Therefore, a very fast read write cycle (t_{RC} = t_{RWC}) is possible with the MB85211.

Page Mode

Page mode operation permits strobing the row-address into the MB85211 while maintaining $\overline{RAS}$ at a logic low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

Description
(Continued)

Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each 256 row addresses (A_0 through A_7) for each chip at least every 4 ms. During refresh, either V_{IL} or V_{IH} is permitted for A_8 and any combination of $\overline{RAS}1$ and $\overline{RAS}2$ are allowed. When all chips are refreshed simultaneously, the average power dissipation of the module must be less than 640 mW at any 100 ms interval.

The MB85211 offers the following three types of refresh.

1. $\overline{RAS}$-Only Refresh;
   $\overline{RAS}$-Only refresh avoids any output during refresh because the output buffer is in high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 row addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Both $\overline{RAS}1$ and $\overline{RAS}2$ can be refreshed simultaneously under the specified power dissipation limit.
2. $\overline{CAS}$-before-$\overline{RAS}$ Refresh;
   $\overline{CAS}$-before-$\overline{RAS}$ refresh available on the MB85211 offers an alternate refresh method. If $\overline{CAS}$ is held low for the specified period (t_{FS}) before $\overline{RAS}$ goes low, on chip refresh control clock generators and the refresh address counter for each chip are enabled, and an internal refresh operation takes place. After the refresh operation has been executed the refresh address counter is automatically incremented for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.
3. Hidden Refresh
   Hidden refresh may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. In MB85211, hidden refresh means $\overline{CAS}$-before-$\overline{RAS}$ refresh and the internal refresh addresses are used, that is no external refresh address is needed. In hidden refresh, $\overline{RAS}1$ and $\overline{RAS}2$ cannot be refreshed at the same time because of data conflict.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then goes low again while $\overline{RAS}$ is held low, the read and write operations are enabled. This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell address (consisting of a row address (9-bits) and a column address (9-bits)) to be accessed can be defined as follows:

1. A ROW ADDRESS—Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set high internally.
2. A COLUMN ADDRESS—All the-bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Procedure

The timing, as shown in $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle, is used for all operations described as follows:

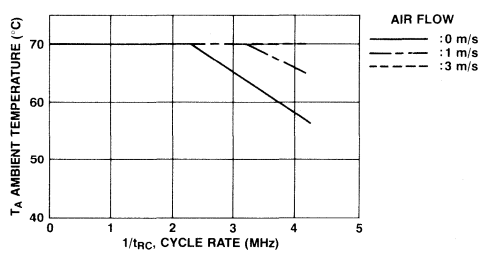
1. Initialize the internal refresh counter. For this operation, the 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
2. Write a test pattern of lows into memory cells at a single column address and 256 row addresses.
3. By using read-modify-write cycle, read the lows written at the last step and write a new high in the same cycle. This cycle is repeated 256 times, and highs are written into the 256 memory cells.
4. Read the high written at the last step.
5. Compliment the test pattern and repeat the steps 2, 3 and 4.

Decoupling and Noise Reduction Recommendations for MB85211

To minimize noise induction between signal lines as well as between signal and power supply lines, good board design practice requires consideration of the following:

1. Provide a capacitor of approx. a few μF for each module—even though the MB85211 has two or four decoupling capacitors of 0.15 μF on each module.
2. Remove noise, overshoot and undershoot from the address, control and data-input lines, so that the MB85211 won't latch wrong signals due to the noise induction between signal lines, and between signal and power supply lines.
3. Keep enough timing margin and remove critical timing in the board design to avoid the problem mentioned in Item 2 above.
4. In order to avoid noise induction on the IN line at the falling edge of $\overline{W}$ when the

MB85211 Derating Curve



delayed write or read-modify-write cycle is used, the falling edge of $\overline{W}$ signal should not coincide with the transition point of address and OUT signals. Since decoupling capacitors on the module board can't smooth the output current at the OUT pin, noise is introduced on the power supply line (V_{CC} or V_{SS}) and also on the IN line at t_{RAC} or t_{CAC} in the read cycle.

5. Provide an appropriate damping if necessary, to avoid excessive overshoot or undershoot on the TTL input waveform.

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C*1
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.4		6.5	V	
Input low voltage	V_{IL}	−2.0		0.8	V	

Note: *1 Maximum ambient temperature is permissible under certain conditions.

Capacitance
(T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance A_0 to A_8	C_{IN1}		70	pF
Input Capacitance $\overline{RAS}1$ and $\overline{RAS}2$	C_{IN2}		50	pF
Input Capacitance $\overline{CAS}$	C_{IN3}		90	pF
Input Capacitance $\overline{WE}$	C_{IN4}		60	pF
Input Capacitance D_{IN0} to D_{IN3}	C_{IN5}		19	pF
Output Capacitance D_{OUT0} to D_{OUT3}	C_{OUT}		21	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB85211-12 Min	MB85211-12 Max	MB85211-15 Min	MB85211-15 Max	Unit
Operating current*1 Average power supply current (one $\overline{RAS}$*2, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		278		246	mA
Standby current Standby power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		36		36	mA
Refresh current 1*1 Average power supply current ($\overline{CAS}$ = V_{IH}, all $\overline{RAS}$ cycling; t_{RC} = min)	I_{CC3}		440		400	mA
Page mode current*1 Average power supply current (one $\overline{RAS}$*3 = V_{IL}, $\overline{CAS}$ cycling; t_{NC} = min)	I_{CC4}		138		118	mA
Refresh current 2*2 Average power supply current (all $\overline{RAS}$ cycling, $\overline{CAS}$-before-RAS)	I_{CC5}		480		440	mA
Input leakage current Any input (0 ≤ V_{IN} ≤ 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)	$I_{I(L)}$	−80	80	−80	80	μA
Output leakage current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	$I_{O(L)}$	−80	80	−80	80	μA
Output levels Output high voltage (I_{OH} = −5 mA) Output low voltage (I_{OL} = 4.2 mA)	V_{OH} V_{OL}	2.4	 0.4	2.4	 0.4	V

Notes: *1 I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
*2 $\overline{RAS}$ of the selected chip is cycling and another $\overline{RAS}$ is in V_{IH}.
*3 $\overline{RAS}$ of the selected chip is in V_{IL} and another $\overline{RAS}$ is in V_{IH}.

AC Characteristics[*1,2,3]
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB85211-12 Min	MB85211-12 Max	MB85211-15 Min	MB85211-15 Max	Unit
Time between refresh	t_{REF}		4		4	ms
Random read/write cycle time[*12]	t_{RC}	230		260		ns
Read-write-cycle time[*12]	t_{RWC}	230		260		ns
Access time from $\overline{RAS}$[*4,6]	t_{RAC}		120		150	ns
Access time from $\overline{CAS}$[*5,6]	t_{CAC}		60		75	ns
Output buffer turn off delay	t_{OFF}	0	25	0	30	ns
Transition time	t_T	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	100		100		ns
$\overline{RAS}$ pulse width	t_{RAS}	120	100000	150	100000	ns
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns
$\overline{CAS}$ pulse width	t_{CAS}	60	100000	75	100000	ns
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ delay time[*7,8]	t_{RCD}	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ set up time	t_{CRS}	20		20		ns
Row address set up time	t_{ASR}	0		0		ns
Row address hold time	t_{RAH}	12		15		ns
Column address set up time	t_{ASC}	0		0		ns
Column address hold time	t_{CAH}	20		25		ns
Read command set up time	t_{RCS}	0		0		ns
Read command hold time referenced to $\overline{CAS}$[*11]	t_{RCH}	0		0		ns
Read command hold time referenced to $\overline{RAS}$[*11]	t_{RRH}	20		20		ns
Write command set up time[*9]	t_{WCS}	0		0		ns
Write command hold time	t_{WCH}	20		25		ns
Write command pulse width	t_{WP}	20		25		ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	50		60		ns

Notes:

*1 An initial pause of 200 μs is required after power-up. And then several cycles (any 8 cycles to perform refresh are adequate) are required before proper device operation is achieved. If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

*2 AC characteristics assume t_T = 5 ns.

*3 V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).

*4 Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

*5 Assumes that $t_{RCD} \geq t_{RCD}$ (max).

*6 Measured with a load equivalent to 2 TTL loads and 100 pF.

*7 Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

*8 t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T = 5 ns) + t_{ASC} (min).

*9 t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.

*11 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

*12 Minimum cycle time is dependent on the ambient temperature and cooling conditions.

AC Characteristics[*1,2,3]
(Continued)
(Recommended operating conditions unless otherwise noted.)

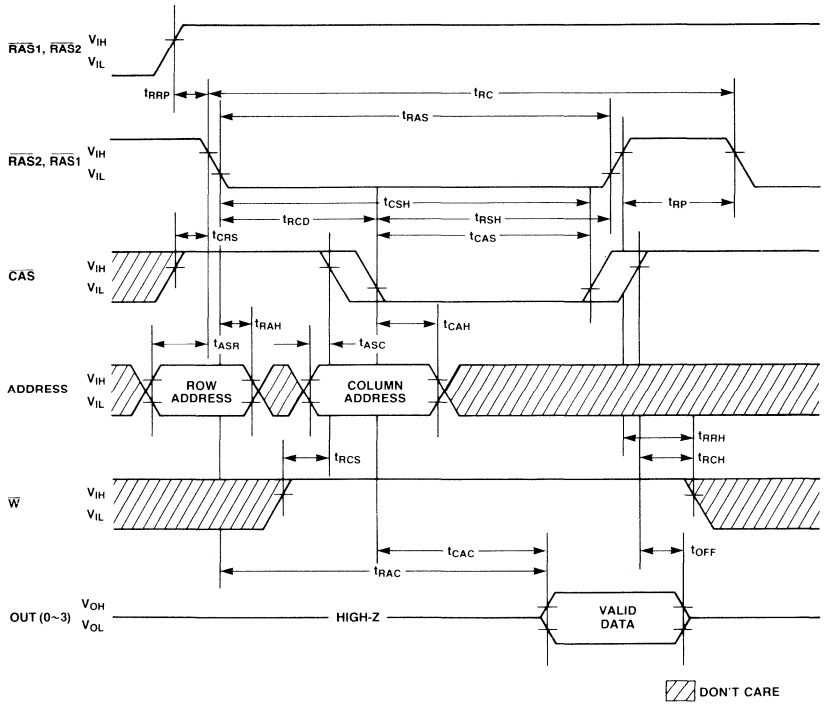
Parameter	Symbol	MB85211-12 Min	MB85211-12 Max	MB85211-15 Min	MB85211-15 Max	Unit
Write command to $\overline{CAS}$ lead time	t_{CWL}	50		60		ns
Data in set up time	t_{DS}	0		0		ns
Data in hold time	t_{DH}	20		25		ns
$\overline{CAS}$ to $\overline{W}$ delay[*9]	t_{CWD}	20		25		ns
Refresh set up time for $\overline{CAS}$ referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$	t_{FCS}	25		30		ns
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$	t_{FCH}	25		30		ns
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	20		20		ns
Page mode read/write cycle time	t_{PC}	120		150		ns
Page mode read-write cycle time	t_{PRWC}	120		150		ns
Page mode $\overline{CAS}$ precharge time	t_{CP}	50		65		ns
Refresh counter test cycle time	t_{RTC}	375		430		ns
Refresh counter test $\overline{RAS}$ pulse width	t_{TRAS}	265	10000	320	10000	ns
$\overline{RAS}$1 to $\overline{RAS}$2 precharge time	t_{RRP}	0		0		ns
Refresh counter test $\overline{CAS}$ precharge time[*10]	t_{CPT}	60		70		ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CRP}	25		30		ns

Notes: *9 t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of the data out is indeterminate.

*10 Test mode write cycle only.

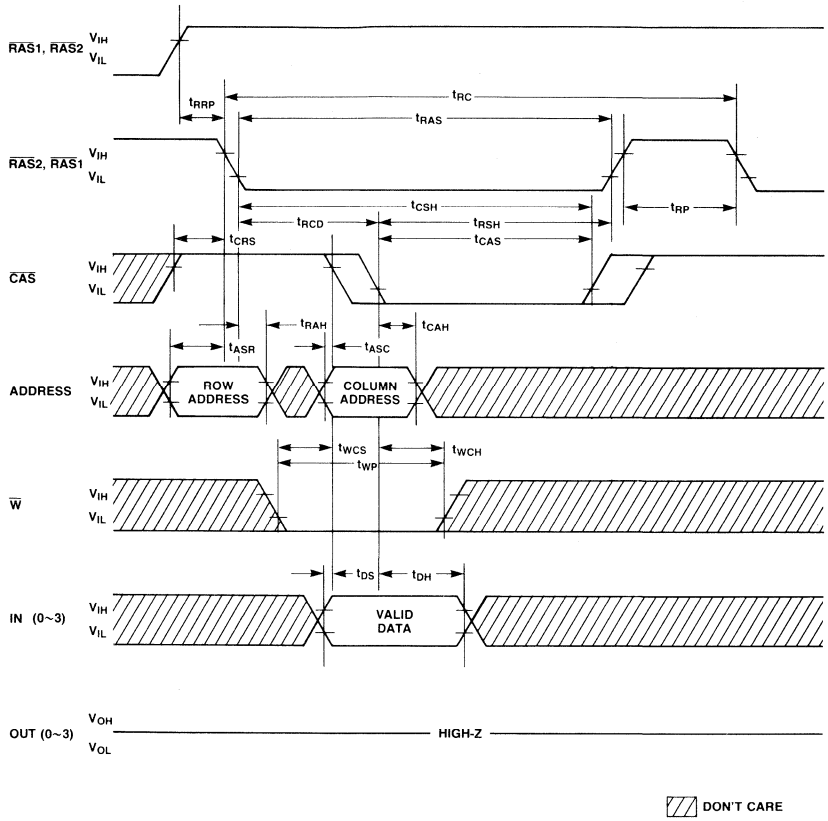
Timing Diagrams

Read Cycle



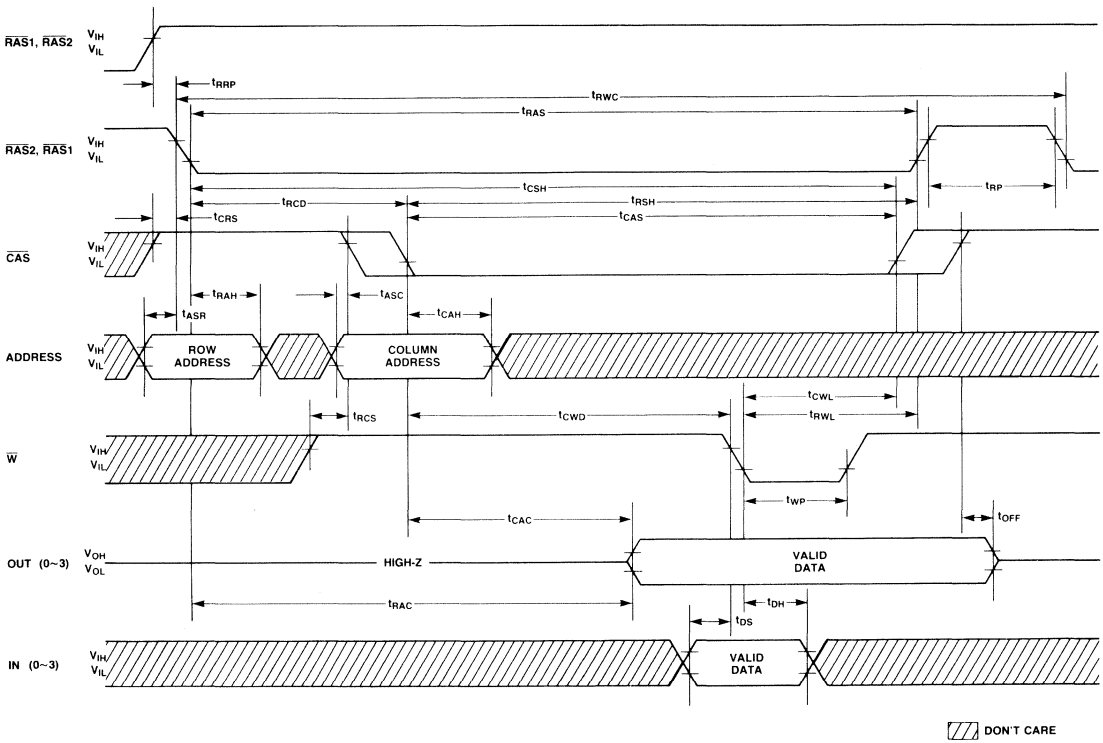
Timing Diagrams
(Continued)

Write Cycle (Early Write)



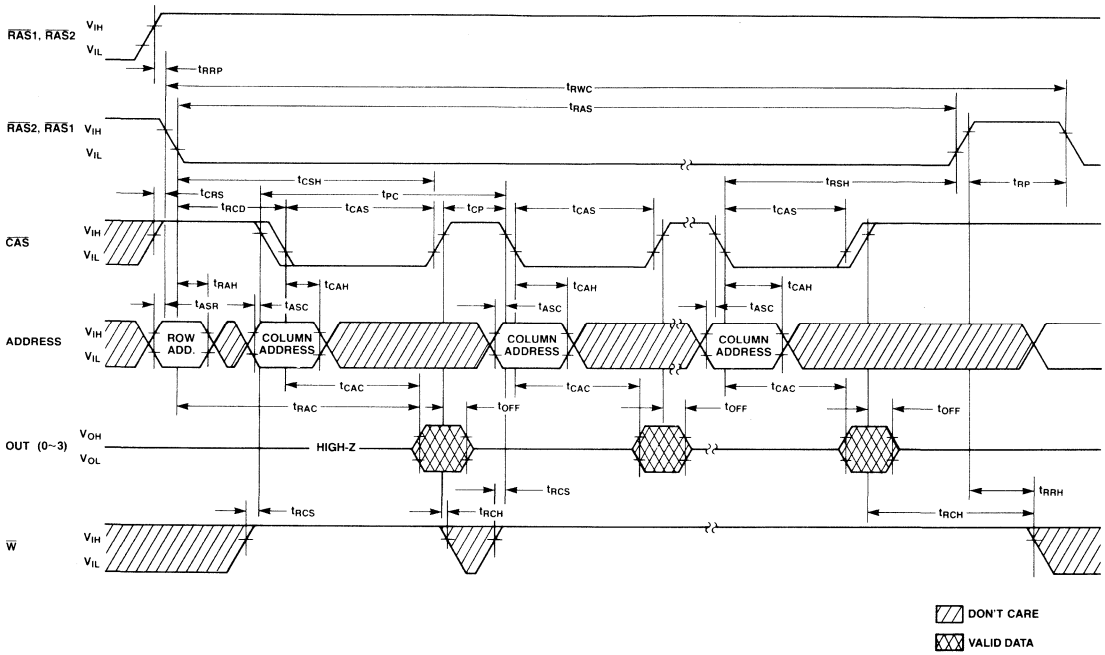
Timing Diagrams
(Continued)

Read-Write/Read-Modify-Write Cycle



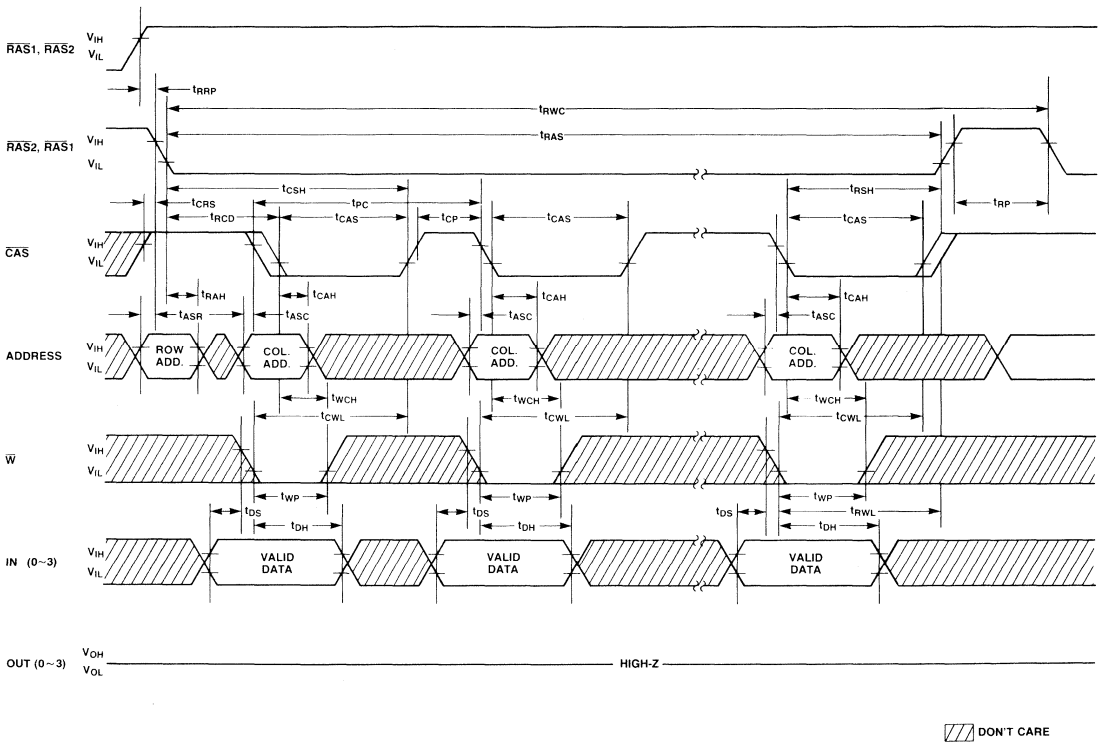
Timing Diagrams
(Continued)

Page Mode Read Cycle



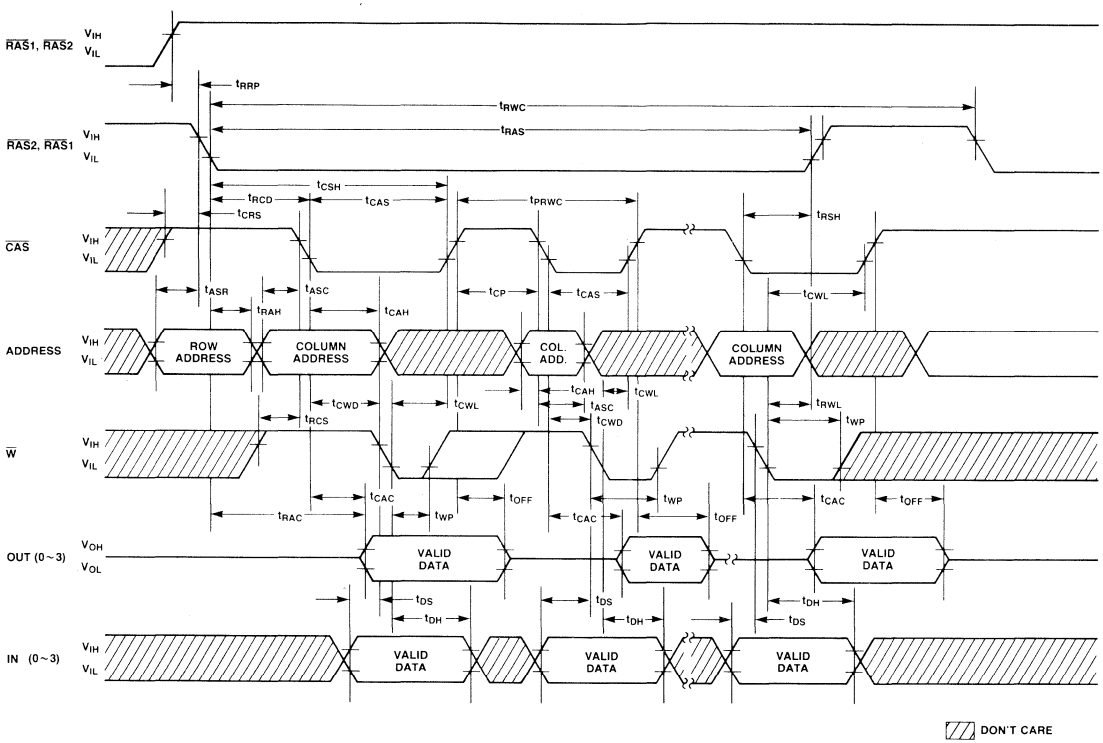
Timing Diagrams
(Continued)

Page Mode Write Cycle



Timing Diagrams
(Continued)

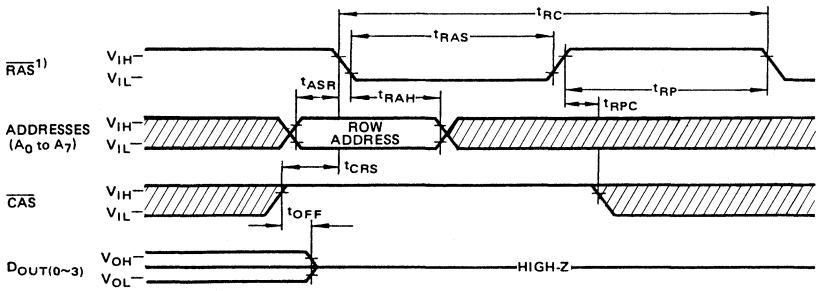
Page Mode Read-Write Cycle



Timing Diagrams
(Continued)

$\overline{RAS}$-Only Refresh Cycle

Note: $\overline{WE}$, $D_{IN(0\sim3)}$ = Don't care, $A_8 = V_{IH}$ or V_{IL}

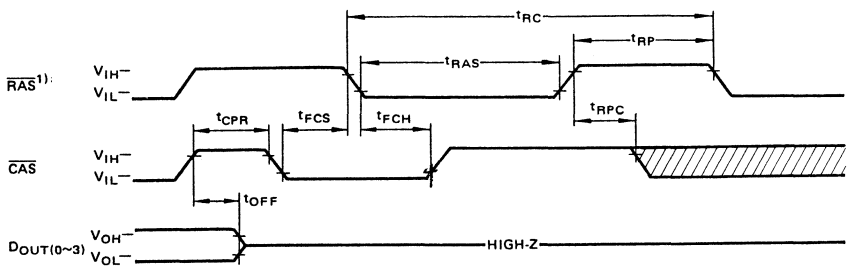


NOTE: *1 BOTH $\overline{RAS}$1 AND $\overline{RAS}$2 CAN BE ACTIVATED SIMULTANEOUSLY.

Don't Care

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

Note: Address, $\overline{WE}$, $D_{IN(0\sim3)}$ = Don't care

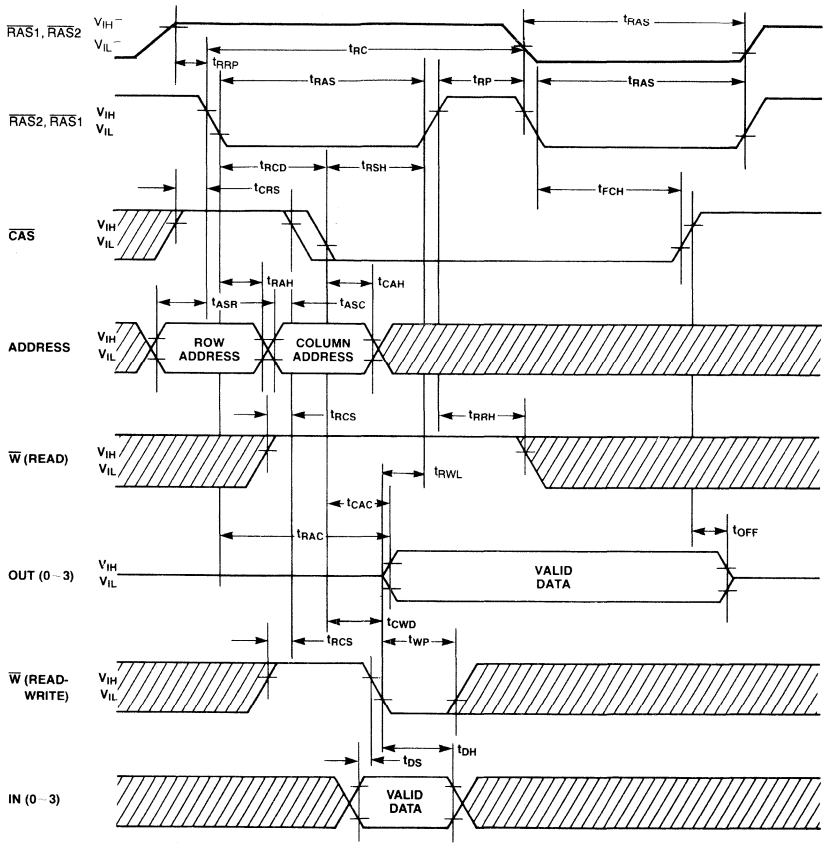


NOTE: *1 BOTH $\overline{RAS}$1 AND $\overline{RAS}$2 CAN BE ACTIVATED SIMULTANEOUSLY.

Don't Care

Timing Diagrams
(Continued)

Hidden Refresh Cycle

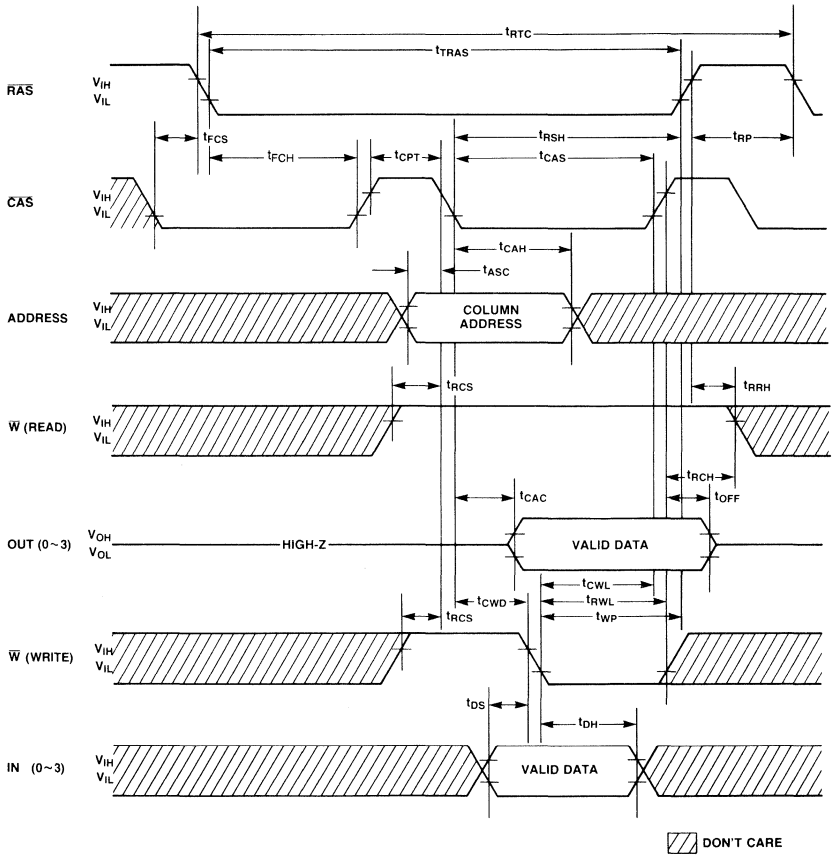


NOTE: *1 IT IS FOR SELECTED CHIP, OTHER RAS IS IN V_{IH}.

DON'T CARE

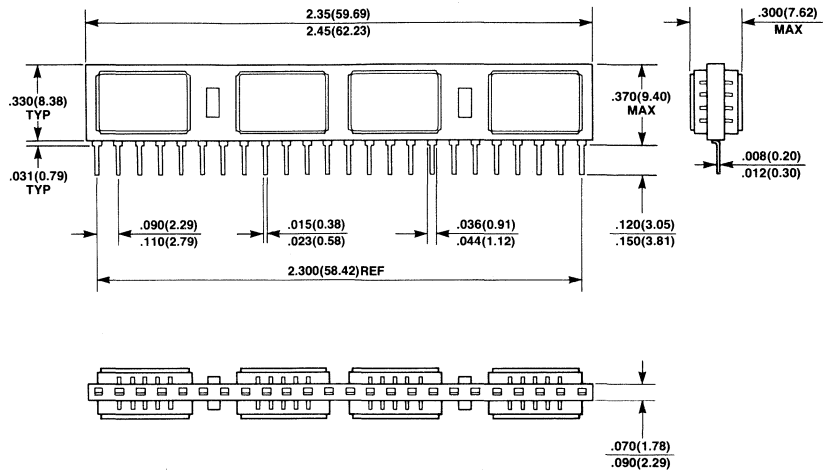
Timing Diagrams
(Continued)

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



Package Dimensions
Dimensions in Inches
(millimeters)

24-Lead Single In-Line Package Module
(Module No.: MSP-24S-CC03)



Preliminary

MOS Memories

FUJITSU

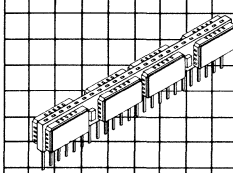
■ MB85213-12, MB85213-15

262,144 x 8-Bit Dynamic
Random Access Memory
SIP Module

Description

The Fujitsu MB85213 is a fully decoded, 262,144 word x 8-bit NMOS dynamic random access memory module consisting of eight MB81257 DRAMs in 18-pad LCC packages mounted on a 24-pin multilayer ceramic substrate.

The MB85213 is intended for use in memory applications where large memory capacity is required within limited physical volume. Significant size reduction can be realized in applications such as mainframe memory, buffer memory, desk top computers and peripheral storage.



MSP-24S-CC02

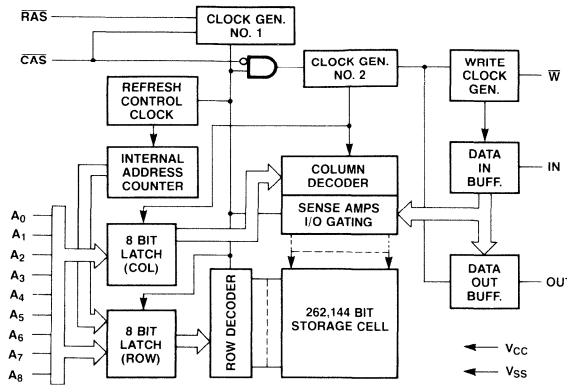
Features

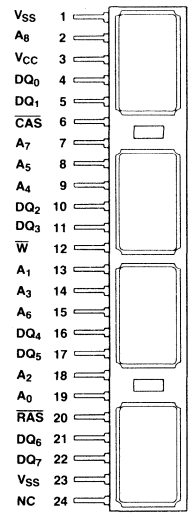
- **262,144 x 8 DRAM, 24 pin SIP (MB81257x8)**
- **Row access time**
  120 ns max. (MB85213-12)
  150 ns max. (MB85213-15)
- **Cycle time**
  230 ns min. (MB85213-12)
  260 ns min. (MB85213-15)
- **Nibble cycle time**
  65 ns min. (MB85213-12)
  80 ns min. (MB85213-15)
- **Single + 5V supply, ±10% tolerance**
- **Low power (active)**
  2860 mW max. (MB85213-12)
  2508 mW max. (MB85213-15)
  198 mW max. (standby)
- **4 ms/256 refresh cycles capability**
- **$\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$ and Hidden refresh capability**
- **Nibble Mode Capability**
- **On-chip latches for Addresses and Data-in**
- **All inputs and outputs are TTL compatible.**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

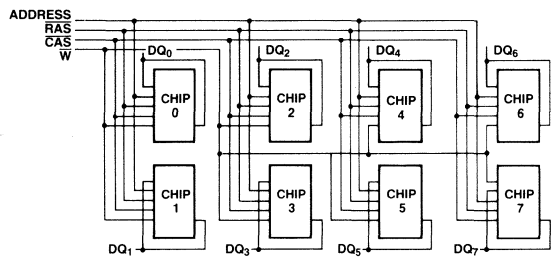
MB85213 Block Diagrams and Pin Assignment

Block Diagram for Each Chip





Functional Block Diagram



FUNCTIONAL TRUTH TABLE

$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$DQ_0 - DQ_7$	FUNCTION
H	H	Don't Care	High-Z	Standby
L	L	H	Valid Data out*1	Read cycle
L	L	L	Valid Data in*2	Write cycle
L	L	Don't Care	Latched Data out	Hidden refresh cycle
H—L*3	H—L	Don't Care	High-Z	$\overline{CAS}$-before-$\overline{RAS}$ refresh cycle*3
L	H	Don't Care	High-Z	$\overline{RAS}$-only refresh cycle

Notes: *1 DQ pins are output mode.
*2 DQ pins are input mode.
*3 $t_{FCS} \geq t_{FCS}$ (min).

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	8.0	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Description

Simple Timing Requirement

The MB85213 has improved circuitry that eases timing requirements for high speed access operations. The MB85213 can operate under the condition of t_{RCD} (max) = t_{CAC} thus providing optimal timing for address multiplexing. In addition, the MB85213 has the minimal hold times of address (t_{CAH}), $\overline{W}$ (t_{WCH}) and IN (t_{DH}). Fujitsu has made timing requirements that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, t_{DHR}. As a result, the hold times of the column address, IN and $\overline{W}$ are not restricted by t_{RCD}.

Address Inputs

A total of eighteen binary input address bits are required to decode parallel 8 bits data of 2,097,152 storage cells within the MB85213. Nine row address bits are established on the input pins (A_0 through A_8) and are latched with $\overline{RAS}$. Nine column address bits are established on the input pins and latched with $\overline{CAS}$. All row addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

Write Enable

The read mode or write mode is selected with the $\overline{W}$ input. A high on the $\overline{W}$ selects read mode, low selects write mode. The data inputs are disabled when read mode is selected.

Data Pins

The input and output terminal of each LCC is directly connected on the mother board. The write cycle should be early write cycle in order to avoid data conflict between output data and input data.

Data Input

The 8-bit data are written into the MB85213 through the DQ pins (DQ_0 through DQ_7) during a write (early write) cycle. The falling edge of $\overline{CAS}$ is strobe for the data input register. The set up and hold times are referenced to $\overline{CAS}$.

Data Output

The output buffer of each chip is three state TTL compatible with a fan out of two standard TTL loads. The output are in high impedance state until $\overline{CAS}$ is brought low. In a read cycle, the output is valid after t_{RAC} from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from the falling edge of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to a high.

Nibble Mode

Nibble Mode allows high speed serial read or write access of 2, 3 or 4 bits of data. The data that will be accessed during nibble mode is determined by the 8 row addresses and the 8 column addresses. The 2 bits of addresses (CA_8, RA_8) are used to select 1 of 4 nibble bits for initial access. After the first bit is accessed by normal mode, the following nibble bits can be accessed by toggling $\overline{CAS}$ high then low while $\overline{RAS}$ remains low. Toggling $\overline{CAS}$ causes RA_8 and CA_8 to be incremented internally while all other address bits are held constant. This accesses the next nibble bit in sequence. If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. (See example below.) In the nibble mode, the direction of DQ pins, output or input, is determined by $\overline{W}$ state strobed by $\overline{CAS}$ falling edge on the first normal mode. Therefore, if the first normal mode cycle is write cycle, the direction of DQ pins is input mode during the succeeding nibble cycle regardless of $\overline{W}$ state. And if the first normal mode cycle is read cycle, the followed nibble mode cycles must be read cycle in order to avoid data conflict between input data and output data because the direction of DQ pins is output mode.

Description
(Continued)

Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row addresses (A_0 through A_7) for each chip at least every 4 ms. During refresh, either V_{IL} or V_{IH} is permitted for A_8.

The MB85213 offers the following three types of refresh.

1) $\overline{RAS}$-Only Refresh;
$\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in high impedance state unless CAS is brought low. Strobing each of 256 row addresses with RAS will cause all bits in each row to be refreshed.

2) $\overline{CAS}$-before-$\overline{RAS}$ Refresh;
$\overline{CAS}$-before-$\overline{RAS}$ refresh available on the MB85213 offers an alternate refresh method. If $\overline{CAS}$ is held low for the specified period (t_{FCS}) before the falling edge of RAS, on chip refresh control clock generators and the refresh address counter for each chip are enabled, and an internal refresh operation takes place. After the refresh operation has been executed the refresh address counter is automatically incremented for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

3) Hidden Refresh;
Hidden refresh may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. In MB85213, hidden refresh means $\overline{CAS}$-before-$\overline{RAS}$ refresh and the internal refresh addresses are used, that is, no external refresh address is needed.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then goes low again while $\overline{RAS}$ is held low, the read and write operations are enabled. This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell address (consisting of a row address (9 bits) and a column address (9 bits)) to be accessed can be defined as follows:

1) A ROW ADDRESS—Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set high internally.
2) A COLUMN ADDRESS—All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of CAS.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Procedure

The timing, as shown in $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle, is used for all operations described as follows:

1) Initialize the internal refresh counter. For this operation, the 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
2) Write a test pattern of lows into memory cells at a single column address and 256 row addresses.
3) By using read-modify-write cycle, read the lows written at the last step and write a new high in the same cycle. This cycle is repeated 256 times, and highs are written into the 256 memory cells.
4) Read the high written at the last step.
5) Compliment the test pattern and repeat the steps 2, 3 and 4.

Nibble Mode Address Sequence Example

SEQUENCE	NIBBLE BIT	RA_8	ROW ADDRESS	CA_8	COLUMN ADDRESS	
$\overline{RAS}$/$\overline{CAS}$ (normal mode)	1	0	10101010	0	10101010	input addresses
toggle $\overline{CAS}$ (nibble mode)	2	1	10101010	0	10101010	
toggle $\overline{CAS}$ (nibble mode)	3	0	10101010	1	10101010	generated internally
toggle $\overline{CAS}$ (nibble mode)	4	1	10101010	1	10101010	
toggle $\overline{CAS}$ (nibble mode)	1	0	10101010	0	10101010	sequence repeats

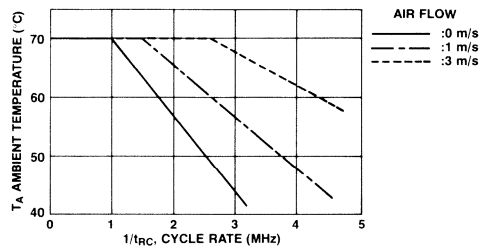
Description
(Continued)

Decoupling and Noise Reduction Recommendations for MB85213

To minimize noise induction between signal lines as well as between signal and power supply lines, good board design practice requires consideration of the following:

1) Provide a capacitor of approx. a few μF for each module—even though the MB85213 has two or four decoupling capacitors of 0.15 μF on each module.
2) Remove noise, overshoot and undershoot from the address, control and data-input lines, so that the MB85213 won't latch wrong signals due to the noise induction between signal lines, and between signal and power supply lines.
3) Keep enough timing margin and remove critical timing in the board design to avoid the problem mentioned in Item 2 above.
4) In order to avoid noise induction on the IN line at the falling edge of $\overline{W}$ when the delayed write or read-modify-write cycle is used, the falling edge of $\overline{W}$ signal should not coincide with the transition point of address and OUT signals. Since decoupling capacitors on the module board can't smooth the output current at the OUT pin, noise is introduced on the power supply line (V_{CC} or V_{SS}) and also on the IN line at t_{RAC} or t_{CAC} in the read cycle.
5) Provide an appropriate damping if necessary, to avoid excessive overshoot or undershoot on the TTL input waveform.

MB85213 Derating Curve



Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C*1
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.4		6.5	V	
Input low voltage	V_{IL}	−2.0		0.8	V	

Note: *1 Maximum ambient temperature is permissible under certain conditions. See figure for derating curve.

Capacitance
(T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input capacitance A_0 to A_8	C_{IN1}		70	pF
Input capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$	C_{IN2}		90	pF
Input capacitance IN	C_{IN3}		17	pF
Output capacitance OUT	C_{OUT}		17	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB85213-12 Min	MB85213-12 Max	MB85213-15 Min	MB85213-15 Max	Unit
Operating current*1 Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		520		456	mA
Standby current Standby power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		36		36	mA
Refresh current 1*1 Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min)	I_{CC3}		440		400	mA
Nibble mode current*1 Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{NC} = min)	I_{CC4}		160		144	mA
Refresh current 2*1 Average power supply current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min.)	I_{CC5}		480		440	mA
Input leakage current Input leakage current, any input ($0 \leq V_{IN} \leq 5.5V$, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)	$I_{I(L)}$	−80	80	−80	80	μA
Output leakage current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)	$I_{O(L)}$	−10	10	−10	10	μA
Output levels Output high voltage (I_{OH} = −5 mA) Output low voltage (I_{OL} = 4.2 mA	V_{OH} V_{OL}	2.4	 0.4	2.4	 0.4	V

Note: *1 I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC Characteristics*1,2,3
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB85213-12 Min	MB85213-12 Max	MB85213-15 Min	MB85213-15 Max	Unit
Time between refresh	t_{REF}		4		4	ms
Random read/write cycle time*12	t_{RC}	230		260		ns
Access time from $\overline{RAS}$*4,5	t_{RAC}		120		150	ns
Access time from $\overline{CAS}$*5,6	t_{CAC}		60		75	ns
Output buffer turn off delay	t_{OFF}	0	25	0	30	ns
Transition time	t_T	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	100		100		ns
$\overline{RAS}$ pulse width	t_{RAS}	120	100000	150	100000	ns
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns

Notes: *1 An initial pause of 200 μs is required after power up. And then several cycles (any 8 cycles to perform refresh are adequate) are required before proper device operation is achieved. If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

*2 AC characteristics assume t_T = 5 ns.

*3 V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).

*4 Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

*5 Assumes that $t_{RCD} \geq t_{RCD}$ (max).

*6 Measured with a load equivalent to 2 TTL loads and 100 pF.

*12 The minimum cycle time is dependent on the ambient temperature and cooling conditions.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB85213-12 Min	MB85213-12 Max	MB85213-15 Min	MB85213-15 Max	Unit
$\overline{CAS}$ pulse width	t_{CAS}	60	100000	75	100000	ns
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ delay time*7,8	t_{RCD}	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ set up time	t_{CRS}	20		20		ns
Row address set up time	t_{ASR}	0		0		ns
Row address hold time	t_{RAH}	12		15		ns
Column address set up time	t_{ASC}	0		0		ns
Column address hold time	t_{CAH}	20		25		ns
Read command set up time	t_{RCS}	0		0		ns
Read command hold time referenced to $\overline{CAS}$*11	t_{RCH}	0		0		ns
Read command hold time referenced to $\overline{RAS}$*11	t_{RRH}	20		20		ns
Write command set up time*9	t_{WCS}	0		0		ns
Write command pulse width	t_{WP}	20		25		ns
Write command hold time	t_{WCH}	20		25		ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	50		60		ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	50		60		ns
Data in set up time	t_{DS}	0		0		ns
Data in hold time	t_{DH}	20		25		ns
$\overline{CAS}$ set up time referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)	t_{FCS}	25		30		ns
$\overline{CAS}$ hold time referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$)	t_{FCH}	25		30		ns
$\overline{RAS}$ precharge to $\overline{CAS}$ active time ($\overline{CAS}$-before-$\overline{RAS}$)	t_{RPC}	20		20		ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$)	t_{CPR}	25		30		ns
Nibble mode read/write cycle time	t_{NC}	65		80		ns
Nibble mode access time	t_{NCAC}		30		40	ns
Nibble mode $\overline{CAS}$ pulse width	t_{NCAS}	30		40		ns
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	25		30		ns

Notes: *7 Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

*8 t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T = 5 ns) + t_{ASC} (min).

*9 t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout entire cycle.

*11 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

AC Characteristics

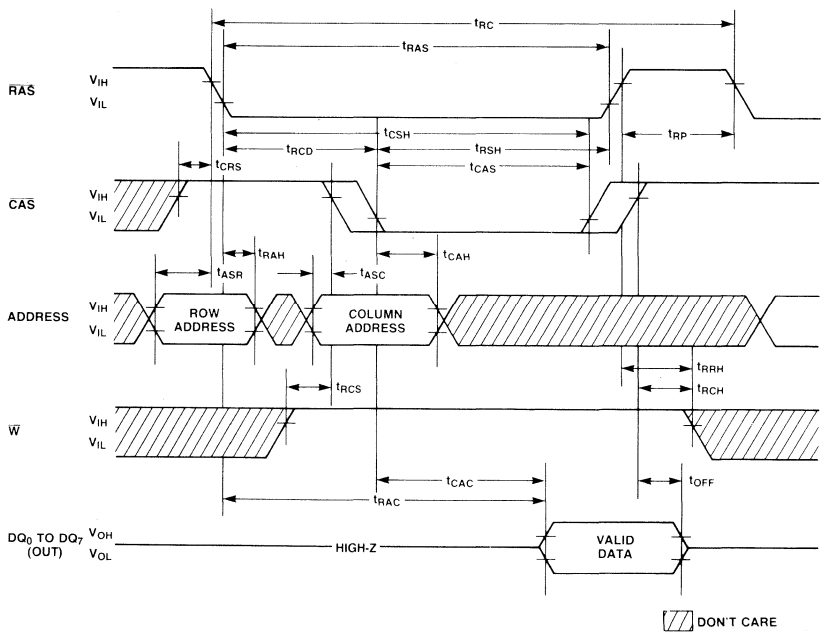
(Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB85213-12 Min	MB85213-12 Max	MB85213-15 Min	MB85213-15 Max	Unit
Nibble mode read $\overline{RAS}$ hold time	t_{NRRSH}	30		40		ns
Nibble mode write $\overline{RAS}$ hold time	t_{NWRSH}	50		60		ns
Nibble mode $\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{RNH}	20		20		ns
Refresh counter test cycle time*10	t_{RTC}	360		415		ns
Refresh counter test $\overline{RAS}$ pulse width*10	t_{TRAS}	250	10000	305	10000	ns
Refresh counter test $\overline{CAS}$ precharge time*10	t_{CPT}	60		70		ns

Notes: *10 Test mode write cycle only.

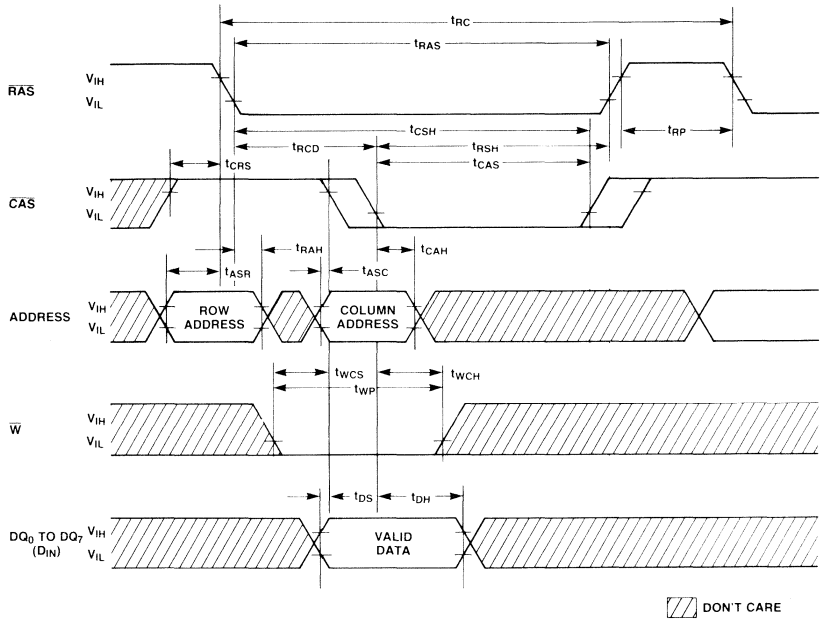
Timing Diagrams

Read Cycle

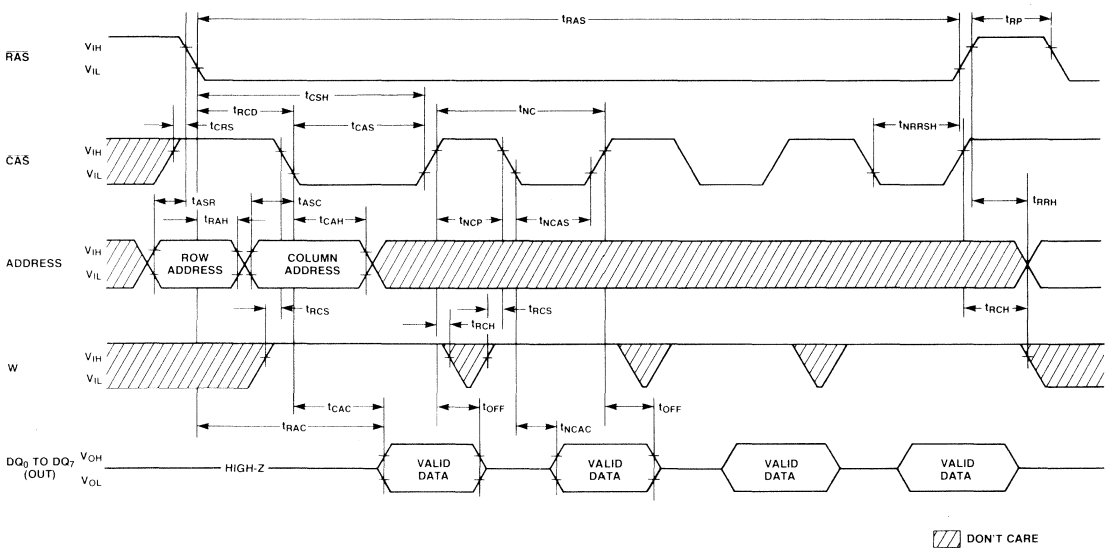


Timing Diagrams
(Continued)

Write Cycle

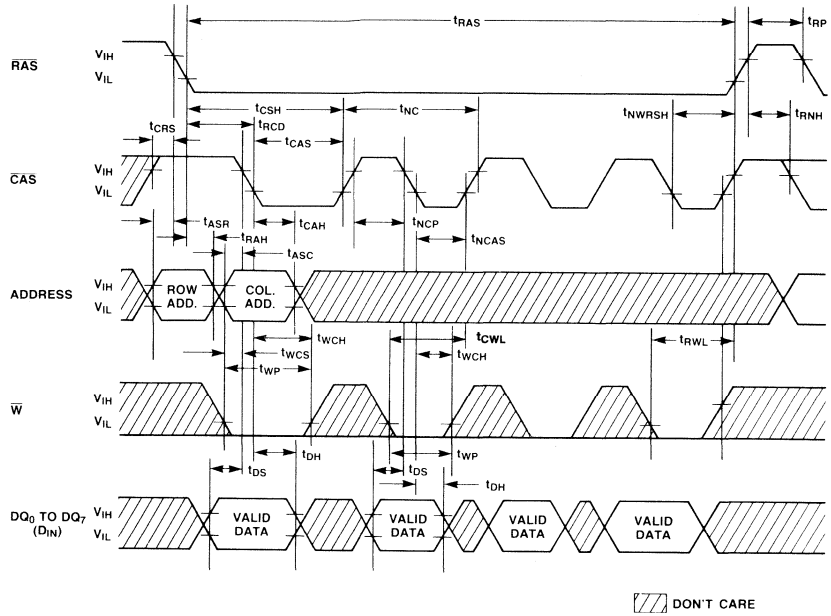


Nibble Mode Read Cycle



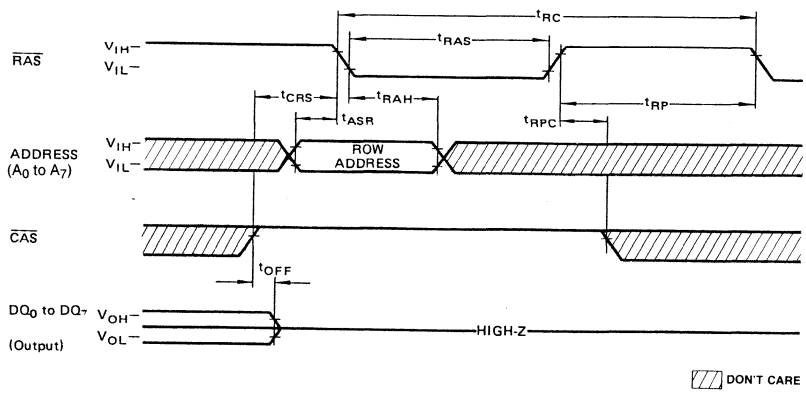
Timing Diagrams
(Continued)

Nibble Mode Write Cycle



RAS-only Refresh Cycle

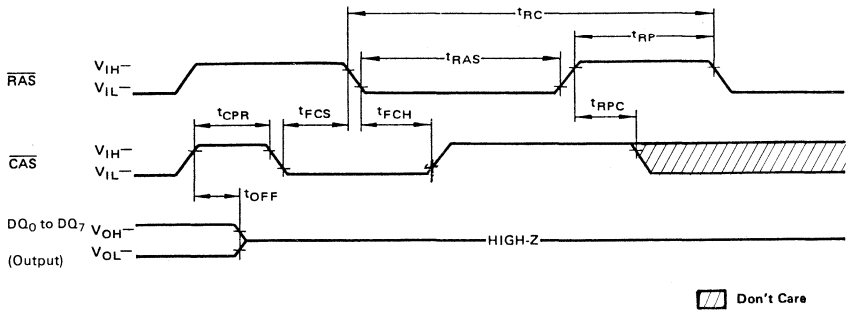
Note: $\overline{W}$ = Don't Care, $A_8 = V_{IH}$ or V_{IL}



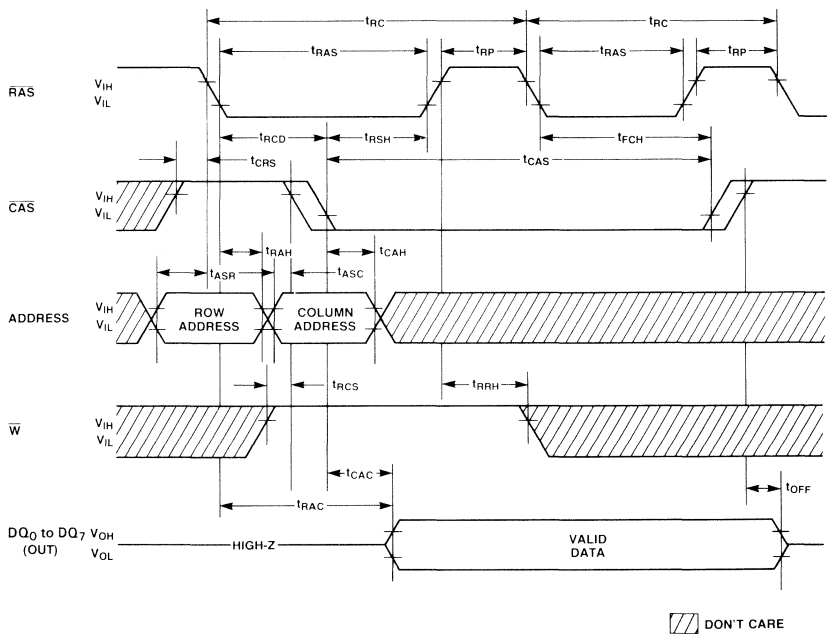
Timing Diagrams
(Continued)

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

Note: Address, $\overline{WE}$ = Don't Care

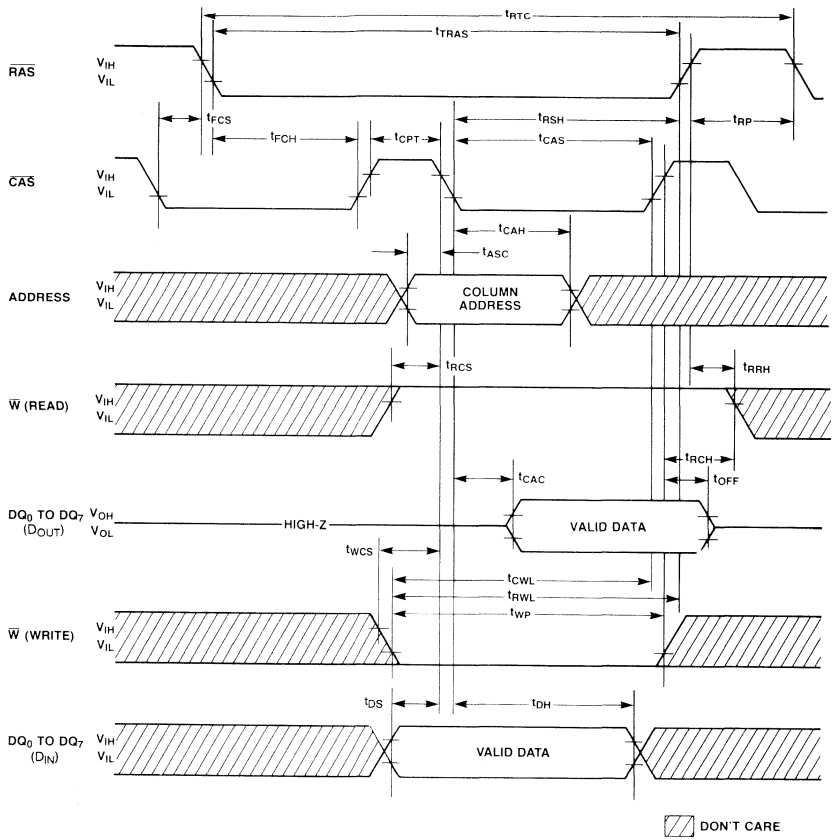


Hidden Refresh Cycle



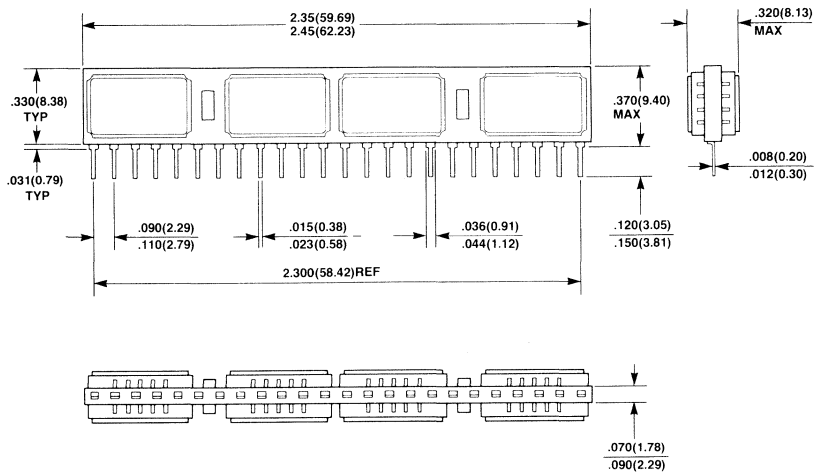
Timing Diagrams
(Continued)

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle



Package Dimensions
Dimensions in Inches
(millimeters)

24-Lead Single In-Line Package Module
(Module No.: MSP-24S-CC02)



Preliminary

MOS Memories

FUJITSU

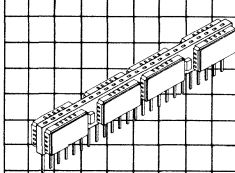
■ MB85214-12, MB85214-15

MOS 262,144 x 8-Bit
Dynamic Random Access
Memory Module

Description

The Fujitsu MB85214 is a fully decoded, 262,144 word x 8-bit NMOS dynamic random access memory module consisting of eight MB81256 DRAMs in 18-pad LCC packages mounted on a 24-pin multilayer ceramic substrate.

The MB85214 is intended for use in memory applications where large memory capacity is required within limited physical volume. Significant size reduction can be realized in applications such as mainframe memory, buffer memory, desk top computers and peripheral storage.



MSP-24S-CC02

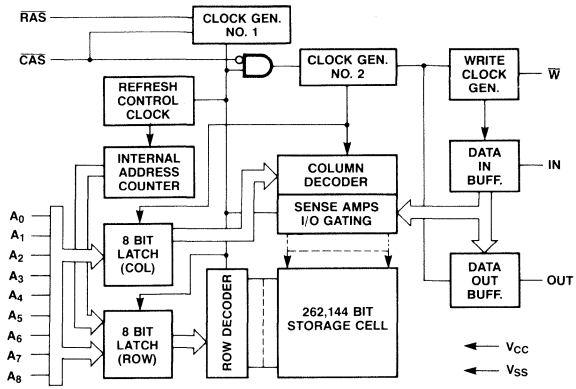
Features

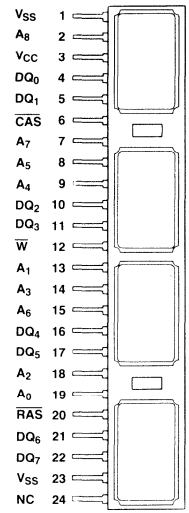
- **262,144 x 8 DRAM 24-pin SIP (MB81256 x 8)**
- **Row access time**
  120 ns max. (MB85214-12)
  150 ns max. (MB85214-15)
- **Cycle time**
  230 ns min. (MB85214-12)
  260 ns min. (MB85214-15)
- **Page Cycle Time**
  120 ns min. (MB85214-12)
  150 ns min. (MB85214-15)
- **Single +5V supply, ±10% tolerance**
- **Low power (active)**
  2860 mW max. (MB85214-12)
  2508 mW max. (MB85214-15)
  198 mW max. (Standby)
- **4 ms/256 cycle refresh**
- **$\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$ and hidden refresh capability**
- **Page mode capability**
- **On-chip latches for addresses and data-in**
- **All inputs and outputs are TTL compatible**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

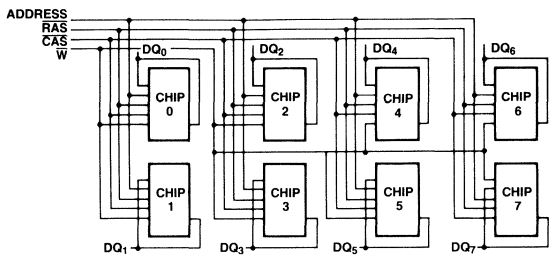
MB85214 Block Diagrams and Pin Assignment

Block Diagram for Each Chip





Functional Block Diagram



FUNCTIONAL TRUTH TABLE

$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	DQ_0 to DQ_7	Function
H	H	Don't care	High-Z	Standby
L	L	H	Valid data out *1	Read cycle
L	L	L	Valid data in *2	Write cycle
L	L	Don't care	High-Z	$\overline{CAS}$-before-$\overline{RAS}$ refresh cycle *3
L	H	Don't care	High-Z	$\overline{RAS}$-only refresh cycle

Notes: *1 DQ pins are output mode.
*2 DQ pins are input mode.
*3 $t_{FCS} \geq t_{FCS}$ (min).

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Storage temperature	T_{STG}	−55 to +150	°C
Power dissipation	P_D	8.0	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Description

Simple Timing Requirement:

The MB85214 has improved circuitry that eases timing requirements for high speed access operations. The MB85214 can operate under the condition of t_{RCD} (max) = t_{CAC} thus providing optimal timing for address multiplexing. In addition, the MB85214 has the minimal hold times of address (t_{CAH}), $\overline{W}$ (t_{WCH}) and IN (t_{DH}). The MB85214 provides higher throughput in interleaved memory system applications. Fujitsu has made timing requirement that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, and t_{DHR}. As a result, the hold times of the column address, IN and $\overline{W}$ are not restricted by t_{RCD}.

Address Inputs

A total of eighteen binary input address bits are required to decode any 8-bits of data in 2,097,152 locations within the MB85214.

Nine row address bits are established on the input pins (A_0 through A_8) and are latched with $\overline{RAS}$.

Nine column address bits are established on the input pins and latched with $\overline{CAS}$. All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

Write Enable

The read mode or write mode is selected with the $\overline{W}$ input. A high on the $\overline{W}$ selects read mode, low selects write mode. The data inputs are disabled when read mode is selected.

Data Pins

The input and output terminal of each LCC is directly connected on the mother board to reduce the number of I/0 pins. The write cycle should be early write cycle in order to avoid conflict between output data and input data.

Data Input

The 8-bit data are written into the MB85214 during a write (early write) cycle. The falling edge of $\overline{CAS}$ is strobe for the data input register.

The set up and hold times are referenced to $\overline{CAS}$.

Data Output

The output buffer of each chip is three state TTL compatible with a fan out of two standard TTL loads.

The output is in high impedance state until $\overline{CAS}$ is brought low. In a read cycle, the output is valid after t_{RAC} from the falling edge of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from the falling edge of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to a high level.

Page-Mode

Page-mode operation permits strobing the row-address into the MB85214 while maintaining $\overline{RAS}$ at low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the falling edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of 256 row addresses (A_0 ~ A_7) at least every 4 ms. During refresh, either V_{IL} or V_{IH} is permitted for A_8.

The MB85214 offers the following three types of refresh.

1. $\overline{RAS}$-Only Refresh; $\overline{RAS}$-Only refresh avoids any output during refresh because the output buffer is in high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 row addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed.
2. $\overline{CAS}$-before-$\overline{RAS}$ Refresh; $\overline{CAS}$-before-$\overline{RAS}$ refresh available on the MB85214 offers an alternate refresh method. If $\overline{CAS}$ is held low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter for each chip are enabled, and an internal refresh operation takes place. After the refresh operation has been executed the refresh address counter is automatically incremented for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. So, by performing 256 cycles for $\overline{CAS}$-before-$\overline{RAS}$ refresh, all bits in a module are refreshed.

Description
(Continued)

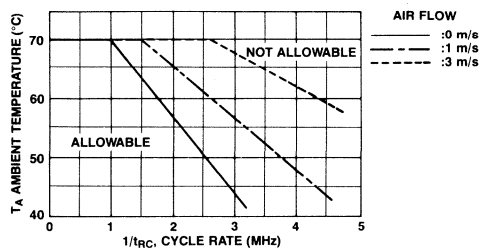
3. Hidden Refresh;
   Hidden refresh may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. In the MB85214, hidden refresh means $\overline{CAS}$-before-$\overline{RAS}$ refresh and the internal refresh addresses are used, that is, no external refresh address is needed.

Decoupling and Noise Reduction Reocmmendations for MN85214

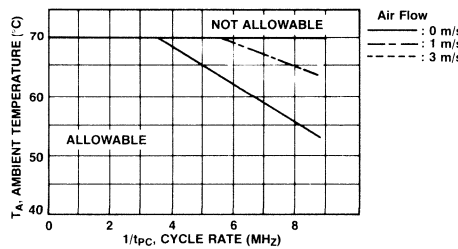
To minimize noise induction between signal lines as well as between signal and power supply lines, good board design practice requires consideration of the following:

1. Provide a capacitor for approx. a few μF for each module, though the MB85214 has four decoupling capacitors of 0.15μF on the each modules.
2. Remove noise, overshoot and undershoot from the address, control and DQ lines, so that the MB85214 won't latch wrong signals due to the noise induction between signal lines, and between signal and power supply lines.
3. Keep enough timing margin and remove critical timing in the board design, to avoid the problem mentioned in the above item 2.
4. Provide an appropriate damping if necessary, to avoid excessive overshoot or undershoot on the TTL input waveforms.

MB85214 Derating Curve (Normal Cycle)



MB85214 Derating Curve (Page Mode Cycle)



Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C*1
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.4		6.5	V	
Input low voltage	V_{IL}	−2.0		0.8	V	

Note: *1 Maximum ambient temperature is permissible under certain conditions. See the derating curves for normal cycle and page mode cycle.

Capacitance
(T_A = 25°C)

Parameter	Symbol	Typ	Max	Unit
Input capacitance A_0 to A_8	C_{IN1}		70	pF
Input capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$	C_{IN2}		90	pF
Input capacitance IN	C_{IN3}		17	pF
Output capacitance OUT	C_{OUT}		17	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
Operating current*1 Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	MB85214-12 MB85214-15	I_{CC1}		520 456	mA
Standby current Standby power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}		36	mA
Refresh current 1*1 Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	MB85214-12 MB85214-15	I_{CC3}		440 400	mA
Page mode current*1 Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	MB85214-12 MB85214-15	I_{CC4}		240 200	mA
Refresh current 2*1 Average power supply current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min.)	MB85214-12 MB85214-15	I_{CC5}		480 440	mA
Input leakage current Input leakage current, any input (0 ≤ V_{IN} ≤ 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)		$I_{I(L)}$	−80	80	μA
Output leakage current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		$I_{O(L)}$	−10	10	μA
Output levels Output high voltage (I_{OH} = −5 mA) Output low voltage (I_{OL} = 4.2 mA)		V_{OH} V_{OL}	2.4	0.4	V

Note: *1 I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC Characteristics*1,2,3
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB85214-12 Min	MB85214-12 Max	MB85214-15 Min	MB85214-15 Max	Unit
Time between refresh	t_{REF}		4		4	ms
Random read/write cycle time*4	t_{RC}	230		260		ns
Access time from $\overline{RAS}$*5,6	t_{RAC}		120		150	ns

Notes:: *1 An initial pause of 200 μs is required after power-up, followed by any 8 cycles, before proper device operation is achieved. If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
*2 AC characteristics assume t_T 5 ns.
*3 V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min.) and V_{IL} (max.).
*4 The minimum cycle time is dependent on the ambient temperature and cooling conditions. See the Normal Cycle derating curve.
*5 Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
*6 Measured with a load equivalent of 2 TTL loads and 100 pF.

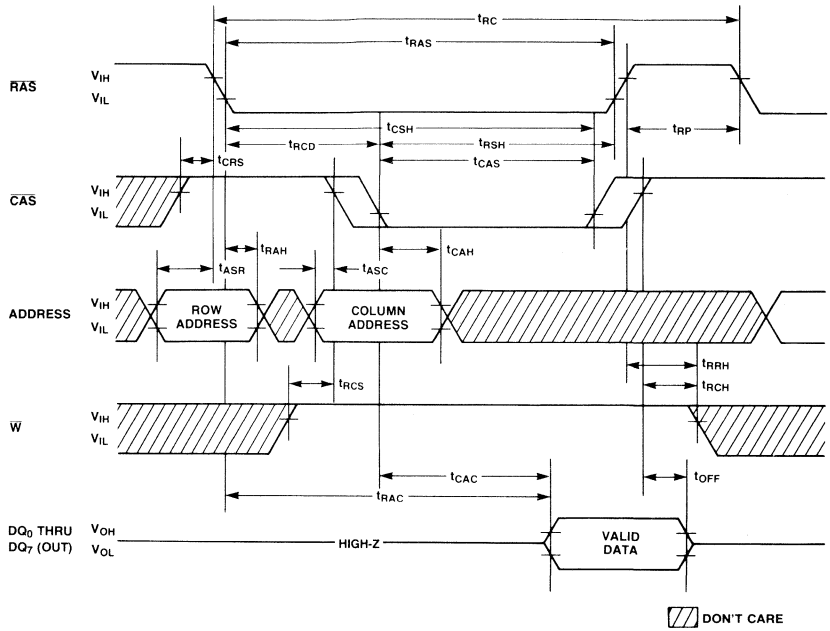
AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB85214-12 Min	MB85214-12 Max	MB85214-15 Min	MB85214-15 Max	Unit
Access time from $\overline{CAS}$*6,7	t_{CAC}		60		75	ns
Output buffer turn off delay	t_{OFF}	0	25	0	30	ns
Transition time	t_T	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	100		100		ns
$\overline{RAS}$ pulse width	t_{RAS}	120	100000	150	100000	ns
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns
$\overline{CAS}$ pulse width	t_{CAS}	60	100000	75	100000	ns
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ delay time*8,9	t_{RCD}	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ set up time	t_{CRS}	20		20		ns
Row address set up time	t_{ASR}	0		0		ns
Row address hold time	t_{RAH}	12		15		ns
Column address set up time	t_{ASC}	0		0		ns
Column address hold time	t_{CAH}	20		25		ns
Read command set up time	t_{RCS}	0		0		ns
Read command hold time referenced to $\overline{CAS}$*10	t_{RCH}	0		0		ns
Read command hold time referenced to $\overline{RAS}$*10	t_{RRH}	20		20		ns
Write command set up time	t_{WCS}	0		0		ns
Write command pulse width	t_{WP}	20		25		ns
Write command hold time	t_{WCH}	20		25		ns
Data in set up time	t_{DS}	0		0		ns
Data in hold time	t_{DH}	20		25		ns
Refresh set up time for $\overline{CAS}$ referenced to RAS ($\overline{CAS}$-before-$\overline{RAS}$-cycle)	t_{FCS}	25		30		ns
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$-cycle)	t_{FCH}	25		30		ns
$\overline{RAS}$ precharge to $\overline{CAS}$ active time (refresh cycle)	t_{RPC}	20		20		ns
Page mode read/write cycle time*11	t_{PC}	120		150		ns
Page mode $\overline{CAS}$ precharge time	t_{CP}	50		65		ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CPR}	25		30		ns

Notes:
*7 Assumes that $t_{RCD} \geq t_{RCD}$ (max).
*8 Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
*9 t_{RCD} (min) = t_{RAH} (min) + $2t_T$ (t_T = 5 ns) + t_{ASC} (min).
*10 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
*11 The minimum cycle time is dependent on the ambient temperature and cooling conditions. See the Page Mode Cycle derating curve.

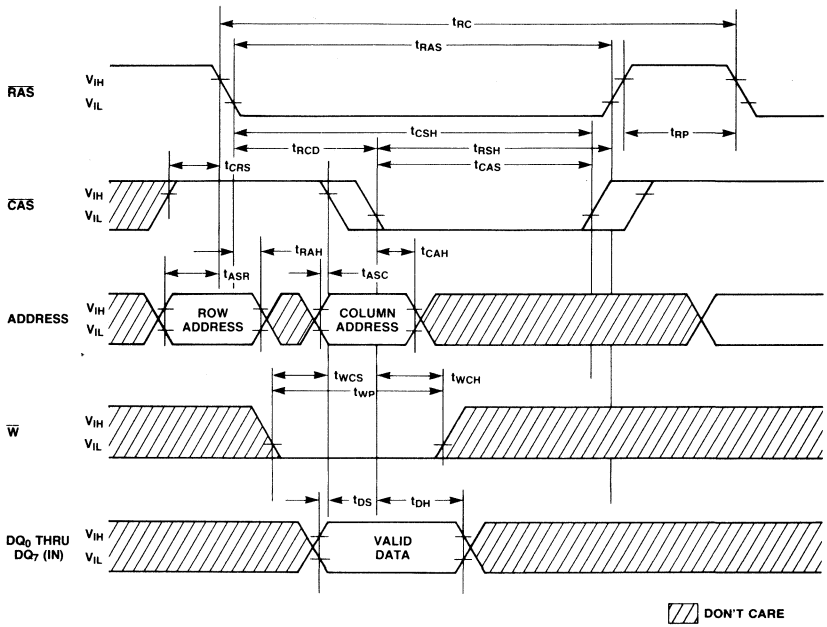
Timing Diagrams

Read Cycle



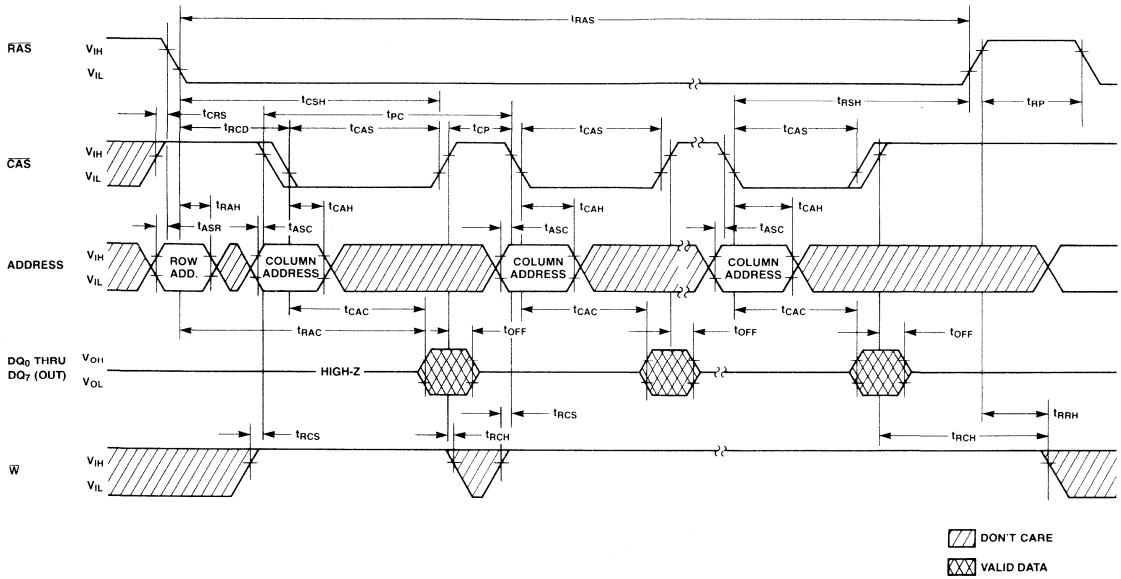
Timing Diagrams
(Continued)

Write Cycle (Early Write)

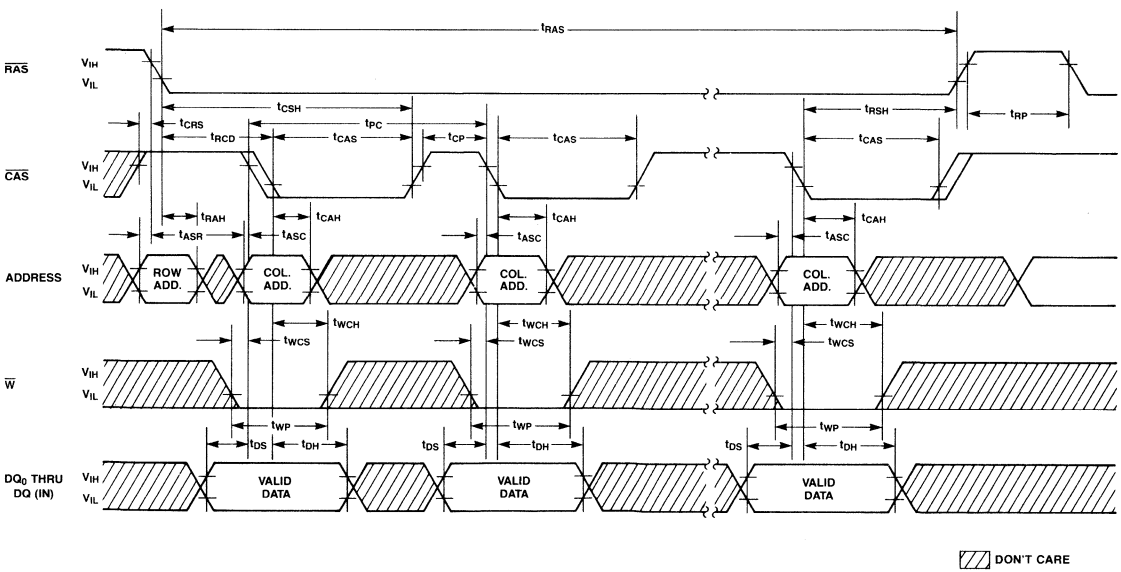


Timing Diagrams
(Continued)

Page Mode Read Cycle

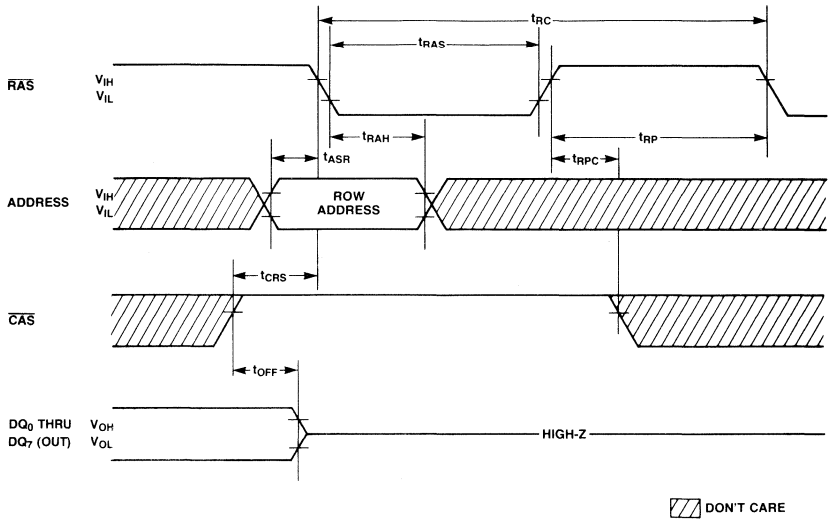


Page Mode Write Cycle

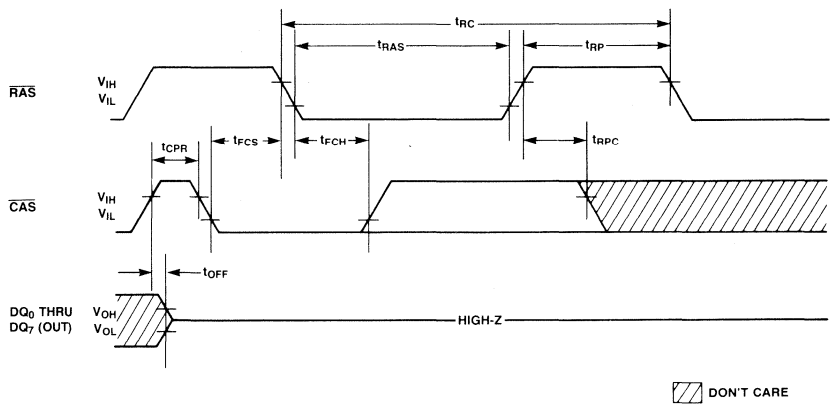


Timing Diagrams
(Continued)

$\overline{RAS}$-only Refresh Cycle
Note: $\overline{W}$ = Don't Care

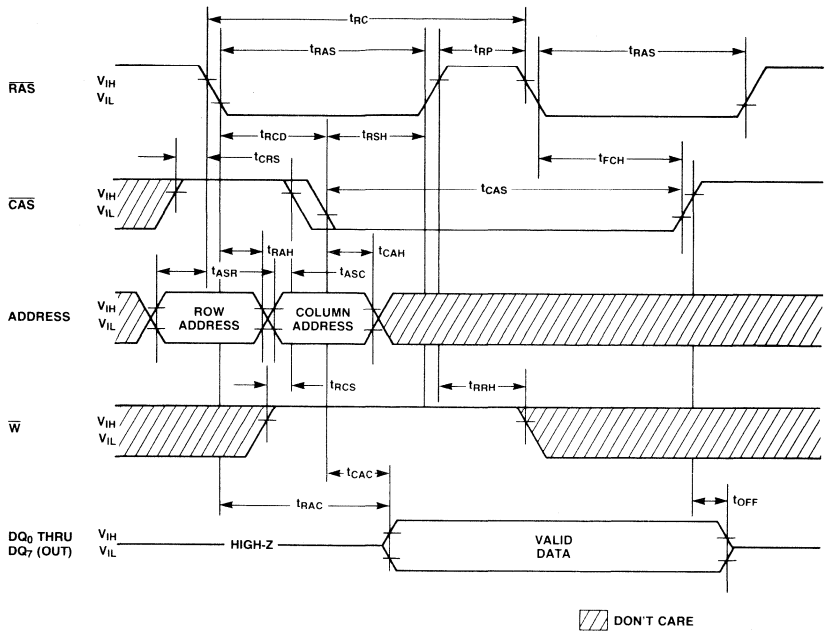


$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle
Note: Address $\overline{W}$ = Don't Care



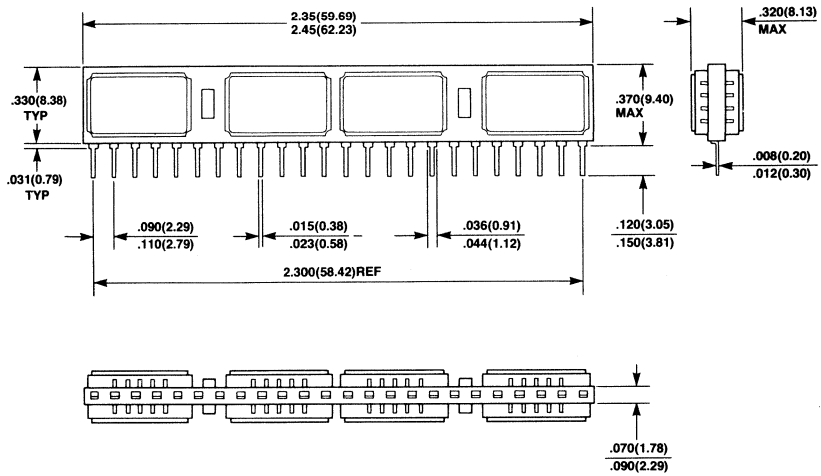
Timing Diagrams
(Continued)

Hidden Refresh Cycle



Package Dimensions
Dimensions in inches
(millimeters)

24-Lead Single In-Line Package Module
(Module No.: MSP-24S-CC02)



Preliminary

MOS Memories

FUJITSU

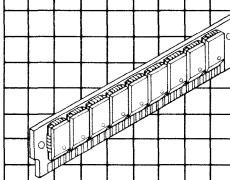
■ MB85227-12, MB85227-15

262,144 x 9-Bit
Dynamic Random Access
Memory Module

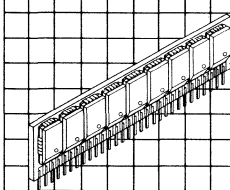
Description

The Fujitsu MB85227 is a fully decoded, 262,144 word x 9-bit NMOS dynamic random access memory module consisting of nine MB81256 DRAMs in 18-lead plastic LCC packages mounted on a 30-pin Single-In Line Package (SIP).

The MB85227 is intended for use in memory applications utilizing parity where large memory capacity is required within limited physical volume. Significant size reduction can be realized in applications such as mainframe memory, buffer memory, desk top computers and peripheral storage.



MSS-30P-P01 (PDPB)



MSP-30P-P01 (PDPS)

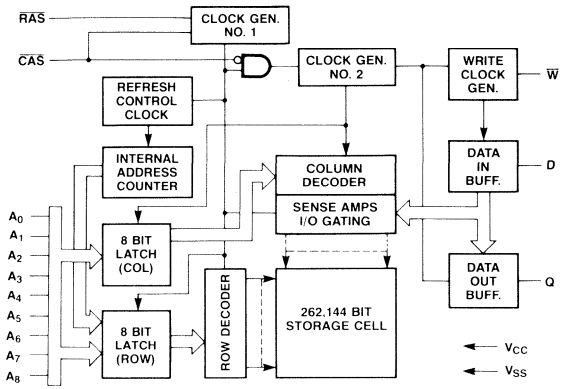
Features

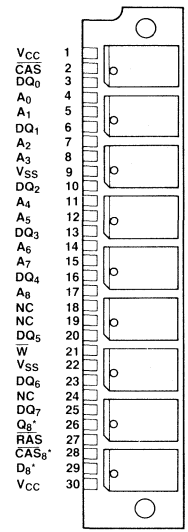
- **262,144 x 9 DRAM 30-pin SIP (MB81256 x 9)**
- **Row access time**
  120 ns max. (MB85227-12)
  150 ns max. (MB85227-15)
- **Cycle time**
  230 ns min. (MB85227-12)
  260 ns min. (MB85227-15)
- **Page cycle time**
  120 ns min. (MB85227-12)
  150 ns min. (MB85227-15)
- **Single + 5V supply, ±10%tolerance**
- **Low power (active)**
  3218 mW max. (MB85227-12)
  2822 mW max. (MB85227-15)
  226 mW max. (Standby)
- **4 ms 256 cycle refresh**
- **$\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$ and Hidden refresh capability**
- **Page mode capability**
- **On-chip latches for Addresses and Data-in**
- **All inputs and outputs are TTL compatible**
- **(D_8, Q_8) is generally used for parity and is controlled by $\overline{CAS}_8$**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB85227 Block Diagrams and Pin Assignment

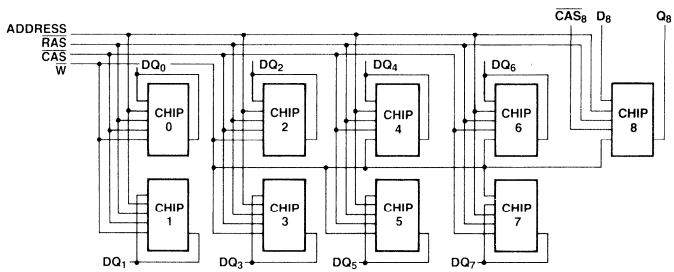
Block Diagram For Each Chip





*; For parity bit.

Functional Block Diagram



FUNCTIONAL TRUTH TABLE

$\overline{RAS}$	$\overline{CAS}$ and $\overline{CAS_8}$	$\overline{WE}$	DQ_0 to DQ_7, D_8 and Q_8	Function
H	H	Don't Care	High-Z	Standby
L	L	H	Valid Data Out1)	Ready Cycle
L	L	L	Valid Data In2)	Write Cycle
L	L3)	Don't Care	High-Z	$\overline{CAS}$-before $\overline{RAS}$ Refresh cycle
L	H	Don't Care	High-Z	$\overline{RAS}$-only Refresh cycle
L	H ($\overline{CAS}$) L ($\overline{CAS_8}$)	H → L4)	High-Z (DQ_0 to DQ_7) Valid Data In (D_8) Valid Data Out (Q_8)	$\overline{RAS}$-only Refresh cycle (Except for Parity bit) Read-Write/Read-Modify-Write (Parity bit)

Notes 1): DQ Pins are output mode.
2): DQ pins are input mode.
3): $t_{FCS} \geq t_{FCS}$ (min).
4): $t_{CWD} \geq t_{CWD}$ (min).

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Storage temperature	T_{STG}	−55 to 125	°C
Power dissipation	P_D	4.5	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Description

Simple Timing Requirement

The MB85227 has improved circuitry that eases timing requirements for high speed access operations. The MB85227 can operate under the condition of t_{RCD} (max.) = t_{CAC}, thus providing optimal timing for address multiplexing. In addition, the MB85227 has minimal hold times of address (t_{CAH}), $\overline{W}$ (t_{WCH}) and D (t_{DH}). Fujitsu has made timing requirements that are referenced to $\overline{RAS}$ non-restrictive and deleted them from the data sheet. These include t_{AR}, t_{WCR}, and t_{DHR}. As a result, the hold times of the column address. D and $\overline{W}$ are not restricted by t_{RCD}.

Address Inputs

A total of eighteen binary input address bits are required to decode any 9-bits of data in 2359296 storage cells within the MB85227.

Nine row address bits are established on the input pins (A_0 through A_8) and latched with $\overline{RAS}$.

Nine column address bits are established on the input pins and latched with $\overline{CAS}$. All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row addresses to column addresses.

Write Enable

The read mode or write mode is selected with the $\overline{W}$ input. A logic "high" on the $\overline{W}$ dictates read mode. A logic "low" dictates write mode. Data inputs are disabled when read mode is selected.

Data Pins

The input and output pins of each PLCC except for parity bit are directly connected on the mother board to minimize the number of I/O pins. The write cycle should be early write cycle in order to avoid data conflict between output data and input data. However, it is possible to execute read-modify-write cycle on the parity bit because the input and output of parity bit are separated.

Data Input

The 9-bit data are written through the DQ pins (DQ_0 to DQ_7 and D_8) during write (early write) cycle.

The falling edge of $\overline{CAS}$ is triggered by the data input register. The set up and hold times are referenced to $\overline{CAS}$.

Data Output

The output buffer of each chip is three-state TTL compatible with a fan out of two standard TTL loads.

The outputs are in high impedance state until $\overline{CAS}$ is brought low. In a read cycle, the output is valid after t_{RAC} from the transition of $\overline{RAS}$ when t_{RCD} (max.) is satisfied, or after t_{CAC} from the transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.). Data remain valid until $\overline{CAS}$ is returned to high.

Page-Mode

Page-mode operation permits strobing the row-address into the MB85227 while maintaining $\overline{RAS}$ at a logic low throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the falling edge of $\overline{RAS}$ is saved. Access and cycle times are decreased because the time normally required to strobe a new row address is eliminated.

Refresh

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of 256 row addresses (A_0 through A_7) at least every 4 ms. During refresh, either V_{IL} or V_{IH} is permitted for A_8.

The MB85227 offers the following three types of refresh.

1) $\overline{RAS}$-Only Refresh; $\overline{RAS}$-Only refresh avoids any output during refresh because the output buffer is in high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 row addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed.
2) $\overline{CAS}$-before-$\overline{RAS}$ Refresh; $\overline{CAS}$-before-$\overline{RAS}$ refresh available on the MB85227 offers an alternate refresh method. If $\overline{CAS}$ is held "low" for the specified period (t_{FCS}) before $\overline{RAS}$ goes "low", on chip refresh control clock generators and the refresh address counter for each chip are enabled, and an internal refresh operation takes place.

Description
(continued)

After the refresh operation has been executed the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation. So, by performing 256 cycles for $\overline{CAS}$-before-$\overline{RAS}$ refresh, all bits in a module are refreshed.

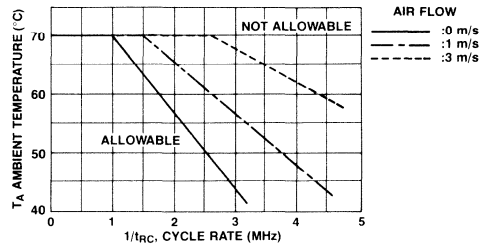
3) Hidden Refresh;
Hidden refresh may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. For the MB85227 a hidden refresh cycle is a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle and the internal refresh addresses are used. No external refresh address is needed.

Decoupling and Noise Reduction Recommendations for MB85227

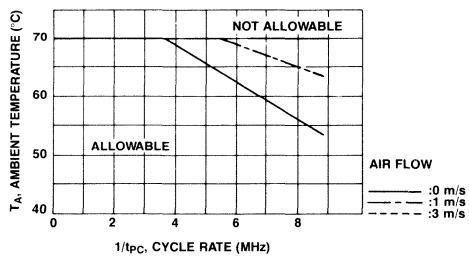
To minimize noise induction between signal lines as well as between signal and power supply lines, good board design practice requires consideration of the following:

1. Provide a capacitor of approximately a few μF for each module, even though the MB85227 has the decoupling capacitors of 0.15 μF on each module. (0.22 μF x 9)
2. Remove noise, overshoot and undershoot from the address, control and DQ lines, so that the MB85227 will not latch spurious signals due to the noise induction between signal lines and between signal and power supply lines.
3. Keep enough timing margin and remove critical timing in the board design, to avoid the problem mentioned in the above item 2.
4. Provide an appropriate damping if necessary, to avoid excessive overshoot or undershoot on the TTL input waveforms.

MB85227 Derating Curve Normal Cycle



MB85227 Derating Curve Page Mode Cycle



Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C*1
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.4		6.5	V	
Input low voltage	V_{IL}	−2.0		0.8	V	

Note: *1 Maximum ambient temperature is permissible under certain conditions. See the derating curves for normal cycle and for page mode cycle.

Capacitance
(T_A = 25°C, f = 1MHz)

Parameter	Symbol	Typ	Max	Unit
Input capacitance, A_0 to A_8	C_{IN1}		75	pF
Input capacitance, $\overline{RAS}$	C_{IN2}		80	pF
Input capacitance, $\overline{CAS}$	C_{IN3}		70	pF
Input capacitance, $\overline{W}$	C_{IN4}		55	pF
Input capacitance, $\overline{CAS}_8$	C_{IN5}		10	pF
Input capacitance, D_8	C_{IN6}		7	pF
I/O capacitance, DQ_0 to DQ_7	C_{IO}		17	pF
Output capacitance, Q_8	C_0		12	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
Operating current*1 average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	MB85227-12	I_{CC1}		585	mA
	MB85227-15			513	
Standby current standby power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}		41	mA
Refresh current 1*1 average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	MB85227-12	I_{CC3}		495	mA
	MB85227-15			450	
Page mode current*1 average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	MB85227-12	I_{CC4}		270	mA
	MB85227-15			225	
Refresh current 2*1 average power supply current ($\overline{CAS}$-before-$\overline{RAS}$: t_{RC} = min.)	MB85227-12	I_{CC5}		540	mA
	MB85227-15			495	
Input leakage current (except for DQ_0 ~ DQ_7) input leakage current, any input (0 ≤ V_{IN} ≤ 5.5V, V_{CC} = 5.5V, V_{SS} = 0V, all other pins not under test = 0V)		$I_{I(L)1}$ (CAS_8, D_8)	−10	10	μA
		$I_{I(L)2}$ (others)	−90	90	
DQ and Q_8 leakage current (data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V) each DQ is high impedance		$I_{O(L)}$	−10	10	μA
Output levels output high voltage (I_{OH} = −5 mA) output low voltage (I_{OL} = 4.2 mA)		V_{OH}	2.4		V
		V_{OL}		0.4	

Note: *1 I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

AC Characteristics[*1,2,3]
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB85227-12 Min	MB85227-12 Max	MB85227-15 Min	MB85227-15 Max	Unit
Time between refresh	t_{REF}		4		4	ms
Random read/write cycle time[*4]	t_{RC}	230		260		ns
Access time from $\overline{RAS}$[*5,6]	t_{RAC}		120		150	ns
Access time from $\overline{CAS}$[*6,7]	t_{CAC}		60		75	ns
Output buffer turn off delay	t_{OFF}	0	25	0	30	ns
Transition time	t_T	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	100		100		ns
$\overline{RAS}$ pulse width	t_{RAS}	120	100000	150	100000	ns
$\overline{RAS}$ hold time	t_{RSH}	60		75		ns
$\overline{CAS}$ pulse width	t_{CAS}	60	100000	75	100000	ns
$\overline{CAS}$ hold time	t_{CSH}	120		150		ns
$\overline{RAS}$ to $\overline{CAS}$ delay time[*8,9]	t_{RCD}	22	60	25	75	ns
$\overline{CAS}$ to $\overline{RAS}$ set up time	t_{CRS}	20		20		ns
Row address set up time	t_{ASR}	0		0		ns
Row address hold time	t_{RAH}	12		15		ns
Column address set up time	t_{ASC}	0		0		ns
Column address hold time	t_{CAH}	20		25		ns
Read command set up time	t_{RCS}	0		0		ns
Read command hold time referenced to $\overline{CAS}$[*10]	t_{RCH}	0		0		ns
Read command hold time referenced to $\overline{RAS}$[*10]	t_{RRH}	20		20		ns
Write command set up time	t_{WCS}	0		0		ns
Write command pulse width	t_{WP}	20		25		ns
Write command hold time	t_{WCH}	20		25		ns
Data in set up time	t_{DS}	0		0		ns
Data in hold time	t_{DH}	20		25		ns
Refresh set up time for $\overline{CAS}$ referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$-cycle)	t_{FCS}	25		30		ns
Refresh hold time for CAS referenced to $\overline{RAS}$ ($\overline{CAS}$-before-$\overline{RAS}$-cycle)	t_{FCH}	25		30		ns

Notes:

*1 An initial pause of 200 μs is required after power-up, followed by any 8 cycles before proper device operation is achieved. If internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

*2 AC characteristics assume t_T = 5 ns.

*3 V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min.) and V_{IL} (max.).

*4 The minimum cycle time is dependent on the ambient temperature and cooling conditions. See Normal Cycle Diagram for derating curve.

*5 Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

*6 Measured with a load equivalent to 2 TTL loads and 100 pF.

*7 Assumes that $t_{RCD} \geq t_{RCD}$ (max.).

*8 Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.

*9 t_{RCD} (min.) $= t_{RAH}$ (min.) + $2t_T$ (t_T = 5 ns) + t_{ASC} (min.).

*10 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

AC Characteristics

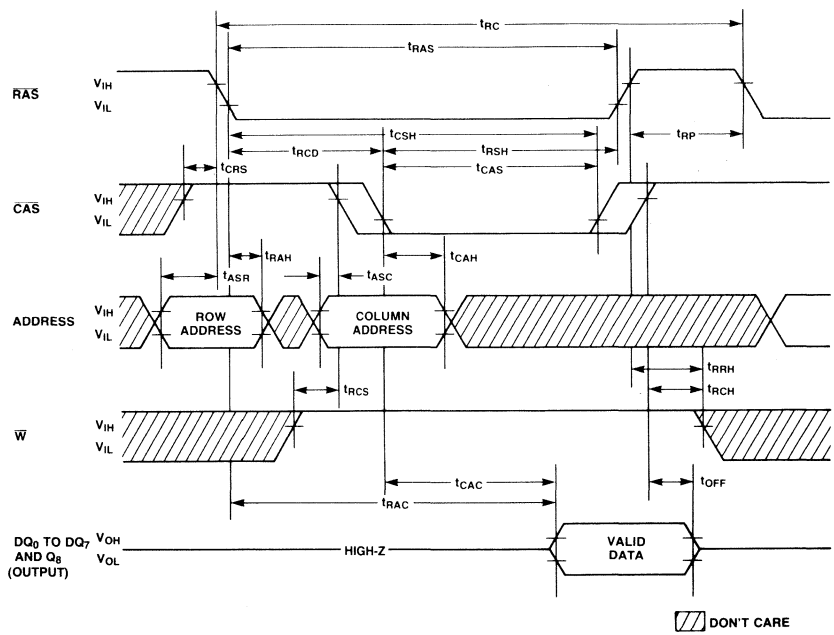
(Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB85227-12 Min	MB85227-12 Max	MB85227-15 Min	MB85227-15 Max	Unit
$\overline{RAS}$ precharge to $\overline{CAS}$ active time (refresh cycle)	t_{RPC}	20		20		ns
Page mode read/write cycle time*11	t_{PC}	120		150		ns
Page mode $\overline{CAS}$ precharge time	t_{CP}	50		65		ns
$\overline{CAS}$ precharge time ($\overline{CAS}$-before-$\overline{RAS}$ cycle)	t_{CPR}	25		30		ns
Write command to $\overline{RAS}$ lead time*12	t_{RWL}	50		60		ns
Write command to $\overline{CAS}$ lead time*12	t_{CWL}	50		60		ns
$\overline{CAS}$ to $\overline{W}$ delay time*12	t_{CWD}	20		25		ns
Read-write cycle time*12	t_{RWC}	230		260		ns

Notes: *11 The minimum cycle time is dependent on the ambient temperature and cooling conditions. See Fig. 4 for derating curve.
*12 Only for parity bit.

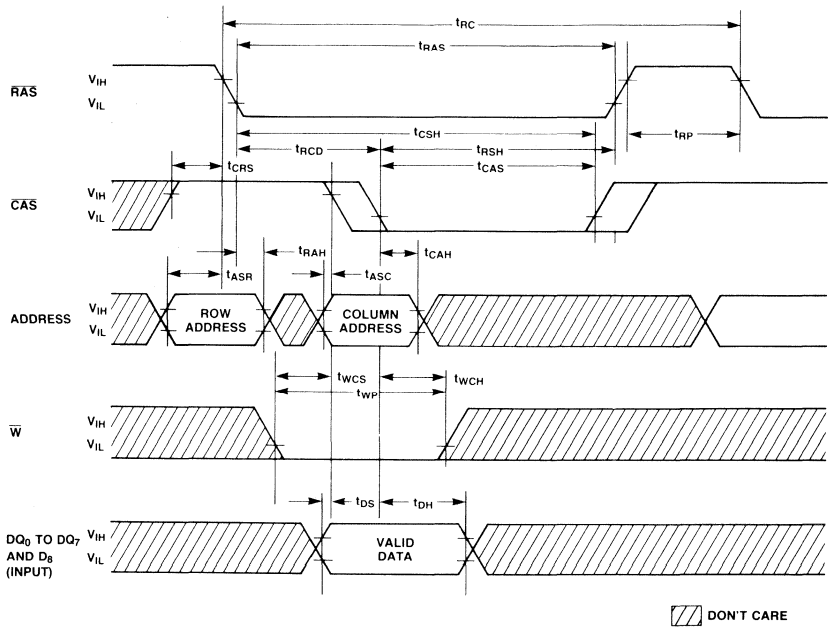
Timing Diagrams

Read Cycle



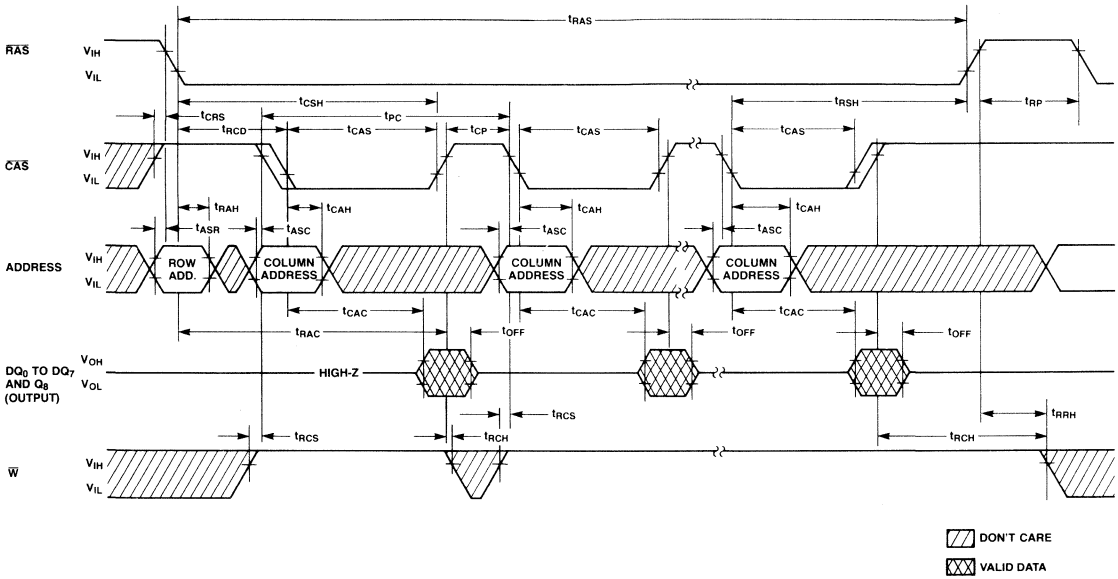
Timing Diagrams
(Continued)

Write Cycle (Early Write)



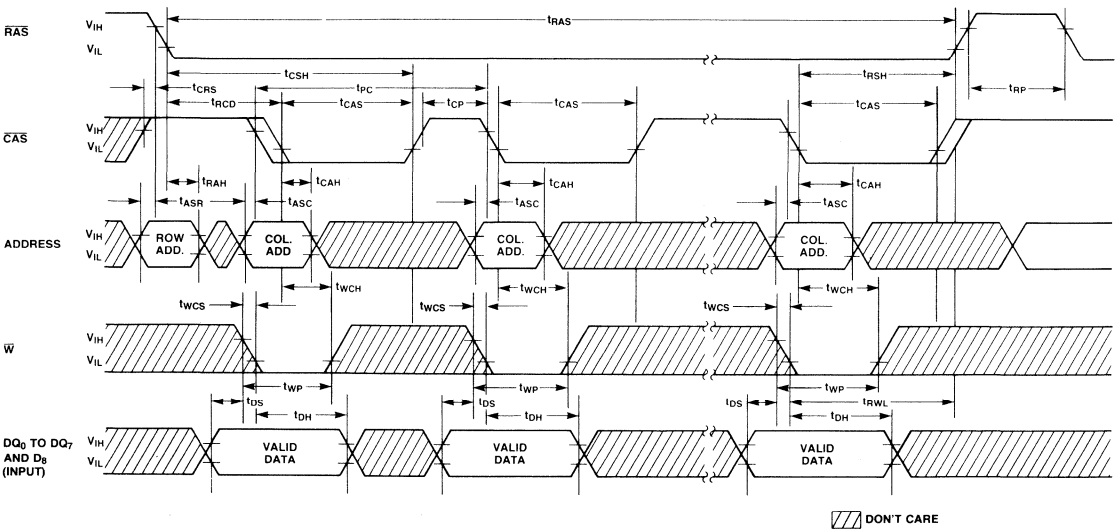
Timing Diagrams
(Continued)

Page Mode Read Cycle



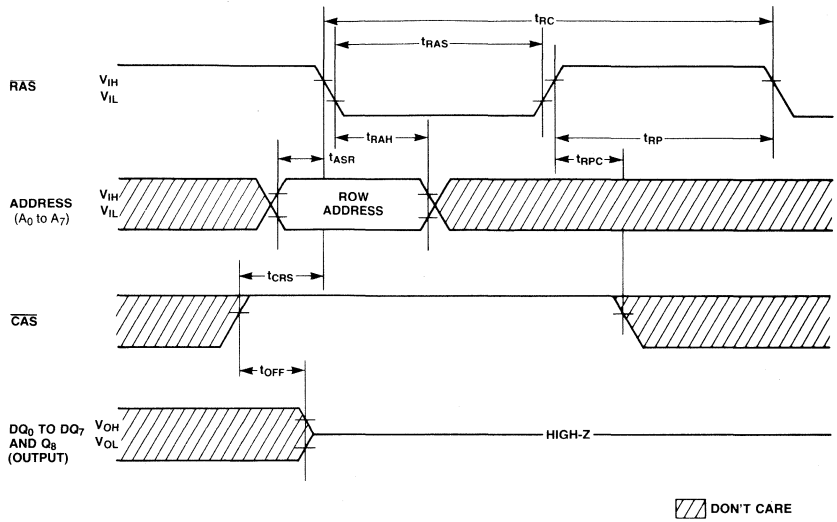
Timing Diagrams
(Continued)

Page Mode Write Cycle

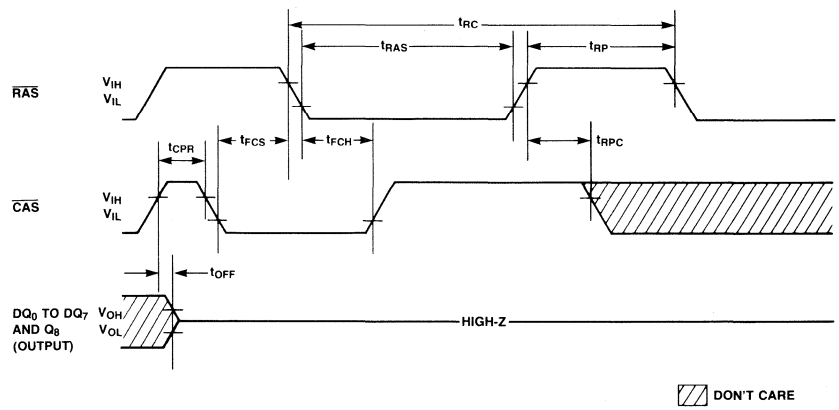


Timing Diagrams
(Continued)

$\overline{RAS}$-Only Refresh Cycle
Note: $\overline{W}$ = Don't Care, $A_8 = V_{IH}$ or V_{IL}

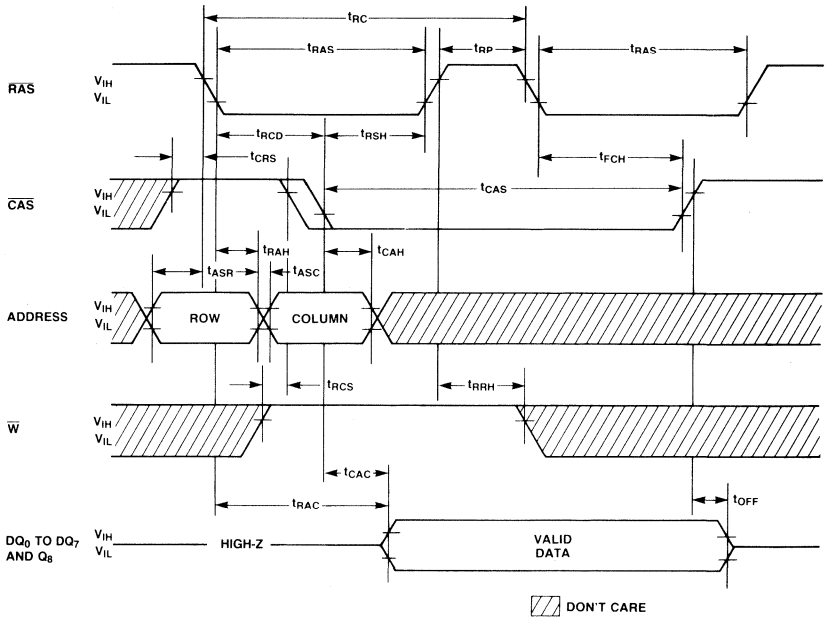


$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle
Note: Address, $\overline{W}$ = Don't Care



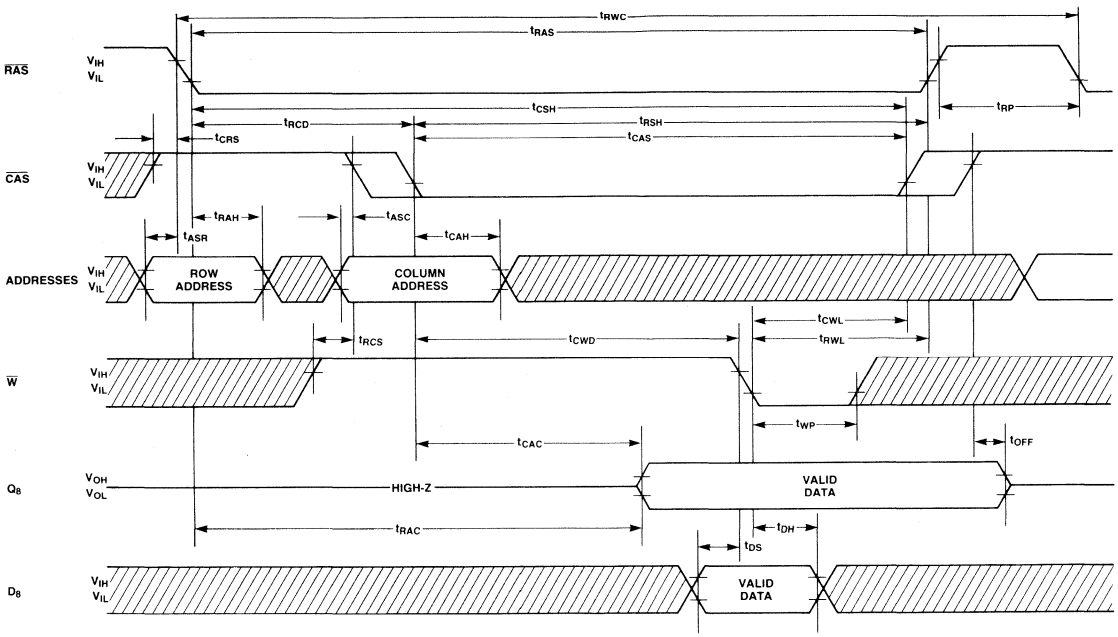
Timing Diagrams
(Continued)

Hidden Refresh Cycle



Timing Diagrams
(Continued)

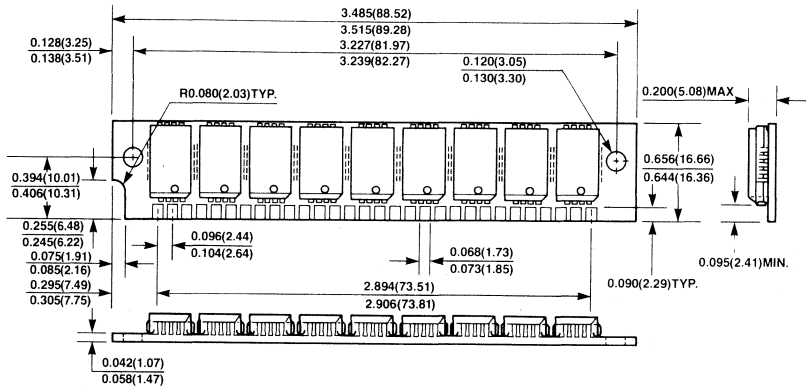
Read-Write/Read-Modify-Write Cycle*



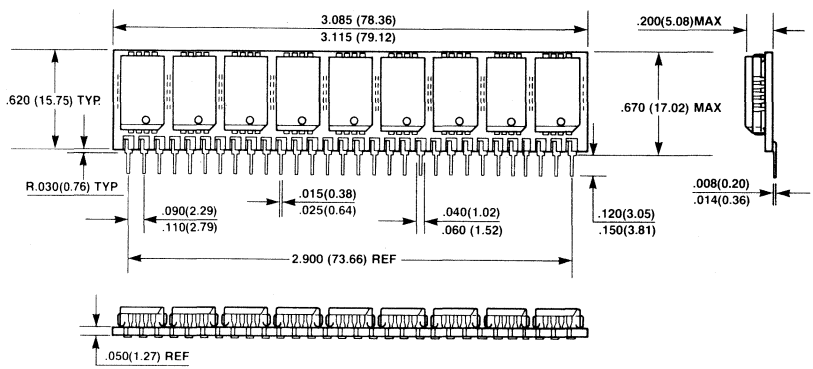
*; ONLY FOR PARITY BIT.

Package Dimensions
Dimensions in inches
(millimeters)

256K x 9 PLCC Module (MSS-30P-P01) (PDPB)



256K x 9 PLCC Module (MSP-30P-P01) (PDPS)



CMOS Dynamic RAMs

MB81C258 2-2
MB81C466 2-22

MB81C258-10, MB81C258-12, MB81C258-15

262,144 Word x 1-Bit Static Column CMOS Dynamic RAM

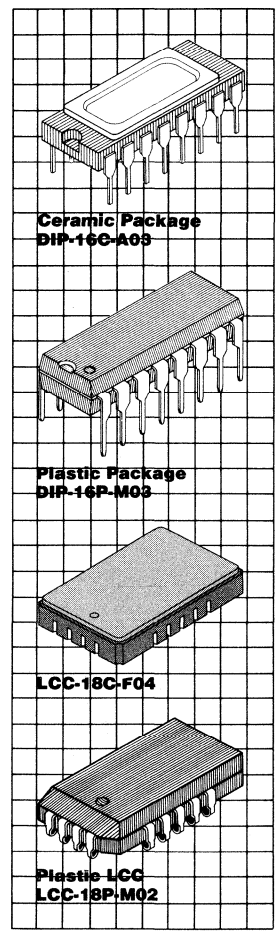
Description

The Fujitsu MB81C258 is a 262,144 x 1 CMOS Static Column Dynamic Random Access Memory (SC DRAM) designed for high speed, high performance applications such as mainframe memory, buffer memory, graphics terminals, video RAM, and peripheral storage devices where high speed access, very low power dissipation, compact layout, and low cost are required.

The SC DRAM features a static mode of operation in which very fast random access within the same row is performed by changing the column address. The advantage of using the SC DRAM is to achieve the fast read or write operation of the static mode by using dynamic memory.

The MB81C258 has fully TTL compatible inputs and output. It operates on a single +5V ±10% power supply. An on-chip substrate bias generator provides high performance operation. The SC DRAM contains on-chip address input and data input latches.

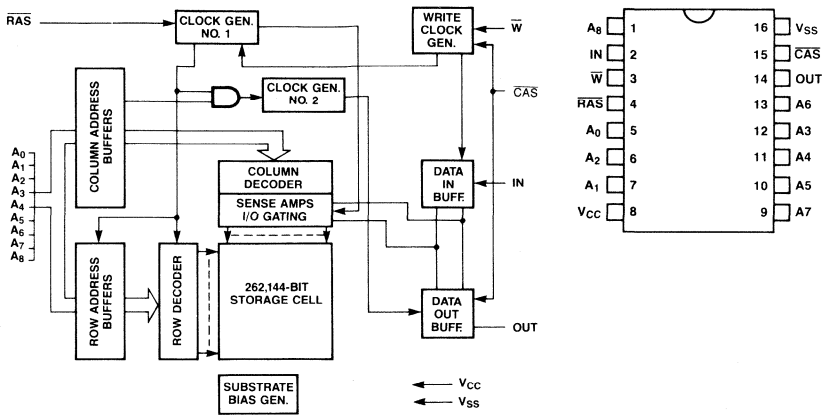
The MB81C258 is fabricated using Fujitsu's silicon gate CMOS advanced triple-layer polysilicon process which decreases power dissipation. This is particularly advantageous in hand-held computer systems which are backed-up by batteries.



Features

- **262,144 x 1 SC DRAM, 16-pin DIP/18-pad LCC**
- **Silicon-gate, CMOS, single transistor cell**
- **Row access time:**
  100 ns max. (MB81C258-10)
  120 ns max. (MB81C258-12)
  150 ns max. (MB81C258-15)
- **Static access time:**
  45 ns max. (MB81C258-10)
  55 ns max. (MB81C258-12)
  70 ns max. (MB81C258-15)
- **Random cycle time:**
  200 ns min. (MB81C258-10)
  230 ns min. (MB81C258-12)
  260 ns min. (MB81C258-15)
- **Static mode cycle time:**
  50 ns min. (MB81C258-10)
  60 ns min. (MB81C258-12)
  75 ns min. (MB81C258-15)
- **Single +5V supply, ±10% tolerance**
- **Low power**
  Active 330 mW max. at t_{SC} = 40 ns
  Standby 1.65 mW max. with CMOS level input
- **4 ms/256 refresh cycles**

MB81C258 Block Diagram and Pin Assignment



FUNCTIONAL TRUTH TABLE

RAS	CAS	W	ADDRESS	IN	OUT	FUNCTION
H	H	H	Don't Care	Don't Care	High-Z	Standby
L	L	H	R/C Address Valid	Don't Care	Valid Data	Short Read Cycle
L	L	L	R/C Address Valid	Valid Data	High-Z*1	Short Write Cycle
L	L	H	R/C Address Valid*2	Don't Care	Valid Data	Static Mode Read Cycle
L	L	L	R/C Address Valid*2	Valid Data	High-Z*1	Static Mode Write Cycle
L	L	L/H	R/C Address Valid*2	Valid Data	Valid Data or High-Z*1	Static Mode Mixed Cycle
L	H	Don't Care	R Address Valid	Don't Care	High-Z	RAS Only Refresh Cycle

Notes: *1 $t_{WS} \geq t_{WS}$ (min.) and $t_{WH} \geq t_{WH}$ (min.). Otherwise indeterminate.
*2 Row addresses are not necessary after first cycle.

Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}, V_{CC}	−1.0 to 7.0	V
Operating temperature (ambient)		T_{OP}	0 to 70	°C
Storage temperature	Ceramic / Plastic	T_{STG}	−55 to +150 / −55 to +125	°C
Power dissipation		P_D	1.0	W
Short circuit output current		I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Value Min	Value Typ	Value Max	Unit	Operating Temperature
Supply voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C ambient
	V_{SS}	0	0	0	V	
Input high voltage all inputs	V_{IH}	2.4		6.5	V	
Input low voltage all inputs	V_{IL}	−1.0		0.8	V	

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input capacitance, A_0 to A_8 and IN	C_{IN1}		7	pF
Input capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$	C_{IN2}		10	pF
Output capacitance, OUT	C_{OUT}		7	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB81C258-10 Min	MB81C258-10 Max	MB81C258-12 Min	MB81C258-12 Max	MB81C258-15 Min	MB81C258-15 Max	Unit
Operating current*1 Average power supply current ($\overline{CAS}$ = V_{IL}; $\overline{RAS}$ cycling; t_{RC} = min.)	I_{CC1}		60		50		45	mA
Standby current Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}; TTL level)	I_{CC2}		2		2		2	mA
Standy current Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}; CMOS level)	I_{CC2}		0.3		0.3		0.3	mA
Static mode Operating current*1 Average power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IL}; address; cycling; t_{SC} = min.)	I_{CC3}		60		50		45	mA
$\overline{CAS}$-before-$\overline{RAS}$ refresh current* Average power supply current ($\overline{CAS}$-before-$\overline{RAS}$ refresh; t_{RC} = min.)	I_{CC4}		55		45		40	mA
Input leakage current Input leakage current, any input (V_{CC} = 5.0V, V_{SS} = 0V; 0V ≤ V_{IN} ≤ 5.5V; all other pins not test = 0V)	$I_{I(L)}$	−10	10	−10	10	−10	10	μA
Output leakage current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	$I_{O(L)}$	−10	10	−10	10	−10	10	μA
Output levels Output high voltage (I_{OH} = −5 mA)	V_{OH}	2.4		2.4		2.4		
Output low voltage (I_{OL} = 4.2 mA)	V_{OL}		0.4		0.4		0.4	V

AC Characteristics
(Recommended operating conditions unless otherwise noted.)*1,2

Parameter	Symbol	MB81C258-10 Min	MB81C258-10 Max	MB81C258-12 Min	MB81C258-12 Max	MB81C258-15 Min	MB81C258-15 Max	Unit
Time between refresh	t_{REF}		4		4		4	ms
Random read/write cycle time	t_{RC}	200		230		260		ns
Read-modify-write cycle time	t_{RWC}	245		285		325		ns
Access time from $\overline{RAS}$*3,5	t_{RAC}		100		120		150	ns
Access time from $\overline{CAS}$*5	t_{CAC}		25		30		35	ns
Output buffer turn off delay time	t_{OFF}	0	25	0	25	0	30	ns
Transition time	t_T	3	50	3	50	3	50	ns
Column address access time*4,5	t_{AA}		45		55		70	ns
Output hold time from column address change	t_{AOH}	5		5		5		ns
Access time from $\overline{W}$ precharge	t_{WPA}		30		35		45	ns
Access time relative to last write*6	t_{ALW}		90		110		140	ns
$\overline{RAS}$ precharge time	t_{RP}	90		100		100		ns
$\overline{RAS}$ pulse width	t_{RAS}	65	100000	75	100000	95	100000	ns
$\overline{RAS}$ hold time (read)	t_{RSH}	25		30		35		ns
Write latched data hold time	t_{WOH}	0		0		0		ns
$\overline{CAS}$ pulse width (read)	t_{CAS}	25	100000	30	100000	35	100000	ns
$\overline{CAS}$ pulse width (write)	t_{CAS}	15	100000	20	100000	25	100000	ns
$\overline{CAS}$ hold time (read)	t_{CSH}	100		120		150		ns
$\overline{CAS}$ hold time (write)	t_{CSH}	80		95		115		ns
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	75	25	90	30	115	ns
$\overline{CAS}$ to $\overline{RAS}$ set up time	t_{CRS}	20		25		30		ns
Row address set up time	t_{ASR}	0		0		0		ns
Row address hold time	t_{RAH}	15		15		20		ns
Column address set up time*7	t_{ASC}	0		0		0		ns
Column address hold time*7	t_{CAH}	15		15		20		ns
$\overline{RAS}$ to column address delay time*8,9	t_{RAD}	20	50	20	65	25	80	ns
Column address hold time referenced to $\overline{RAS}$	t_{AR}	100		120		150		ns

Notes:
*1. An Initial pause ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}) of 200 μs is required after power-up followed by any 8 $\overline{RAS}$-only cycles before proper device operation is achieved. If the internal refresh counter to effective a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
*2. AC characteristics assume t_T = 5 ns, V_{IN} = 0V to 3V, V_{IH} = 2.4V, V_{IL} = 0.8V, V_{OH} = 2.4V, and V_{OL} = 0.4V.
*3. Assumes that $t_{RAD} \leq t_{RAD}$ (max). If t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RAD} exceeds the value shown.
*4. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
*5. Measured with a load equivalent to 2 TTL loads and 100 pF.
*6. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recommended value then t_{ALW} is increased by the amount that t_{LWAD} exceeds t_{LWAD} (max).
*7. Write Cycle Only.
*8. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
*9 t_{RAD} (min) = t_{RAH} (min) + t_T (t_T = 5 ns).

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)*1,2

Parameter	Symbol	MB81C258-10 Min	MB81C258-10 Max	MB81C258-12 Min	MB81C258-12 Max	MB81C258-15 Min	MB81C258-15 Max	Unit
Write address hold time referenced to $\overline{RAS}$	t_{AWR}	80		90		110		ns
Read address to $\overline{RAS}$ lead time	t_{RAL}	45		55		70		ns
Column address hold time referenced to $\overline{RAS}$ rising time*10	t_{AHR}	15		15		20		ns
Last write to column address delay time*11,12	t_{LWAD}	20	45	20	55	25	70	ns
Column address hold time referenced to last write	t_{AHLW}	90		110		140		ns
Read command set up time referenced to $\overline{CAS}$	t_{RCS}	0		0		0		ns
Read command hold time referenced to $\overline{RAS}$*13	t_{RRH}	10		10		10		ns
Read command hold time referenced to $\overline{CAS}$*13	t_{RCH}	0		0		0		ns
$\overline{W}$ pulse width	t_{WP}	15		20		25		ns
$\overline{W}$ inactive time	t_{WI}	15		20		25		ns
Write command hold time	t_{WCH}	15		20		25		ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	25		30		35		ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	25		30		35		ns
$\overline{RAS}$ to $\overline{W}$ delay time*14	t_{RWD}	100		120		150		ns
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	25		30		35		ns
Column address to $\overline{W}$ delay time	t_{AWD}	45		55		70		ns
$\overline{RAS}$ to second write delay time	t_{RSWD}	100		120		150		ns
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	80		95		115		ns
$\overline{RAS}$ precharge time from last write	t_{RPLW}	135		155		165		ns
Write set up time for output disable*14	t_{WS}	0		0		0		ns
Write hold time for output disable*14	t_{WH}	0		0		0		ns
IN set up time	t_{DS}	0		0		0		ns
IN hold time	t_{DH}	15		15		20		ns
IN hold time referenced to $\overline{RAS}$	t_{DHR}	80		90		110		ns
Refresh set up time for $\overline{CAS}$ referenced to $\overline{RAS}$ ($\overline{C}$-B-$\overline{R}$)	t_{FCS}	20		25		30		ns
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$ ($\overline{C}$-B-$\overline{R}$)	t_{FCH}	20		25		30		ns
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$)	t_{CPR}	20		25		30		ns
$\overline{RAS}$ precharge time to $\overline{CAS}$ active time (refresh cycles)	t_{RPC}	20		20		20		ns

Notes: *10. t_{AHR} is specified to latch column address by the rising edge of $\overline{RAS}$.

*11. Operation within the t_{LWAD} (max) limit insures that t_{ALW} (max) can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled by t_{AA}.

*12. t_{LWAD} (min) = t_{CAH} (min) + t_T (t_T = 5 ns).

*13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

*14. t_{WS}, t_{WH}, and t_{RWD} are specified as a reference point only. If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), the data output pin will remain High-Z state throughout entire cycle. It $t_{RWD} \geq t_{RWD}$ (min). The data output will contain data read from the selected cell.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)*1,2

Parameter	Symbol	MB81C258-10 Min	MB81C258-10 Max	MB81C258-12 Min	MB81C258-12 Max	MB81C258-15 Min	MB81C258-15 Max	Unit
Static mode read/write cycle time	t_{SC}	50		60		75		ns
Static mode read-modify-write cycle time	t_{SRWC}	95		115		145		ns
Static mode $\overline{CAS}$ precharge time	t_{CP}	15		20		25		ns
Refresh counter test cycle time*15	t_{RTC}	440		520		610		ns
Refresh counter test $\overline{RAS}$ pulse width*15	t_{TRAS}	340	10000	410	10000	500	10000	ns
Refresh counter test $\overline{CAS}$ precharge time*15	t_{CPT}	50		60		70		ns
Refresh counter test $\overline{RAS}$ to column address delay time*15,16	t_{CADT}		100		120		150	ns
Refresh counter test access time from $\overline{CAS}$*15	t_{CACT}		135		165		205	ns
Refresh counter test $\overline{CAS}$ to $\overline{W}$ delay time*15	t_{CWDT}	135		165		205		ns

Notes: *15. $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only.
*16. Operation within the t_{CADT} (max) limit insures that t_{CACT} (max) can be met. t_{CADT} (max) is specified as a reference point only; if t_{CADT} is greater than the specified t_{CADT} (max) limit, the access time is controlled by t_{CACT}.

Description

Address Inputs

A total of eighteen binary input address bits are required to decode any one of the 262,144 storage cells within the MB81C258. Nine row address bits are established on the address input pins (A_0 to A_8) and latched with the Row Address Strobe ($\overline{RAS}$). The nine column address bits are established on the address input pins (A_0 to A_8) after the Row Address Hold Time has been satisfied. In the read cycle, the column addresses are not latched by the Column Address Strobe ($\overline{CAS}$), so the column address must be stable until the output becomes valid. In write cycle, the column addresses are latched by the later falling edge of $\overline{CAS}$ or $\overline{W}$.

Write Enable

Read or Write cycle is selected with the $\overline{W}$ inputs. A high on $\overline{W}$ selects read cycle and low selects write cycle. The write operation is asserted on the latter falling edge of $\overline{CAS}$ or $\overline{W}$. (Both $\overline{CAS}$ and $\overline{W}$ are low.) The time period of the write operation is determined by internal circuit, thus next write cycle will be inhibited during the write cycle.

Column Address Strobe

The Column Address Strobe ($\overline{CAS}$) is used for not only strobing column address inputs but also controlling output buffer. When $\overline{CAS}$ is high, all DRAM operations (Read, write, and read-modify-write cycles) except for refresh cycles are inhibited regardless of the state of $\overline{RAS}$ and $\overline{W}$. When $\overline{CAS}$ is low all DRAM operations can be achieved in compliance with the state of $\overline{W}$.

Data Input

Data is written into the MB81C258 during write or read-modify-write cycle. The input data is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{W}$.

Data Output

The output buffer is three state TTL compatible with a fan out of two standard TTL loads. Data out has the same polarity as data in. The output is in high impedance state until $\overline{CAS}$ is brought low. In a read cycle, the access time is determined by the following conditions:

1) t_{RAC} from the falling edge of $\overline{RAS}$.
2) t_{AA} from the column address inputs.
3) t_{CAC} from the falling edge of $\overline{CAS}$.

When both t_{RCD} and t_{RAD} satisfy their maximum limits,
$t_{RAS} = t_{RCD} + t_{CAC}$ or
$t_{RAC} = t_{RAD} + t_{AA}$.

Data output remains valid while the column address inputs are kept constant. However, when $\overline{CAS}$ goes high, the output returns to a high impedance state. In the static mode, the output data is internally latched by the later falling edge of $\overline{CAS}$ or $\overline{W}$ and remains valid internally until either returns to high.

Static Mode

The static mode operation allows continuous read, write, or read-modify-write cycle within a row by applying new column address. In the static mode, $\overline{CAS}$ can be kept low throughout static mode operation. The following four cycles are allowed in the static mode.

1) Static mode read cycle;
In a static mode read cycle, the access time of read cycle after first read cycle is t_{AA} from the column address input. The data remains valid for a time t_{AOH} after the column address is changed.

2) Static mode write cycle;
In a static mode write cycle, the data is written into the cell triggered by the later falling edge of $\overline{CAS}$ or $\overline{W}$. If both t_{WS} and t_{WH} are greater than their minimum limits, the data output pin is kept high in an impedance state through the static mode write cycle.

3) Static mode read-modify-write cycle;
In the static mode read-modify-write cycle, $\overline{W}$ goes low after t_{AWD} from the column address inputs and t_{CWD} from the falling edge of $\overline{CAS}$. The data and column address inputs are strobed and latched by the falling edge of $\overline{W}$.

4) Static mode mixed cycle;
Static mode read, write, and read-modify-write cycles can be mixed in any order.

In the next read cycle of static mode write cycle or read-modify-write cycle, the access time is determined by the following conditions.

1) t_{ALW} from the falling edge of $\overline{W}$ at previous write cycle.
2) t_{AA} from the column address inputs
3) t_{WPA} from the rising edge of $\overline{W}$ at the read cycle.
4) t_{CAC} from the falling edge of $\overline{CAS}$.

$\overline{RAS}$-only Refresh

Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses ($A_0 \sim A_7$) at least every 4 ms. $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought "low." Strobing each of the 256 row-addresses ($A_0 \sim A_7$) with $\overline{RAS}$ will cause all bits in each row to be refreshed. $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh

$\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB81C258 offers an alternate refresh method. If $\overline{CAS}$ is held "low" for the specified period (t_{FCS}) before $\overline{RAS}$ goes to "low", on-chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

Hidden Refresh

A hidden refresh cycle may take place while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time. For the MB81C258, a hidden refresh cycle is a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The internal refresh address counter provides the refresh addresses as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refesh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to "high" and then goes to "low" again while $\overline{RAS}$ is held "low", the read and write operation are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 9 row address bits and 9 column address bits defined as follows:

A row address;
Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set "high" internally.

A column address;
All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of $\overline{CAS}$.

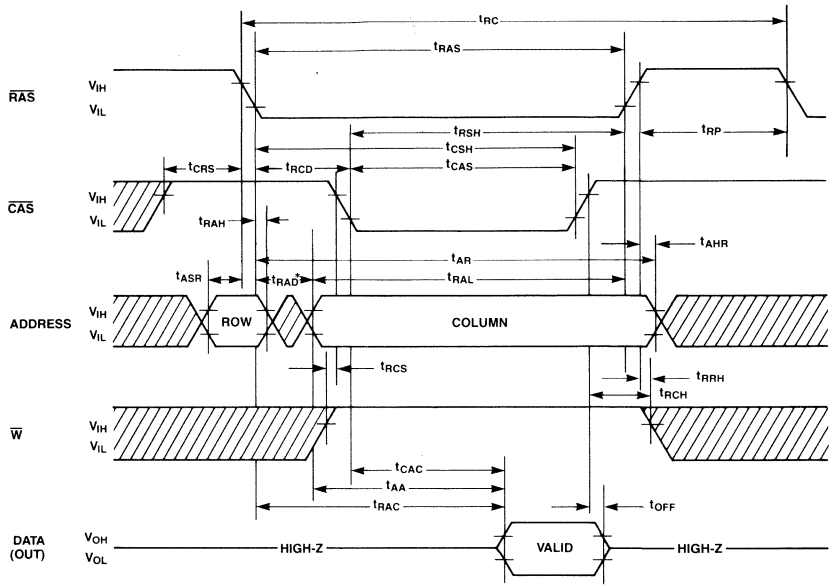
Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

The timing, as shown in the $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle, is used for all the following operations:

1) Initialize the internal refresh counter. For this operation, 8 cycles are required.
2) Write a test pattern of "low"s into memory cells at a single column address and 256 row address.
3) Using a read-modify-write cycle, read the "low" written at the last operation (Step 2) and write a new "high" in the same cycle. This cycle is repeated 256 times, and "high"s are written into the 256 memory cells.
4) Read the "high"s written at the last operation (Step 3).
5) Complement the test pattern and repeat steps 2, 3 and 4.

Timing Diagrams

Read Cycle

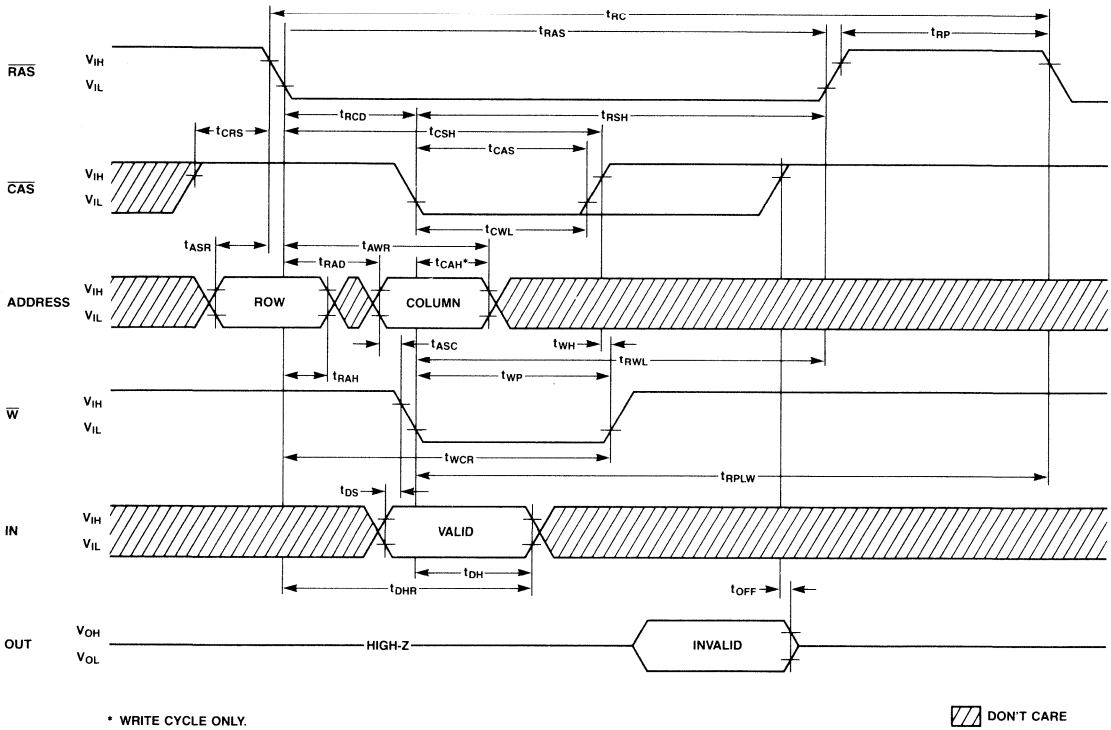


*; IF $t_{RAD} \geq t_{RAD}$ (MAX), ACCESS TIME IS t_{AA}.

DON'T CARE

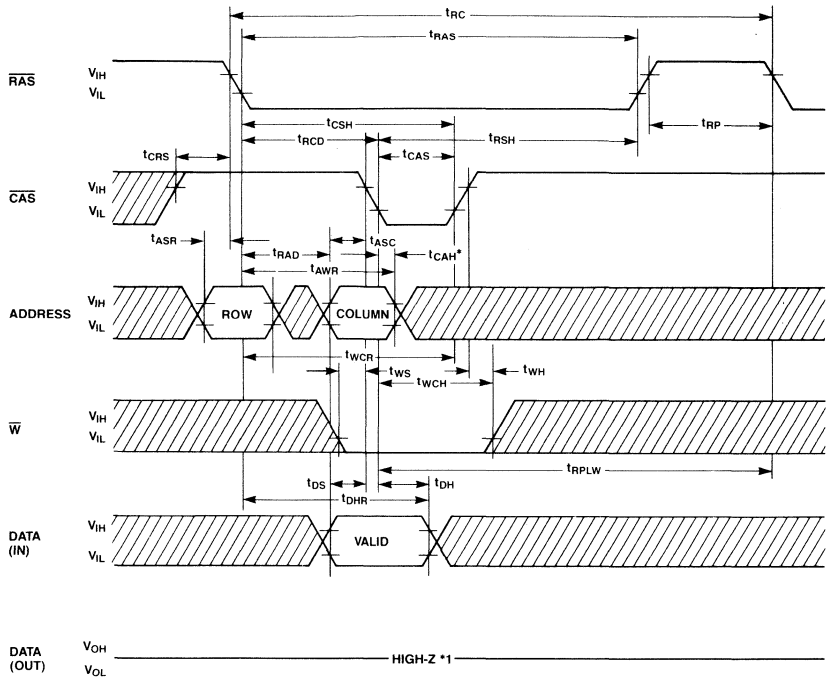
Timing Diagrams
(Continued)

Write Cycle ($\overline{W}$ Controlled)



Timing Diagrams
(Continued)

Write Cycle ($\overline{CAS}$ controlled)

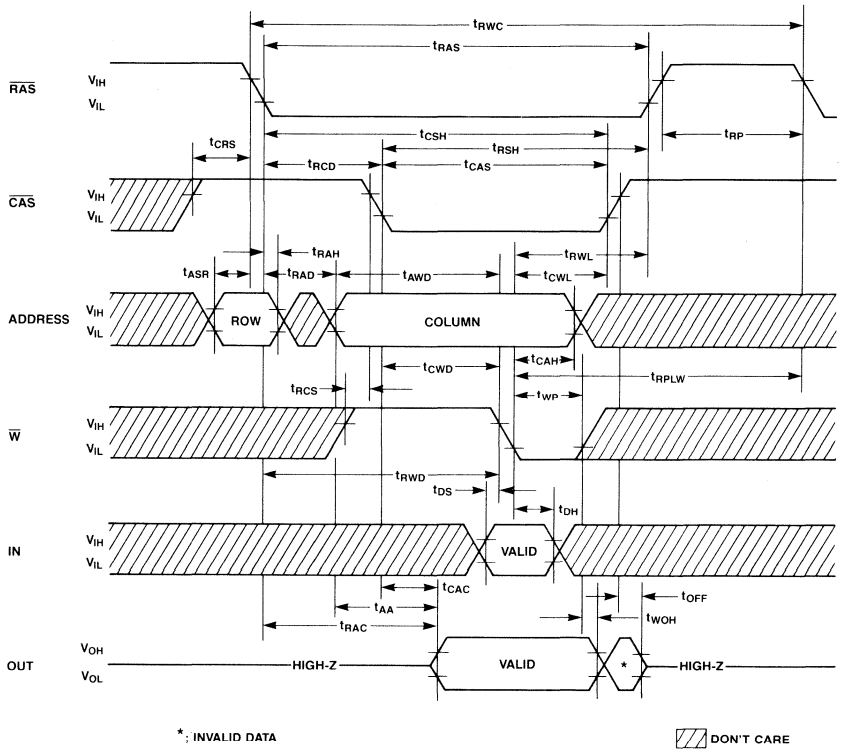


*1 IF $t_{WS} \geq t_{WS}$ (MIN.) AND $t_{WH} \geq t_{WH}$ (MIN.), OUT IS HIGH-Z.
*2 WRITE CYCLE ONLY.
DON'T CARE

DON'T CARE

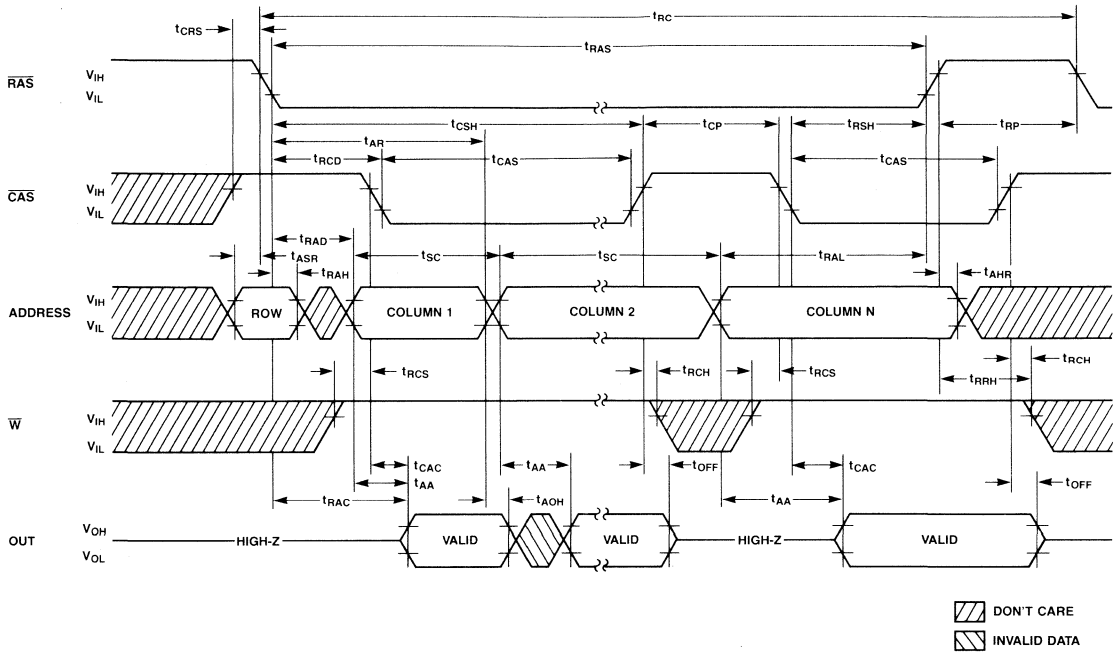
Timing Diagrams
(Continued)

Read-Modify-Write Cycle



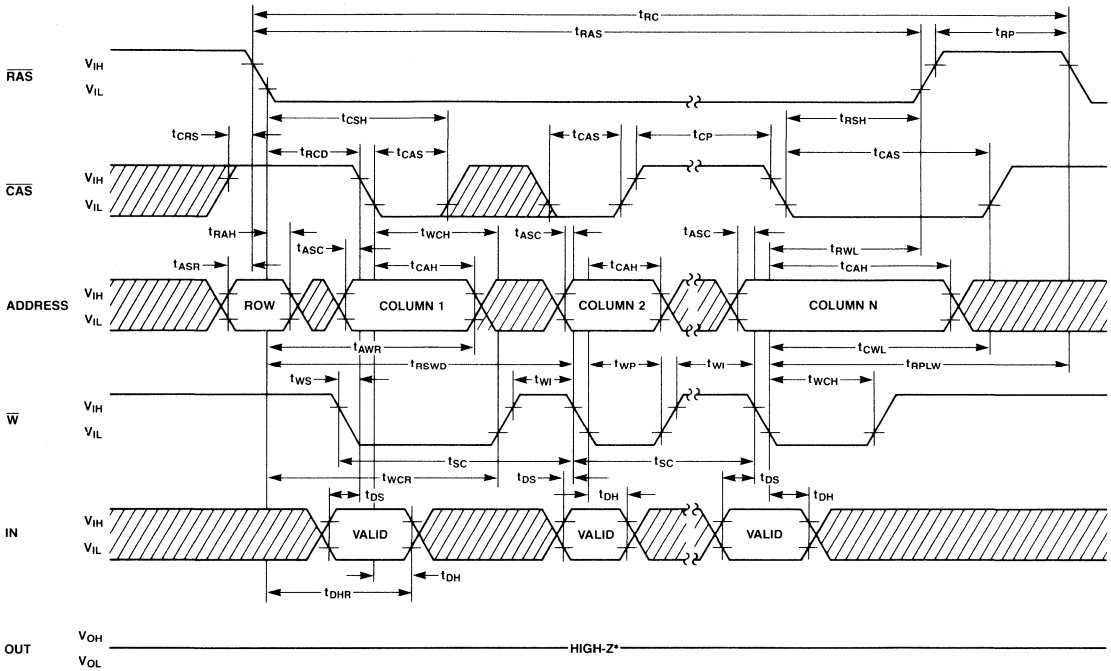
Timing Diagrams
(Continued)

Static Mode Read Cycle



Timing Diagrams
(Continued)

Static Mode Write Cycle

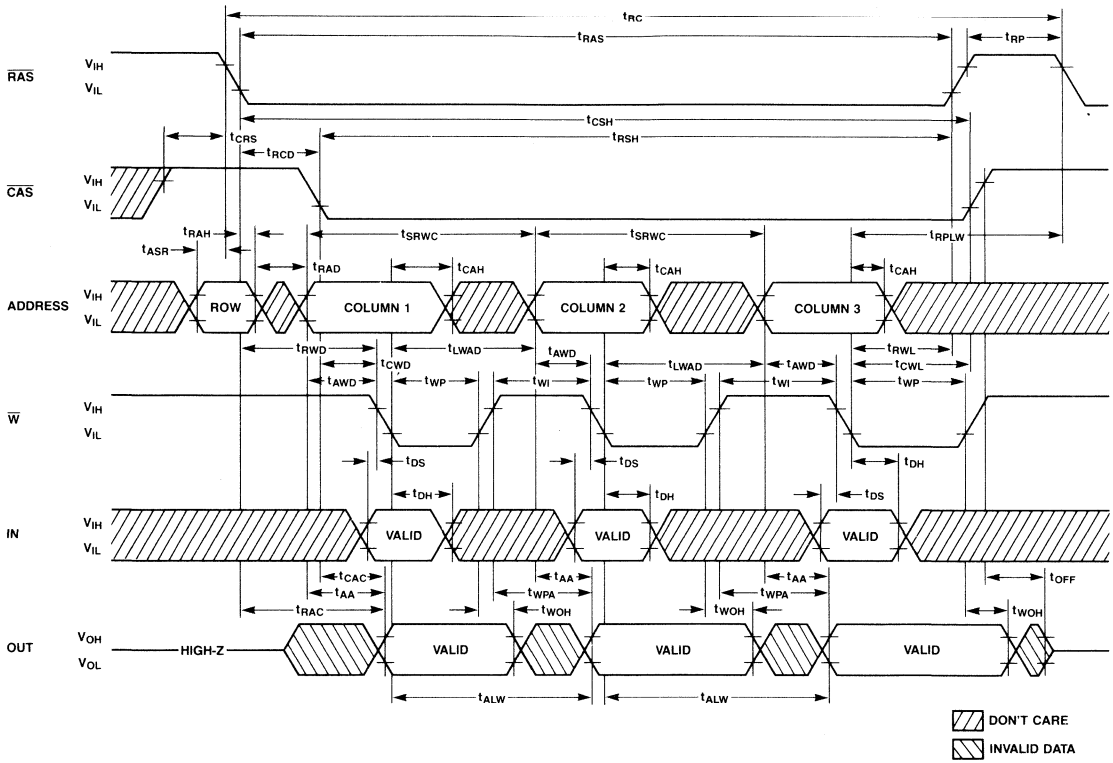


* IF $t_{WS} \geq t_{WS}$ (MIN.) AND $t_{WH} \geq t_{WH}$ (MIN.), OUT IS HIGH-Z.

DON'T CARE

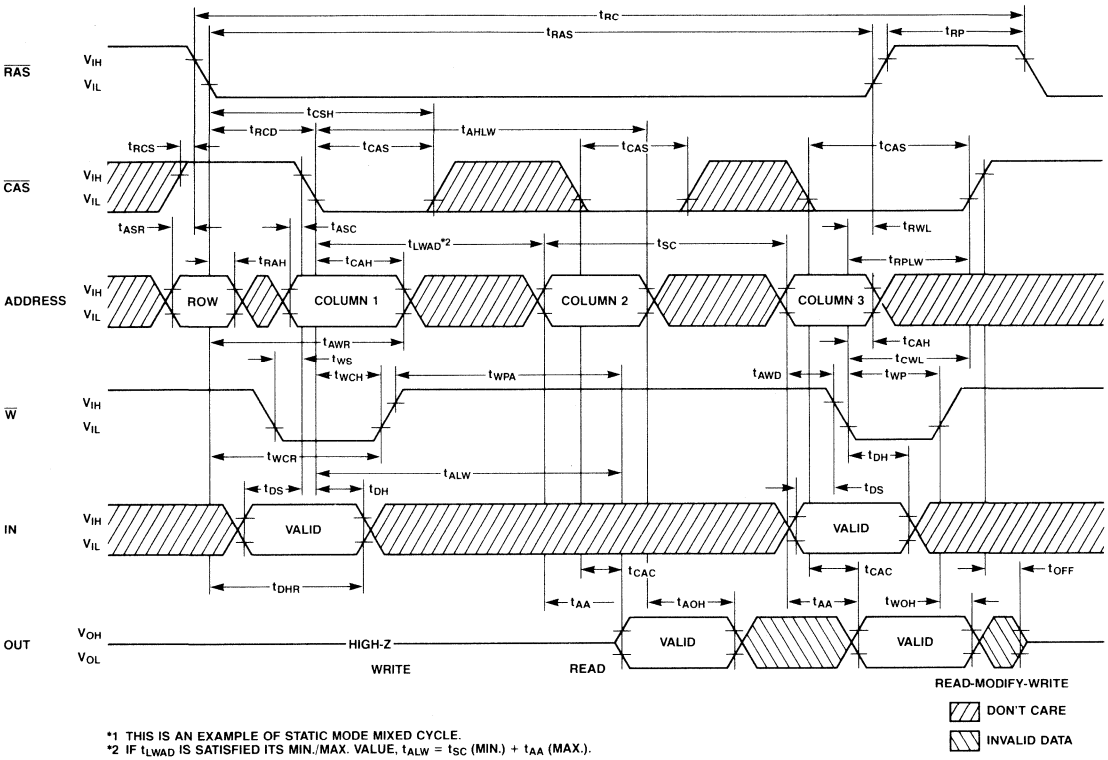
Timing Diagrams
(Continued)

Static Mode Read-Modify-Write Cycle



Timing Diagrams
(Continued)

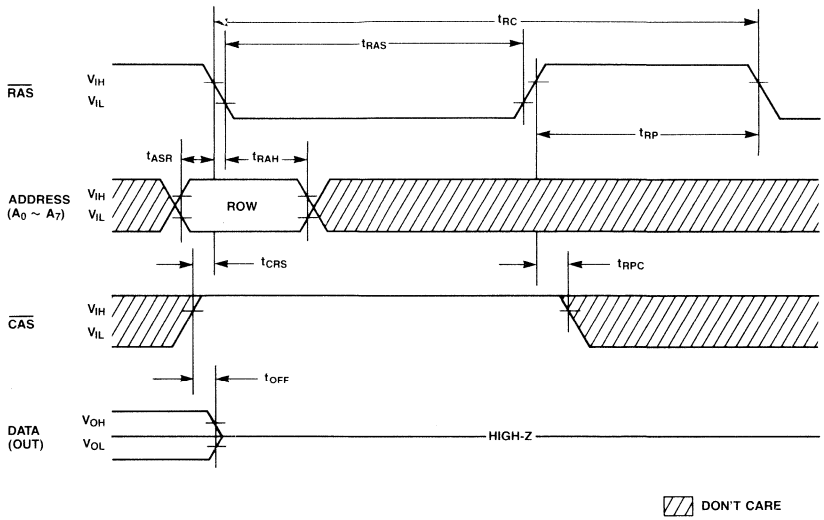
Static Mode Mixed Cycle*1



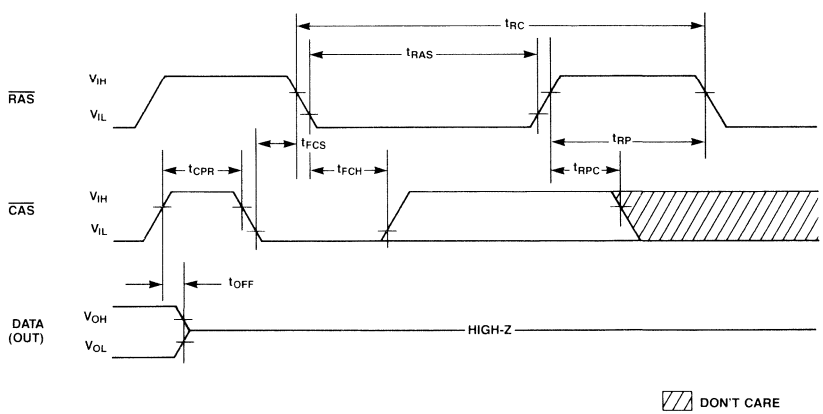
*1 THIS IS AN EXAMPLE OF STATIC MODE MIXED CYCLE.
*2 IF t_{LWAD} IS SATISFIED ITS MIN./MAX. VALUE, $t_{ALW} = t_{SC}$ (MIN.) + t_{AA} (MAX.).

Timing Diagrams
(Continued)

$\overline{RAS}$-Only Refresh Cycle
(Note: W, IN = Don't Care, A_8 = V_{IH} or V_{IL})

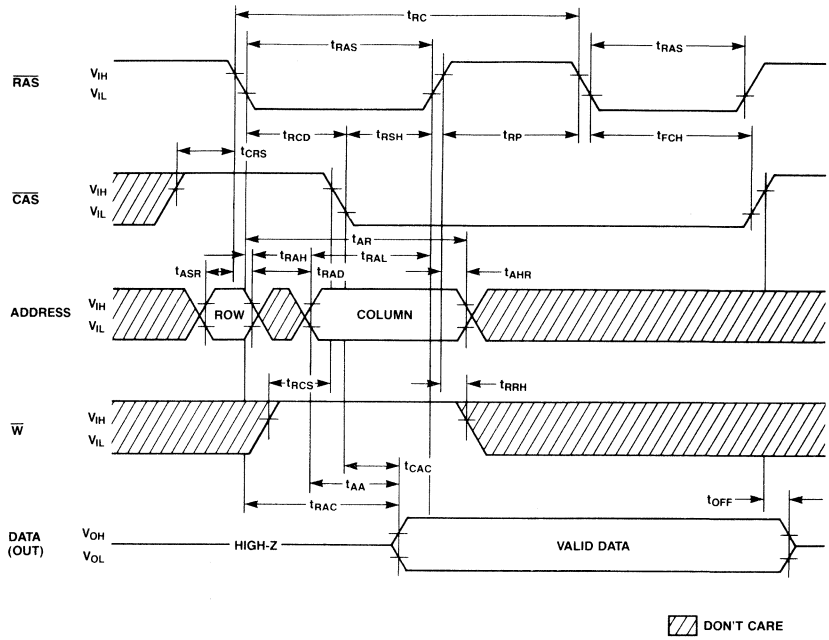


$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle
(Note: Address, W, IN = Don't Care)



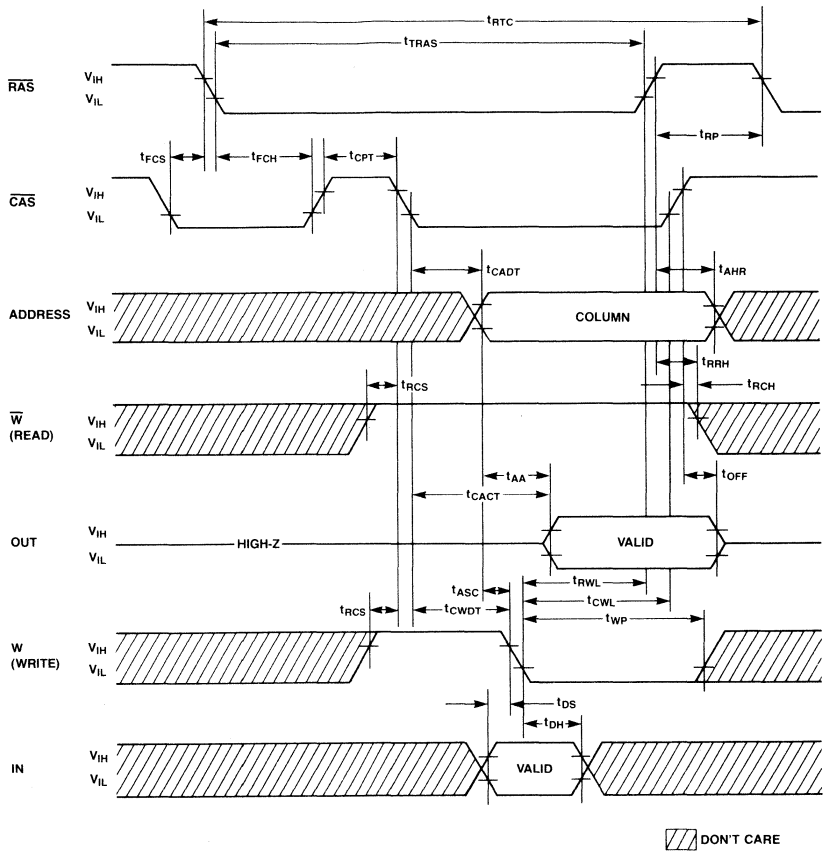
Timing Diagrams
(Continued)

Hidden Refresh Cycle



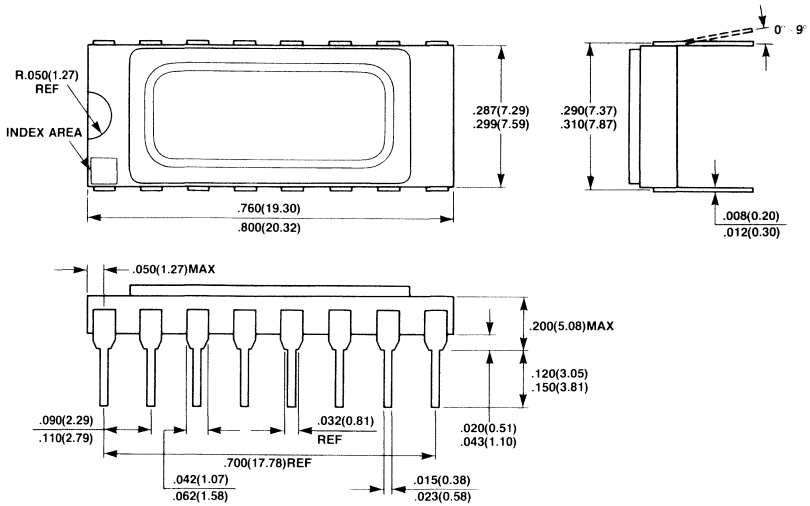
Timing Diagrams

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle

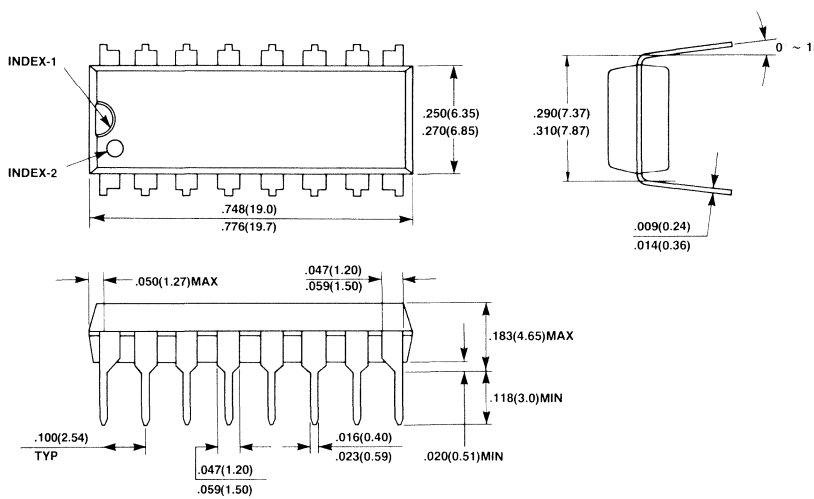


Package Dimensions
Dimensions in inches
(millimeters)

16 Lead Ceramic (Metal Seal) Dual In-Line Package
(Case No.: DIP-16C-A03)

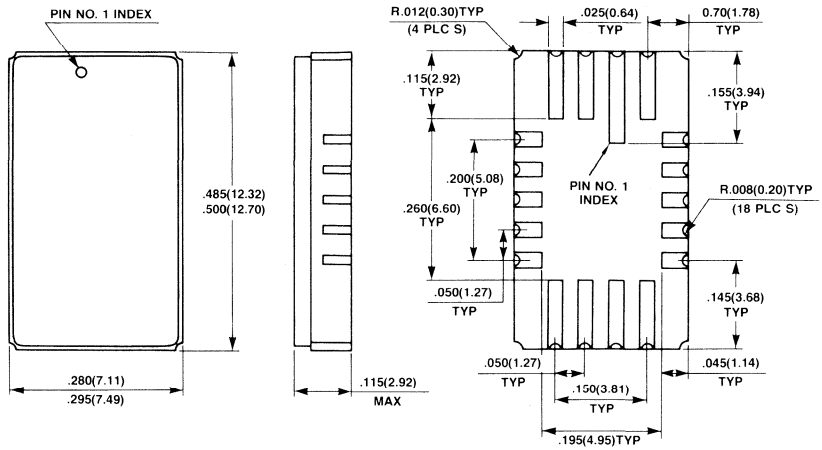


16 Lead Plastic Dual In-Line Package
(Case No.: DIP-16P-M03)

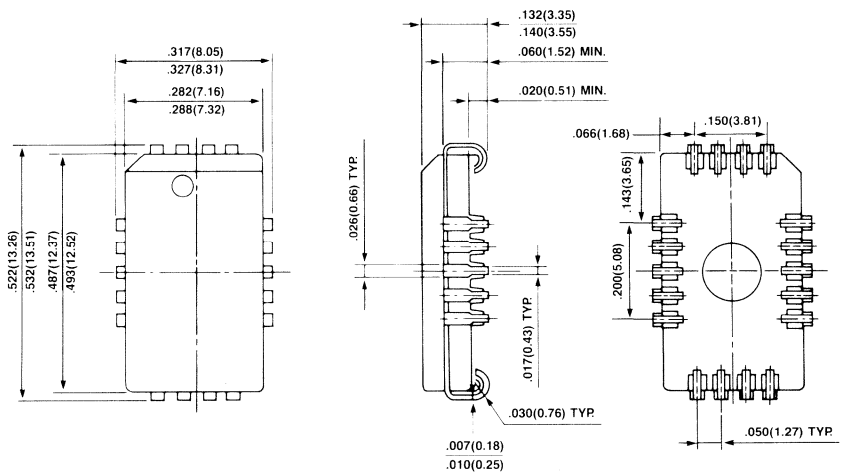


Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

18-Pad Ceramic (Frit Seal) Leadless Chip Carrier
(Case No.: LCC-18C-F04)



18-Lead Plastic Chip Carrier
LCC-18P-M02



MB81C466-10, MB81C466-12, MB81C466-15

65,536 x 4 Static Column CMOS Dynamic Random Access Memory

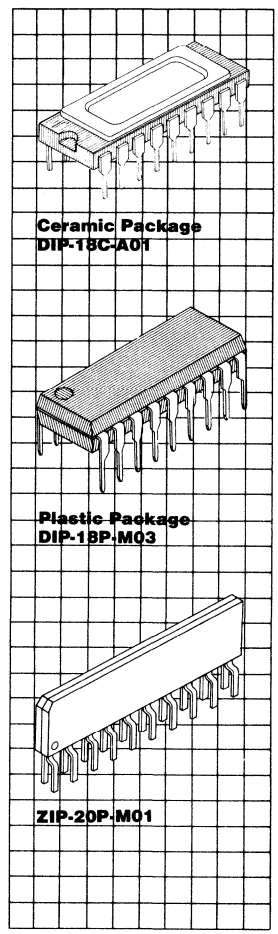
Description

The MB81C466 is a 262,144-bit (configured as 65,536 x 4-bits) CMOS Static Column Dynamic Random Access Memory (SC DRAM). The design is optimized for high speed, high performance applications, such as mainframe memory, buffer memory, graphics terminals, video RAM, and peripheral storage devices where high speed access, very low power dissipation, compact layout and low cost are required.

The SC DRAM features a static mode of operation in which very fast random access within the same row is performed by changing the column address. The advantage of using the SC DRAM is to achieve the fast read or write operation of the static mode by using dynamic memory.

The MB81C466 has fully TTL compatible inputs and outputs. It operates on a single +5V ± 10% power supply. An on-chip substrate bias generator provides high performance operation. The SC DRAM contains on-chip address input and data input latches.

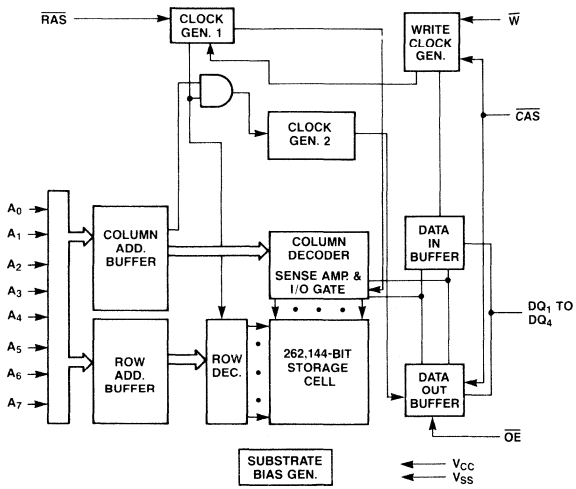
The MB81C466 is fabricated using Fujitsu's silicon gate CMOS and Fujitsu advanced triple-layer polysilicon process which decreases power dissipation, and can easily be used in battery (backed-up) systems such as hand held computers.

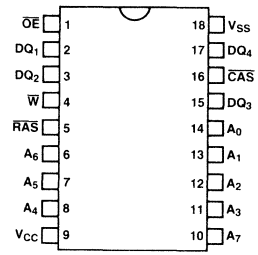


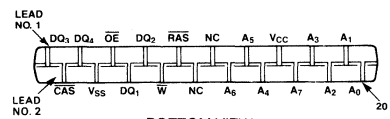
Features

- **65,536 x 4 SC DRAM, 18-pin package**
- **Silicon-gate, CMOS, Single transistor cell**
- **Row access time**
  100 ns max. (MB81C466-10)
  120 ns max. (MB81C466-12)
  150 ns max. (MB81C466-15)
- **Address access time**
  45 ns max. (MB81C466-10)
  55 ns max. (MB81C466-12)
  70 ns max. (MB81C466-15)
- **Random cycle time**
  200 ns min. (MB81C466-10)
  230 ns min. (MB81C466-12)
  260 ns min. (MB81C466-15)
- **Static cycle time**
  50 ns min. (MB81C466-10)
  60 ns min. (MB81C466-12)
  75 ns min. (MB81C466-15)
  Single +5V supply, ±10% tolerance
- **Low power, (Active)**
  385 mW max. (MB81C466-10)
  330 mW max. (MB81C466-12)
  275 mW max. (MB81C466-15)
  11 mW max. (Standby with TTL level input)
  1.1 mW max. (Standby with CMOS el input)
- **4 ms/256 refresh cycles**
- **On chip substrate bias**
- **Static Mode Boundary 256 x 4-Bit/Page**
- **Common I/O ($\overline{OE}$ Control)**
- **Fast $\overline{CAS}$ Control**
- **Edge triggered write operation**
- **Internal write period control**
- **$\overline{RAS}$-only, $\overline{CAS}$-before $\overline{RAS}$ refresh capability**

MB81C466 Block Diagram and Pin Assignment







BOTTOM VIEW

Absolute Maximum Ratings

Ratings		Symbol	Value	Unit
Voltage on any pin relative to V_{SS}		V_{IN}, V_{OUT}, V_{CC}	−1.0 to 7.0	V
Storage Temperature	Ceramic Plastic	T_{STG}	−55 to +155 −55 to +125	°C
Power Dissipation		P_D	1.0	W
Short circuit output current		—	50	mA

Recommended Operating Conditions

(Referenced to V_{SS})

Paramater	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply voltage	V_{CC} V_{SS}	4.5 0	5.0 0	5.5 0	V	0°C to +70°C
Input high voltage, all inputs	V_{IH}	2.4		6.5	V	
Input low voltage, all inputs	V_{IL}	−1.0		0.8	V	

Capacitance

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input capacitance, A_0 to A_7	C_{IN1}		7	pF
Input capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{OE}$	C_{IN2}		10	pF
Input/output capacitance, DQ_1 − DQ_4	C_{IO}		7	pF

DC Characteristics

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Max	Unit
Operating current*1 average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min)	MB81C466-10	I_{CC1}		70	mA
	MB81C466-12			60	
	MB81C466-15			50	
Standby current power supply current	TTL level $\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	I_{CC2}		2	mA
	CMOS level $\overline{RAS}$ = $\overline{CAS}$ = V_{CC} ± 0.2V			0.3	
Static mode operating current*1 average power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IL}, $\overline{W}$ or address cycling; t_{SC} = min)	MB81C466-10	I_{CC3}		70	mA
	MB81C466-12			60	
	MB81C466-15			50	
Refresh current average power supply current ($\overline{CAS}$-before-$\overline{RAS}$; t_{RC} = min)	MB81C466-10	I_{CC4}		55	mA
	MB81C466-12			55	
	MB81C466-15			45	
Input leakage current input leakage current, any input (V_{CC} = 5.5V, V_{SS} = 0V, 0V ≤ V_{IN} ≤ 5.5V all other pins not under test = 0V)		$I_{I(L)}$	−10	10	μA
Output leakage current (data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		$I_{O(L)}$	−10	10	μA
Output levels output high voltage (I_{OH} = −5 mA)		V_{OH}	2.4		V
output low voltage (I_{OL} = 4.2 mA)		V_{OL}		0.4	

Note: *1 I_{CC} is dependent on output loading and cycle rates. The specified values are obtained with the output open.

AC Characteristics

(Recommended operating conditions unless otherwise noted.)*1,2

Parameter	Symbol	MB81C466-10 Min	MB81C466-10 Max	MB81C466-12 Min	MB81C466-12 Max	MB81C466-15 Min	MB81C466-15 Max	Unit
Time between refresh	t_{REF}		4		4		4	ms
Random read/write cycle time	t_{RC}	200		230		260		ns
Read-modify-write cycle time	t_{RWC}	270		315		360		ns
Access time from $\overline{RAS}$*3,5	t_{RAC}		100		120		150	ns
Access time from $\overline{CAS}$*5	t_{CAC}	25			30		35	ns
Output buffer turn off delay time	t_{OFF}	0	25	0	25	0	30	ns
Transition time	t_T	3	50	3	50	3	70	ns
Column address access time*4,5	t_{AA}		45		55		55	ns
Output hold time from column address change	t_{AOH}	5		5		5		ns
Access time from W precharge	t_{WPA}		30		35		45	ns
Access time relative to last write*6	t_{ALW}		90		110		140	ns

Notes: *1 An initial pause ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}) of 200 μs is required after power-up, followed by any 8 $\overline{RAS}$-only cycles, before proper device operation is achieved. If the internal refresh counter is to be effective, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required.

*2 AC characteristics assume t_T = 5 ns, V_{IN} = 0V to 3V, V_{IH} = 2.4V, V_{IL} = 0.8V, V_{OH} = 2.4V, and V_{OL} = 0.4V.

*3 Assumes that $t_{RAD} \geq t_{RAD}$ (max). If t_{RAD} is greater than the maximum recommended value then t_{RAC} is increased by the amount that t_{RAD} exceeds t_{RAD} (max).

*4 Assumes that $t_{RAD} \geq t_{RAD}$ (max).

*5 Measured with a load equivalent to 2 TTL loads and 100 pF.

*6 Assumes that $t_{LWAD} \geq t_{LWAD}$ (max). If t_{LWAD} is greater than the maximum recommended value then t_{ALW} is increased by the amount that t_{LWAD} exceeds t_{LWAD} (max).

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)*1,2

Parameter	Symbol	MB81C466-10 Min	MB81C466-10 Max	MB81C466-12 Min	MB81C466-12 Max	MB81C466-15 Min	MB81C466-15 Max	Unit
$\overline{RAS}$ precharge time	t_{RP}	90		100		100		ns
$\overline{RAS}$ pulse width	t_{RAS}	65	100000	75	100000	95	100000	ns
$\overline{RAS}$ hold time (read)	t_{RSH}	25		30		35		ns
$\overline{CAS}$ pulse width (read)	t_{CAS}	25	100000	30	100000	35	100000	ns
$\overline{CAS}$ pulse width (write)	t_{CAS}	15	100000	20	100000	25	100000	ns
$\overline{CAS}$ hold time (read)	t_{CSH}	100		120		150		ns
$\overline{CAS}$ hold time (write)	t_{CSH}	80		95		115		ns
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	75	25	90	30	115	ns
$\overline{CAS}$ to $\overline{RAS}$ set up time	t_{CRS}	20		25		30		ns
Row address set up time	t_{ASR}	0		0		0		ns
Row address hold time	t_{RAH}	15		15		20		ns
Column address set up time*7	t_{ASC}	0		0		0		ns
Column address hold time*7	t_{CAH}	15		15		20		ns
$\overline{RAS}$ to column address delay time*8,9	t_{RAD}	20	55	20	65	25	80	ns
Column address hold time referenced to $\overline{RAS}$	t_{AR}	100		120		150		ns
Write address hold time referenced to $\overline{RAS}$	t_{AWR}	80		90		110		ns
Read address to $\overline{RAS}$ lead time	t_{RAL}	45		55		70		ns
Column address hold time referenced to $\overline{RAS}$ rising time*10	t_{AHR}	15		15		20		ns
Last write to column address delay time*11,12	t_{LWAD}	20	45	20	55	25	70	ns
Column address hold time referenced to last write	t_{AHLW}	90		110		140		ns
Read command set up time referenced to $\overline{CAS}$	t_{RCS}	0		0		0		ns
Read command hold time referenced to $\overline{RAS}$*13	t_{RRH}	10		10		10		ns
Read command hold time referenced to $\overline{CAS}$*13	t_{RCH}	0		0		0		ns
$\overline{W}$ pulse width	t_{WP}	15		20		25		ns
$\overline{W}$ inactive time	t_{WI}	15		20		25		ns
Write command hold time	t_{WCH}	15		20		25		ns
Write command to $\overline{RAS}$ lead time	t_{RWL}	25		30		35		ns
Write command to $\overline{CAS}$ lead time	t_{CWL}	25		30		35		ns

Notes:
*7 Write Cycle only.
*8 Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
*9 t_{RAD} (min) = t_{RAH} (min) + t_T (t_T = 5 ns).
*10 t_{AHR} is specified to latch column address by the rising edge of RAS.
*11 Operation within the t_{LWAD} (max) limit insures that t_{ALW} (max) can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled by T_{AA}.
*12 t_{LWAD} (min) = t_{CAH} (min) + t_T (t_T = 5 ns).
*13 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)*1,2

Parameter	Symbol	MB81C466-10 Min	MB81C466-10 Max	MB81C466-12 Min	MB81C466-12 Max	MB81C466-15 Min	MB81C466-15 Max	Unit
$\overline{RAS}$ to $\overline{W}$ delay time*14	t_{RWD}	125		150		185		ns
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	50		60		70		ns
Column address to $\overline{W}$ delay time	t_{AWD}	70		85		100		ns
$\overline{RAS}$ to second write delay time	t_{RSWD}	100		120		150		ns
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	80		95		115		ns
$\overline{RAS}$ precharge time from last write	t_{RPLW}	135		155		165		ns
Write set up time for output disable*14	t_{WS}	0		0		0		ns
Write hold time for output disable*14	t_{WH}	0		0		0		ns
IN set up time	t_{DS}	0		0		0		ns
IN hold time	t_{DH}	0		15		20		ns
IN hold time referenced to $\overline{RAS}$	t_{DHR}	80		90		110		ns
Access time from $\overline{OE}$	t_{OEA}		25		30		35	ns
$\overline{OE}$ to data in delay time	t_{OED}	20		25		30		ns
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	0	20	0	25	0	30	ns
$\overline{OE}$ hold time referenced to $\overline{RAS}$*15	t_{OEHR}	20		20		20		ns
$\overline{OE}$ hold time referenced to $\overline{CAS}$*15	t_{OEHC}	10		20		20		ns
Refresh set up time for $\overline{CAS}$ referenced to $\overline{RAS}$ ($\overline{C}$-B-$\overline{R}$)	t_{FCS}	25		25		30		ns
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$ ($\overline{C}$-B-$\overline{R}$)	t_{FCH}	25		25		30		ns
$\overline{CAS}$ precharge time ($\overline{C}$-B-$\overline{R}$)	t_{CPR}	25		25		30		ns
$\overline{RAS}$ precharge time to $\overline{CAS}$ active time (refresh cycles)	t_{RPC}	20		20		20		ns
Static mode read/write cycle time	t_{SC}	50		60		75		ns
Static mode read-modify-write cycle time	t_{SRWC}	120		145		180		ns
Static mode $\overline{CAS}$ precharge time	t_{CP}	15		20		25		ns
$\overline{OE}$ to $\overline{RAS}$ inactive set up time	t_{OES}	25		30		35		ns
IN to $\overline{CAS}$ delay time*16	t_{DZC}	0		0		0		ns
IN to $\overline{OE}$ delay time*16	t_{DZO}	0		0		0		ns
Refresh counter test cycle time*17	t_{RTC}	465		550		645		ns

Notes: *14 t_{WS}, and t_{RWD} are specified as a reference point only. If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), the data output pin will remain High-Z state throughout entire cycle. It $t_{RWD} \geq t_{RWD}$ (min). The data output will contain data read from the selected cell.

*15 Either t_{OEHR} or t_{OEHC} is satisfied, output is disabled.

*16 Either t_{DZC} or t_{DZO} must be satisfied.

*17 CAS-before-RAS refresh counter test cycle only.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)*1,2

Parameter	Symbol	MB81C466-10 Min	MB81C466-10 Max	MB81C466-12 Min	MB81C466-12 Max	MB81C466-15 Min	MB81C466-15 Max	Unit
Refresh counter test $\overline{RAS}$ pulse width*17	t_{TRAS}	365	10000	440	10000	535	10000	ns
Refresh counter test $\overline{CAS}$ precharge time*17	t_{CPT}	50		60		70		ns
Refresh counter test $\overline{RAS}$ to column address delay time*17	t_{CADT}		100		120		150	ns
Refresh counter test access time from $\overline{CAS}$*17	t_{CACT}		135		165		205	ns
Refresh counter test $\overline{CAS}$ to $\overline{W}$ delay time*17	t_{CWDT}	135		165		205		ns

Notes: *17 $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only.

Description

Address Inputs

A total of sixteen binary input address bits are required to decode parallel 4-bits of the 262,144 storage cells within the MB81C466. Eight row address bits are established on the address input pins (A_0 to A_7) and latched with the Row Address Strobe ($\overline{RAS}$). Eight column address bits are established on the address input pins (A_0 to A_7) after the Row Address Hold Time has been satisfied. In read cycle, the column addresses are not latched by the Column Address Strobe ($\overline{CAS}$), so the column address must be stable until the output becomes valid. In write cycle, the column addresses are latched by the later falling edge of $\overline{CAS}$ or $\overline{W}$.

Write Enable

Read or Write cycle is selected with the $\overline{W}$ inputs. A high on $\overline{W}$ selects read cycle and low selects write cycle. The write operation is asserted on the latter falling edge of $\overline{CAS}$ or $\overline{W}$ (Both $\overline{CAS}$ and $\overline{W}$ are low.). The time period of the write operation is determined by internal circuit, thus the next write operation will be inhibited during the write operation.

Data Pins

Data Inputs;
Data is written into the MB81C466 during write or read-modify-write cycle. The input data is strobed and latched by the later falling edge of $\overline{CAS}$ or $\overline{W}$.

Data Output

The output buffer is three-state TTL compatible with a fan out of two standard TTL loads. Data out has the same porality as data in. The output is in high impedance state until $\overline{CAS}$ is brought low. In a read cycle, the access time is determined by the following conditions:

1. t_{RAC} from the falling edge of $\overline{RAS}$.
2. t_{AA} from the column address inputs.
3. t_{CAC} from the falling edge of $\overline{CAS}$.
4. t_{OEA} from the falling edge of $\overline{OE}$.

When both t_{RCD} and t_{RAD} satisfy their maximum limits, $t_{RAC} = t_{RCD} + t_{CAC}$ or $t_{RAC} = t_{RAD} + t_{AA}$.

Data output remains valid while the column address inputs are kept constant. However, when either $\overline{CAS}$ or $\overline{OE}$ goes high, the output returns to a high impedance state. In the static write cycle ($\overline{CAS}$ controlled), if both $t_{WS} \geqslant t_{WS}$ (min) and $t_{WH} \geqslant t_{WH}$ (min) are met, data pins are input mode regardless of the state of $\overline{OE}$.

Output Enable

The $\overline{OE}$ controls the impedance of the output buffers. If the $\overline{OE}$ is high the output buffers are in the high impedance state. If the $\overline{OE}$ is low the output buffers are in the low impedance state. In the write cycle ($\overline{W}$ controlled), the $\overline{OE}$ must be high before the data applied to DQ pins. When $\overline{W}$ controlled write cycles is not used, $\overline{OE}$ can be low throughout the operation.

Static Mode

The static mode operation allows continuous read, write, or read-modify-write cycle within a row by applying new column address. In the static mode, $\overline{CAS}$ can be kept low throughout static mode operation. The following four cycles are allowed in the static mode.

1. Static mode read cycle;
   In a static mode read cycle, the access time is t_{RAC} from the falling edge of $\overline{RAS}$ or t_{AA} from the column address input or t_{OEA} from the falling edge of $\overline{OE}$. The data remains valid for a time t_{AOH} after the column address is changed.
2. Static mode write cycle;
   In a static mode write cycle, the data is written into the cell triggered by the later falling edge of $\overline{CAS}$ or $\overline{W}$. If both t_{WS} and t_{WH} are greater than their minimum limits, the data output pin is kept high impedance state through the static mode write cycle. The $\overline{OE}$ must be high before the data are applied to DQ pins.

Description
(Continued)

3. Static mode read-modify-write cycle;
   In a static mode read-modify-write cycle, $\overline{W}$ goes low after t_{AWD} from the column address inputs and t_{CWD} from the falling edge of $\overline{CAS}$. the data and column address inputs are strobed and latched by the falling edge of $\overline{W}$. The $\overline{OE}$ must be high before the data are applied to DQ pins.
4. Static mode mixed cycle;
   In a static mode, read, write, and read-modify-write cycles can be mixed in any order.

In the next static mode read, write cycle or read-modify-write cycle, the access time is determined by the following conditions.

1. t_{ALW} from the falling edge of $\overline{W}$ at previous write cycle.
2. t_{AA} from the column address inputs.
3. t_{WPA} from the rising edge of $\overline{W}$ at the read cycle.
4. t_{CAC} from the falling edge of $\overline{CAS}$.
5. t_{OEA} from the falling edge of $\overline{OE}$.

Refresh

Refresh of dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row addresses (A_0 to A_7 at least every 4 ms.)

The MB81C466 offers the following three types of refresh.

1. $\overline{RAS}$ only refresh;
   $\overline{RAS}$-only refresh avoids any output during refresh because the output buffer is high in the impedance state due to $\overline{CAS}$ = high. Strobing of each 256 row address (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed.
2. $\overline{CAS}$-before-$\overline{RAS}$ refresh;
   $\overline{CAS}$-before-$\overline{RAS}$ refreshing available on the MB81C466 offers an alternate refresh method. If $\overline{CAS}$ is held low for the specified period (t_{FCS}) before $\overline{RAS}$ goes low, on chip refresh control clock generator and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.
3. Hidden refresh;
   A hidden refresh cycle may take place while maintaining latest valid data at the output pin by extending the $\overline{CAS}$ low time. For the MB81C466, a hidden refresh cycle is $\overline{CAS}$-before-$\overline{RAS}$ refresh. The internal refresh address counter provides the refresh address, as in a normal $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test

A special timing sequence using $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method of verifying the function of $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry. After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes to high and then goes to low again while $\overline{RAS}$ is held low, the read and read-modify-write cycles are enabled according to the state of $\overline{W}$. This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell address, consisting of a row address (8-bits) and a column address (8-bits), to be accessed are shown below.

ROW ADDRESS—Bits A_0 to A_7 are provided by the refresh counter.

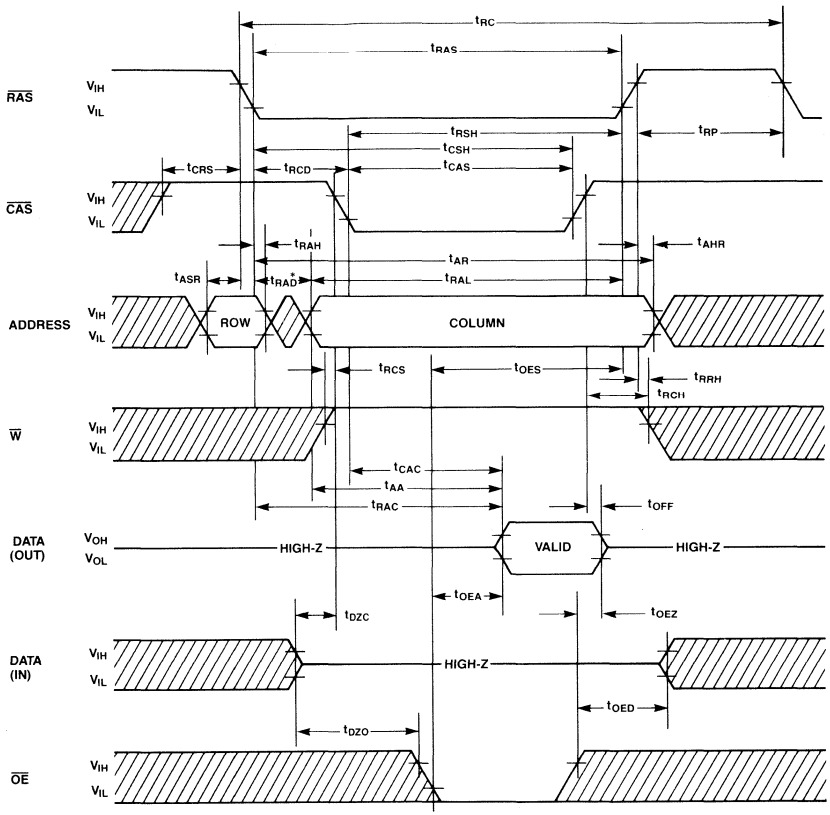
COLUMN ADDRESS—All the bits A_0 to A_7 are provided by externally after t_{CADT}.

The recommended procedure of $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test is shown below. The timing of $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle should be used.

1) Initialize the internal refresh address counter by using eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
2) Throughout the test, use the same column address.
3) Using a write cycle, write 0s to all 256 row addresses.
4) Using $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle in read-modify-write mode, read the 0 written in step 3), and simultaneously write 1 to the same cell. This step is repeated 256 times and row address is generated by internal refresh address counter.
5) Using a normal read cycle, read back the 1 written in step 4), from all 256 locations.
6) Complement the test pattern and repeat step 3), 4), and 5).

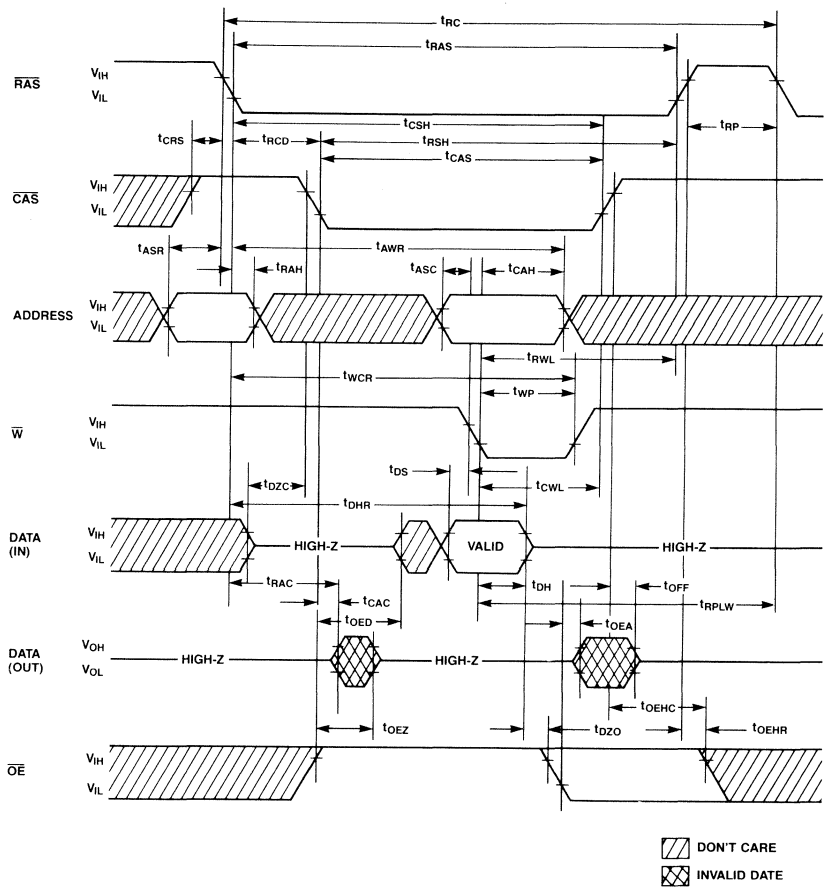
Timing Diagrams

Read Cycle



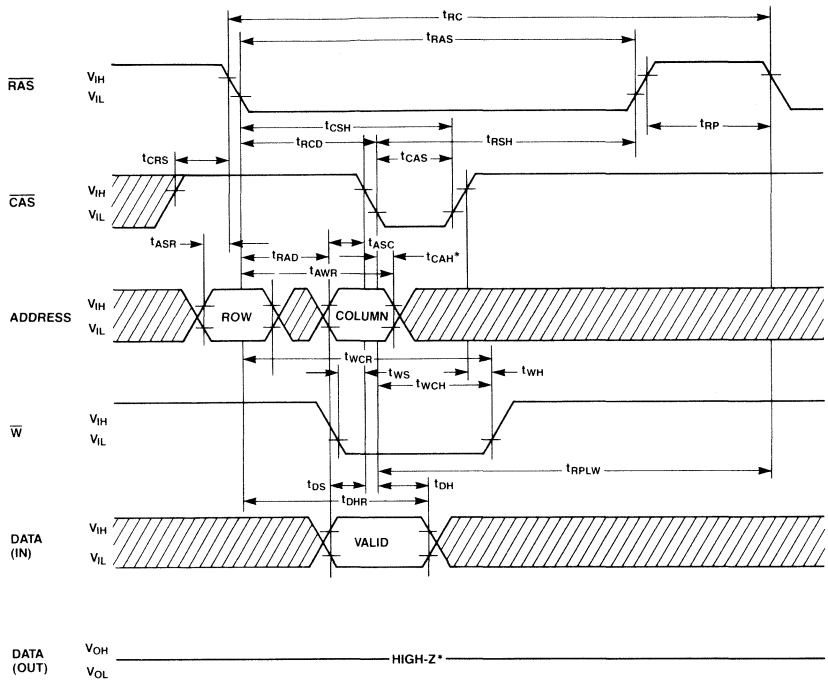
Timing Diagrams
(Continued)

Write cycle ($\overline{W}$ controlled)



Timing Diagrams
(Continued)

Write Cycle ($\overline{CAS}$ Controlled)
$\overline{OE}$; Don't Care

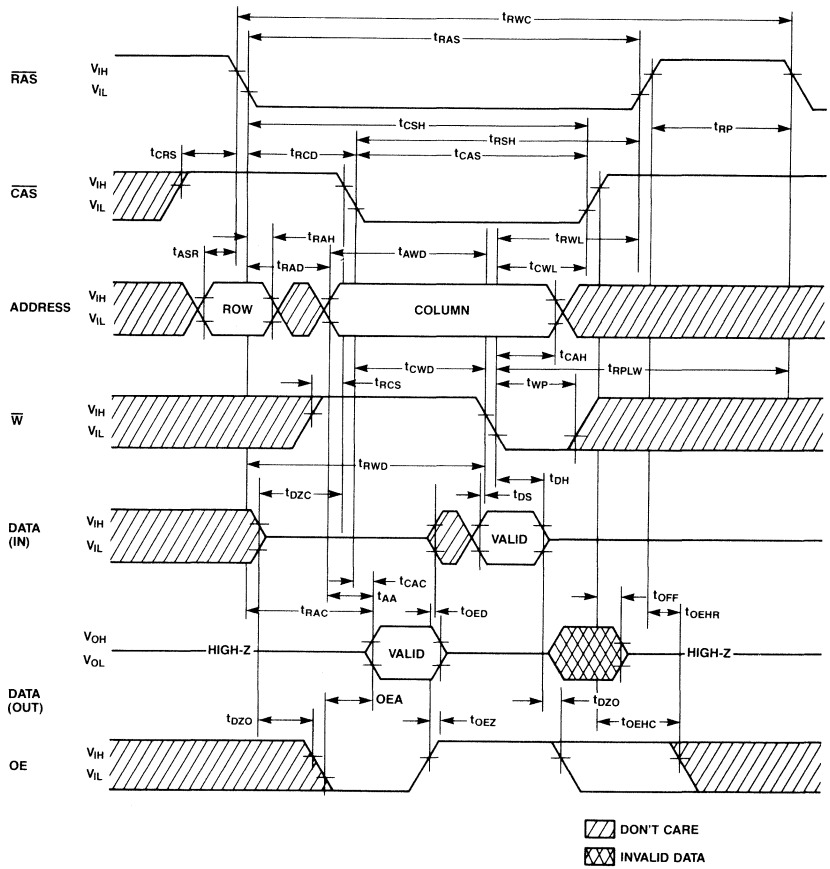


* IF OE IS KEPT HIGH THROUGH A CYCLE OR $t_{WS} \geq t_{WS}$ (MIN) and $t_{WH} \geq t_{WH}$ (MIN) ARE MET, DQ PINS ARE KEPT HIGH IMPEDANCE STATE.

DON'T CARE

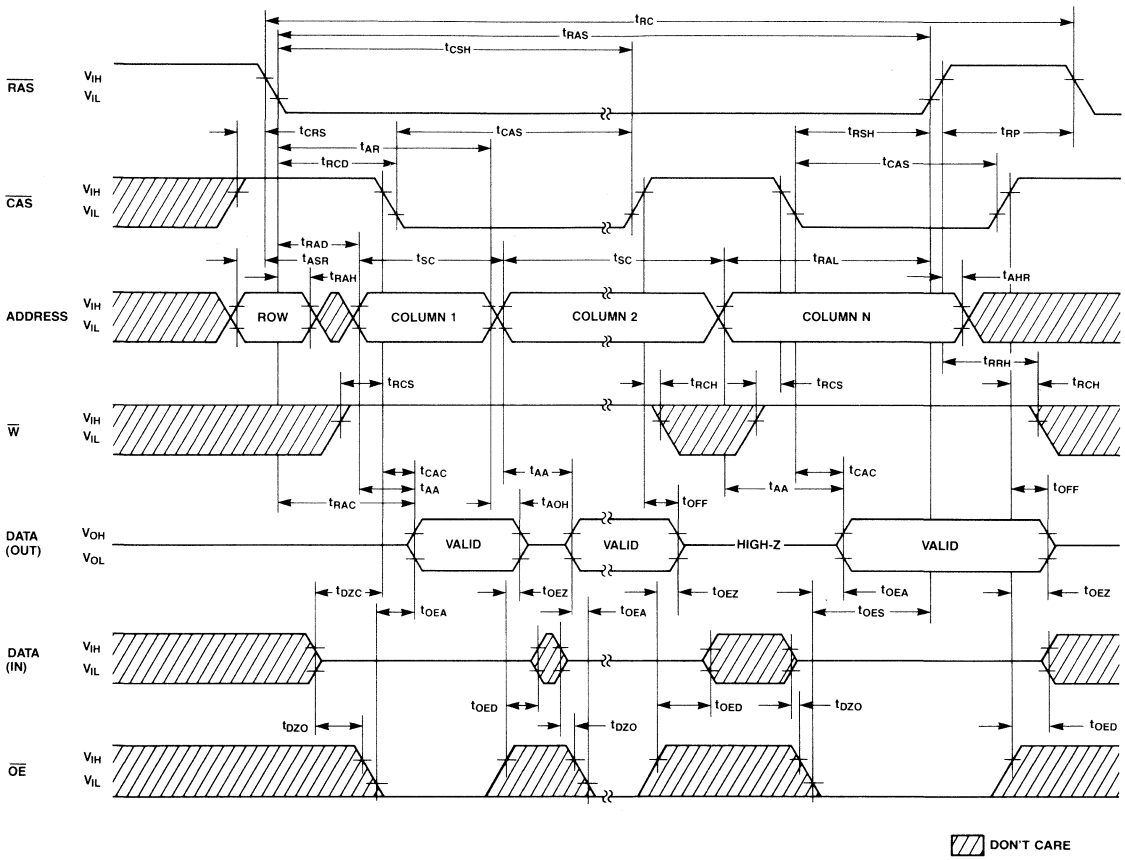
Timing Diagrams
(Continued)

Read-Modify-Write Cycle



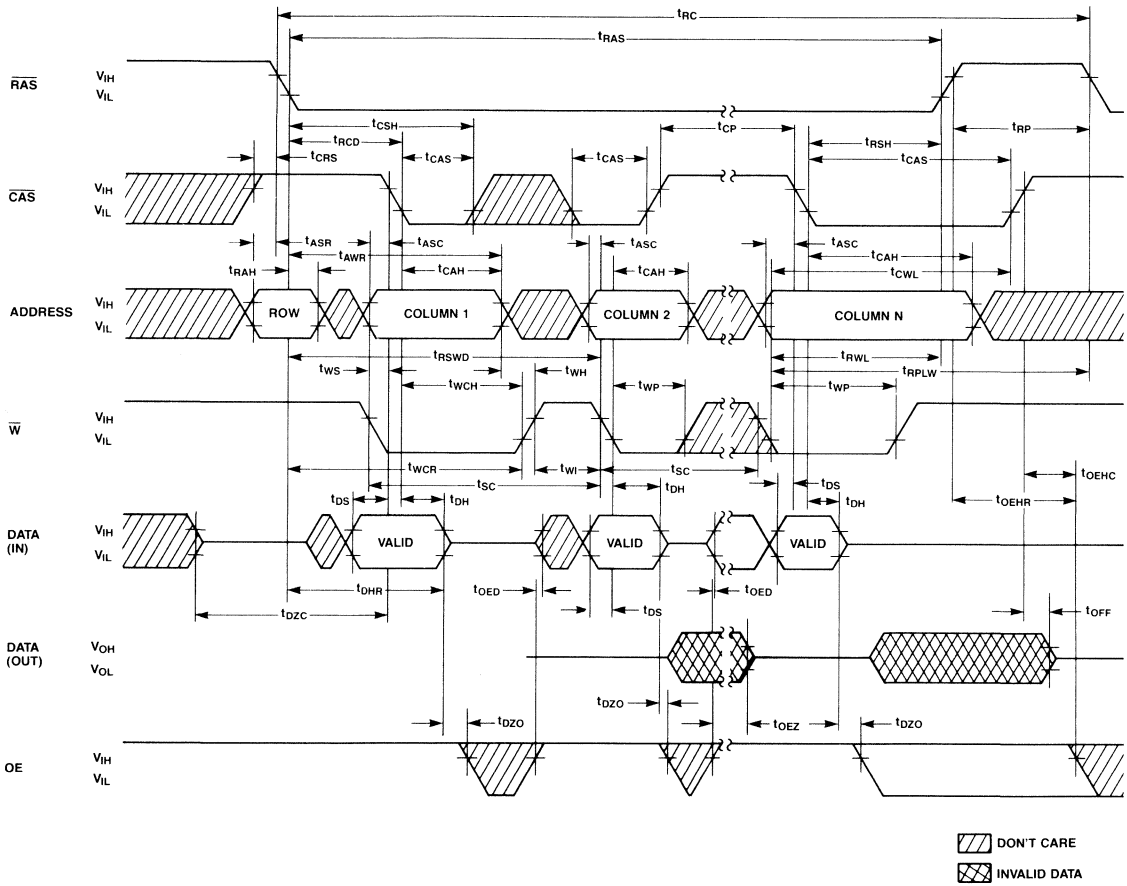
Timing Diagrams
(Continued)

Static Mode Read Cycle



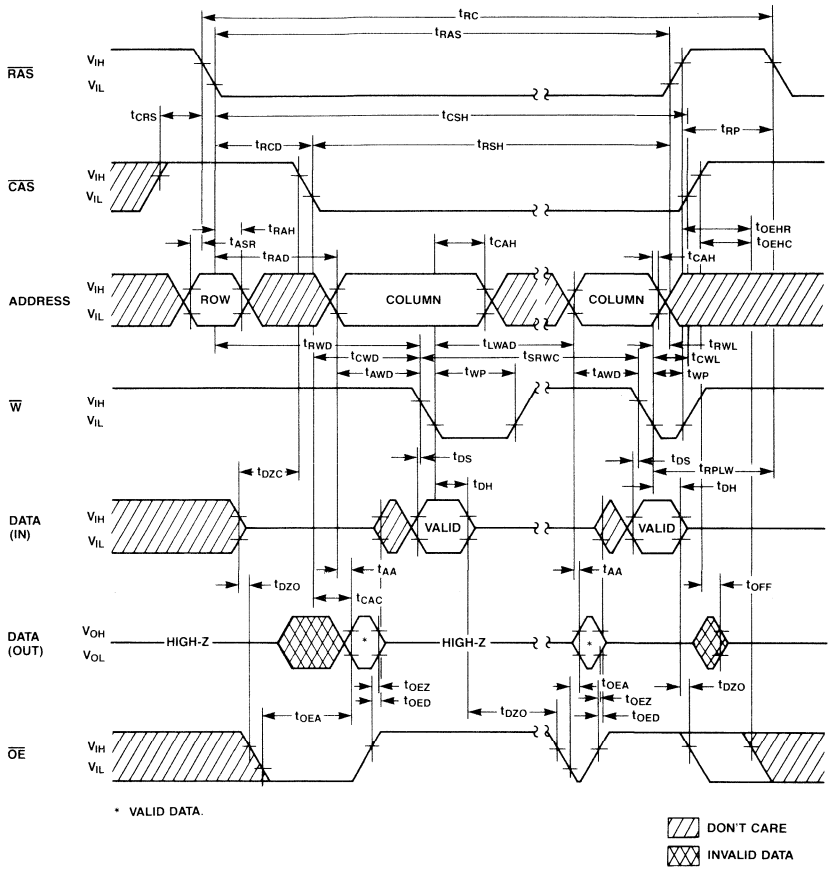
Timing Diagrams
(Continued)

Static Mode Write Cycle



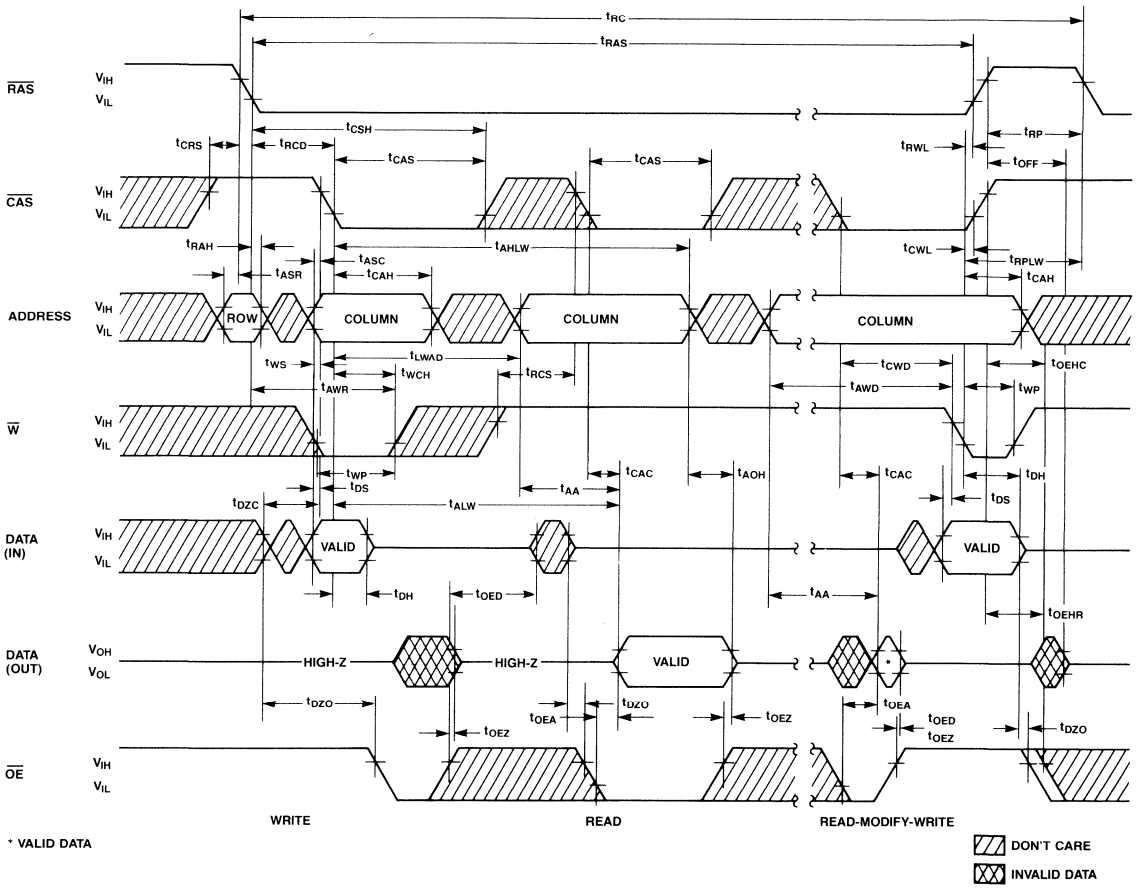
Timing Diagrams
(Continued)

Static Mode Read-Modify-Write Cycle



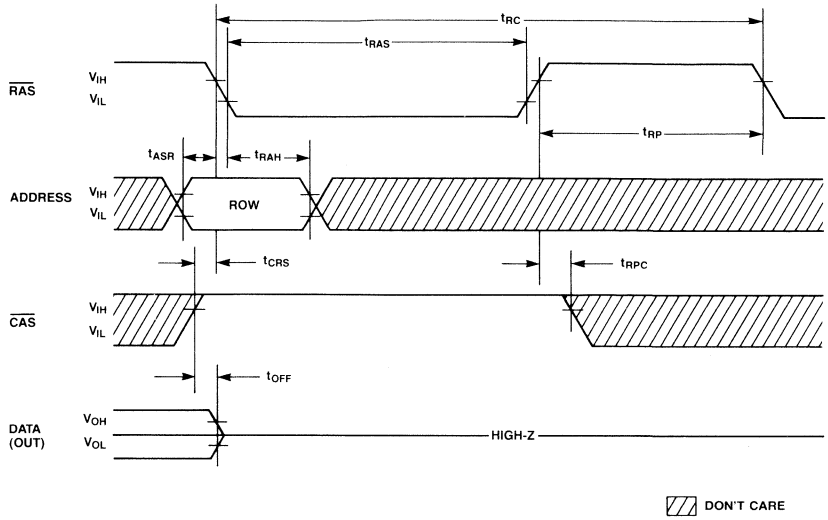
Timing Diagrams
(Continued)

Static Mode Mixed Cycle

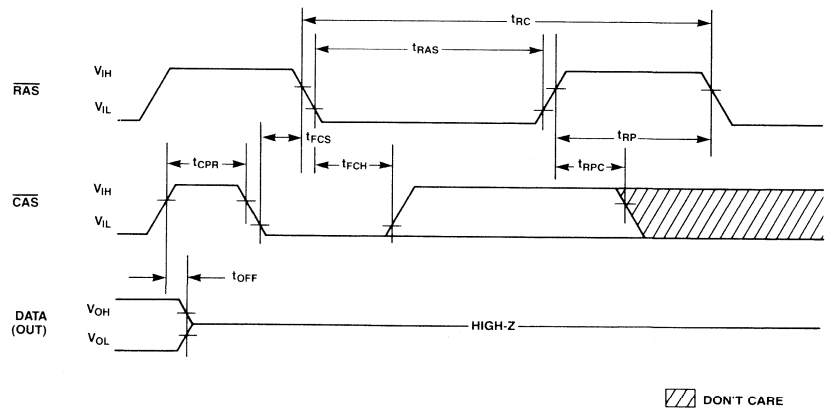


Timing Diagrams
(Continued)

$\overline{RAS}$-Only Refresh Cycle
(Note; $\overline{W}$, $\overline{OE}$, IN = Don't Care)

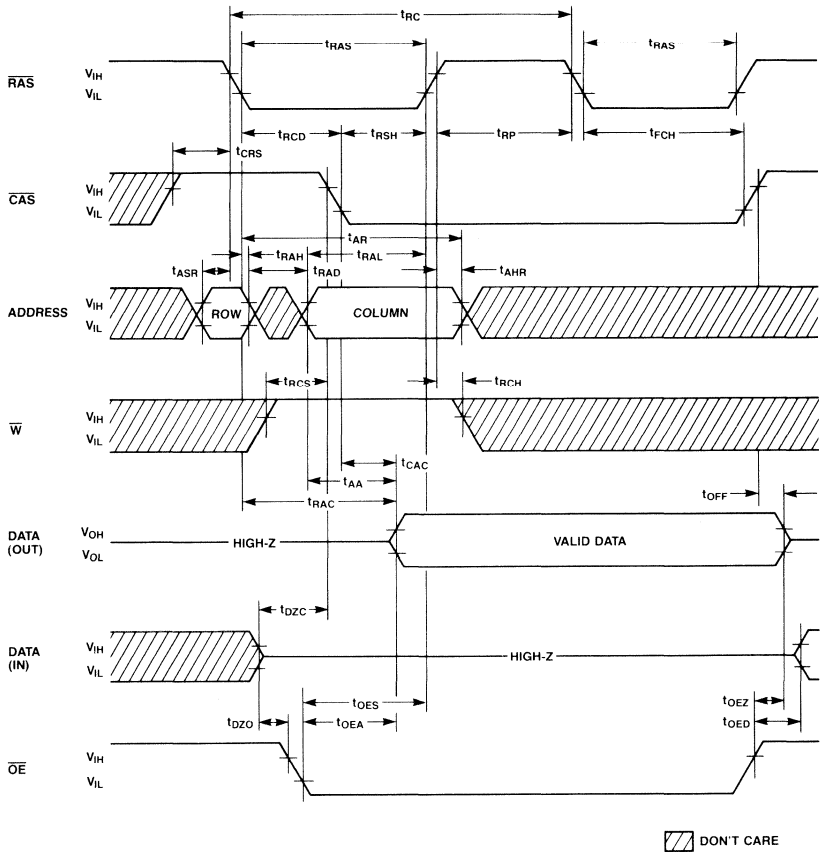


$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle
(Note; Address, $\overline{W}$, $\overline{OE}$, IN = Don't Care)



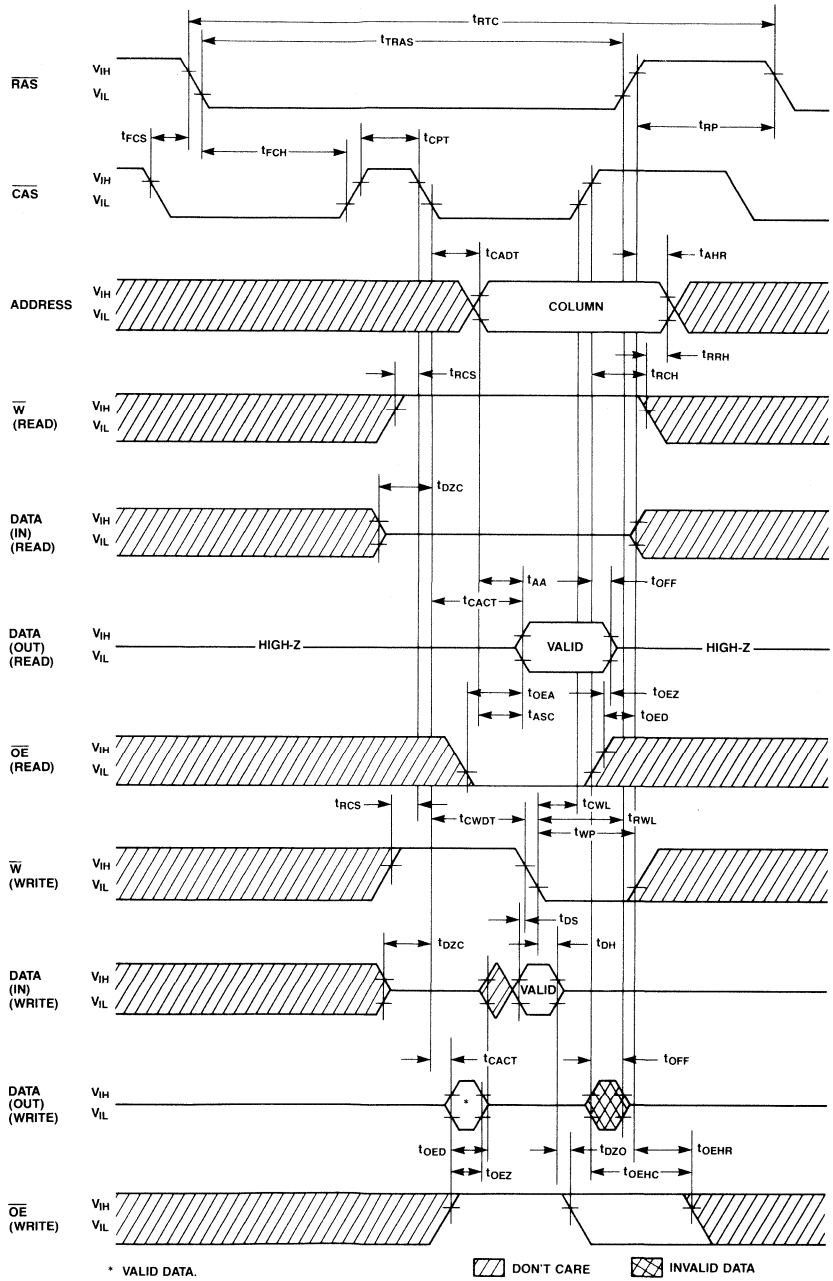
Timing Diagrams
(Continued)

Hidden Refresh Cycle



Timing Diagrams
(Continued)

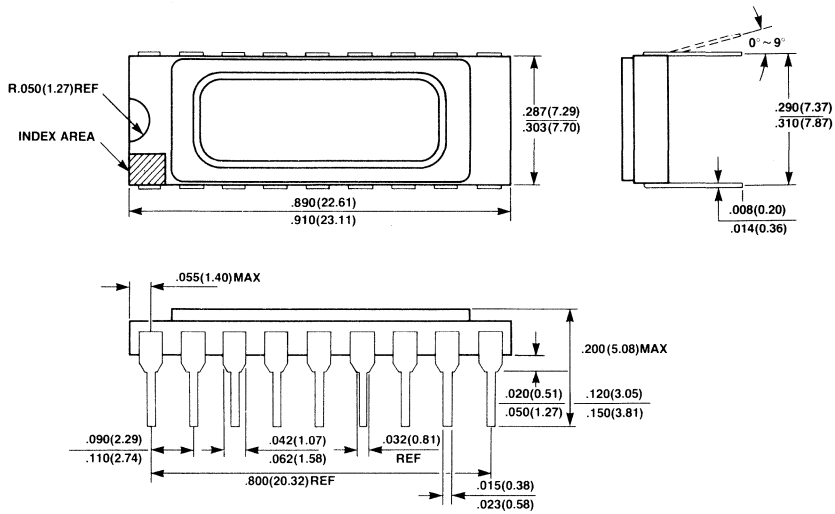
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



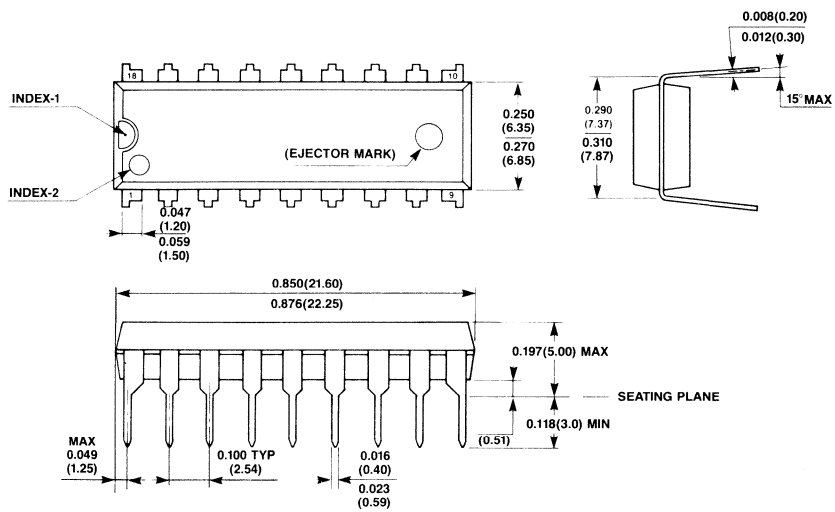
Package Dimensions

Dimensions in inches
(millimeters)

18-Lead Ceramic (Metal Seal) Dual-In-Line Package (Case No.: DIP-18C-A01)

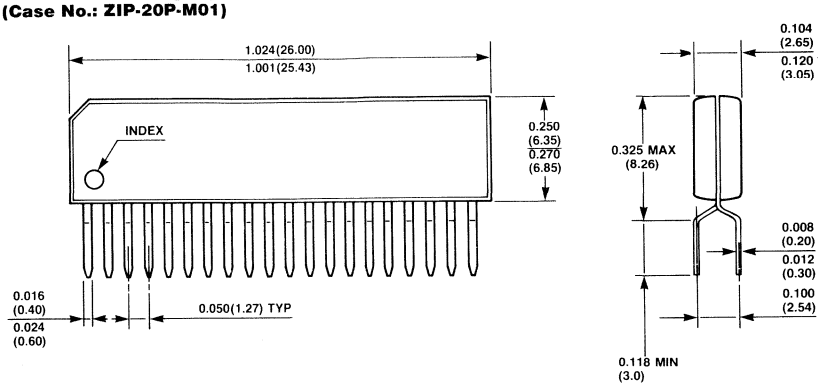


18-Lead Plastic Dual-In-Line Package (Case No.: DIP-18P-M03)



Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

20-Lead Plastic ZigZag-In-Line Package
(Case No.: ZIP-20P-M01)



CMOS Static RAMs

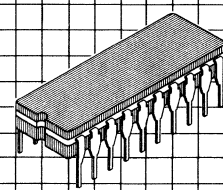
MB81C67 3-2
MB81C67-W 3-8
MB81C68 3-16
MB81C68-A 3-24
MB81C68-W 3-31
MB81C69A 3-39
MB81C71 3-46
MB81C74 3-54
MB81C78 3-55
MB81C79 3-64
MB81C86 3-73
MB8416/8416L 3-80
MB8416A/8416AL 3-88
MB8416W 3-96
MB8417/8417L 3-102
MB8417A/8417AL 3-110
MB8418/8418L 3-118
MB8418A/8418AL 3-125
MB8464/8464L/8464LL 3-132
MB8464X/8464W 3-144
MB8464A/8464AL/8464ALL 3-154
MB8464AW 3-166
MB84256/84256L 3-177

■ MB81C67-35, MB81C67-45
CMOS 16,384-BIT
Static Random Access Memory

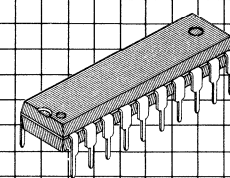
Description

The Fujitsu MB81C67 is a 16,384 words by 1-bit static Random Access Memory fabricated using a C-MOS silicon gate process for peripheral circuitry, and N-Channel silicon gate MOS technology for the memory cell array. Separate input/output pins are provided. All devices are fully compatible with TTL logic families in all respects: inputs, output levels and loading, and in the use of a single, +5 V DC supply.

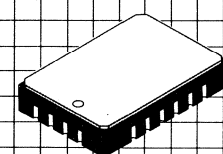
For ease of use, chip enable (/E) permits the selection of an individual device when outputs of multiple devices are OR-tied, and automatically powers the MB81C67 down when not enabled. This device offers the advantages of low power dissipation, low cost, and high performance.



Cerdip Package
DIP-20C-C03



Plastic Package
DIP-20P-M01

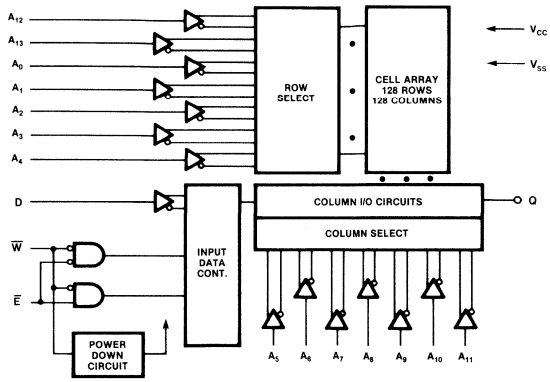


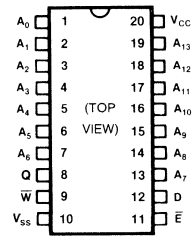
Ceramic LCC
LCC-20C-F01

Features

- 16,384 words x 1 bit organization
- Static operation: no clocks or refresh required
- Fast Access Time:
  MB81C67-35
  TAVQV = TELQV = 35 ns max.
  MB81C67-45
  TAVQV = TELQV = 45 ns max.
- Single +5V supply ±10% tolerance
- Separate data input and output
- TTL compatible inputs and output
- Three-state output with OR-tie capability
- Chip enable for simplified memory expansion, automatic power down
- All inputs and output have protection against static charge
- Standard 20-pin DIP package
- Pin compatible with Fujitsu MB8167A

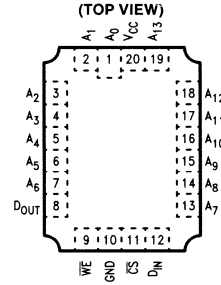
MB81C67 Block Diagram and Pin Assignments





Cerdip and Plastic DIP

(TOP VIEW)



(LCC-20C-F01)

Truth Table

$\overline{E}$	$\overline{W}$	Mode	Output	Power
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	Q	ACTIVE

Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Supply Voltage		V_{CC}	−0.5 to +7	V
Input voltage on any pin with respect to GND		V_{IN}	−3.5 to +7	V
Output voltage on any pin with respect to GND		V_{OUT}	−0.5 to +7	V
Temperature Under Bias		T_{BIAS}	−10 to +85	°C
Storage Temperature	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−40 to +125	
Power Dissipation		P_D	1.0	W
Output Current		I_{OUT}	±20	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Capacitance
(T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	—	5	pF
$\overline{E}$ Capacitance ($V_{\overline{E}}$ = 0V)	$C_{\overline{E}}$	—	7	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}	—	8	pF

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−3.0*	—	0.8	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Ambient Temperature	T_A	0	—	70	°C

* −3.0 V Min. for Pulse width less than 20 ns. (V_{IL} Min = −1.0 V at DC level)

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Max	Unit
Input Leakage Current	V_{IN} = 0V to V_{CC}	I_{LI}	−2	+2	μA
Output Leakage Current	$\overline{E} = V_{IH}$, V_{OUT} = 0V to V_{CC}	I_{LO}	−2	+2	μA
Active Supply Current	$\overline{E} = V_{IL}$, I_{OUT} = 0mA $V_{IN} = V_{IL}$ or V_{IH}	I_{CC1}	—	40	mA
Operating Supply Current	$\overline{E} = V_{IL}$, I_{OUT} = 0mA Cycle = min, CL = 0pF	I_{CC2}	—	60	mA
Standby Supply Current	$\overline{E} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	I_{SB1}		15	mA
Standby Supply Current	$\overline{E} = V_{IH}$	I_{SB2}	—	25	mA
Output Low Voltage	I_{OL} = 16mA	V_{OL}	—	0.4	V
Output High Voltage	I_{OH} = −4mA	V_{OH}	2.4	—	V

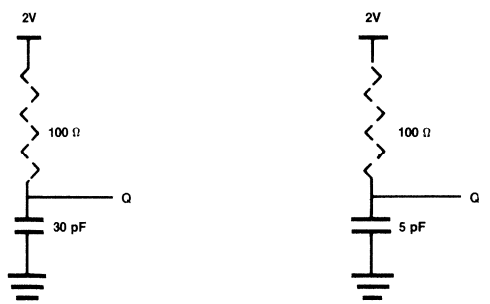
AC Characteristics
Recommended operating conditions unless otherwise noted.)

Read Cycle		MB 81C67-35		MB 81C67-45	
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**
Read Cycle Time	TAVAX	35	—	45	—
Address Access Time	TAVQV	—	35	—	45
Chip Select Access Time	TELQV	—	35	—	45
Output Hold from Address Change	TAXQX	5	—	5	—
Chip Enable to Output in Low-Z	TELQX	5	—	5	—
Chip Enable to Output in High-Z	TEHQZ	0	25	0	25
Chip Selection to Power UP	TELIH	0		0	
Chip Deselection to Power Down	TEHIL		30		40

AC Test Conditions

Input Pulse Levels: 0.6V to 2.4V
Input Pulse Rise and Fall Times: 5ns
Timing Measurement Reference Levels: Inputs: 1.5V
Output: 1.5V

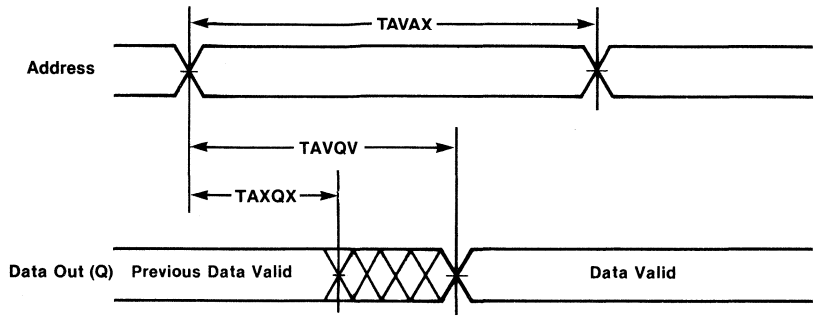
Output Load:



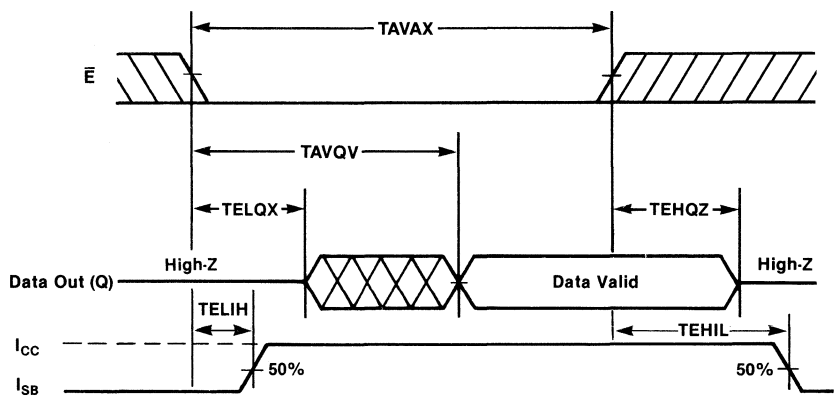
(For TEHQZ, TWLQZ, TELQX, TWHQX)

Read Cycle Timing Diagram*1

Read Cycle: Address Controlled *2



Read Cycle: $\overline{E}$ Controlled *3



Note: *1) $\overline{W}$ is high for Read cycle.
*2) Device is continuously selected, $\overline{E} = V_{IL}$.
*3) Address valid prior to or coincident with $\overline{E}$ transition low.

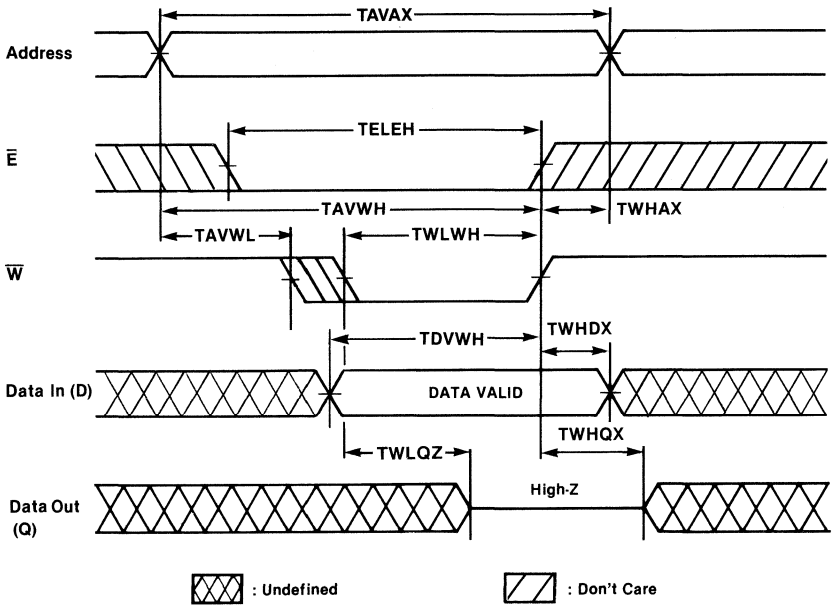
: Undefined
: Don't Care

Write Cycle

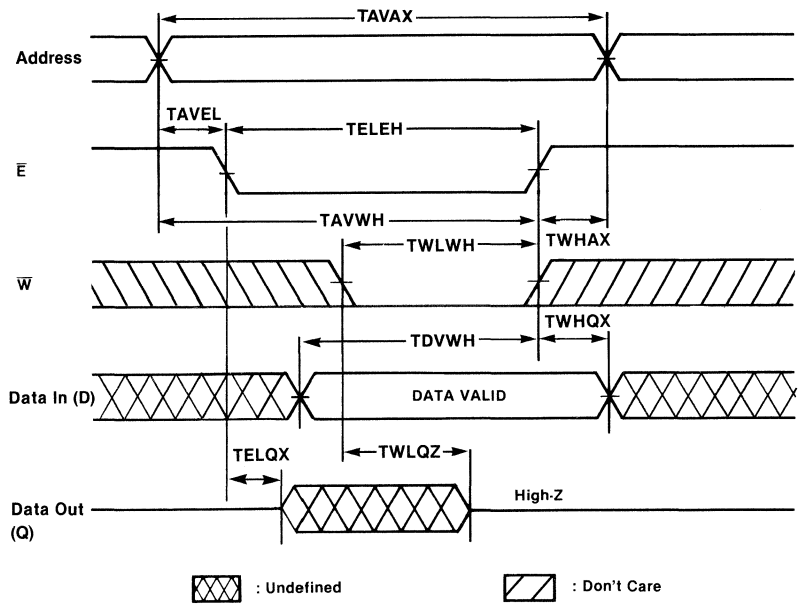
Parameter	Symbol	MB 81C67-35 Min	MB 81C67-35 Max	MB 81C67-45 Min	MB 81C67-45 Max
Write Cycle Time	TAVAV	35	—	45	—
Chip Enable to End of Write	TELEH	30	—	35	—
Address Valid to End of Write	TAVWH	30	—	35	—
Address Setup Time	TAVWL	0	—	0	—
Write Pulse Width	TWLWH	20	—	25	—
Data Valid to End of Write	TDVWH	20	—	20	—
Write Recovery Time	TWHAX	0	—	0	—
Data Hold Time	TWHDX	0	—	0	—
Write Enable to Output in High-Z	TWLQZ	0	25	0	25
Output Active from End of Write	TWHQX	0	25	0	25

Write Cycle Timing Diagram

Write Cycle: $\overline{W}$ Controlled

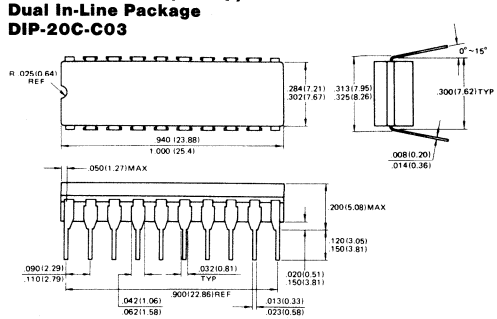


Write Cycle: $\overline{E}$ Controlled

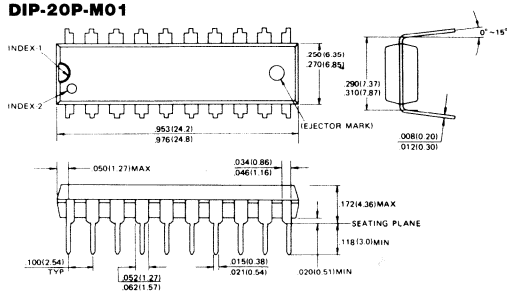


Package Dimensions

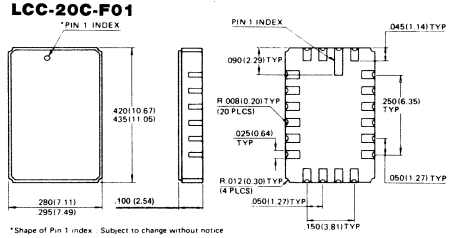
20-Lead Ceramic (Cerdip) Dual In-Line Package DIP-20C-C03



20-Lead Plastic Dual In-Line Package DIP-20P-M01



20-Pad Ceramic (Frit Seal) Leadless Chip Carrier LCC-20C-F01



*Shape of Pin 1 index. Subject to change without notice

MB81C67-45-W, MB81C67-55-W

CMOS 16,384-Bit Static Random Access Memory

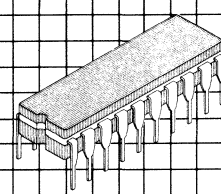
Description

The Fujitsu MB81C67 is a 16,384 word x 1-bit static random access memory fabricated with a CMOS silicon gate process. This device is fully static and requires no clock or timing strobes. All pins are TTL compatible and a single 5 volt power supply is required.

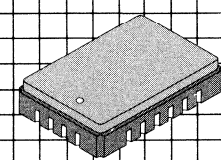
For ease of use, chip enable ($\overline{E}$) permits the selection of an individual package when outputs are OR-tied, and automatically powers down the MB81C67. All devices offer the advantages of low power dissipation, low cost, and high performance.

Features

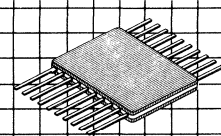
- **Organization: 16,384 words x 1-bit**
- **Static operation: no clocks or refresh required**
- **Fast access time: 45 ns max. (MB81C67-45-W) 55 ns max. (MB81C67-55-W)**
- **Single +5V supply, ±10% tolerance**
- **Separate data input and output**
- **TTL compatible inputs and output**
- **Three-state output with OR-tie capability**
- **Chip enable for simplified memory expansion, automatic power down**
- **All inputs and output have protection against static charge**
- **Standard 20-pin DIP package**
- **Pin compatible with Fujitsu MB8167A**



Ceramic Package CERDIP DIP-20C-C03



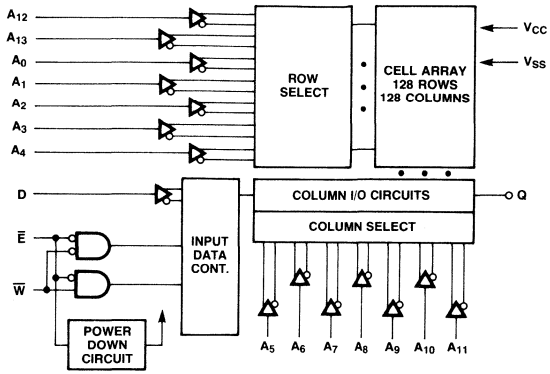
LCC-20C-F01

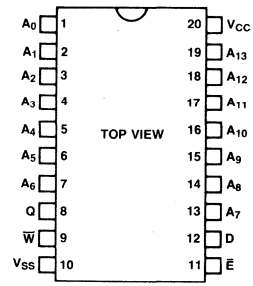


Ceramic Flatpack FPT-20C-C02

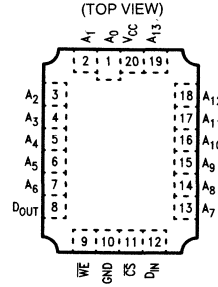
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB81C67 Block Diagram and Pin Assignment





(TOP VIEW)



(LCC-20C-F01)

TRUTH TABLE

$\overline{E}$	$\overline{W}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	HIGH-Z	ACTIVE
L	H	READ	Q	ACTIVE

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	−0.5 to +7.0	V
Input voltage on any pin with respect to V_{SS}	V_{IN}	−3.5 to +7.0	V
Output voltage on any pin with respect to V_{SS}	V_{OUT}	−0.5 to +7.0	V
Temperature under bias	T_{BIAS}	−55 to +125	°C
Storage temperature	T_{STG}	−65 to +150	°C
Power dissipation	P_D	1.0	W
Output current	I_{OUT}	±20	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low voltage	V_{IL}	−2.0*1		0.7	V
Input high voltage	V_{IH}	2.3		6.0	V
Ambient temperature	T_A	−55		125	°C

Note: *1 −2.0 min. for pulse width less than 20 ns (V_{IL} min. = −0.5V at DC level).

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input capacitance (V_{IN} = 0V)	C_{IN}		5	pF
$\overline{E}$ capacitance (V_E = 0V)	$C_{\overline{E}}$		7	pF
Output capacitance (V_{OUT} = 0V)	C_{OUT}		8	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Max	Unit
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	−10	10	μA
Output leakage current	$\overline{E} = V_{IH}$, V_{OUT} = 0V to V_{CC}	I_{LO}	−50	50	μA
Active supply current	$\overline{E} = V_{IL}$, I_{OUT} = 0 mA $V_{IN} = V_{IL}$ or V_{IH}	I_{CC1}		60	mA
Operating supply current	$\overline{E} = V_{IL}$, I_{OUT} = 0 mA Cycle = min, C_L = 0 pF	I_{CC2}		70	mA
Standby supply current	$\overline{E} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	I_{SB1}		25	mA
Standby supply current	$\overline{E} = V_{IH}$	I_{SB2}		35	mA
Output low voltage	I_{OL} = 8 mA	V_{OL}		0.4	V
Output high voltage	I_{OH} = −4 mA	V_{OH}	2.4		V

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

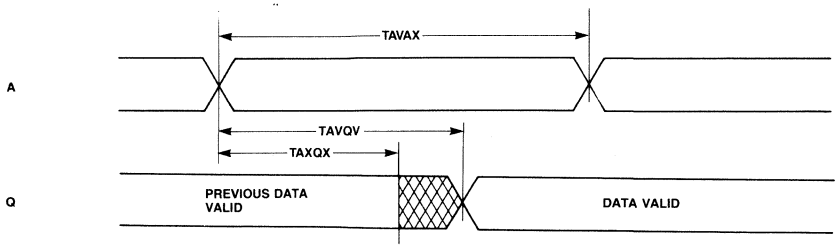
Read Cycle

		MB81C67-45-W		MB81C67-55-W		
Parameter	Symbol	Min	Max	Min	Max	Unit
Read cycle time	TAVAV	45		55		ns
Address access time	TAVQV		45		55	ns
Chip select access time	TELQV		45		55	ns
Output hold from address change	TAXQX	5		5		ns
Chip enable to output active	TELQZ	5		5		ns
Chip enable to output in high-Z	TEHQZ	0	25	0	30	ns

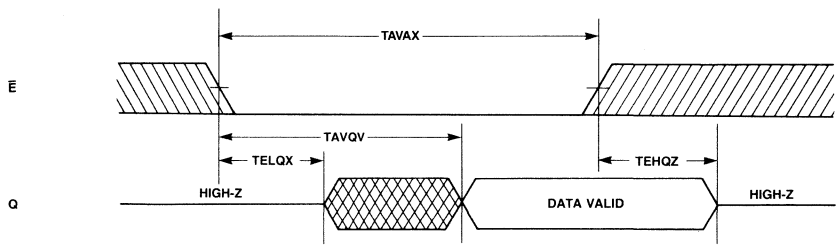
AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Read Cycle Timing Diagram *1

Read Cycle: Address Controlled *2



Read Cycle: $\overline{E}$ Controlled *3



NOTE: *1 $\overline{W}$ IS HIGH FOR READ CYCLE.
*2 DEVICE IS CONTINUOUSLY SELECTED, $\overline{E} = V_{IL}$. $\overline{E}$
*3 ADDRESS VALID PRIOR TO OR COINCIDENT WITH TRANSITION LOW

DON'T CARE
UNDEFINED

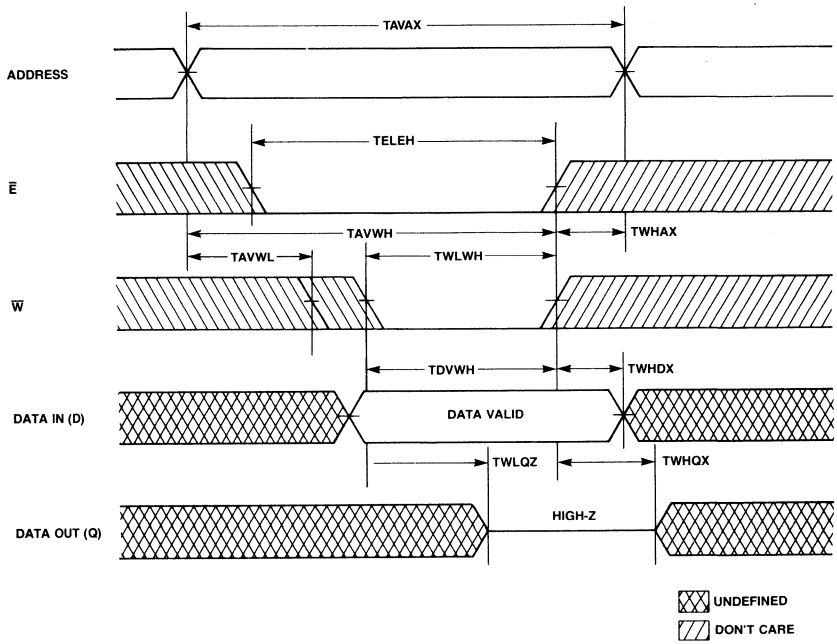
Write Cycle

Parameter	Symbol	MB81C67-45-W Min	MB81C67-45-W Max	MB81C67-55-W Min	MB81C67-55-W Max	Unit
Write cycle time	TAVAX	45		55		ns
Chip enable to end of write	TEIEH	35		45		ns
Address valid to end of write	TAVWH	35		45		ns
Address setup time	TAVWL	5		5		ns
Write pulse width	TWLWH	25		30		ns
Data valid to end of write	TOVWH	20		25		ns
Write recovery time	TWHAX	5		5		ns
Data hold time	TWHDX	0		5		ns
Write enable to output in high-Z	TWHQZ	0	25	0	30	ns
Output active from end of write	TWHQX	0	25	0	30	ns

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle Timing Diagram

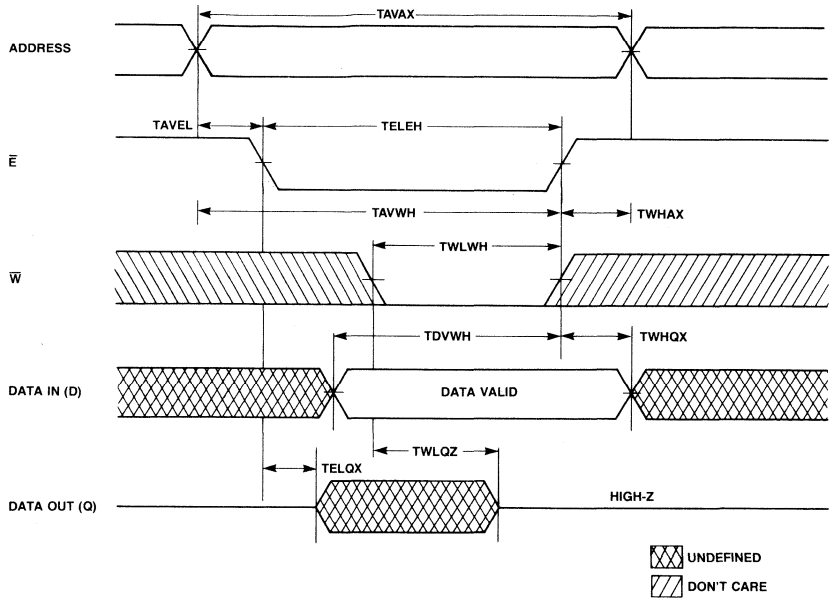
Write Cycle: $\overline{W}$ Controlled



AC Characteristics

(Continued)
(Recommended operating conditions unless otherwise noted.)

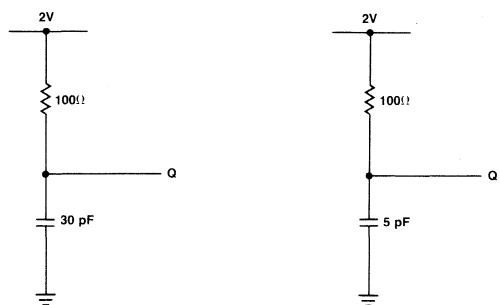
Write Cycle: $\overline{E}$ Controlled



AC Test Conditions

Input Pulse Levels:	0V to 3.0V
Input Pulse Rise and Fall Times:	5 ns
Timing Measurement Reference Levels:	Input: 1.5V
	Output: 0.8/2.2

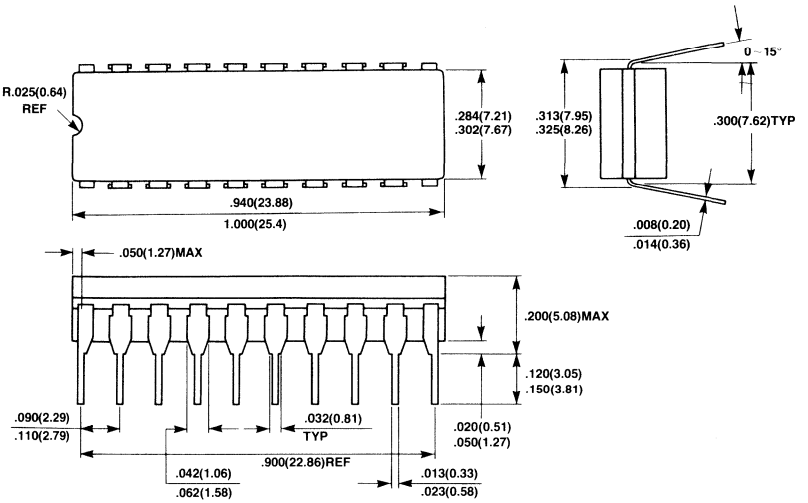
Output load:



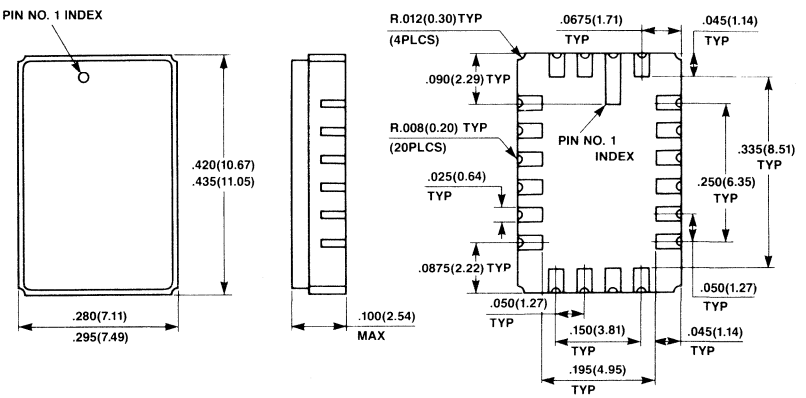
(FOR TEHQZ, TWLQZ, TELQZ, AND TWHQZ

Package Dimensions
Dimensions in inches
(millimeters)

20-Lead Ceramic (CERDIP) Dual In-Line Packages
(Case No.: DIP-20C-C03)

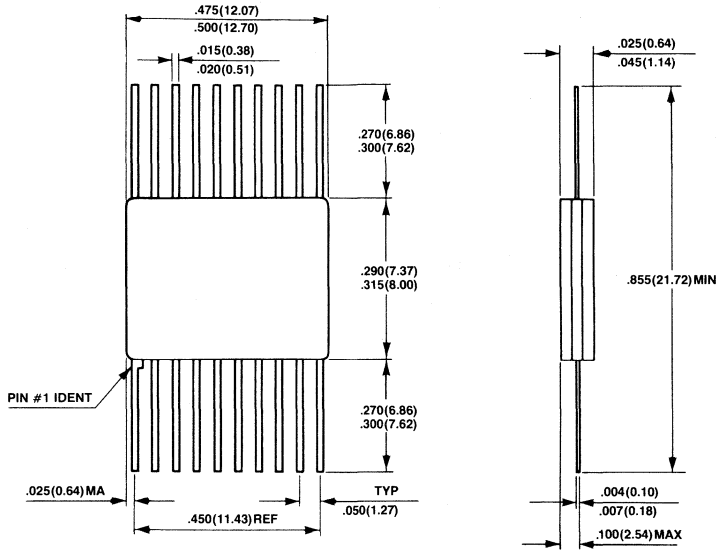


20-Pad Ceramic (Frit Seal) Leadless Chip Carrier
(Case No.: LCC-20C-F01)



Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

20-Lead Ceramic (Cerdip) Flat Package
(Case No.: FPT-20C-C02)



MB81C68-35, MB81C68-45

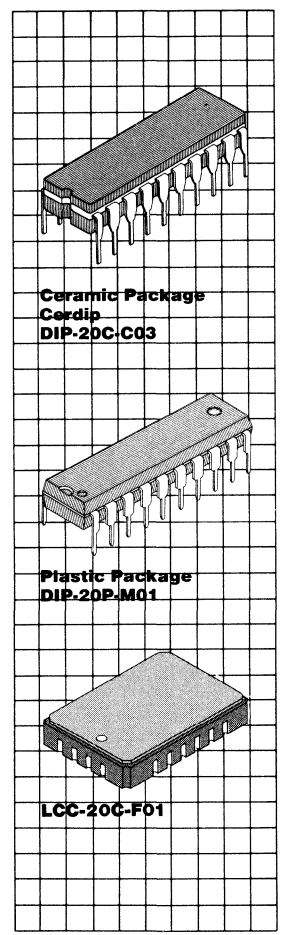
16,384-Bit Static Random Access Memory with Automatic Power Down

Description

The Fujitsu MB81C68 is a 4,096 word x 4-bit static random access memory fabricated using C-MOS silicon gate technology. This device is fully static and requires no clock or timing strobe. All pins are TTL compatible, and a single +5 volt power supply required.

A separate chip enable ($\overline{E}$) pin simplifies multipackage system design. It permits the selection of an individual package when outputs are OR-tied. Furthermore, when selecting a single package by $\overline{E}$, the other deselected devices automatically power down.

The MB81C68 offers the advantages of low power dissipation, low cost, and high performance.

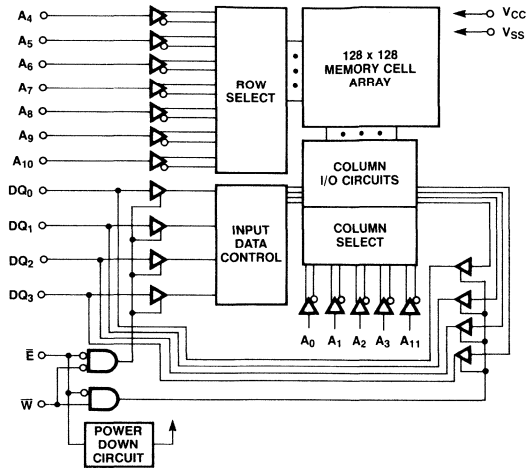


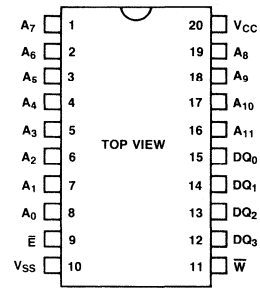
Features

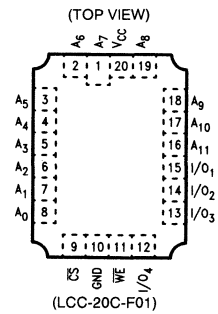
- **Organization: 4,096 words x 4-bits**
- **Static operation: no clocks or timing strobe required**
- **Fast access time: TAVQV = TELQV = 35 ns max. (MB81C68-35) TAVQV = TELQV = 45 ns max. (MB81C68-45)**
- **Single +5V supply ±10% tolerance**
- **TTL compatible inputs and outputs**
- **Low power consumption: 385 mw max. (operating) 138 mw max. (standby)**
- **Three-state outputs with OR-tie capability**
- **Chip enable for simplified memory expansion, automatic power down**
- **All inputs and outputs have protection against static charge**
- **Standard 20-pin DIP package**
- **Pin compatible with Fujitsu MB8168**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB81C68 Block Diagram and Pin Assignments







(LCC-20C-F01)

TRUTH TABLE

Ē	W̄	MODE	DQ	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	D_{IN}	ACTIVE
L	H	READ	OUT	ACTIVE

Absolute Maximum Ratings

(See Note)

Rating	Symbol		Value	Unit
Supply voltage	V_{CC}		−0.5 to +7	V
Input voltage on any pin with respect to V_{SS}	V_{IN}		−3.5 to +7	V
Output voltage on any DQ pin with respect to V_{SS}	V_{OUT}		−0.5 to +7	V
Output current	I_{OUT}		±20	mA
Power dissipation	P_D		1.0	W
Temperature under bias	T_{BIAS}		−10 to +85	°C
Storage temperature	T_{STG}	Ceramic	−65 to +150	°C
		Plastic	−45 to +125	

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low voltage	V_{IL}	−0.5*		0.8	V
Input high voltage	V_{IH}	2.2		6.0	V
Ambient temperature	T_A	0		70	°C

Note: *−2.0V min for pulse width less than 20 ns.

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input capacitance (V_{IN} = 0V)*	C_{IN}		7	pF
DQ capacitance ($V_{I/O}$ = 0V)*	$C_{I/O}$		7	pF

Note: *This parameter is sampled and not 100% tested.

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	−10		10	μA
Output leakage current	$\overline{E} = V_{IH}$, $V_{I/O}$ = 0V to V_{CC}	I_{LO}	−10		10	μA
Active (DC) supply current	I_{OUT} = 0 mA	I_{CC1}			50	mA
Operating supply current	I_{OUT} = 0 mA, cycle = min	I_{CC2}			70	mA
Standby supply current	$\overline{E} = V_{CC}$ $V_{IN} = V_{SS}$ or V_{CC}	I_{SB1}			15	mA
Standby supply current	$\overline{E} = V_{IH}$	I_{SB2}			25	mA
Output low voltage	I_{OL} = 8 mA	V_{OL}			0.4	V
Output high voltage	I_{OH} = −4 mA	V_{OH}	2.4			V

AC Characteristics

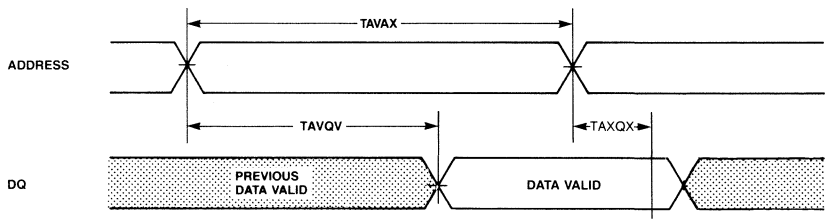
(Recommended operating conditions unless otherwise noted.)

Read Cycle

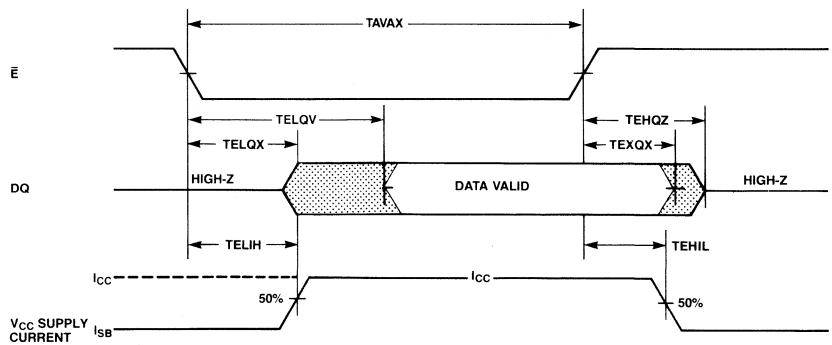
Parameter	Symbol	MB81C68-35 Min	MB81C68-35 Max	MB81C68-45 Min	MB81C68-45 Max	Unit
Read cycle time	TAVAX	35		45		ns
Address access time	TAVQV		35		45	ns
Chip enable access time	TELQV		35		45	ns
Output hold from address change	TAXQX	5		5		ns
Output hold from $\overline{E}$	TEXQX	0		0		ns
Power up from $\overline{E}$	TELIH	0		0		ns
Chip enable to output in low-Z	TELQX	5		5		ns
Chip deselection to output in high-Z	TEHQZ	0	15	0	20	ns
Power down from $\overline{E}$	TEHIL		30		40	ns

Read Cycle Timing Diagrams*1

Read Cycle: Address Controlled*2



Read Cycle: $\overline{E}$ Controlled*3



NOTES: *1 $\overline{W}$ IS HIGH FOR READ CYCLE.
*2 DEVICE IS CONTINUOUSLY SELECTED, $\overline{E} = V_{IL}$.
*3 ADDRESS VALID PRIOR TO OR COINCIDENT WITH $\overline{E}$ TRANSITION LOW.

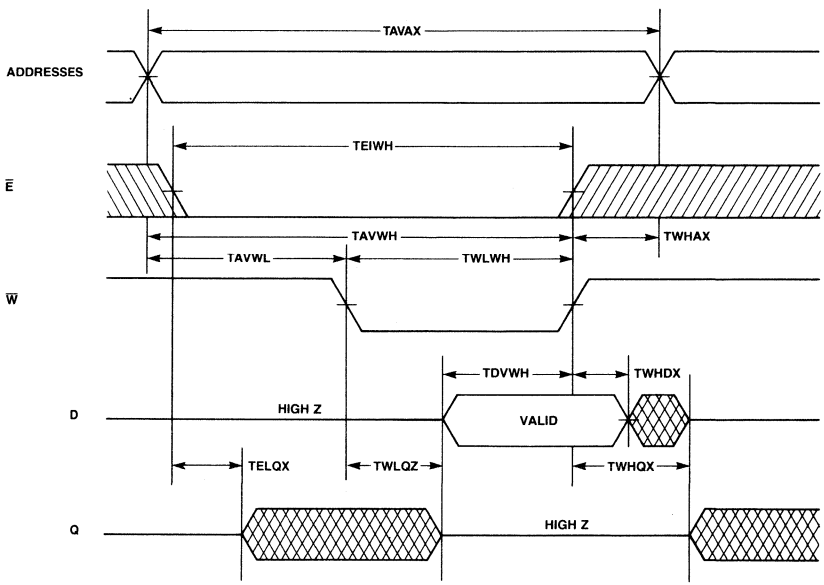
AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle

Parameter	Symbol	MB81C68-35 Min	MB81C68-35 Max	MB81C68-45 Min	MB81C68-45 Max	Unit
Write cycle time	TAVAX	35		45		ns
Chip enable to end of write	TEIWH	30		35		ns
Address valid to end of write	TAVWH	30		35		ns
Address setup time	TAVWL, TAVEL	0		0		ns
Write pulse width	TWLWH	30		35		ns
Data setup time	TDVWH	20		20		ns
Write recovery time	TWHAX, TEHAX	0		0		ns
Data hold time	TWHDX	0		0		ns
Output high-Z from $\overline{W}$	TWLQZ		15		15	ns
Output low-Z from $\overline{W}$	TWHQX	5		5		ns

Write Cycle Timing Diagram

Write Cycle: $\overline{W}$ Controlled[*1 *2]



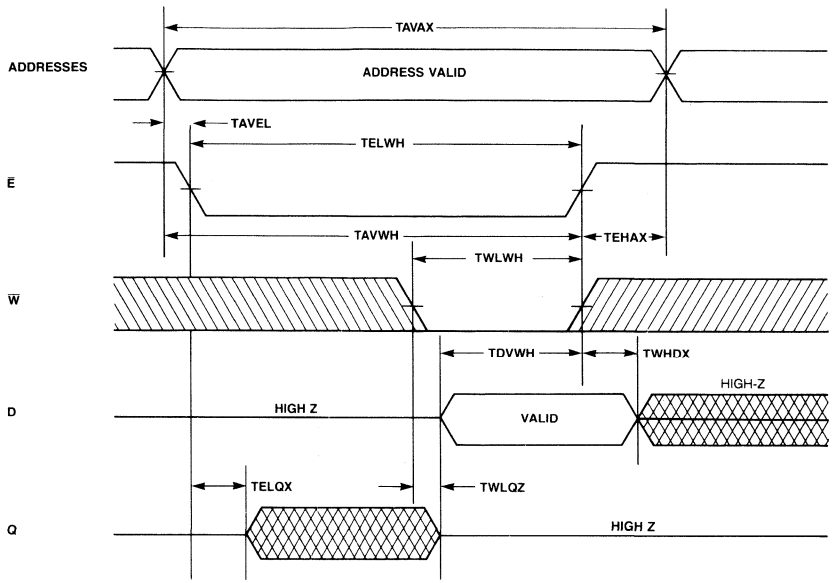
NOTES: *1 IF $\overline{E}$ GOES HIGH SIMULTANEOUSLY WITH $\overline{W}$ HIGH, THE OUTPUT REMAINS IN A HIGH IMPEDANCE STATE.
*2 $\overline{E}$ OR $\overline{W}$ MUST BE HIGH DURING ADDRESS TRANSITIONS.

UNDEFINED
DON'T CARE

AC Characteristics
(continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle Timing Diagram

Write Cycle: $\overline{E}$ Controlled[*1,*2]



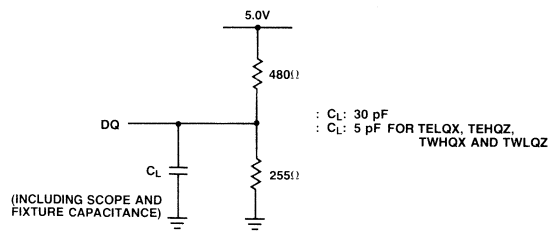
NOTES: *1 IF $\overline{E}$ GOES HIGH SIMULTANEOUSLY WITH $\overline{W}$ HIGH, THE OUTPUT REMAINS IN A HIGH IMPEDANCE STATE.
*2 $\overline{E}$ OR $\overline{W}$ MUST BE HIGH DURING ADDRESS TRANSITIONS.

UNDEFINED
DON'T CARE

AC Test Conditions

Input pulse levels:	0V to 3.0V
Input pulse rise and fall times:	5 ns (Transient time between 0.8V and 2.2V)
Timing measurement reference levels:	Input: 1.5V
	Output: 1.5V

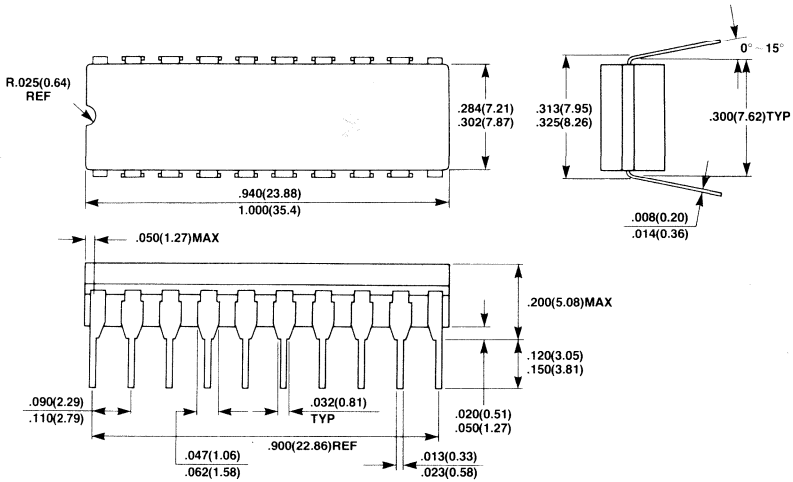
Output Load:



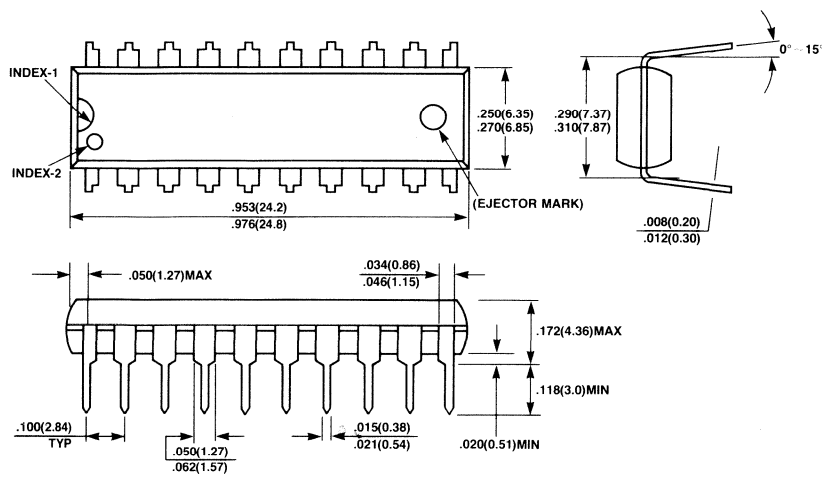
Package Dimensions

Dimensions in inches
(millimeters)

20-Lead Ceramic (Cerdip) Dual In-Line Package (Case No.: DIP-20C-C03)

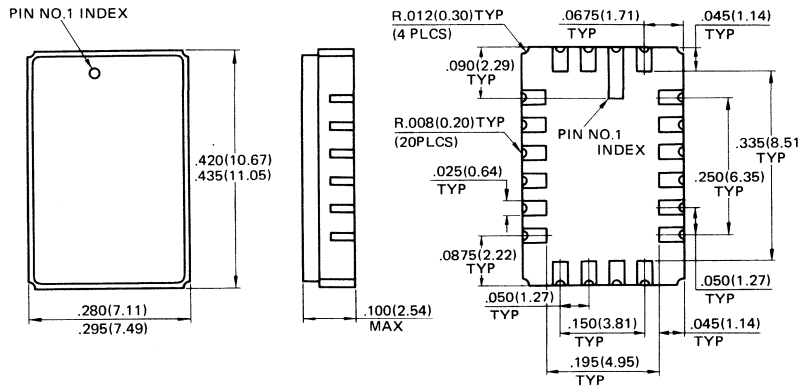


20-Lead Plastic Dual In-Line Package (Case No.: DIP-20P-M01)



Package Dimensions
(continued)
Dimensions in inches
(millimeters)

20-Pad Ceramic (Frit Seal) Leadless Chip Carrier
(Case No.: LCC-20C-F01)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

Preliminary

FUJITSU

■ MB81C68A-25, MB81C68A-30, MB81C68A-35

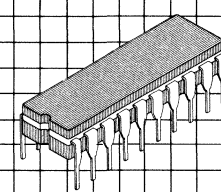
4K x 4(16,384) Bit Super High Speed Random Access Memory with Automatic Power Down

Description

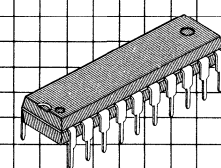
The Fujitsu MB81C68A is a 4,096 word x 4-bit static random access memory fabricated using CMOS silicon gate process. This device is fully static and required no clock or timing strobes. All pins are TTL compatible, and a single +5V volt power supply is required.

A separate chip enable ($\overline{E}$) pin simplifies multipackage systems design. It permits the selection of an individual package when outputs are OR-tied. Furthermore, when selecting a single package by $\overline{E}$, the other deselected packages automatically power down.

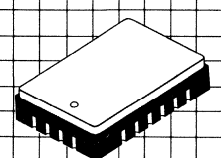
All Fujitsu devices offer the advantages of low power dissipation, low cost, and high performance.



CERDIP package
DIP-20C-C03



Plastic Package
DIP-20P-M01



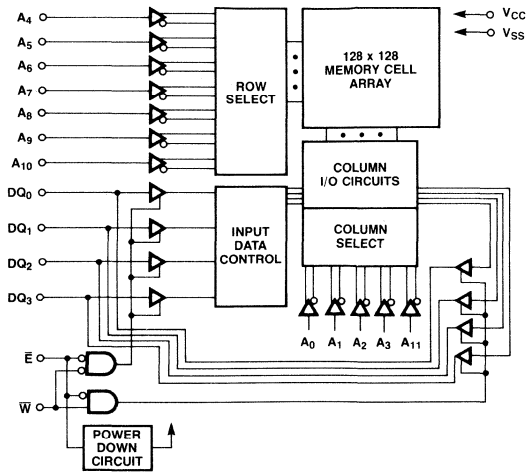
LCC-20C-F01

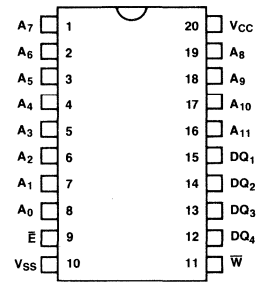
Features

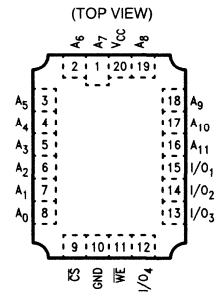
- **Organization: 4K words x 4-bits**
- **Static operation: no clocks or timing strobe required**
- **Fast access time: TAVAV = TAVQV = 25 ns max. (MB81C68A-25) TAVAV = TAVQV = 30 ns max. (MB81C68A-30) TAVAV = TAVQV = 35 ns max. (MB81C68A-35)**
- **Low power consumption 70 mA max. (active) 25 mA max. (standby, TTL input levels) 15 mA max. (standby, CMOS input levels)**
- **Single +5V supply ±10%**
- **TTL compatible inputs and outputs**
- **Standard 20 pin DIP**
- **Automatic power down mode**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB81C68A Block Diagram and Pin Assignments







(LCC-20C-F01)

TRUTH TABLE

$\overline{E}$	$\overline{W}$	MODE	D/Q	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	IN	ACTIVE
L	H	READ	OUT	ACTIVE

Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Supply voltage		V_{CC}	−0.5 to +7	V
Input voltage on any pin with respect to GND		V_{IN}	−3.5 to +7	V
Output voltage on any I/O pin with respect to GND		V_{OUT}	−0.5 to +7	V
Output current		I_{OUT}	±20	mA
Power dissipation		P_D	1.0	W
Temperature under bias		T_{BIAS}	−10 to +85	°C
Storage temperature	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−45 to +125	

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low voltage	V_{IL}	−0.5*		0.8	V
Input high voltage	V_{IH}	2.2		6.0	V
Ambient temperature	T_A	0		70	°C

Note: * −2.0V min. for pulse width less than 20 ns.

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input capacitance (V_{IN} = 0V)	C_{IN}		5	pF
D/Q capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$		7	pF
$\overline{CS}$ capacitance ($V_{\overline{CS}}$ = 0V)	$C_{\overline{CS}}$		6	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	−10		10	μA
Output leakage current	$\overline{E}$ = V_{IH}, V_{IO} = 0V to V_{CC}	I_{LO}	−10		10	μA
Active (DC) supply current	I_{OUT} = 0 mA, $\overline{CS}$ = V_{IL}, V_{IN} = V_{IL} or V_{IH}	I_{CC1}		25	50	mA
Operating supply current	I_{OUT} = 0 mA, cycle = min, $\overline{CS}$ = V_{IL}	I_{CC2}		40	70	mA
Standby supply current	$\overline{E}$ = V_{CC} −0.2V, V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} −0.2V	I_{SB1}		0.5	15	mA
Standby supply current	$\overline{E}$ = V_{IH}	I_{SB2}		10	25	mA
Output low voltage	I_{OL} = 8 mA	V_{OL}			0.4	V
Output high voltage	I_{OH} = −4 mA	V_{OH}	2.4			V

AC Characteristics

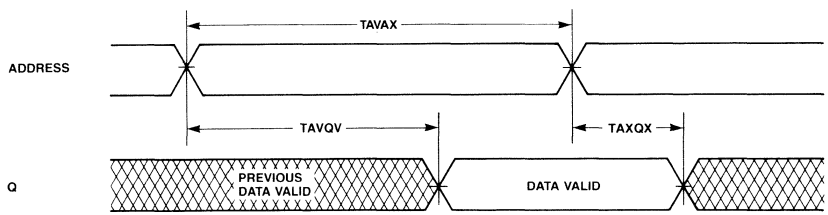
(Recommended operating conditions unless otherwise noted.)

Read Cycle

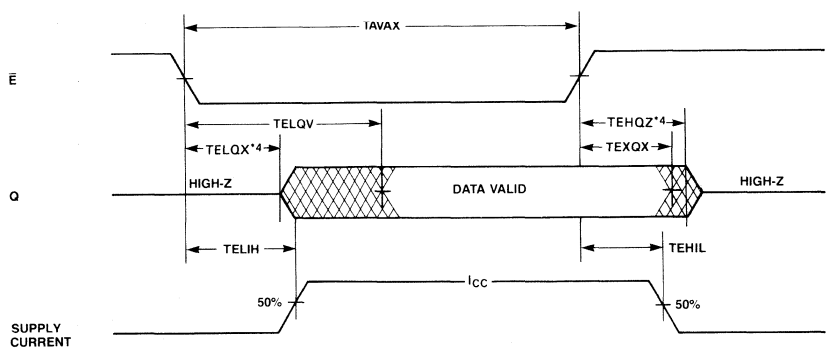
Parameter	Symbol	MB81C68A-25 Min	MB81C68A-25 Max	MB81C68A-30 Min	MB81C68A-30 Max	MB81C68A-35 Min	MB81C68A-35 Max	Unit
Read cycle time	TAVAX	25		30		35		ns
Address access time	TAVQV		25		30		35	ns
Chip select access time	TELQV		25		30		35	ns
Output hold from address change	TAXQX	3		3		3		ns
Output hold from $\overline{E}$	TEXQX	0		0		0		ns
Chip enable to output in Low-Z	TELQX	5		5		5		ns
Chip deselection to output in High-Z	TEHQZ		10		13		15	ns
Power up from $\overline{E}$	TELIH	0		0		0		ns
Power down from $\overline{E}$	TEHIL		20		25		30	ns

Read Cycle Timing Diagram*1

Read Cycle: Address Controlled*2



Read Cycle: $\overline{E}$ Controlled*3



NOTES: *1 $\overline{W}$ IS HIGH FOR READ CYCLE.
*2 DEVICE IS CONTINUOUSLY SELECTED, $\overline{E} = V_{IL}$.
*3 ADDRESS VALID PRIOR TO OR COINCIDENT WITH $\overline{E}$ TRANSITION LOW.
*4 TRANSITION IS MEASURED AT THE POINT OF ±0.5 V FROM STEADY-STATE VOLTAGE.

UNDEFINED
DON'T CARE

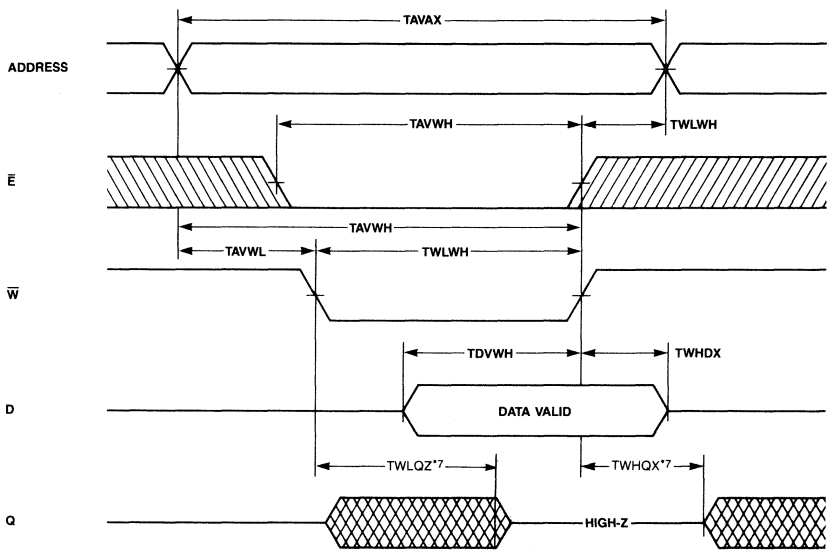
AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle

Parameter	Symbol	MB81C68A-25 Min	MB81C68A-25 Max	MB81C68A-30 Min	MB81C68A-30 Max	MB81C68A-35 Min	MB81C68A-35 Max	Unit
Write cycle time	TAVAX	25		30		35		ns
Chip enable to end of write	TEIWH	20		25		30		ns
Address valid to end of write	TAVWH	20		25		30		ns
Address setup time	TAVWL TAVEL	0		0		0		ns
Write pulse width	TWLWH	20		25		30		ns
Data setup time	TDVWH	13		15		15		ns
Write recovery time	TWHAX TEHAX	2		2		2		ns
Data hold time	TWHDX	0		0		0		ns
Output High-Z from $\overline{W}$	TWLQZ		10		13		15	ns
Output Low-Z from $\overline{W}$	TWHQX	5		5		5		ns

Write Cycle Timing Diagrams

Write Cycle: $\overline{W}$ Controlled*5,6



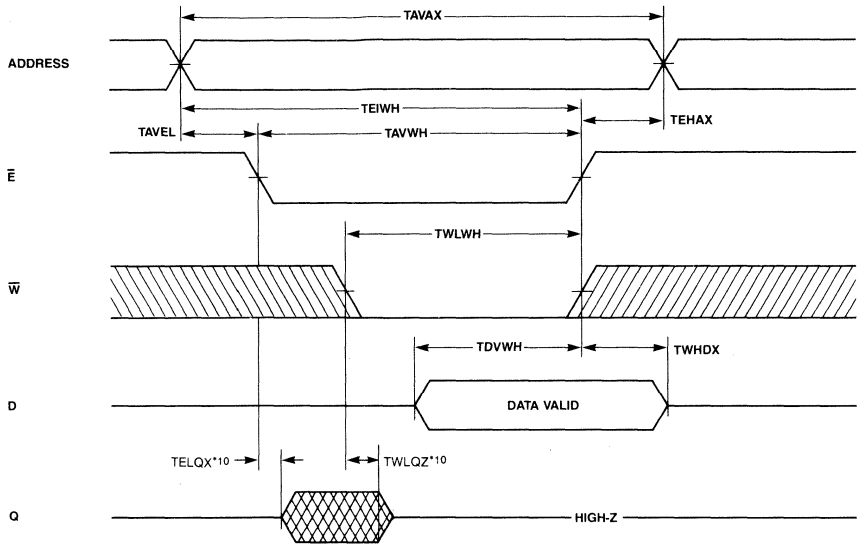
NOTE: *5 IF $\overline{E}$ GOES HIGH SIMULTANEOUSLY WITH $\overline{W}$ HIGH, THE OUTPUT REMAINS IN A HIGH IMPEDANCE STATE.
*6 $\overline{E}$ OR $\overline{W}$ MUST BE HIGH DURING ADDRESS TRANSITIONS.
*7 TRANSITION IS MEASURED AT THE POINT OF ±0.5 V FROM STEADY STATE VOLTAGE.

DON'T CARE
UNDEFINED

AC Characteristics

(Continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle: $\overline{E}$ Controlled*8,9

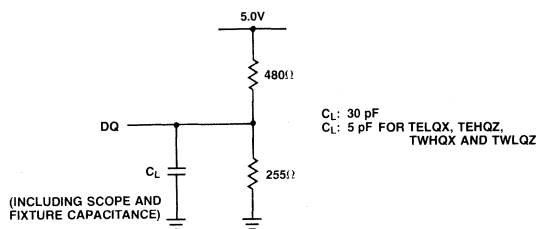


NOTE: *8 IF $\overline{E}$ GOES HIGH SIMULTANEOUSLY WITH $\overline{W}$ HIGH, THE OUTPUT REMAINS IN A HIGH IMPEDANCE STATE.
*9 $\overline{E}$ OR $\overline{W}$ MUST BE HIGH DURING ADDRESS TRANSITIONS.
*10 TRANSITION IS MEASURED AT THE POINT OF ±0.5 V FROM STEADY STATE VOLTAGE.

DON'T CARE
UNDEFINED

AC Test Condition

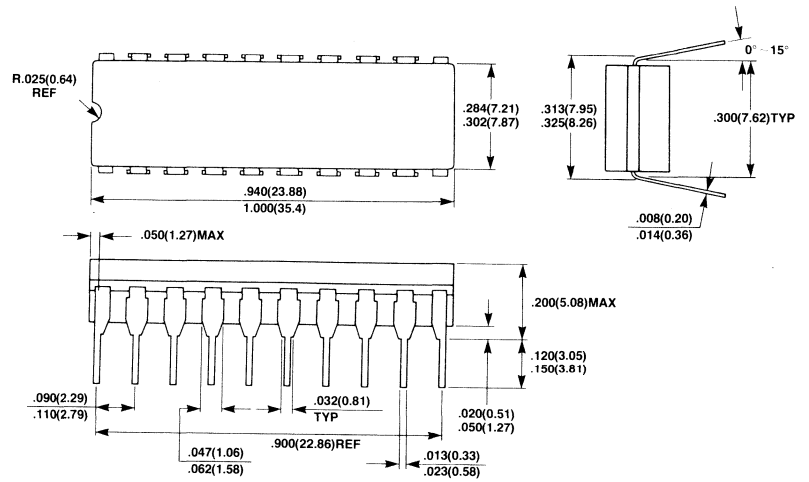
Input Pulse Levels:	0V to 3.0V
Input Pulse Rise and Fall Times:	5 ns (Transient Time between 0.8V and 2.2V)
Timing Reference Levels:	Input: 1.5V
Output Load:	Output: 1.5V



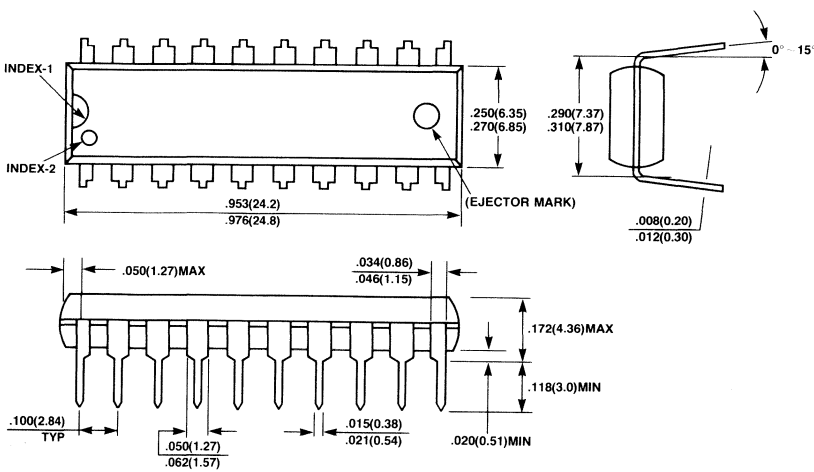
Package Dimensions

Dimensions in inches
(millimeters)

20-Lead Ceramic (Cerdip) Dual In-Line Package (Case No.: DIP-20C-C03)



20-Lead Plastic Dual In-Line Package (Case No.: DIP-20P-M01)



MB81C68-45-W, MB81C68-55-W

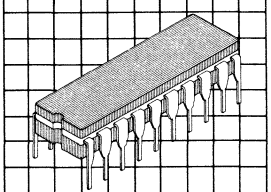
CMOS 16,384-Bit Static Random Access Memory With Automatic Power Down

Description

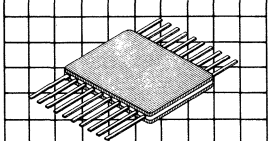
The Fujitsu MB81C68 is a 4,096 word x 4-bit static random access memory fabricated using CMOS silicon gate process. This device is fully static and requires no clock or timing strobe. All pins are TTL compatible, and a single +5 volt power supply is required.

A separate chip enable (E) pin simplifies multipackage systems design. It permits the selection of an individual package when outputs are OR-tied. Furthermore when selecting a single package by E, the other deselected devices automatically power down.

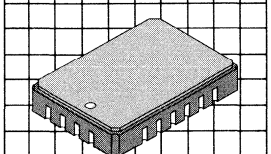
The MB81C68W offers the advantages of low power dissipation, and high performance.



Ceramic Package
CERDIP
(DIP-20C-C03)



FPT-20C-C02



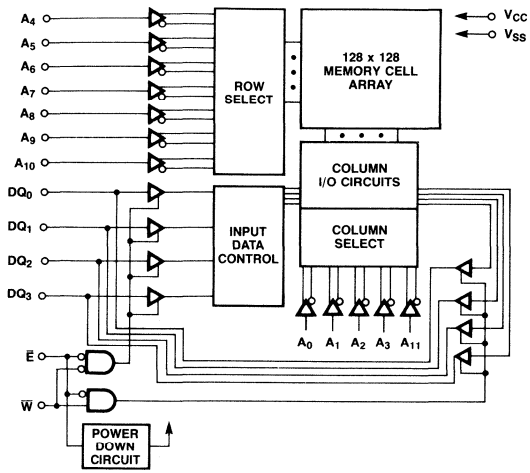
LCC-20C-A01

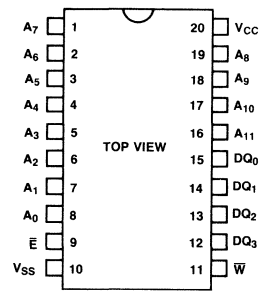
Features

- **Organization: 4096 words x 4-bits**
- **Static operation: no clocks or timing strobe required**
- **Fast access time: TAVQV = TELQV = 45 ns max. (MB81C68-45-W) TAVQV = TELQV = 55 ns max. (MB81C68-55-W)**
- **Low power consumption: 385 mW max. (Operating) 138 mW max. (Standby)**
- **Single +5V supply, ±10% tolerance**
- **TTL compatible inputs and outputs**
- **Three-state outputs with OR-tie capability**
- **Chip enable for simplified memory expansion, automatic power down**
- **All inputs and outputs have protection against static charge**
- **Standard 20-pin DIP package**
- **Pin compatible with Fujitsu MB8168**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB81C68W Block Diagram and Pin Assignment





TRUTH TABLE

$\overline{E}$	$\overline{W}$	MODE	DQ	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	IN	ACTIVE
L	H	READ	OUT	ACTIVE

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	−0.5 to +7	V
Input voltage on any pin with respect to V_{SS}	V_{IN}	−3.5 to +7	V
Output voltage on any DQ pin with respect to V_{SS}	V_{OUT}	−0.5 to +7	V
Output current	I_{OUT}	±20	mA
Power dissipation	P_D	1.0	W
Temperature under bias	T_{BIAS}	−55 to +125	°C
Storage temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low voltage	V_{IL}	−0.5*1		0.7	V
Input high voltage	V_{IH}	2.3		6.0	V
Ambient temperature	T_A	−55		125	°C

Note: *1 −1.0V min. for pulse width less than 20 ns.

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input capacitance (V_{IN} = 0V)	C_{IN}		7	pF
I/O capacitance ($V_{I/0}$ = 0V)	$C_{I/O}$		7	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Max	Unit
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	−10	10	μA
Output leakage current	$\overline{E} = V_{IH}$, $V_{I/O}$ = 0V to V_{CC}	I_{LO}	−10	10	μA
Active (DC) supply current	I_{OUT} = 0 mA	I_{CC1}		50	mA
Operating supply current	I_{OUT} = 0 mA, Cycle = min	I_{CC2}		70	mA
Standby supply current	$\overline{E} = V_{CC}$ $V_{IN} = V_{SS}$ or V_{CC}	I_{SB1}		15	mA
Standby supply current	$\overline{E} = V_{IH}$	I_{SB2}		25	mA
Output low voltage	I_{OL} = 8 mA	V_{OL}		0.4	V
Output high voltage	I_{OH} = −4 mA	V_{OH}	2.4		V

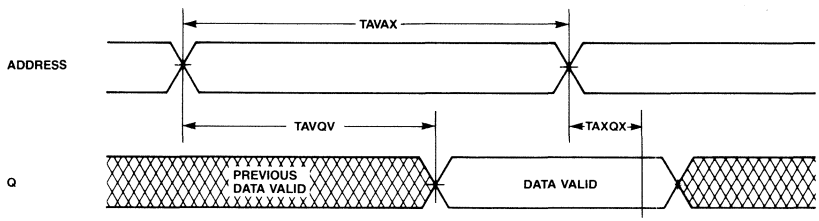
AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Read Cycle

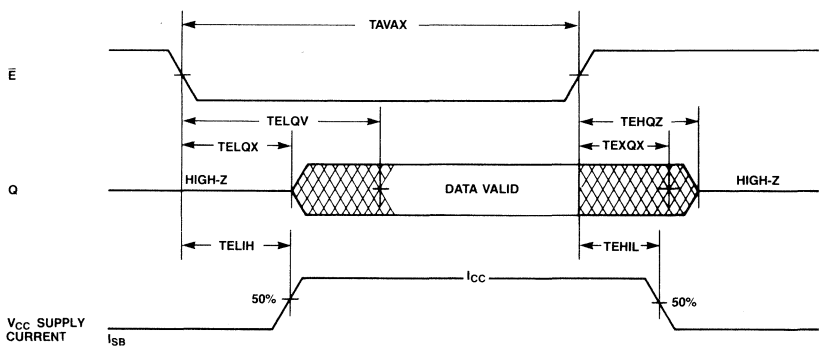
Parameter	Symbol	MB81C68-45-W Min	MB81C68-45-W Max	MB81C68-55-W Min	MB81C68-55-W Max	Unit
Read cycle time	TAVAX	45		55		ns
Address access time	TAVQV		45		55	ns
Chip enable access time	TELQV		45		55	ns
Output hold from address change	TAXQX	3		3		ns
Output hold from $\overline{E}$	TEXQX	0		0		ns
Power up from $\overline{E}$	TELIH	0		0		ns
Chip enable to output in low-Z	TELQX	5		5		ns
Chip deselection to output in high-Z	TEHQZ	0	17	0	20	ns
Power down from $\overline{E}$	TEHIL		40		50	ns

Read Cycle Timing Diagram[*1]

Read Cycle: Address Controlled[*2]



Read Cycle: $\overline{E}$ Controlled[*3]



NOTES: *1 $\overline{W}$ IS HIGH FOR READ CYCLE.
*2 DEVICE IS CONTINUOUSLY SELECTED, $\overline{E} = V_{IL}$.
*3 ADDRESS VALID PRIOR TO OR COINCIDENT WITH $\overline{E}$ TRANSITION LOW.

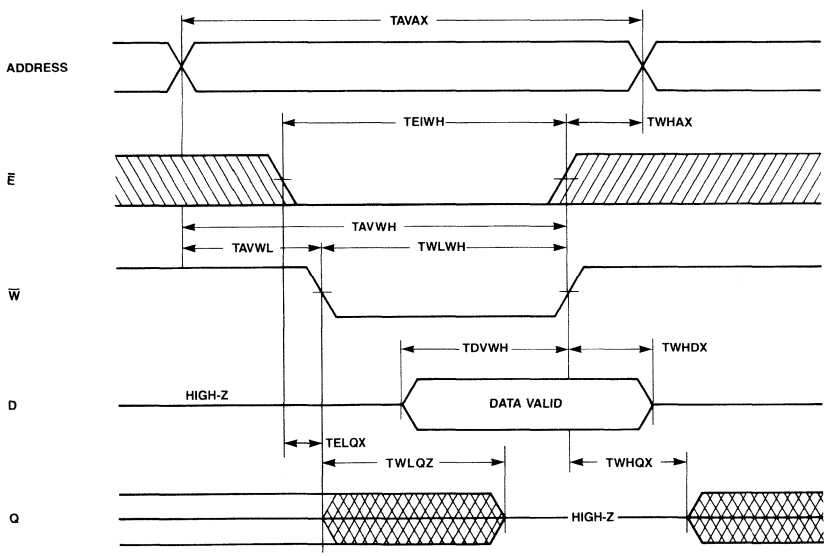
DON'T CARE
UNDEFINED

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle

Parameter	Symbol	MB81C68-45-W Min	MB81C68-45-W Max	MB81C68-55-W Min	MB81C68-55-W Max	Unit
Write cycle time	TAVAX	45		55		ns
Chip selection to end of write	TEIWH	40		45		ns
Address valid to end of write	TAVWH	40		45		ns
Address setup time	TAVWL, TAVEL	0		0		ns
Write pulse width	TWLWH	40		45		ns
Data setup time	TDVWH	23		25		ns
Write recovery time	TWHAX, TEHAX	5		5		ns
Data hold time	TWHDX	3		3		ns
Output high-Z from $\overline{W}$	TWLQZ		17		20	ns
Output low-Z from $\overline{W}$	TWHQX	5		5		ns

Write Cycle: $\overline{W}$ Controlled*4,5



NOTES: *4) IF $\overline{E}$ GOES HIGH SIMULTANEOUSLY WITH $\overline{W}$ HIGH, THE OUTPUT REMAINS IN A HIGH IMPEDANCE STATE.
*5) $\overline{E}$ OR $\overline{W}$ MUST BE HIGH DURING ADDRESS TRANSITIONS.

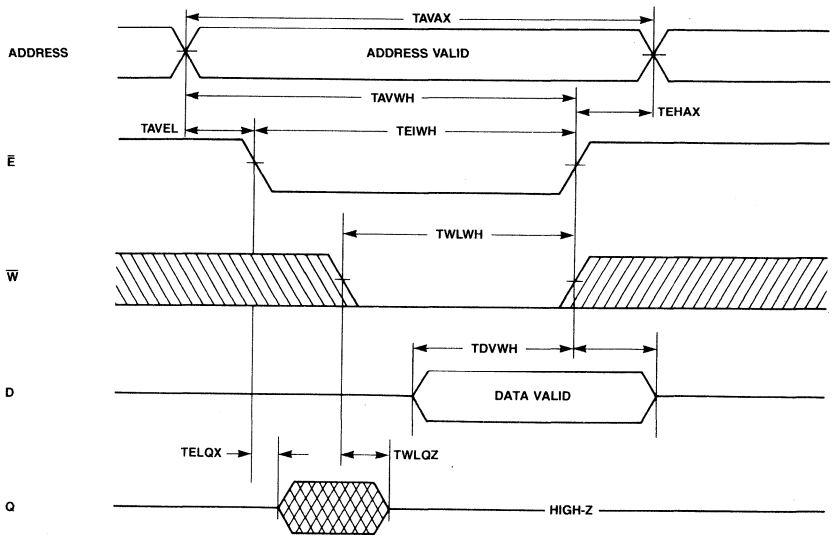
DON'T CARE
UNDEFINED

AC Characteristics

(Continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle Timing Diagram

Write Cycle: $\overline{E}$ Controlled *6,7

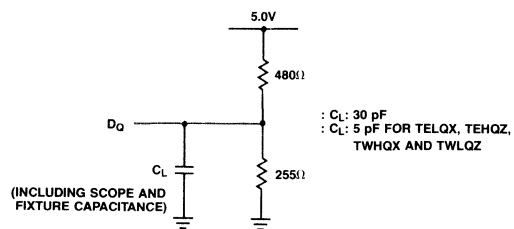


NOTES: *6) IF $\overline{E}$ GOES HIGH SIMULTANEOUSLY WITH $\overline{W}$ HIGH, THE OUTPUT REMAINS IN A HIGH IMPEDANCE STATE.
*7) $\overline{E}$ OR $\overline{W}$ MUST BE HIGH DURING ADDRESS TRANSITIONS.

AC Test Conditions

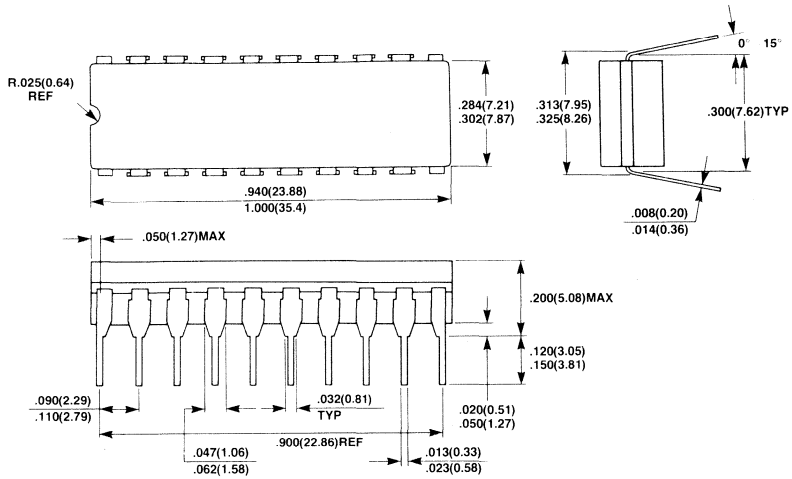
Input Pulse Levels:	0V to 3.0V
Input Pulse Rise and Fall Times:	5 ns (Transient Time between 0.8V and 2.2V)
Timing Reference Levels:	Input: 1.5V
	Output: 1.5V

Output Load:

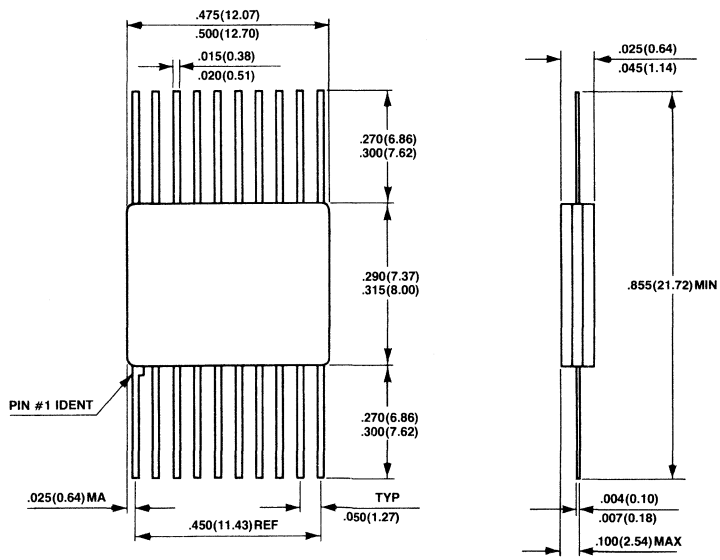


Package Dimensions
Dimensions in inches
(millimeters)

20-Lead Ceramic (CERDIP) Dual In-Line Package
(Case No.: DIP-20C-C03)

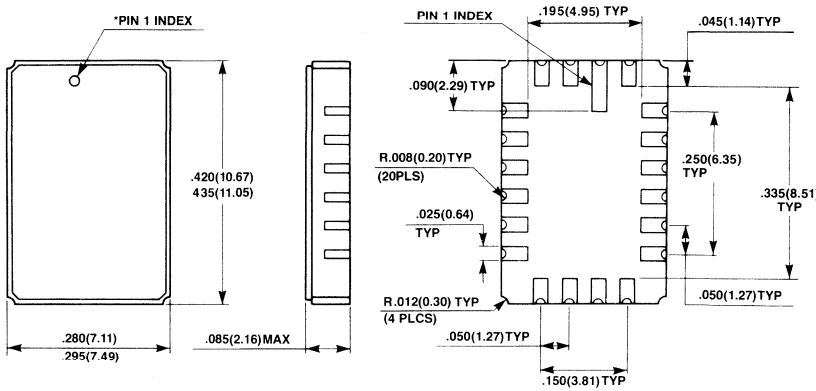


20-Lead Ceramic (Cerdip) Flat Package
(Case No.: FPT-20C-C02)



Package Dimensions
(continued)
Dimensions in inches
(millimeters)

20-Pad Ceramic (Metal Seal) Leadless Chip Carrier
(Case No.: LCC-20C-A01)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

Preliminary

MOS Memories

FUJITSU

■ MB81C69A-25, MB81C69A-30, MB81C69A-35

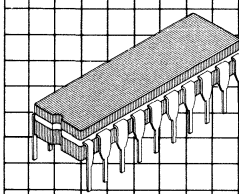
CMOS 16,384-Bit
Static Random Access Memory
with Fast Chip Select Access Time

Description

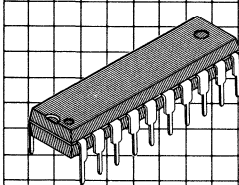
The Fujitsu MB81C69A is a 4,096 word x 4-bit static random access memory fabricated using CMOS silicon gate process. This device is fully static and requires no clock or timing strobe. All pins are TTL compatible, and a single +5 volt power supply is required.

A separate chip enable ($\overline{E}$) pin permits the selection of an individual device when outputs are OR-tied.

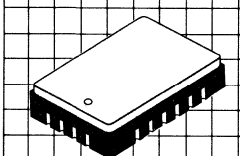
The MB816C69A offers the advantages of low power dissipation, high performance and low cost.



Ceramic Package Cerdip (DIP-20C-C03)



Plastic Package (DIP-20P-M01)



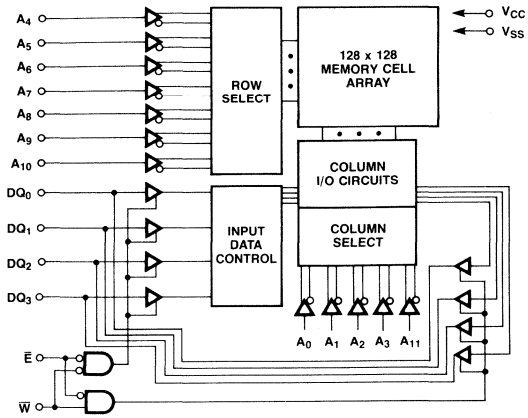
LCC-20C-F01

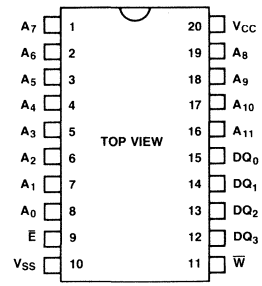
Features

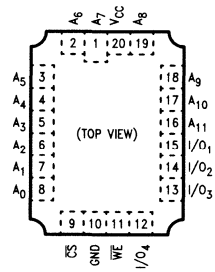
- **Organization: 4,096 words x 4-bits**
- **Static operation: No clocks or timing strobe required**
- **Fast access time: TAVAV = TAVQV = 25 ns max. TELQV = 15 ns max.**
- **Low power consumption: 385 mW max. (Active)**
- **Single +5V supply ±10% tolerance**
- **TTL compatible inputs and outputs**
- **Three-state outputs with OR-tie capability**
- **Chip select for simplified memory expansion**
- **All inputs and outputs have static charge protection**
- **Standard 20-pin DIP**
- **Standard 20-pin LCC**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB81C69A Block Diagram and Pin Assignment







TRUTH TABLE

E	W	MODE	DQ	POWER
H	X	NOT SELECTED	HIGH-Z	ACTIVE
L	L	WRITE	IN	ACTIVE
L	H	READ	OUT	ACTIVE

Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Supply voltage		V_{CC}	−0.5 to +7	V
Input voltage on any pin with respect to GND		V_{IN}	−3.5 to +7	V
Output voltage on any I/O pin with respect to GND		V_{OUT}	−0.5 to +7	V
Output current		I_{OUT}	±20	mA
Power dissipation		P_D	1.0	W
Temperature under bias		T_{BIAS}	−10 to +85	°C
Storage temperature	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−45 to +125	

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low voltage	V_{IL}	−0.5*1		0.8	V
Input high voltage	V_{IH}	2.2		6.0	V
Ambient temperature	T_A	0		70	°C

Note: *1 −2.0V min. for pulse width less than 20 ns.

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input capacitance (V_{IN} = 0V)	C_{IN}		5	pF
Input capacitance ($V_{\overline{ES}}$ = 0V)			6	pF
DQ capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$		7	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Max	Unit
Active supply current	I_{OUT} = 0 mA	I_{CC1}		50	mA
Operating supply current	I_{OUT} = 0 mA, cycle = min.	I_{CC2}		70	mA
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	−10	10	μA
Output leakage current	$\overline{E}$ = V_{IH}, $V_{I/O}$ = 0V to V_{CC}	I_{LO}	−10	10	μA
Output low voltage	I_{OL} = 8 mA	V_{OL}		0.4	V
Output high voltage	I_{OH} = −4 mA	V_{OH}	2.4		V

AC Characteristics

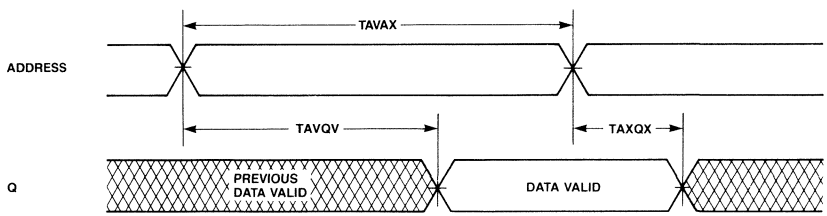
(Recommended operating conditions unless otherwise noted.)

Read Cycle

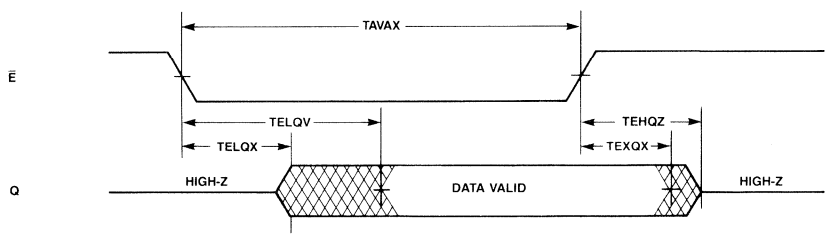
Parameter	Symbol	MB81C69A-25 Min	MB81C69A-25 Max	Unit
Read cycle time	TAVAX	25		ns
Address access time	TAVQV		25	ns
Chip select access time	TELQV		15	ns
Output hold from address change	TAXQX	3		ns
Output hold from $\overline{E}$	TEXQX	0		ns
Chip enable to output in low-Z	TELQX	3		ns
Chip deselection to output in high-Z	TEHQZ		10	ns

Read Cycle Timing Diagram*1

Read Cycle: Address Controlled*2



Read Cycle: $\overline{E}$ Controlled*3



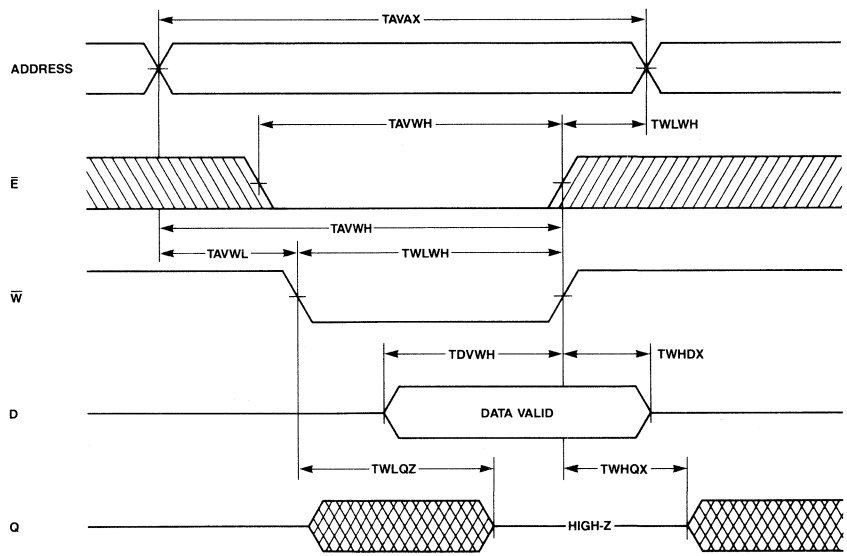
NOTES: *1 $\overline{W}$ IS HIGH FOR READ CYCLE.
*2 DEVICE IS CONTINUOUSLY SELECTED, $\overline{E} = V_{IL}$.
*3 ADDRESS VALID PRIOR TO OR COINCIDENT WITH $\overline{E}$ TRANSITION LOW.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle

Parameter	Symbol	MB81C69A-25 Min	Max	Unit
Write cycle time	TAVAV	25		ns
Chip enable to end of write	TE1WH	20		ns
Address valid to end of write	TAVWH	20		ns
Address setup time	TAVWL TAVEL	0		ns
Write pulse width	TWLWH	20		ns
Data setup time	TDVWH	13		ns
Write recovery time	TWHAX TEHAX	2		ns
Data hold time	TWHDX	0		ns
Output high-Z from $\overline{W}$	TWLQZ		10	ns
Output low-Z from $\overline{W}$	TWHQX	5		ns

Write Cycle: $\overline{W}$ Controlled *4,5

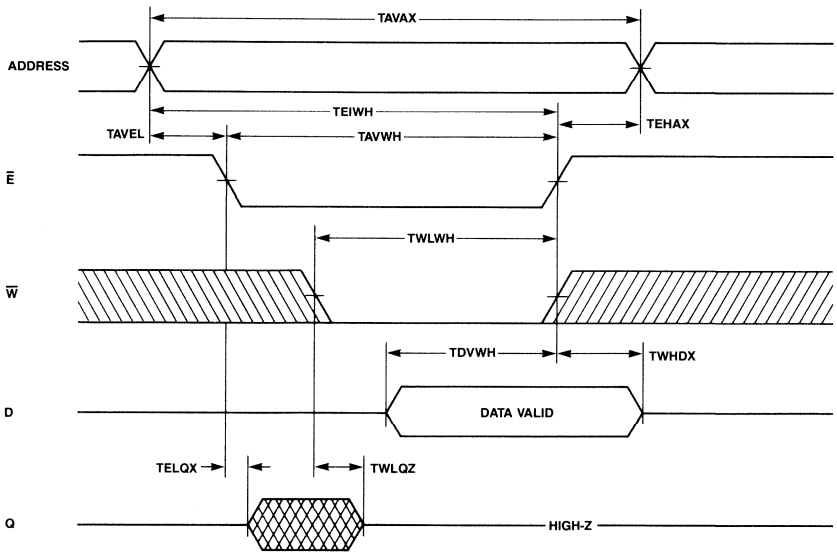


NOTE: *4 IF $\overline{E}$ GOES HIGH SIMULTANEOUSLY WITH $\overline{W}$ HIGH, THE OUTPUT REMAINS IN A HIGH IMPEDANCE STATE.
*5 $\overline{E}$ OR $\overline{W}$ MUST BE HIGH DURING ADDRESS TRANSITIONS.

DON'T CARE
UNDEFINED

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle: $\overline{E}$ Controlled *6,7

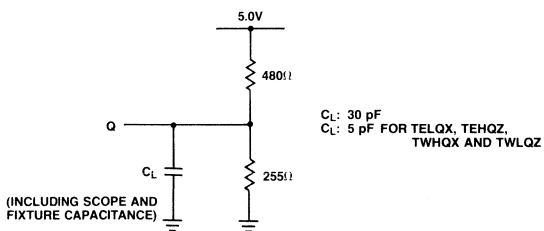


NOTE: *6 IF $\overline{E}$ GOES HIGH SIMULTANEOUSLY WITH $\overline{W}$ HIGH, THE OUTPUT REMAINS IN A HIGH IMPEDANCE STATE.
*7 $\overline{E}$ OR $\overline{W}$ MUST BE HIGH DURING ADDRESS TRANSITIONS.

DON'T CARE
UNDEFINED

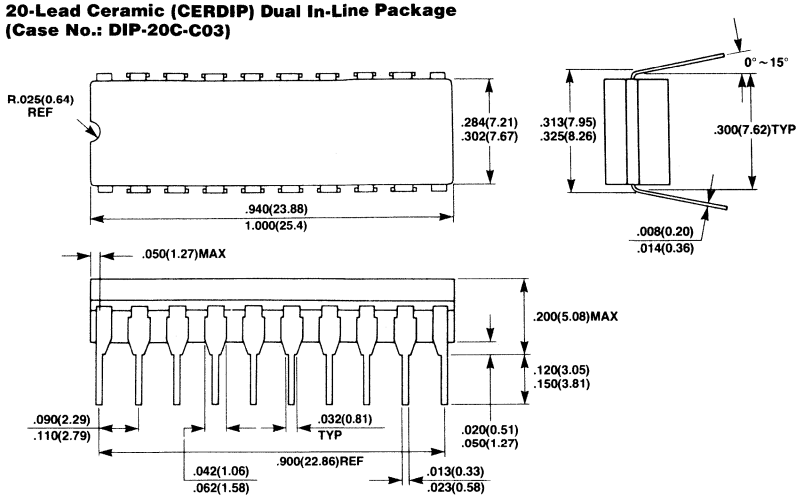
AC Test Condition

Input Pulse Levels:	0V to 3.0V
Input Pulse Rise And Fall Times:	5 ns (Transient Time between 0.8V and 2.2V)
Timing Reference Levels:	Input : 1.5V
Output Load:	Output: 1.5V

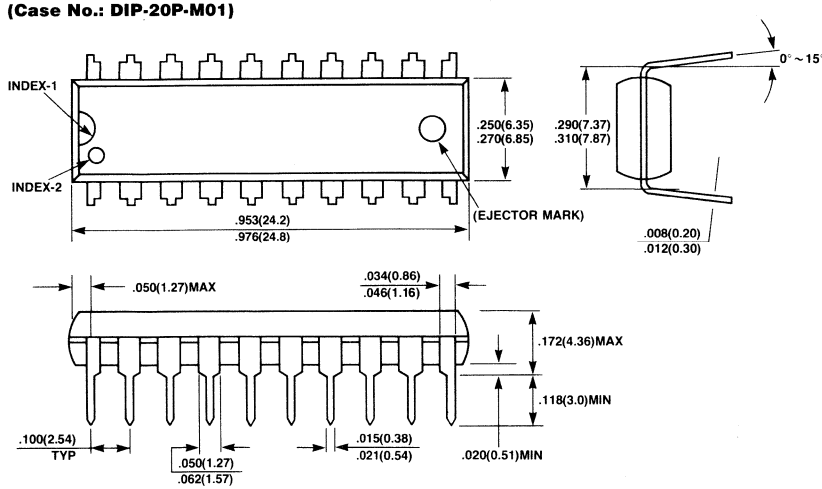


Package Dimensions
Dimensions in inches
(millimeters)

20-Lead Ceramic (CERDIP) Dual In-Line Package
(Case No.: DIP-20C-C03)



20-Lead Plastic Dual In-Line Package
(Case No.: DIP-20P-M01)



Preliminary

MOS Memories

FUJITSU

■ MB81C71-45, MB81C71-55

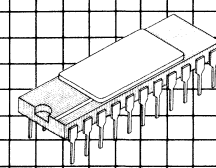
65,536-Bit Static Random Access Memory with Separate Data Input, Data Output and Automatic Power Down

Description

The Fujitsu MB81C71 is a 65,536 word x 1-bit static random access memory fabricated with CMOS technology. It uses fully static circuitry throughout and therefore requires no clocks or refreshing to operate.

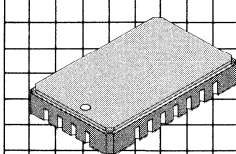
The MB81C71 is designed for memory applications where high performance, low cost, large bit storage and simple interfacing are required.

All pins are TTL compatible and a single +5 volt power supply is required.



Ceramic Package DIP-22C-A02

Plastic Package DIP-22P-M04



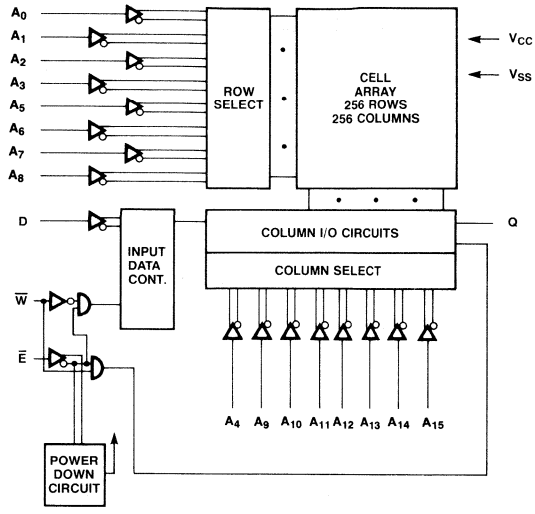
LCC-22C-A01

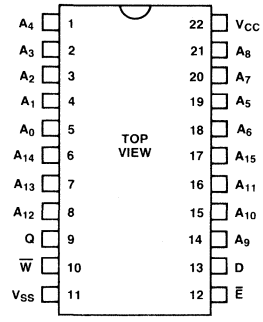
Features

- **Organization 65,536 words x 1-bit**
- **Static operation: no clocks or refresh required**
- **Fast access time: TAVQV = TELQV = 45 ns max. (MB81C71-45) TAVQV = TELQV = 55 ns max. (MB81C71-55)**
- **Single +5V supply ±10% tolerance**
- **Separate data input and output**
- **TTL compatible inputs and outputs**
- **Three-state output with OR-tie capability**
- **Chip enable for simplified memory expansion, automatic power down**
- **All inputs and output have protection against static charge**
- **Standard 300 mil. width 22-pin Dual In-Line package**
- **Standard 22-pad LCC package**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB81C71 Block Diagram and Pin Assignments





TRUTH TABLE

$\overline{E}$	$\overline{W}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	HIGH-Z	ACTIVE
L	H	READ	Q	ACTIVE

Absolute Maximum Ratings
(See Note)

Rating	Symbol		Value	Unit
Supply voltage	V_{CC}		−0.5 to +7	V
Input voltage on any pin with reference to V_{SS}	V_{IN}		−3.5* to +7	V
Output voltage on any pin with reference to V_{SS}	V_{OUT}		−0.5 to +7	V
Output current	I_{OUT}		±50	mA
Power dissipation	P_D		1.0	W
Temperature under bias	T_{BIAS}		−10 to +85	°C
Storage temperature	T_{STG}	Ceramic	−65 to +150	°C
		Plastic	−45 to +125	

*DC: min. = −0.5V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low voltage	V_{IL}	−0.5*		0.8	V
Input high voltage	V_{IH}	2.2		6.0	V
Ambient temperature	T_A	0		70	°C

Note: *−3.0V min. for pulse width less than 20 ns.

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input capacitance (V_{IN} = 0V)	C_{IN}		5	pF
$\overline{E}$ capacitance (V_{IN} = 0V)	$C_{\overline{E}}$		8	pF
Output capacitance (V_{OUT} = 0V)	C_{OUT}		8	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Input leakage current	V_{IN} = 0V to V_{CC} V_{CC} = max.	I_{LI}	−10		10	μA
Output leakage current	$\overline{E}$ = V_{IH}, V_{OUT} = 0V to 4.5 V_{CC} = max.	I_{LO}	−50		50	μA
Operating power supply current	$\overline{E}$ = V_{IL}, V_{CC} = max. I_{OUT} = 0 mA, cycle = min.	I_{CC}			80	mA
Standby current	V_{CC} = min. to max. $\overline{E}$ = V_{CC} −0.2V V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} −0.2V	I_{SB1}			15	mA
	V_{CC} = min. to max. $\overline{E}$ = V_{IH}	I_{SB2}			25	
Output low voltage	I_{OL} = 16 mA	V_{OL}			0.45	V
Output high voltage	I_{OH} = −4 mA	V_{OH}	2.4			V
Peak power on current	V_{CC} = 0 to V_{CC} min. $\overline{E}$ = lower of V_{CC} or V_{IH} min.	I_{PO}			30	mA

AC Characteristics

(Recommended operating conditions unless otherwise noted.)

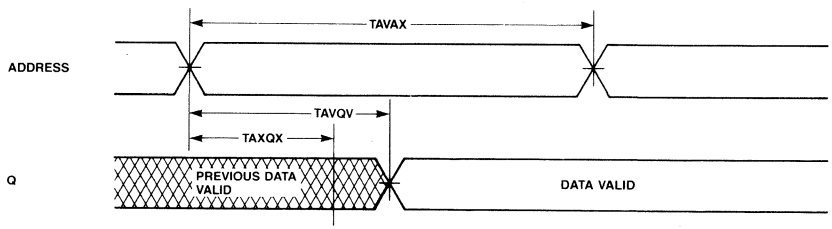
Read Cycle

Parameter	Symbol	MB81C71-45 Min	MB81C71-45 Max	MB81C71-55 Min	MB81C71-55 Max	Unit
Read cycle time*1	TAVAX	45		55		ns
Address access time	TAVQV		45		55	ns
Chip enable access time*2	TELQV		45		55	ns
Output hold from address change	TAXQX	5		5		ns
Chip enable to output in low-Z*3,4	TELQX	5		5		ns
Chip enable to output in high-Z*3,4	TEHQZ	0	25	0	30	ns
Chip enable to power up time	TELIH	0		0		ns
Chip enable to power down	TEHIL		35		40	ns

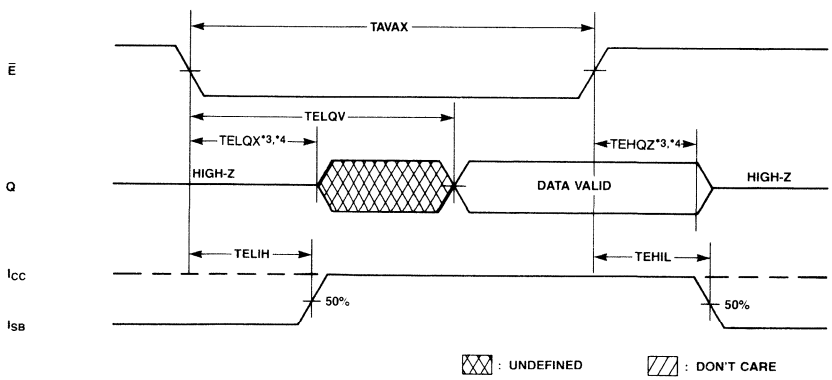
Notes: *1 All read cycles are determined from the last valid address transitioning to the first address transitioning of next cycle.
*2 Chip enable for a finite time is less than TAVAX prior to selection.
*3 Transition is measured at the point of ±500 mV from steady state voltage.
*4 This parameter is measured with the loading specified in Figure 1.

Read Cycle Timing Diagrams

Read Cycle: Address Controlled*1 *2



Read Cycle: $\overline{E}$ Controlled*2



NOTES: *1 $\overline{E}$ IS LOW.
*2 $\overline{W}$ IS HIGH TO READ CYCLES.
*3 TRANSITION IS MEASURED AT THE POINT OF ±500 mV FROM STEADY STATE VOLTAGE.
*4 THIS PARAMETER IS MEASURED WITH THE LOADING SPECIFIED IN FIGURE 1.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

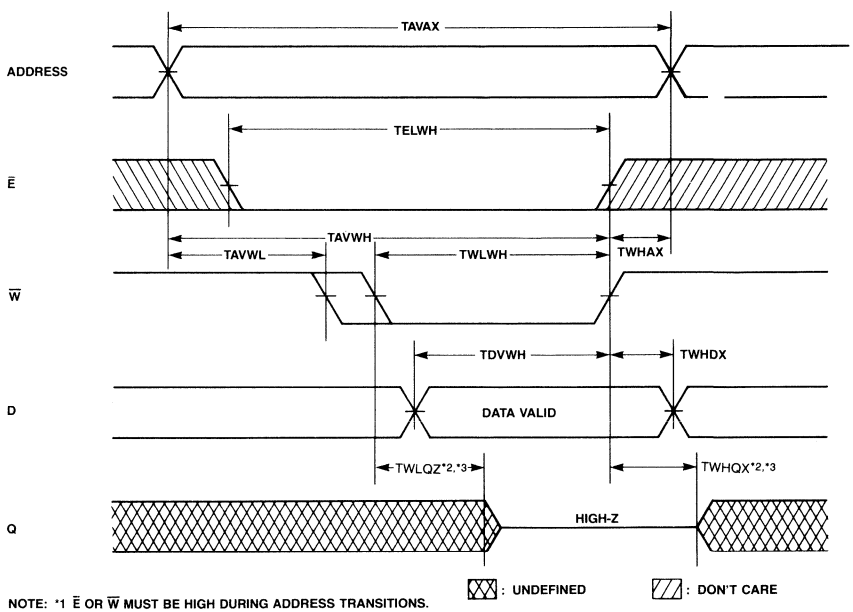
Write Cycle

Parameter	Symbol	MB81C71-45 Min	MB81C71-45 Max	MB81C71-55 Min	MB81C71-55 Max	Unit
Write cycle time	TAVAX	45		55		ns
Chip enable to end of write	TELWH	40		50		ns
Address valid to end of write	TAVWH	40		50		ns
Address setup time	TAVWL	5		5		ns
Address setup time	TAVEL	0		0		ns
Write pulse width	TWLWH	30		35		ns
Data valid to end of write	TDVWH	25		30		ns
Write recovery time	TWHAX	5		5		ns
Data hold time	TWHDX	0		0		ns
Write enable to output in high-Z*1 *2	TWLQZ	0	25	0	30	ns
Output active from end of write*1 *2	TWHQX	0		0		ns

Notes: *1 Transition is measured at the point of ±500 mV from steady state voltage.
*2 This parameter is measured with the loading specified in Figure 1.

Write Cycle Timing Diagrams

Write Cycle: $\overline{W}$ Controlled*1

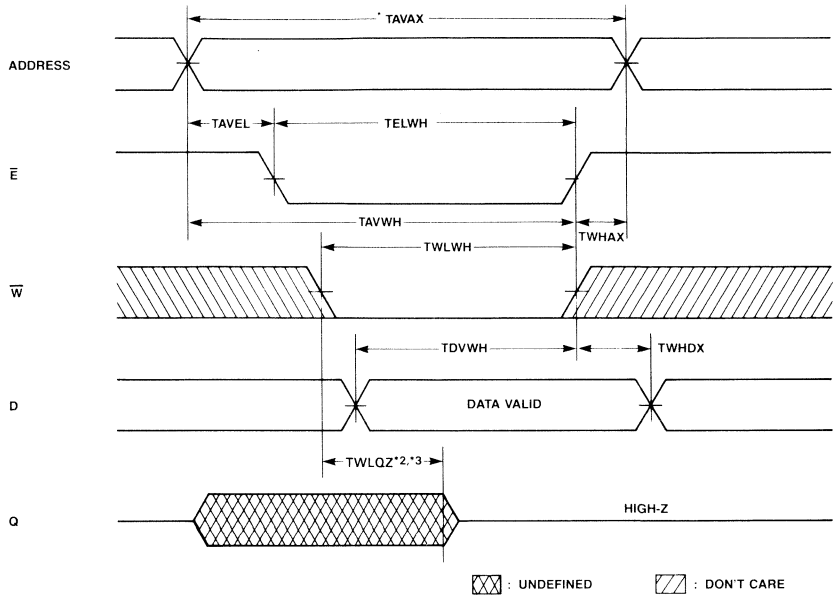


NOTE: *1 $\overline{E}$ OR $\overline{W}$ MUST BE HIGH DURING ADDRESS TRANSITIONS.
*2 TRANSITION IS MEASURED AT THE POINT OF ±500 mV FROM STEADY STATE VOLTAGE.
*3 THIS PARAMETER IS MEASURED WITH THE LOADING SPECIFIED IN FIGURE 1.

AC Characteristics
(continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle Timing Diagram*1

Write Cycle: $\overline{E}$ Controlled



NOTES: * ALL WRITE CYCLES ARE DETERMINED FROM LAST VALID ADDRESS TRANSITIONING TO THE FIRST ADDRESS TRANSITIONING OF NEXT CYCLE.
*1 $\overline{E}$ OR $\overline{W}$ MUST BE HIGH DURING ADDRESS TRANSITIONS.
*2 TRANSITION IS MEASURED AT THE POINT OF ±0.5 V FROM STEADY STATE VOLTAGE.
*3 THIS PARAMETER IS MEASURED WITH THE LOADING SPECIFIED IN FIGURE 1.

AC Test Conditions

Input pulse levels:	0.6V to 2.4V
Input pulse rise and fall times:	5 ns
Timing measurement reference levels:	Input: 1.5V
	Output: 1.5V

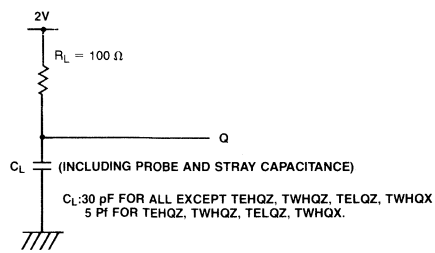
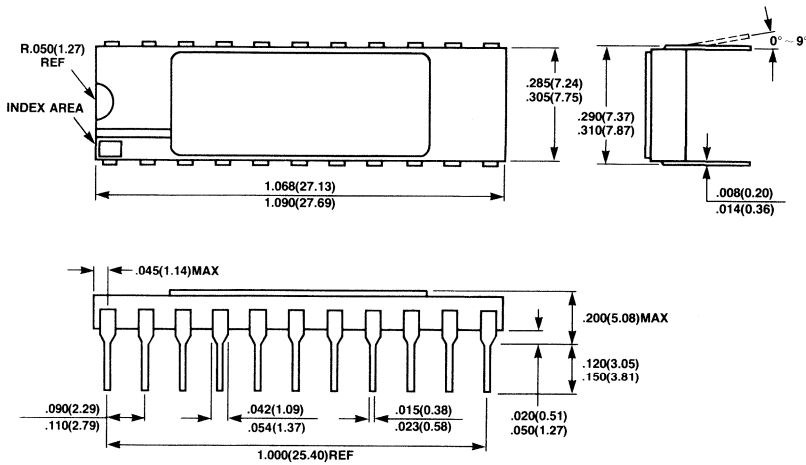


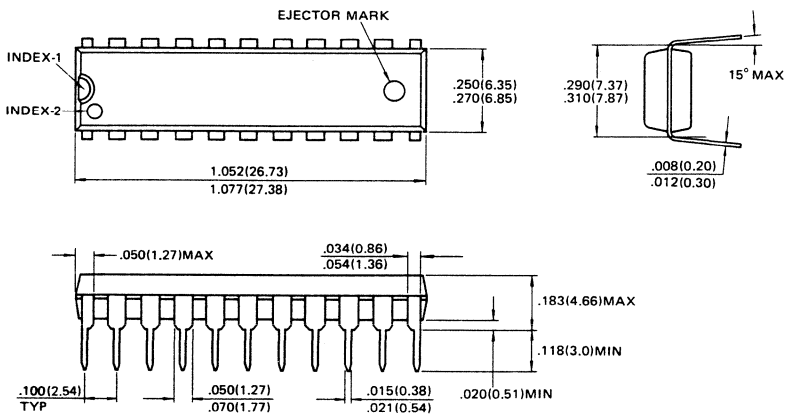
Figure 1. Output Loading

Package Dimensions
Dimensions in inches
(millimeters)

22-Lead Ceramic (Metal Seal) Dual In-Line Package
(Case No.: DIP-22C-A02)

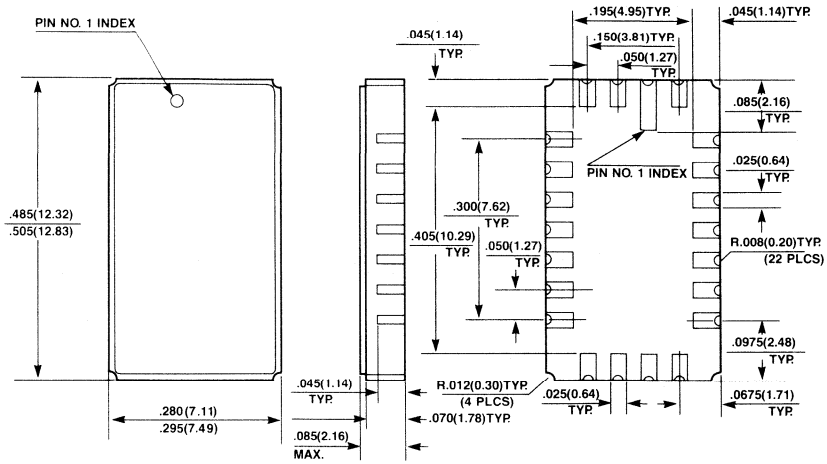


22-Lead Plastic Dual In-Line Package
(Case No.: DIP-22P-M02)



Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

22-Pad Ceramic (Metal Seal) Leadless Chip Carrier
(Case No.: LCC-22C-A01)



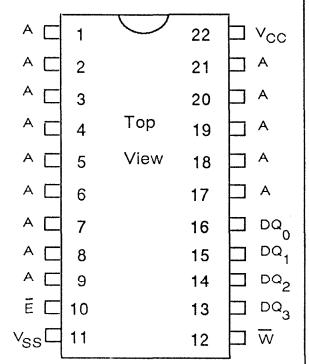
MOS Memories

MB81C74-25, MB81C74-35

64K Bit CMOS Static
Random Access Memory

Description

The Fujitsu MB81C74 is a 16K word by 4-bit static random access memory fabricated using MIX-MOS technology. The memory utilizes asynchronous circuitry and requires no clock or timing strobe. All pins are TTL compatible and a single +5 volt power supply is required.



Features

- **Organization: 16K words x 4-bits**
- **Static operation: no clocks or timing strobe required**
- **Fast Access Time:**
  TAVQV = 25 ns
  (MB81C74-25)
  TAVQV = 35 ns
  (MB81C74-35)
- **Low Power Consumption**
  605 mW max. (active)
  138 mW max. (standby)
- **Single +5 volt ±10% supply**
- **TTL compatible inputs and outputs**
- **NMOS cell and CMOS periphery**
- **Common I/O**
- **22 pin DIP (300mil)**

MB81C78-45, MB81C78-55

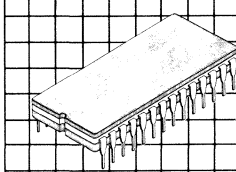
CMOS 65,536-Bit Static Random Access Memory

Description

The Fujitsu MB81C78 is a 8,192 word x 8-bit static random access memory fabricated with a CMOS process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 volt power supply is required.

A separate chip enable ($\overline{E}_1$) pin simplifies multipackage systems design. It permits the selection of an individual package when outputs are OR-tied, and furthermore on selecting a single package by $\overline{E}_1$, the other deselected devices are automatically powered down.

The MB81C78 offers the advantages of lower power dissipation, low cost, and high performance.



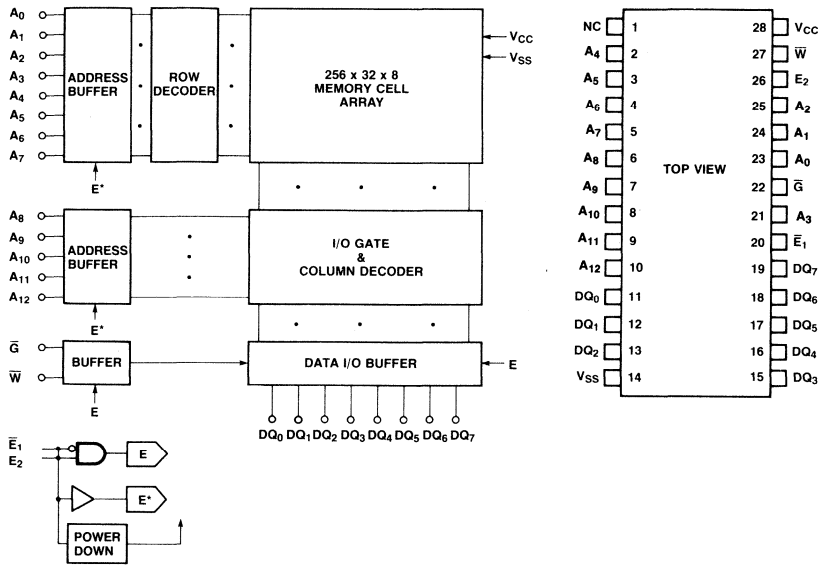
DIP-28C-C02
(CERDIP)

Features

- **Organization: 8192 words x 8-bits**
- **Static operation: no clocks or timing strobe required**
- **Fast access time: TAVQV = TELQV = 45 ns max. (MB81C78-45) TAVQV = TELQV = 55 ns max. (MB81C78-55)**
- **Low power consumption: 660 mW max. (Operating) 138 mW max. (Standby)**
- **Single +5V supply ±10% tolerance**
- **TTL compatible inputs and outputs**
- **Three-state outputs with OR-tie capability**
- **Chip enable for simplified memory expansion, automatic power down**
- **All inputs and outputs have protection against static charge**
- **Standard 28-pin DIP package**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB81C78 Block Diagram and Pin Assignment



TRUTH TABLE

$\overline{W}$	$\overline{E}_1$	E_2	$\overline{G}$	MODE	SUPPLY CURRENT	DQ STATE
X	H	X	X	STANDBY	I_{SB}	HIGH-Z
X	L	L	X	DESELECT	I_{CC}	HIGH-Z
H	L	H	H	OUT DISABLE	I_{CC}	HIGH-Z
H	L	H	L	READ	I_{CC}	OUT
L	L	H	X	WRITE	I_{CC}	IN

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	−0.5 to +7	V
Input voltage on any pin with respect to GND	V_{IN}	−3.5 to +7	V
Output voltage on any DQ pin with respect to GND	V_{OUT}	−0.5 to +7	V
Output current	I_{OUT}	±20	mA
Power dissipation	P_D	1.0	W
Temperature under bias	T_{BIAS}	−10 to +85	°C
Storage temperature	T_{STG} Ceramic	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low voltage*1	V_{IL}	−0.5		0.8	V
Input high voltage	V_{IH}	2.2		6.0	V
Ambient temperature*2	T_A	0		70	°C

Notes: *1 −2.0V min. for pulse width less than 20 ns.
(V_{IL} min. = −0.5V at DC level)
*2 The operating ambient temperature range is guaranteed with transverse airflow exceed 2 m/sec.

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input capacitance (V_{IN} = 0V) ($\overline{E}_1$, E_2, $\overline{G}$, $\overline{W}$)	C_{IN1}		7	pF
Input capacitance (V_{IN} = 0V) (other inputs)	C_{IN2}		6	pF
DQ capacitance ($V_{I/O}$ = 0V)	C_{OUT}		8	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Max	Unit
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	−10	10	μA
Output leakage current	$\overline{E}_1 = V_{IH}$ or $E_2 = V_{IL}$ or $\overline{W} = V_{IL}$ or $\overline{G} = V_{IH}$, V_{OUT} = 0V to V_{CC}	I_{LO}	−10	10	μA
Operating supply current	$\overline{E}_1 = V_{IL}$ I/O = open, cycle = min.	I_{CC}		120	mA
Standby supply current	V_{CC} = min. to max. $\overline{E}_1 = V_{CC} - 0.2$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$	I_{SB1}		15	mA
	V_{CC} = min. to max. $\overline{E}_1 = V_{IH}$	I_{SB2}		25	mA
Output low voltage	I_{OL} = 8 mA	V_{OL}		0.4	V
Output high voltage	I_{OH} = −4 mA	V_{OH}	2.4		V
Peak power-on current	V_{CC} = 0V to V_{CC} min. $\overline{E}_1$ = lower of V_{CC} or V_{IH} min.	I_{PO}		50	mA

AC Characteristics

(Recommended operating conditions unless otherwise noted.)

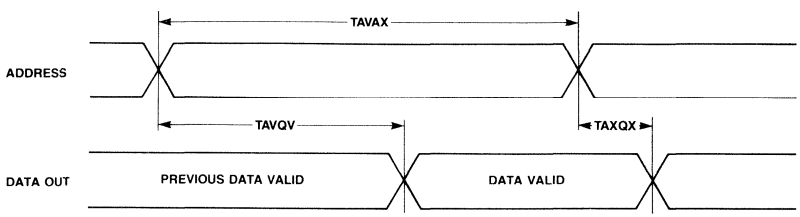
Read Cycle*1

Parameter	Symbol	MB81C78-45 Min	MB81C78-45 Max	MB81C78-55 Min	MB81C78-55 Max	Unit
Read cycle time	TAVAX	45		55		ns
Address access time*2	TAVQV		45		55	ns
Chip enable access time*3	TE1LQV		45		55	ns
Chip enable access time*3	TE2HQV		30		40	ns
Output hold from address change	TAXQX	5		5		ns
Output enable to output valid	TGLQV		20		25	ns
Output active from chip select*4,5	TE1LQX	10		10		ns
Output active from chip select*4,5	TE2HQX	5		5		ns
Output active from output enable*4,5	TGLQZ	0		0		ns
Output disable from chip enable*4,5	TE1LQZ		25		30	ns
Output disable from chip enable*4,5	TE2HQZ		25		30	ns
Output disable from output enable*4,5	TGHQZ		25		30	ns

Notes: *1 $\overline{W}$ is high for read cycle.
*2 Device is continuously selected, $\overline{E}_1 = V_{IL}$, $E_2 = V_{IH}$ and $\overline{G} = V_{IL}$.
*3 Address valid prior to or coincident with $\overline{CS}_1$ transition low, $\overline{CS}_2$ transition high.
*4 Transition is measured at the point of ±500 mV from steady state voltage.
*5 This parameter is measured with specified Load II in Fig. 2.

Read Cycle Timing Diagram*1

Read Cycle: Address Controlled*2

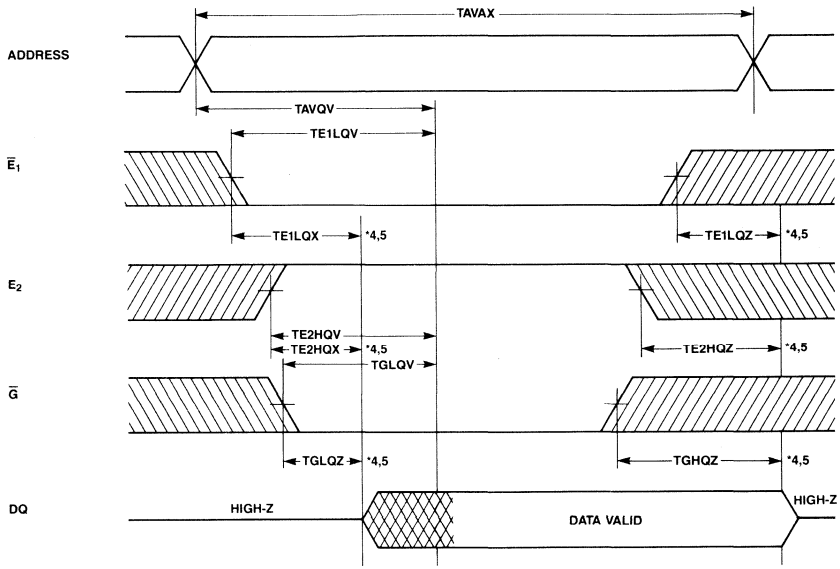


NOTES: *1 $\overline{W}$ IS HIGH FOR READ CYCLE.
*2 DEVICE IS CONTINUOUSLY SELECTED, $\overline{E}_1 = V_{IL}$, $E_2 = V_{IH}$, $\overline{G} = V_{IL}$.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Read Cycle Timing Diagram[*1]

Read Cycle: $\overline{E}_1$, E_2 Controlled[*3]



NOTES: *1 $\overline{W}$ IS HIGH FOR READ CYCLE.
*3 ADDRESS VALID PRIOR TO OR COINCIDENT WITH $\overline{E}_1$ TRANSITION LOW E_2 TRANSITION HIGH.
*4 TRANSITION IS MEASURED AT THE POINT OF ±500 mV FROM STEADY STATE VOLTAGE.
*5 THIS PARAMETER IS MEASURED WITH SPECIFIED LOAD II IN FIG. 2.

DON'T CARE
UNDEFINED

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle[*1]

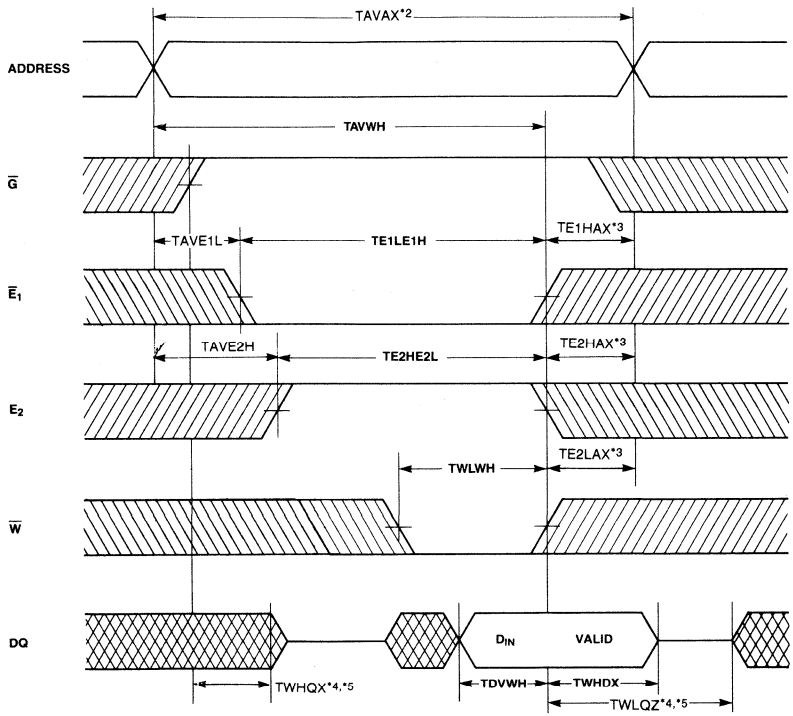
Parameter	Symbol	MB81C78-45 Min	MB81C78-45 Max	MB81C78-55 Min	MB81C78-55 Max	Unit
Write cycle time[*2]	TAVAX	45		55		ns
Chip enable to end of write	TE1LE1H	40		45		ns
	TE2HE2L	25		30		
Address valid to end of write	TAVWH	40		45		ns
Address setup time	TAVWL	5		5		ns
Write pulse width	TWLWH	25		30		ns
Data setup time	TDVWH	25		30		ns
Write recovery time[*3]	TWHAX, TE1HAX, TE2LAX	5		5		ns
Data hold time	TWHDX	0		0		ns
Output high-Z from $\overline{W}$[*4,5]	TWLQZ		20		20	ns
Output low-Z from $\overline{W}$[*4,5]	TWHQX	0		0		ns

Notes: *1 If $\overline{E}_1$ goes high simultaneously with $\overline{W}$ high, the output remains in high impedance state.
*2 All write cycles are determined from the last address transition to the first address transition of next address.
*3 TWHAX is defined from the end point of write mode.
*4 Transition is measured at the point of +500 mV from steady state voltage.
*5 This parameter is measured with specified Load II in Fig. 2.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle Timing Diagram[*1]

Write Cycle 1 ($\overline{E}_1$, E_2 Controlled)



NOTE: *1 **IF $\overline{G}$, $\overline{E}_1$ AND E_2 ARE IN THE READ MODE DURING THIS PERIOD, DQ PINS ARE IN THE OUTPUT STATE SO THAT THE INPUT SIGNALS OF OPPOSITE PHASE TO THE OUTPUTS MUST NOT BE APPLIED.**
*2 ALL WRITE CYCLES ARE DETERMINED FROM THE LAST ADDRESS TRANSITION OF NEXT ADDRESS.
*3 t_{WR} IS DEFINED FROM THE END POINT OF **WRITE** MODE.
*4 TRANSITION IS MEASURED AT THE POINT OF ±0.5 V FROM STEADY STATE VOLTAGE.
*5 THIS PARAMETER IS SPECIFIED WITH LOAD II.

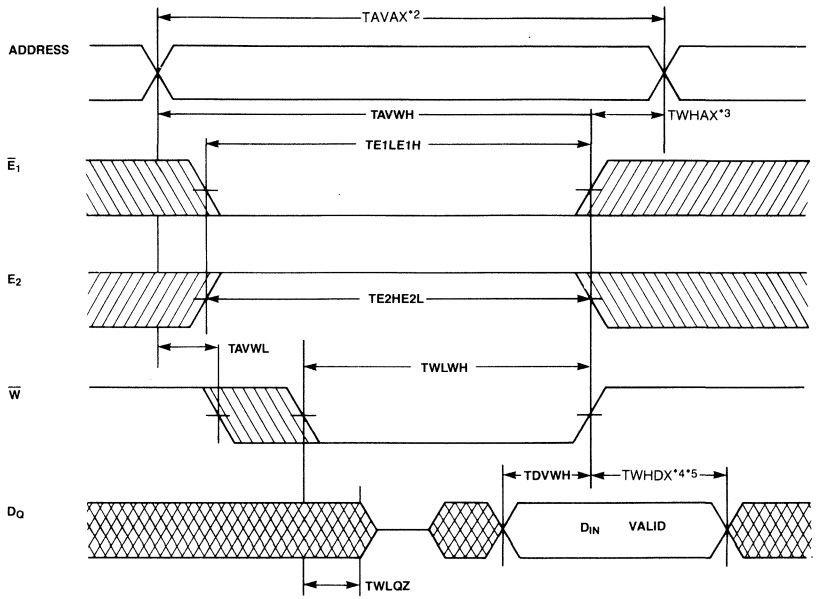
UNDEFINED
DON'T CARE

AC Characteristics

(Continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle Timing Diagram*1

Write Cycle 2 ($\overline{W}$ Controlled)



NOTE: *1 IF $\overline{G}$, $\overline{E}_1$, AND E_2 ARE IN THE READ MODE DURING THIS PERIOD, DQ PINS ARE IN THE OUTPUT STATE SO THAT THE INPUT SIGNALS OF OPPOSITE PHASE TO THE OUTPUTS MUST NOT BE APPLIED.
*2 ALL WRITE CYCLES ARE DETERMINED FROM THE LAST ADDRESS TRANSITION TO THE FIRST ADDRESS TRANSITION OF NEXT ADDRESS.
*3 t_{WR} IS DEFINED FROM THE END POINT OF **WRITE** MODE.
*4 TRANSITION IS MEASURED AT THE POINT OF ±500 mV FROM STEADY STATE VOLTAGE.
*5 THIS PARAMETER IS SPECIFIED WITH LOAD II.

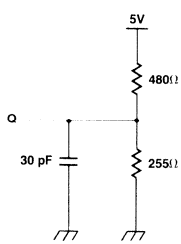
UNDEFINED

AC Test Conditions

Input Pulse Levels:	0.6V to 2.4V
Input Pulse Rise and Fall Times:	5 ns (Transient time between 0.8V and 2.2V)
Timing Measurement Reference Levels:	Input: 1.5V
	Output: 1.5V

Output Load I.

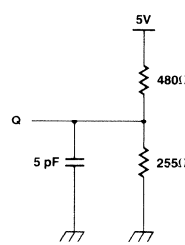
For all except TE1LQH, TE2HQH, TE2LQL, TE2HQL, TWLHQZ, TWHLQZ



(INCLUDING SCOPE AND PROBE CAPACITANCE)

Output Load II.

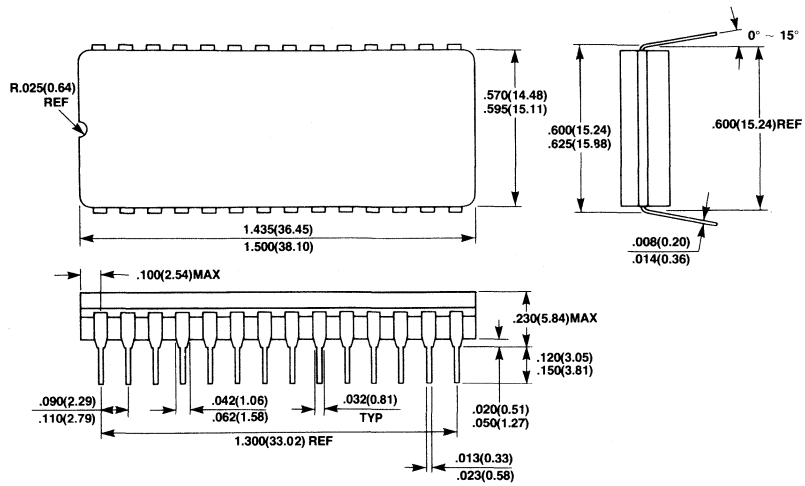
For TE1LQH, TE2HQH, TE2LQL, TE2HQL, TWLHQZ, TWHLQZ



(INCLUDING SCOPE AND PROBE CAPACITANCE)

Package Dimensions
Dimensions in inches
(millimeters)

28-Lead Ceramic (CERDIP) Dual In-Line Package
(Case No.: DIP-28C-C02)



MB81C79-45, MB81C79-55

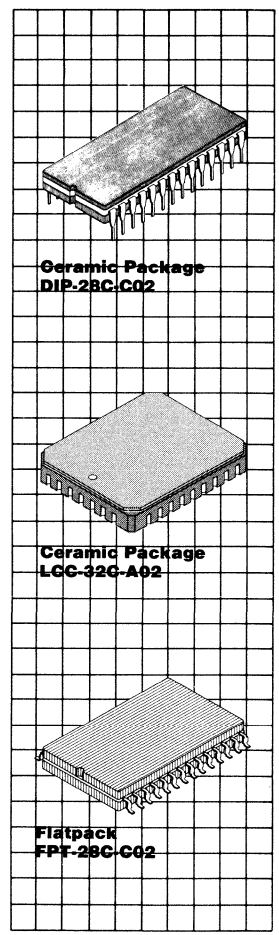
73,728-Bit Static Random Access Memory with Automatic Power Down

Description

The Fujitsu MB81C79 is an 8,192 words x 9-bits static random access memory with a CMOS process. The ninth bit optimizes parity check. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single, +5 volt power supply is required.

A separate chip enable ($\overline{E}_1$) pin simplifies multipackage systems design. It permits the selection of an individual device when outputs or OR-tied, and furthermore on selecting a single device by $\overline{E}_1$ the other deselected devices are automatically powered down.

The MB81C79 offers the advantages of low power dissipation, low cost, and high performance.

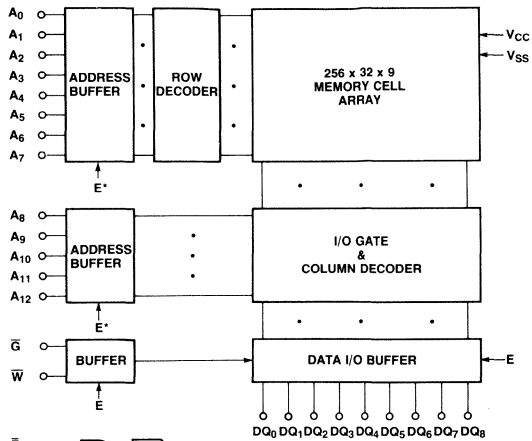


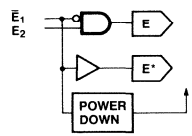
Features

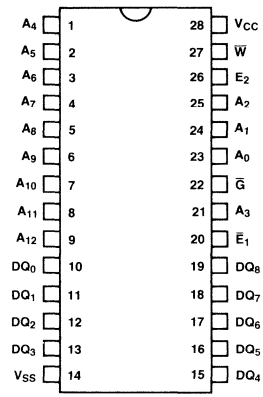
- **Organization: 8,192 words x 9-bits**
- **Static operation: no clocks or timing strobe required**
- **Fast access time: TAVQV = TELQV = 45 ns max. (MB81C79-45) TAVQV = TELQV = 55 ns max. (MB81C79-55)**
- **Low power consumption: 660 mW max. (Operating) 138 mW max. (Standby)**
- **Single +5V power supply**
- **TTL compatible inputs and outputs**
- **Three-state outputs with OR-tie capability**
- **Chip enable for simplified memory expansion, automatic power down**
- **All inputs and outputs have protection against static charge**
- **Standard 28-pin DIP package**
- **Also available in 28-pin ceramic LCC and ceramic Flatpack**

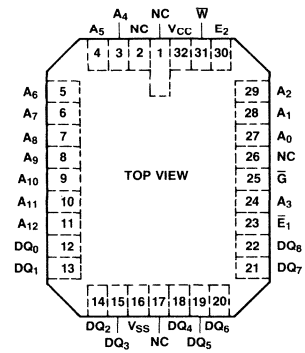
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB81C79 Block Diagram and Pin Assignments









TRUTH TABLE

W	E1	E2	G	MODE	SUPPLY CURRENT	DQ STATE
X	H	X	X	STANDBY	I_{SB}	HIGH-Z
X	L	L	X	DESELECT	I_{CC}	HIGH-Z
H	L	H	H	OUT DISABLE	I_{CC}	HIGH-Z
H	L	H	L	READ	I_{CC}	OUT
L	L	H	X	WRITE	I_{CC}	IN

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	−0.5 to +7	V
Input voltage on any pin with respect to V_{SS}	V_{IN}	−3.5 to +7	V
Output voltage on any D/Q pin with respect to V_{SS}	V_{OUT}	−0.5 to +7	V
Output current	I_{OUT}	±20	mA
Power dissipation	P_D	1.0	W
Temperature under bias	T_{BIAS}	−10 to +85	°C
Storage temperature	T_{STG}	−65 to 150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low voltage	V_{IL}	−2.0*1		0.8	V
Input high voltage	V_{IH}	2.2		6.0	V
Ambient temperature	T_A*2	0		70	°C

Notes: *1 −2.0V min. for pulse width less than 20 ns (V_{IL} min. = −0.5V at DC LEVEL).
*2 The operating ambient temperature range is guaranteed with transverse airflow exceed 2m/sec.

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input capacitance (V_{IN} = 0V) ($\overline{E_1}$, E_2, $\overline{G}$, $\overline{W}$)	C_{IN1}		7	pF
Input capacitance (V_{IN} = 0V) (other inputs)	C_{IN2}		6	pF
D/Q capacitance ($V_{I/O}$ = 0V)	C_{OUT}		8	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Max	Unit
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	−10	10	μA
Output leakage current	$\overline{E_1}$ = V_{IH} or E_2 = V_{IL} or $\overline{G}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	I_{LO}	−10	10	μA
Operating supply current	$\overline{E_1}$ = V_{IL} D/Q = open, cycle = min.	I_{CC}		120	mA
Standby supply current	V_{CC} = min. to max. V_{IN} = 0V or V_{CC}	I_{SB1}		15	mA
	$\overline{E_1}$ = V_{IH}	I_{SB2}		25	mA
Ouptut low voltage	I_{OL} = 8 mA	V_{OL}		0.4	V
Output high voltage	I_{OH} = −4 mA	V_{OH}	2.4		V
Peak power-on current	V_{CC} = 0V to V_{CC} min. $\overline{E_1}$ = lower of V_{CC} or V_{IH} min.	I_{PO}		50	mA

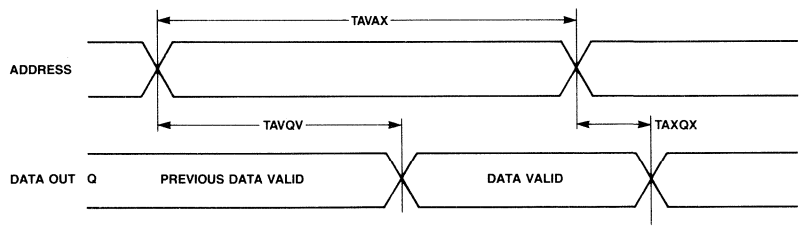
AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Read Cycle

Parameter	Symbol	MB81C79-45 Min	MB81C79-45 Max	MB81C79-55 Min	MB81C79-55 Max	Unit
Read cycle time	TAVAX	45		55		ns
Address access time	TAVQV		45		55	ns
Chip enable access time	TELQV		45		55	ns
	TE2HQV		30		40	ns
Output hold from address change	TAXQX	5		5		ns
Output enable to output valid	TGLQV		20		25	ns
Output active from chip select	TE1LQX	10		10		ns
	TE2HQX	5		5		
Output active from output enable	TGLQX	0		0		ns
Output disable from chip enable	TE1HQZ		25		30	ns
	TE2LQZ		25		30	
Output disable from output enable	TGHQZ		25		30	ns

Read Cycle Timing Diagrams *1

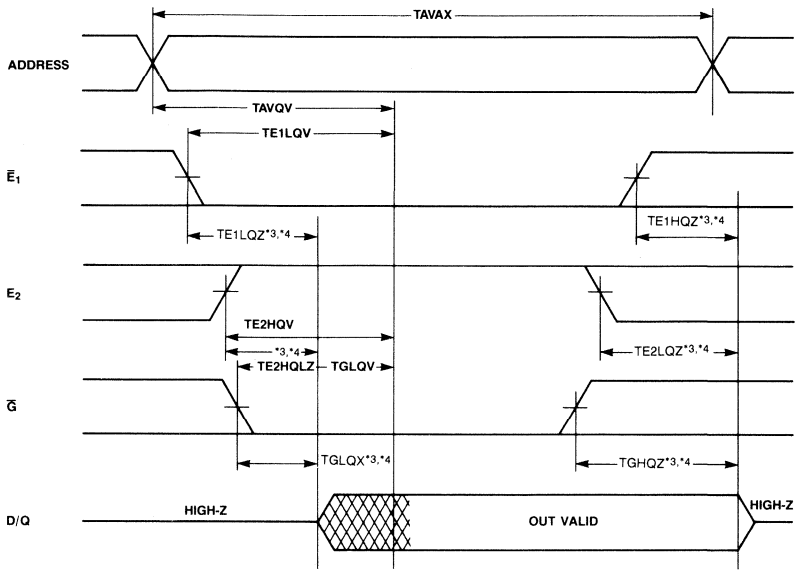
Read Cycle: Address Controlled *2



Notes: *1 $\overline{W}$ IS HIGH FOR READ CYCLE.
*2 DEVICE IS CONTINUOUSLY SELECTED, $\overline{E}_1 = V_{IL}$, $E_2 = V_{IH}$, $\overline{G} = V_{IL}$.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Read Cycle: $\overline{E}_1$ Controlled*1,*2



NOTES: *1 $\overline{W}$ IS HIGH FOR READ CYCLE.
*2 ADDRESS VALID PRIOR TO OR COINCIDENT WITH E_1 TRANSITION LOW, E_2 TRANSITION HIGH.
*3 TRANSITION IS MEASURED AT THE POINT OF ±500 mV FROM STEADY STATE VOLTAGE.
*4 THIS PARAMETER IS MEASURED WITH SPECIFIED LOADING LOAD II IN FIG. 2.

UNDEFINED

Write Cycle*1

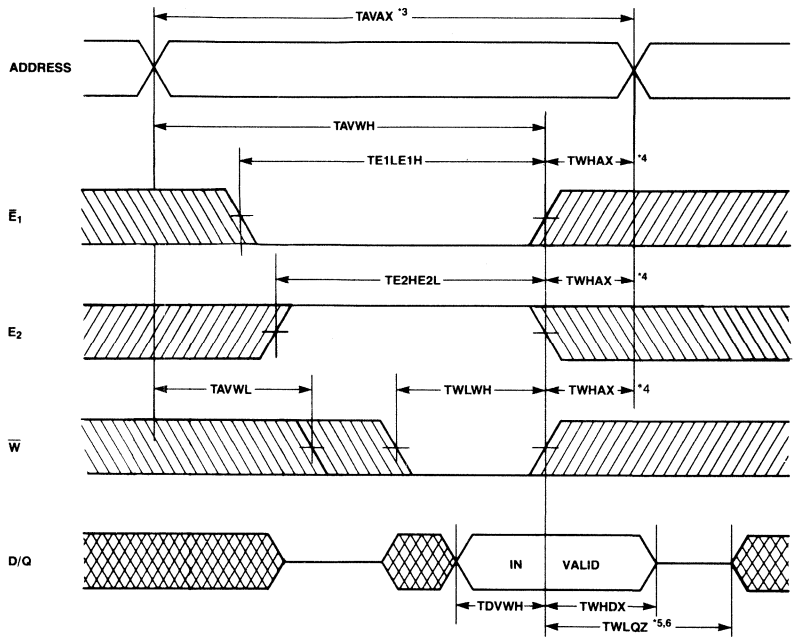
Parameter	Symbol	MB81C79-45 Min	MB81C79-45 Max	MB81C79-55 Min	MB81C79-55 Max	Unit
Write cycle time*2	TAVAX	45		55		ns
Chip enable to end of write	TE1LE1H	40		45		ns
	TE2HE2L	25		30		
Address valid to end of write	TAVWH	40		45		ns
Address setup time	TAVWL	5		5		ns
Write pulse width	TWLWH	25		30		ns
Data setup time	TDVWH	25		30		ns
Write recovery time*3	TWHAX	5		5		ns
Data hold time	TWHDX	0		0		ns
Output high-Z from $\overline{W}$*4,5	TWLQZ		20		20	ns
Output low-Z from $\overline{W}$*4,5	TWHQX	0		0		ns

Notes: *1 If $\overline{E}_1$ goes high simultaneously with $\overline{W}$ high, the output remain is high impedance state.
*2 All write cycles are determined from last address transition to the first address transition of next address.
*3 TWHAX is defined from the end point of Write mode.
*4 Transition is measured at the point of ±500 mV from steady state voltage.
*5 This parameter is measured with specified loading load II in Fig. 2.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle Timing Diagrams

Write Cycle I ($\overline{E}_1$, E_2, Controlled) *1,2

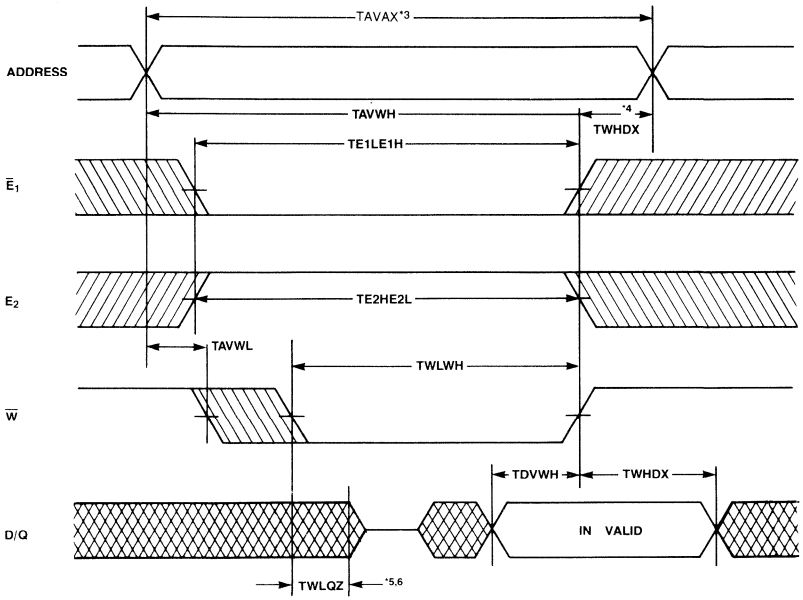


NOTES: *1 IF $\overline{G}$, $\overline{E}_1$ AND E_2 ARE IN THE READ MODE DURING THIS PERIOD, D/Q PINS ARE IN THE OUTPUT STATE SO THAT THE INPUT SIGNALS OF OPPOSITE PHASE TO THE OUTPUTS MUST NOT BE APPLIED.
*2 IF $\overline{E}_1$ GOES HIGH SIMULTANEOUSLY WITH $\overline{W}$ HIGH THE OUTPUT REMAIN IN HIGH IMPEDANCE STATE.
*3 ALL WRITE CYCLES ARE DETERMINED FROM LAST ADDRESS TRANSITION TO THE FIRST ADDRESS TRANSITION OF THE NEXT ADDRESS.
*4 TWHAX IS DEFINED FROM THE END POINT OF WRITE MODE.
*5 TRANSITION IS MEASURED AT THE POINT OF ±500 mV FROM STEADY STATE VOLTAGE.
*6 THIS PARAMETER IS MEASURED WITH SPECIFIED LOADING LOAD II IN FIG. 2

UNDEFINED
DON'T CARE

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle II ($\overline{W}$ Controlled) *1,2



NOTES: *1 IF $\overline{G}$, $\overline{E}_1$ AND E_2 ARE IN THE READ MODE DURING THIS PERIOD, I/O PINS ARE IN THE OUTPUT STATE SO THAT THE INPUT SIGNALS OF OPPOSITE PHASE TO THE OUTPUTS MUST NOT BE APPLIED.
*2 IF $\overline{E}_1$ GOES HIGH SIMULTANEOUSLY WITH $\overline{W}$ HIGH THE OUTPUT REMAIN IN HIGH IMPEDANCE STATE.
*3 ALL WRITE CYCLES ARE DETERMINED FROM LAST ADDRESS TRANSITION TO THE FIRST ADDRESS TRANSITION OF THE NEXT ADDRESS.
*4 TWHAX IS DEFINED FROM THE END POINT OF WRITE MODE.
*5 TRANSITION IS MEASURED AT THE POINT OF ±500 mV FROM STEADY STATE VOLTAGE.
*6 THIS PARAMETER IS MEASURED WITH SPECIFIED LOADING LOAD II IN FIG. 2.

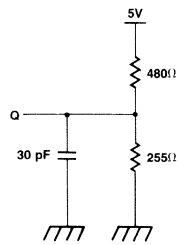
UNDEFINED
DON'T CARE

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

AC Test Conditions

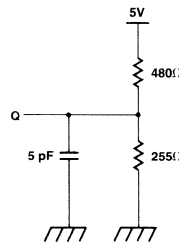
Input pulse levels:	0.6V to 2.4V
Input pulse rate and fall times:	5 ns (transient time between 0.8V and 2.2V)
Timing measurement reference levels:	Input : 1.5V Output: 1.5V

Output Load I.
For all except TE1LQZ, TE1HQZ TWLQZ, TWHQX, TGHQZ, TGLQX



(INCLUDING SCOPE AND FIXTURE CAPACITANCE)

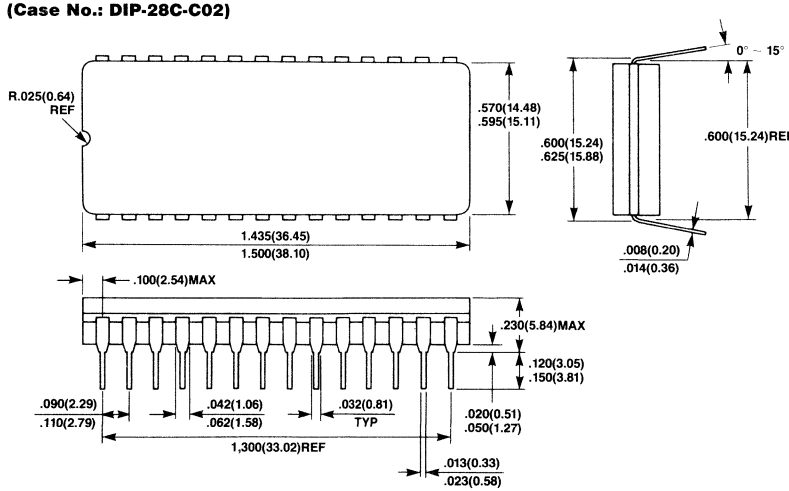
Output Load II.
For TE1LQZ, TE1HQZ, TGHQZ, TGLQX, TWLQZ, TWHQX



(INCLUDING SCOPE AND FIXTURE CAPACITANCE)

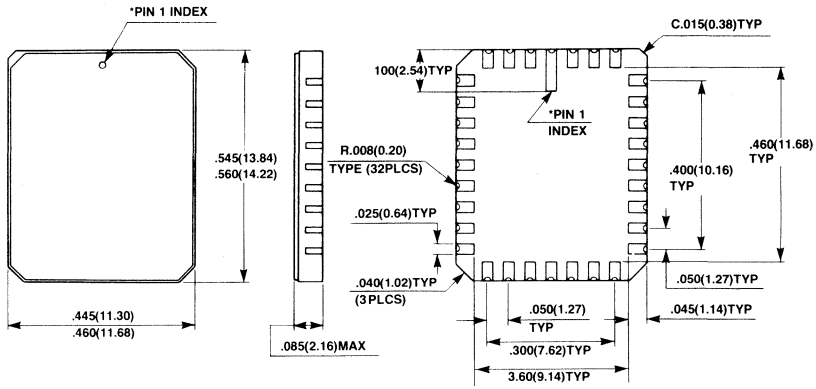
Package Dimensions
Dimensions in inches (millimeters)

28-Lead Ceramic (CERDIP) Dual In-Line Package (Case No.: DIP-28C-C02)



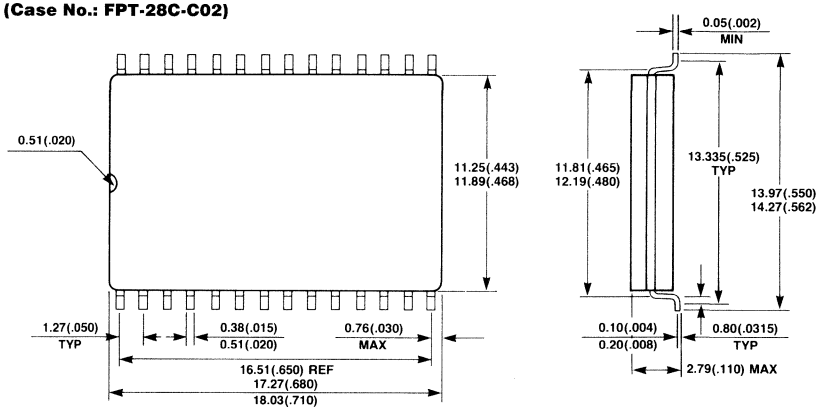
Package Dimensions
Dimensions in inches
(millimeters)
(Continued)

32-Pad Ceramic (Metal Seal) Leadless Chip Carrier
(Case No.: LCC-32C-A02)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

MB81C79 Ceramic Flat Package
(Case No.: FPT-28C-C02)



Preliminary

MOS Memories **FUJITSU**

■ MB81C86-55, MB81C86-70

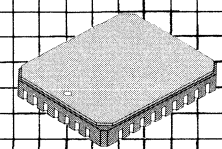
65,536 Words × 4-Bits CMOS Static RAM with Automatic Power Down

Description

The Fujitsu MB81C86 is a 65,536 word by 4-bit Static Random Access Memory fabricated with a CMOS silicon gate process.

The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5 volt power supply is required.

The MB81C86 is ideally suited for use in large computer systems where fast access time and ease of use are required. The MB81C86 offers the advantages of low power dissipation, low cost, and high performance.



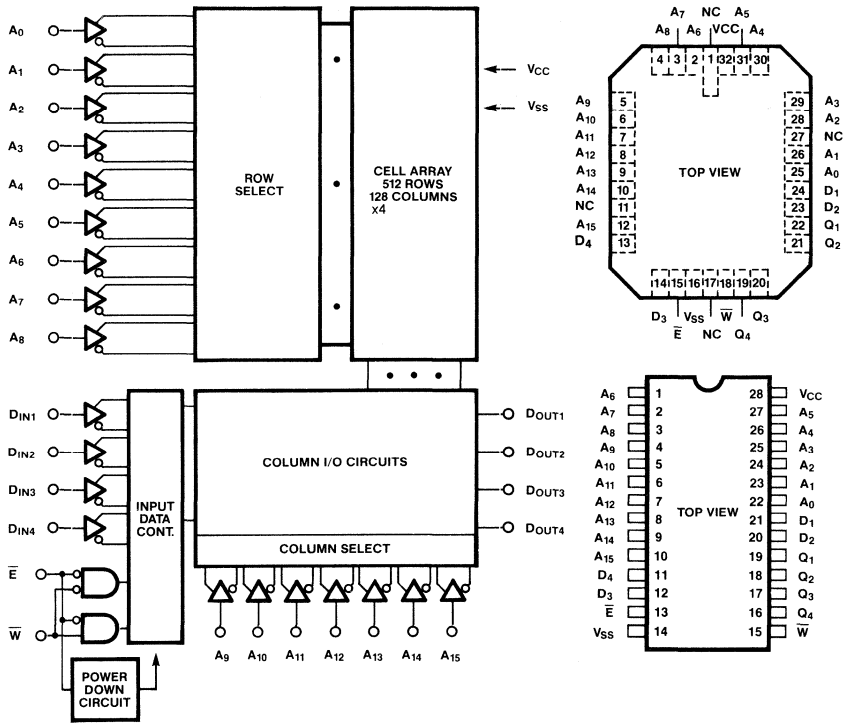
LCC-32C-A02

DIP-28C-A07

Features

- **Organization: 65,536 words × 4-bits**
- **Fast Access Time: TAVQV = TELQV = 55ns max. MB81C86-55 TAVQV = TELQV = 70ns max. MB81C86-70**
- **Completely Static Operation No Clock Required**
- **TTL Compatible Input/Output**
- **Three State Output**
- **Separate Data Input/Output**
- **Single +5 Volt Power Supply, ±10% Tolerance**
- **Low Power Standby: 550 mW max. Active 55 mW max. (Standby)**
- **Available in 28-pin Ceramic Package (600 mil) 32-pin LCC**

Block Diagram & Pin Assignments



Truth Table

$\overline{E}$	$\overline{W}$	Mode	Output	Power
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	HIGH-Z	ACTIVE
L	H	READ	DOUT	ACTIVE

Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-3.0 to +7.0	V
Output Voltage	V_{OUT}	-0.5 to +7.0	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	-10 to +85	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. *Exposure to absolute maximum rating condition for extended periods may affect device reliability.*

Capacitance

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance ($V_{I/O}$ = 0V)	C_{OUT}			8	pF
Input Capacitance (V_{IN} = 0V)	$C_{\overline{CS}}$			7	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			6	pF

Recommended Operating Conditions

(Referenced to VSS)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-3.0*		0.8	V
Input High Voltage	V_{IH}	2.2		6.0	V
Ambient Temperature	T_A	0		70	°C

Note: *-3.0V Min. for pulse width less than 20 ns. (V_{IL} min. = -0.5 V at DC level)

DC Characteristics

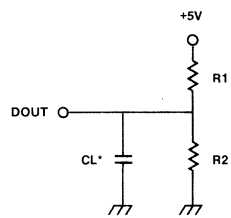
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby Supply Current	I_{SB}		10	mA	$V_{IN} = V_{SS}$ or V_{CC} $\overline{E} = V_{IH}$
Operating Supply Current	I_{CC2}		100	mA	Cycle = Min., I_{OUT} = 0mA
Input Leakage Current	IL_I	−5	5	μA	V_{IN} = 0V to V_{CC}
Output Leakage Current	$IL_{I/O}$	−5	5	μA	$\overline{E} = V_{IH}$ V_{OUT} = 0V to V_{CC}
Output High Voltage	V_{OH}	2.4		V	I_{OH} = −4mA
Output Low Voltage	V_{OL}		0.4	V	I_{OL} = 8mA
Peak Power-on Current	I_{PO}		40	mA	V_{CC} = 0 to V_{CC} min. $\overline{CS}$ = Lower of V_{CC} or V_{IH} min.

Note: All voltages are referenced to V_{SS}.

AC Test Conditions

- Input Pulse Levels: 0.6V to 2.4V
- Input Pulse Rise & Fall Times: 5ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input: V_{IL} = 0.8V, V_{IH} = 2.2V Output: V_{OL} = 0.8V, V_{OH} = 2.2V
- Output Load



*Including Probe and Stray Capacitance

	R1	R2	CL	Parameters Measured
Load I	480Ω	255Ω	30 pF	except TELQX, TEHQX, TWLQZ, TWHQX
Load II	480Ω	255Ω	5 pF	TELQX, TEHQZ, TWLQZ, TWHQX

AC Characteristics

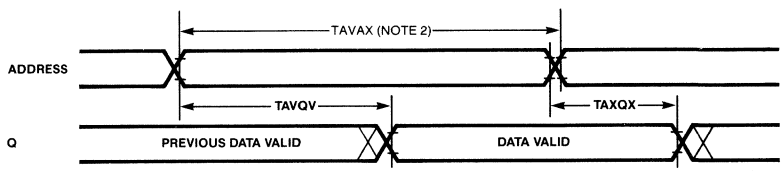
(Recommended operating conditions unless otherwise noted.)

Read Cycle

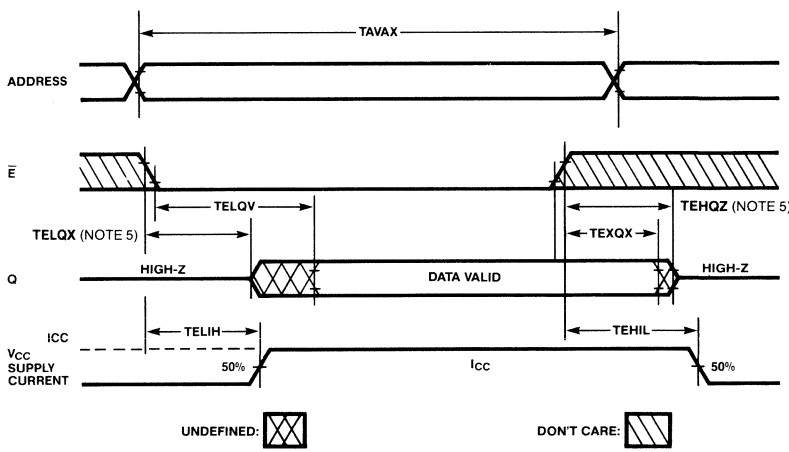
Parameter	Symbol	MB81C86-55 Min	MB81C86-55 Max	MB81C86-70 Min	MB81C86-70 Max	Unit
Read Cycle Time	TAVAX	55		70		ns
Address Access Time	TAVQV		55		70	ns
$\overline{E}$ Access Time	TELQV		55		70	ns
Output Hold from Address Change	TAXQX	5		5		ns
Output Hold from $\overline{E}$	TEXQX	5		5		ns
Chip Selection to Output Low-Z	TELQX	10		10		ns
Chip Deselection to Output High-Z	TEHQZ	5	25	5	25	ns
Power Up from $\overline{E}$	TELIH	0		0		ns
Power Down from $\overline{E}$	TEHIL		40		40	ns

Timing Diagrams (Note 1)

Read Cycle I: Address Controlled (Note 3)



Read Cycle II: $\overline{E}$ Controlled (Note 4)



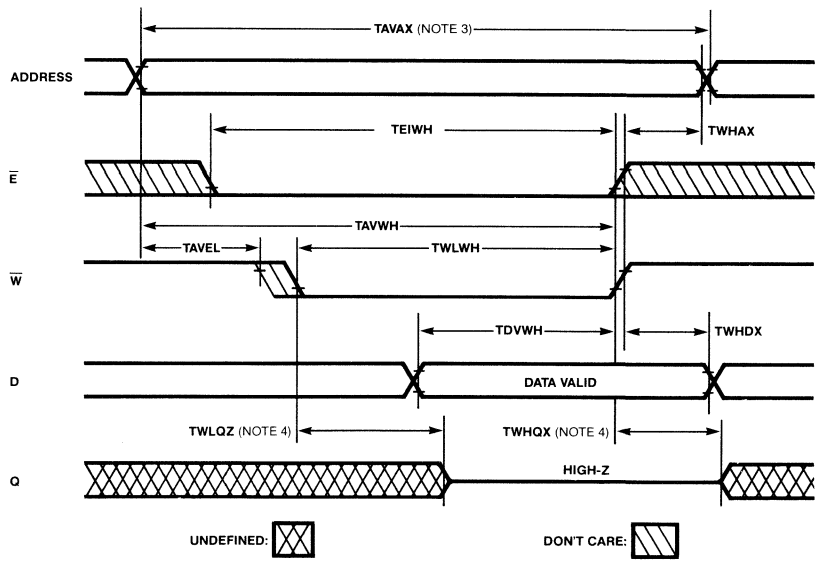
Notes:
1. $\overline{W}$ is high for Read Cycle.
2. All Read Cycle timings are referenced form the last valid address to the first transitioning address.
3. Device is continuously selected, $\overline{E} = V_{IL}$
4. Address valid prior to/or coincident with $\overline{E}$ transition low.
5. Transition is measured ±500 mV from steady state voltage with specified load in Fig. II.

Timing Diagrams (Note 1,2)
(Continued)

Write Cycle

Parameter	Symbol	MB81C86-55 Min	MB81C86-55 Max	MB81C86-70 Min	MB81C86-70 Max	Unit
Write Cycle Time	TAVAX	55		70		ns
Address Valid to End of Write	TAVWH	45		50		ns
Chip Select to End of Write	TEIWH	45		50		ns
Data Valid to End of Write	TDVWH	25		30		ns
Data Hold Time	TWHDX	5		5		ns
Write Pulse Width	TWLWH	30		35		ns
Address Setup Time	TAVWL	5		5		ns
Write Recovery Time	TEHAX	5		5		ns
Output High-Z from $\overline{W}$	TWLQZ	0	25	0	25	ns
Output Low-Z from $\overline{W}$	TWHQX	5	30	5	35	ns

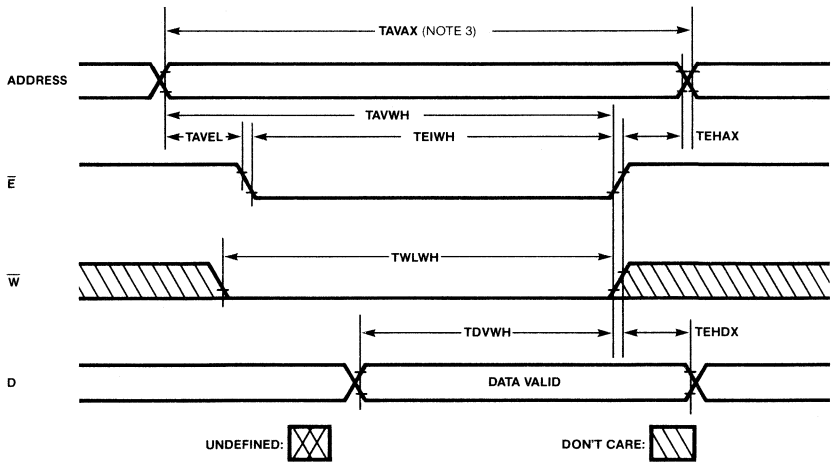
Write Cycle I $\overline{W}$ Controlled



Notes:
1. $\overline{E}$ or $\overline{W}$ must be high during address transitions.
2. If $\overline{E}$ goes high simultaneously with $\overline{W}$ high, the output remains in high impedance state.
3. All Read cycle timings are referenced from the alst valid address to the first transitioning address.
4. Transition measured ±500mV from steady state voltage with specified load in Fig. II.

Timing Diagrams (Note 1,2)
(Continued)

Write Cycle II $\overline{E}$ Controlled

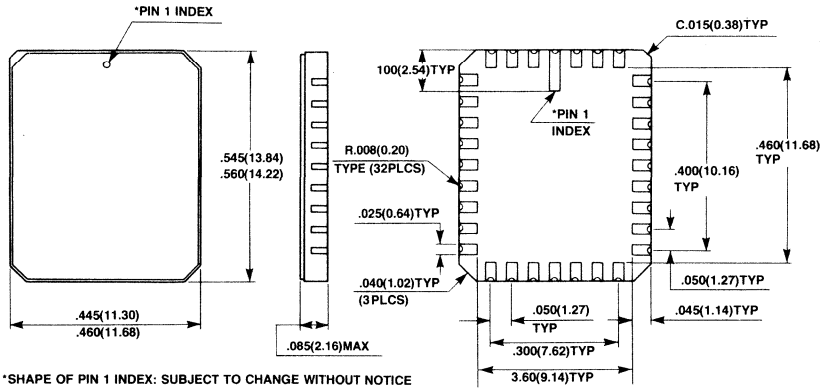


Notes:
1. $\overline{E}$ or $\overline{W}$ must be high during address transitions.
2. If $\overline{E}$ goes high simultaneously with $\overline{W}$ high, the output remains in high impedance state.
3. All Read cycle timings are referenced from the alst valid address to the first transitioning address.

Package Dimensions

Dimensions in inches
(millimeters)

32-Pad Ceramic (Metal Seal) Leadless Chip Carrier
(Case No.: LCC-32C-A02)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

FUJITSU
MICROELECTRONICS, INC.

MB8416-20
MB8416-20L

CMOS 16384-BIT STATIC RANDOM ACCESS MEMORY

DESCRIPTION

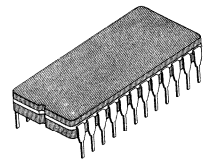
The Fujitsu MB8416 is a 2048 word by 8-bit static random access memory fabricated with high density, high reliability Complementary MOS silicon-gate technology.

The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All input and output pins are TTL-compatible, and a single 5 volt power supply is used. It is possible to retain data at low power supply voltage.

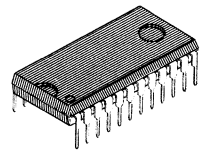
The MB8416 can be optimized for high performance applications such as microcomputer systems where fast access time and ease of use are required. Output Enable ($\overline{G}$) input permits the disable of all outputs when outputs are OR-tied. The MB8416 is packaged in an industry standard 24-pin dual in-line package, or 32-pin leadless chip carrier.

FEATURES

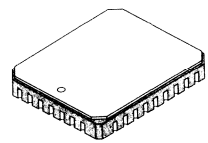
- **Extended temperature range: MB8416-20: −40° to +85°C MB8416-20-L: −40° to +70°C**
- **Organized as 2048 words by 8-bits**
- **Fast Access Time: 200 ns Max.**
- **Low Standby Power: MB8416-20: 55 μW MB8416-20L: 5.5 μW**
- **Completely Static Operation, no clocks required**
- **Single +5 Volt Power Supply**
- **TTL Compatible Inputs/Outputs**
- **Low Data Retention Voltage: 2.0V Min.**
- **Pin compatible with HM6116, TC5517 and μPD446**



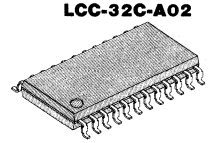
CERDIP PACKAGE DIP-24C-C03



PLASTIC PACKAGE DIP-24P-M02

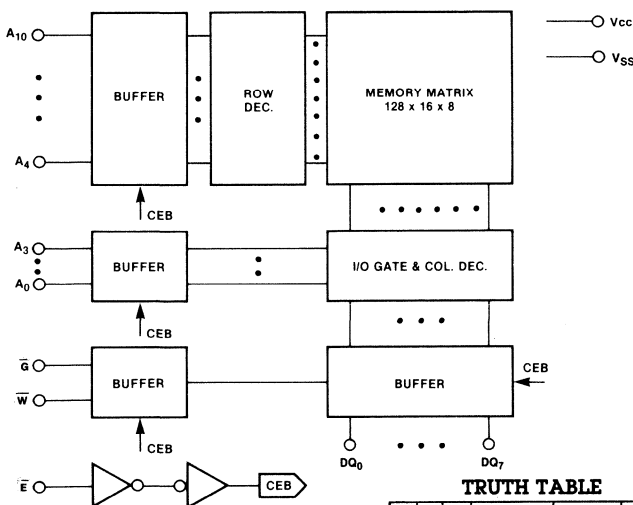


LEADLESS CHIP CARRIER LCC-32C-A02



PLASTIC FLAT PACKAGE FPT-24P-M02

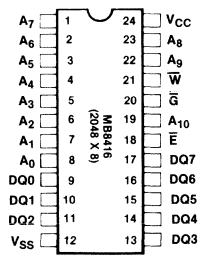
MB8416 BLOCK DIAGRAM

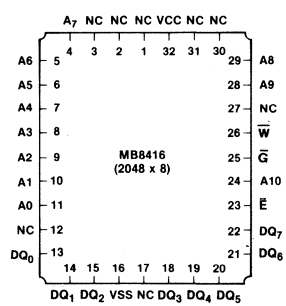


TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	Not Selected	I_{SB}	High-Z
L	H	H	D_{OUT} Disable	I_{CC}	High-Z
L	L	H	Read	I_{CC}	D_{OUT}
L	X	L	Write	I_{CC}	D_{IN}

PIN ASSIGNMENTS





ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Unit
Storage Temperature	Cerdip	T_{stg}	−65	150	°C
	Plastic		−40	125	
Temperature Under Bias		T_{bias}	−40	85	°C
Supply Voltage		V_{CC}	−0.5	8.0	V
Input Voltage		V_{IN}	−0.5	V_{CC} + 0.5	V
Input/Output Voltage		$V_{I/O}$	−0.5	V_{CC} + 0.5	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS} = 0V)

Parameter	Symbol		MB8416 Min	MB8416 Typ	MB8416 Max	Unit
Ambient Temperature	T_A	MB8416-20L	−40	—	+70	°C
		MB8416-20	−40	—	+85	
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Input High Voltage	V_{IH}		2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		−0.3	—	0.8	V

CAPACITANCE

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit	Condition
Input Capacitance	C_{IN}	—	7	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

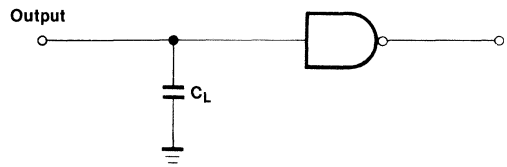
STATIC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Parameter	Condition	Symbol		Min	Max	Units
Standby Supply Current	$\bar{E} = V_{CC} - 0.2$ to $V_{CC} + 0.2V$ $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	I_{SB1}	MB8416-20L	—	1	μA
			MB8416-20	—	10	
Standby Supply Current	$\bar{E} = V_{IH}$ $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	I_{SB2}		—	2	mA
Active Supply Current	$\bar{E} = V_{IL}$ $V_{IN} = V_{IL}$ or V_{IH}; $I_{OUT} = 0$	I_{CC1}		—	60	mA
Operating Supply Current	Cycle = Min, Duty = 100% $I_{OUT} = 0$	I_{CC2}		—	60	mA
Input Leakage Current	V_{IN} = 0V to V_{CC}	I_{LI}		−1.0	1.0	μA
Output Leakage Current	$V_{I/O}$ = 0V to V_{CC} $\bar{E} = V_{IH}$	I_{LO}		−1.0	1.0	μA
Output High Voltage	I_{OUT} = −1.0 mA	V_{OH}		2.4	—	V
Output Low Voltage	I_{OUT} = 4.0 mA	V_{OL}		—	0.4	V

AC TEST CONDITIONS

Input Pulse Levels:	**0.6V to 2.4V**
Input Pulse Rise and Fall Times:	**10 ns**
Input Timing Reference Level:	**0.8V to 2.2V**
Output Timing Reference Level:	**0.8V to 2.2V**
Output Load:	**1 TTL Gate and C_L = 100 pF for all others.**



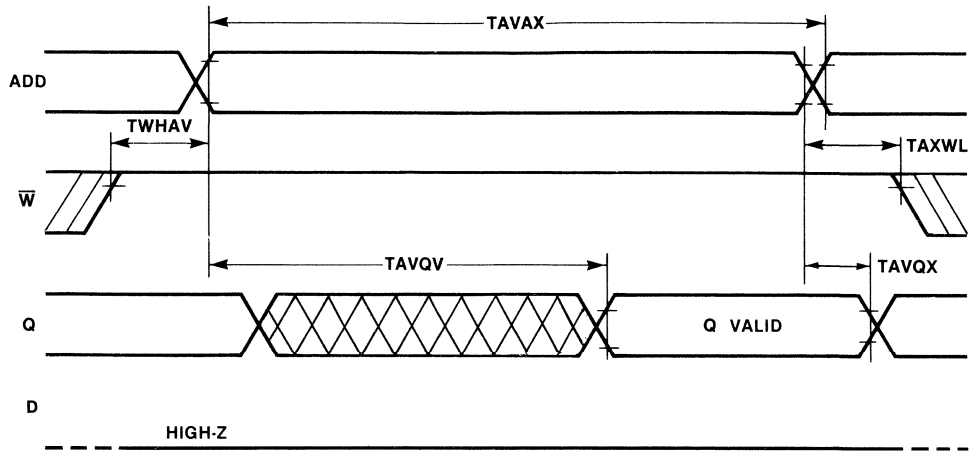
DYNAMIC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	TAVAX	200	—	ns
Write Cycle Time	TAVAX	200	—	ns
Address Access Time	TAVQV	—	200	ns
Chip Enable Access Time	TELQV	—	200	ns
Output Hold from Address Change	TAVQX	15	—	ns
Output Low Z from $\overline{E}$	TELQX	15	—	ns
Output High Z from $\overline{E}$	TEHQZ	—	60	ns
Output Low Z from $\overline{G}$	TGLQX	15	—	ns
Output High Z from $\overline{G}$	TGHQZ	—	60	ns
Output Low Z from $\overline{W}$	TWHQX	15	—	ns
Output High Z from $\overline{W}$	TWLQZ	—	60	ns
Output Enable to Output Valid	TGLQV	—	100	ns
Address Set Up Time	TAVEL, TAVWL	0	—	ns
Read Set Up Time	TWHEL, TWHAV	0	—	ns
Read Hold Time	TAXWL, TEHWL	0	—	ns
Write Set Up Time	TWLEL	0	—	ns
Write Hold Time	TEHWH	0	—	ns
Address Valid to End of Write	TAVWH	160	—	ns
Chip Enable to End of Write	TELEH	160	—	ns
Write Pulse Width	TWLWH	140	—	ns
Write Recovery Time	TWHAX, TEHAX	10	—	ns
Data Set Up Time	TDVEH, TDVWH	60	—	ns
Data Hold Time	TWHDX, TEHDX	0	—	ns

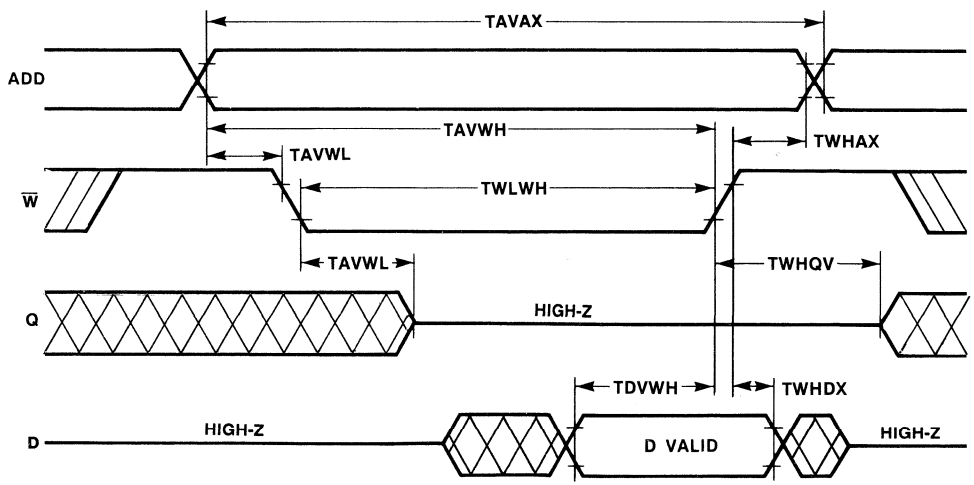
WAVEFORMS

MODE 1: $\overline{W}$ Controlled: ($\overline{E}$ = Low, $\overline{G}$ = Low)

Read Cycle



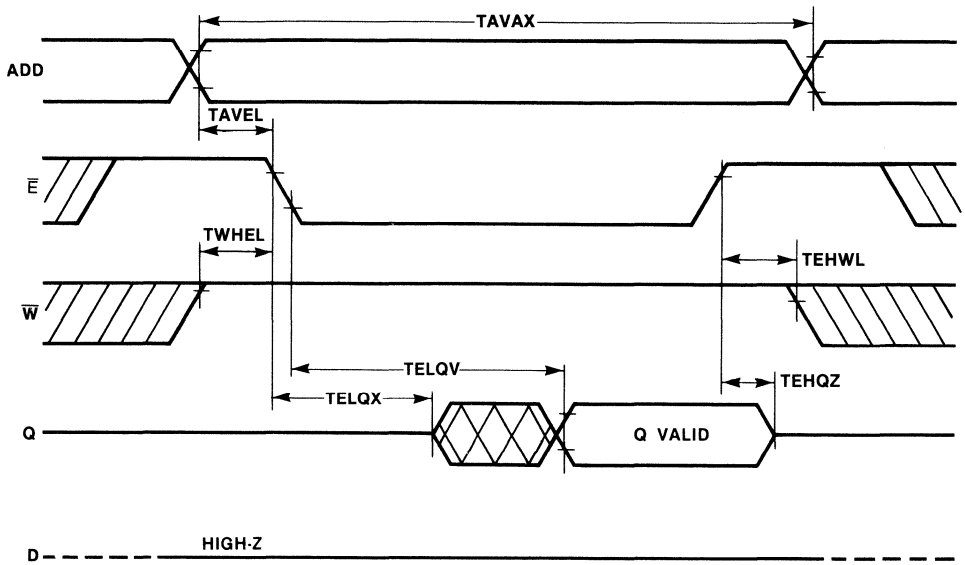
Write Cycle



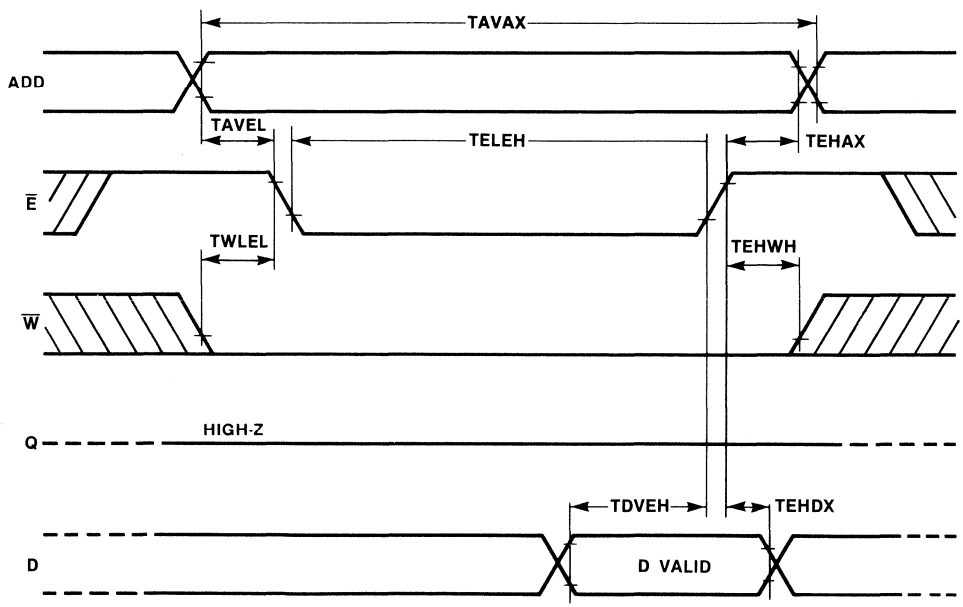
WAVEFORMS (Continued)

MODE 2: $\overline{E}$ Controlled, ($\overline{G}$ = Low)

Read Cycle



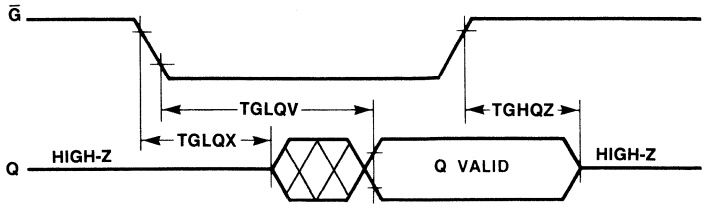
Write Cycle



WAVEFORMS (Continued)

Enable/Disable $\overline{G}$ Controlled; ($\overline{E}$ = Low, $\overline{W}$ = High)

Read Cycle



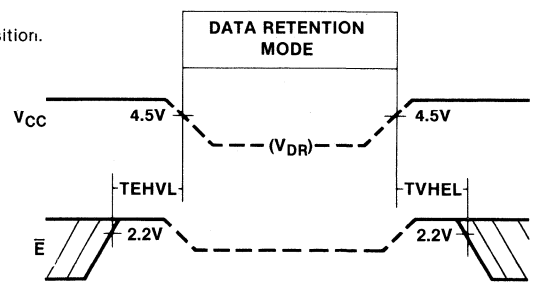
DYNAMIC CHARACTERISTICS

Data Retention Characteristics, NOTES 1, 2, 3 (Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol		Min	Max	Unit
Data Retention Supply Voltage	1	VDR		2.0	5.5	V
Data Retention Supply Current	2	IDR	MB8416-20	—	10	μA
			MB8416-20L	—	1	μA
Data Retention Set Up Time	3	TEHVCL		0	—	ns
Recovery Time	3	TVHEL		60	—	ns

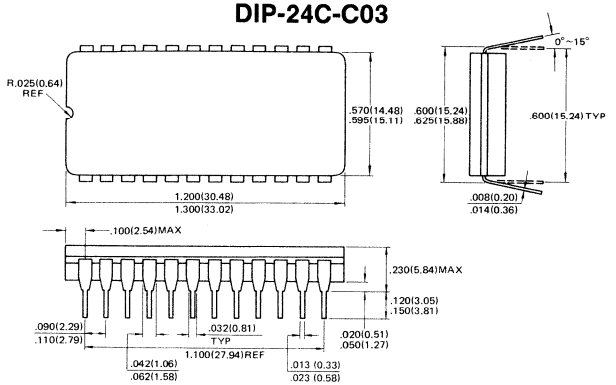
NOTES:

1. $\overline{E}$ = 2.2V to VDR + 0.3V when VDR = 2.5V to 5.5V
   $\overline{E}$ = VDR ± 0.3V when VDR = 2.0 to 2.5V.
2. V_{CC} = VDR = 2.0V, $\overline{E}$ = VDR ± 0.2V V_{IN} = −0.2V to VDR + 0.2V.
3. V_L = 4.5V on the falling transition, V_H = 4.5V on the rising transition.

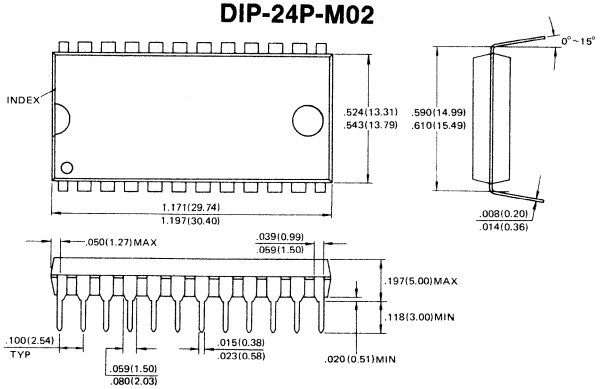


PACKAGE DIMENSIONS Dimensions in inches (millimeters)

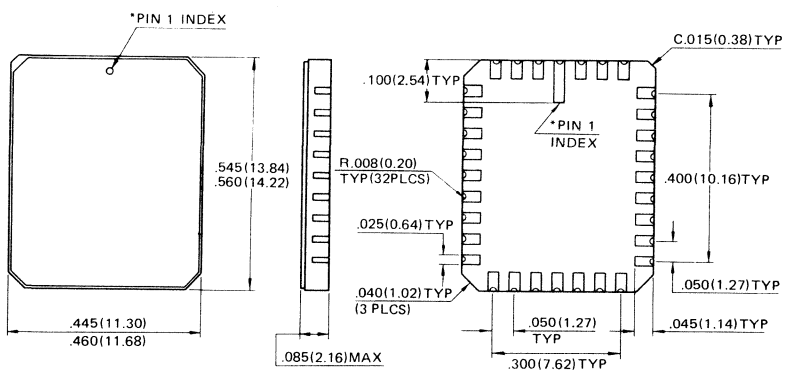
24-LEAD CERDIP DUAL IN-LINE PACKAGE
DIP-24C-C03



24-LEAD PLASTIC DUAL IN-LINE PACKAGE
DIP-24P-M02

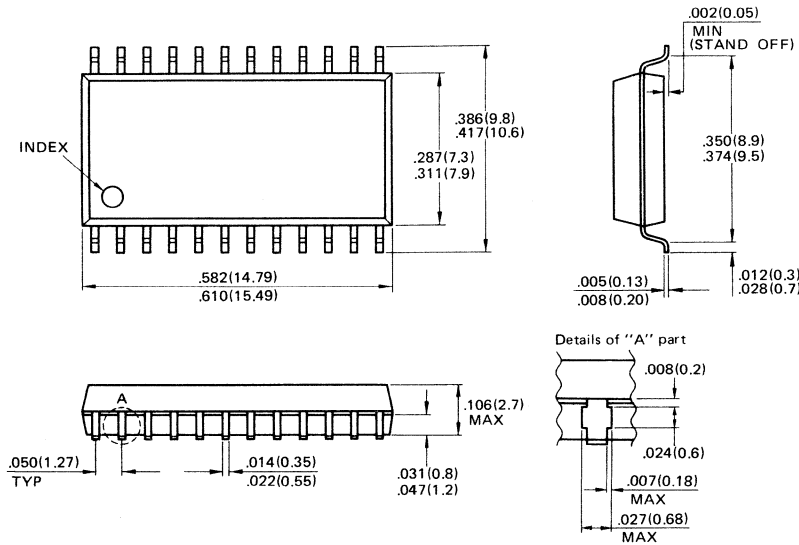


32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
LCC-32-A02



PACKAGE DIMENSIONS Dimensions in inches (millimeters) (Continued)

24-LEAD PLASTIC FLAT PACKAGE
FPT-24P-M02



FUJITSU

■ MB8416A-12, MB8416A-12L, MB8416A-15, MB8416A-15L

CMOS 16,384-Bit Static Random Access Memory

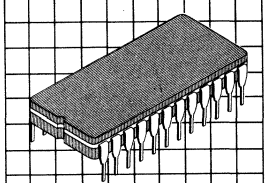
Description

The Fujitsu MB8416A is a 2048-word by 8-bit static random access memory fabricated with CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single 5 volt power supply is required.

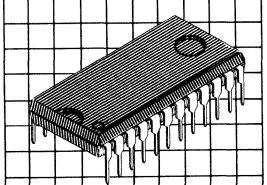
The MB8416A is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost, and high performance.

Features

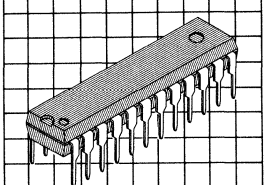
- **Organization: 2048 words x 8-bits**
- **Fast Access Time:**
  120 ns max. (MB8416A-12/12L)
  150 ns max. (MB8416A-15/15L)
- **Completely static operation: No clocks required**
- **TTL compatible inputs/outputs**
- **Three-state output**
- **Common data input/output**
- **Single +5V power supply**
- **Low power standby:**
  5.5 mW max. (MB8416A-12/15)
  275μW max. (MB8416A-12L/15L)
- **Data retention: 2.0V min.**
- **Jedec Standard 24-pin DIP (Ceramic Cerdip/Plastic Mold)**
- **Pin compatible with HM6116, TC5517 and μPD446**
- **Output Enable ($\overline{G}$) pin for precise data bus control**



Ceramic Package(Cerdip)
DIP-24C-C03

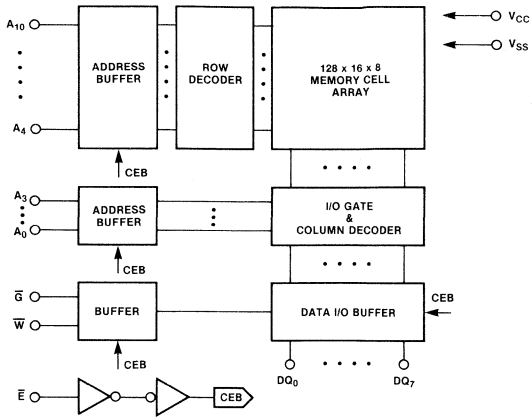


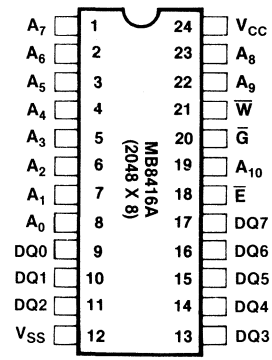
Plastic Package
DIP-24P-M02



Plastic Package
DIP-24P-M03

MB8416A Block Diagram and Pin Assignment





Truth Table

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	I_{SB}	High-Z
L	H	H	D_{OUT} Disable	I_{CC}	High-Z
L	L	H	Read	I_{CC}	D_{OUT}
L	X	L	Write	I_{CC}	D_{IN}

Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Storage Temperature	Cerdip	T_{stg}	−65 to +150	°C
	Plastic		−45 to +125	
Temperature Under Bias		T_{bias}	−10 to +85	°C
Supply Voltage		V_{CC}	−0.5 to +7.0	V
Input Voltage		V_{IN}	−0.5 to V_{CC} + 0.5	V
Input/Output Voltage		$V_{I/O}$	−0.5 to V_{CC} + 0.5	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$	—	—	10	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}	—	—	7	pF

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Ambient Temperature	T_A	0	—	70	°C

DC Characteristics

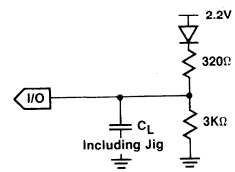
(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol	MB8416A-12/15 Min	MB8416A-12/15 Max	MB8416A-12L/15L Min	MB8416A-12L/15L Max	Unit
Standby Supply Current 1	$\overline{E} = V_{CC} - 0.2$ to $V_{CC} + 0.2V$, $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	I_{SB1}	—	1	—	0.05	mA
Standby Supply Current 2	$\overline{E} = V_{IH}$, $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	I_{SB2}	—	2	—	1	mA
Active Supply Current	$\overline{E} = V_{IL}$ $V_{IN} = V_{IL}$ or V_{IH}; $I_{OUT} = 0$	I_{CC1}	—	60	—	60	mA
Operating Supply Current	Cycle = Min, Duty = 100% $I_{OUT} = 0$	I_{CC2}	—	60	—	60	mA
Input Leakage Current	$V_{IN} = 0V$ to V_{CC}	I_{LI}	−1.0	1.0	−1.0	1.0	μA
Output Leakage Current	$V_{I/O} = 0V$ to V_{CC} $\overline{E} = V_{IH}$ or $\overline{G} = V_{IH}$	I_{LO}	−1.0	1.0	−1.0	1.0	μA
Output High Voltage	$I_{OUT} = -1.0$ mA	V_{OH}	2.4	—	2.4	—	V
Output Low Voltage	$I_{OUT} = 4.0$ mA	V_{OL}	—	0.4	—	0.4	V

Note: All voltages are referenced to GND.

AC Test Conditions

Input Pulse Levels: 0.6V to 2.4V
Input Pulse Rise and Fall Times: 5ns
(Transient Time between 0.8V and 2.2V)
Timing Reference Levels: Input: $V_{IL} = 0.8V$, $V_{IH} = 2.2V$
Output: $V_{OL} = 0.8V$, $V_{OH} = 2.2V$
Output Load: $C_L = 5_{PF}$ for TEHQZ, TGHQZ and TWHQZ
$C_L = 100$ pF for all others.



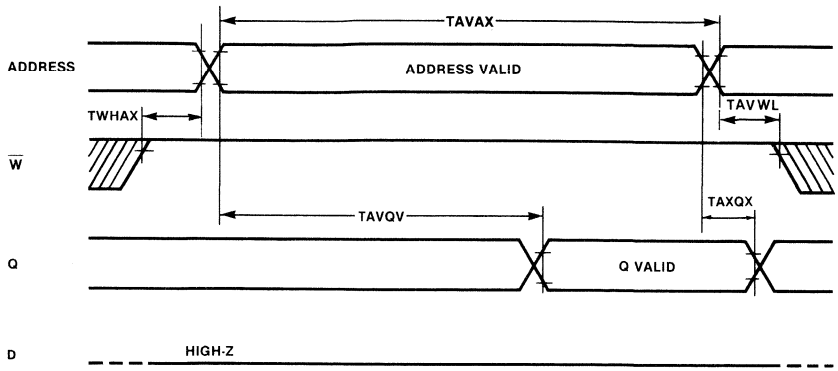
AC Characteristics

(Recommended operating conditions unless otherwise noted.)

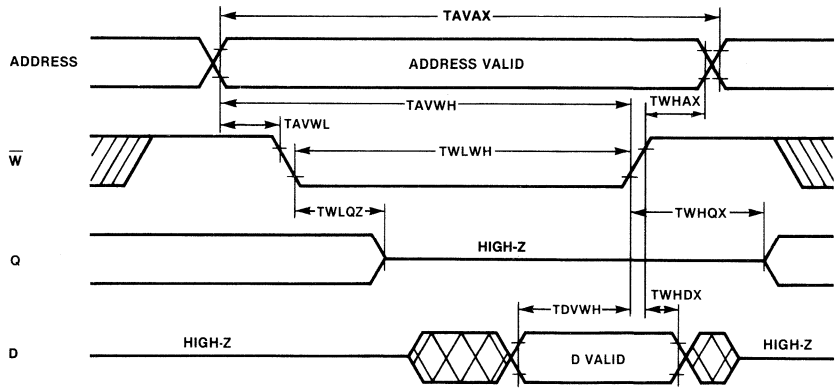
Parameter	Symbol	MB8416A-12/12L Min	MB8416A-12/12L Max	MB8416A-15/15L Min	MB8416A-15/15L Max	Unit
Read Cycle Time	TAVAX	120	—	150	—	ns
Write Cycle Time	TAVAX	120	—	150	—	ns
Address Access Time	TAVQV	—	120	—	150	ns
Chip Enable Access Time	TELQV	—	120	—	150	ns
Output Hold from Address Change	TAXQX	15	—	15	—	ns
Output Low Z from $\overline{E}$	TELQX	15	—	15	—	ns
Output High Z from $\overline{E}$	TEHQZ	—	40	—	50	ns
Output Low Z from $\overline{G}$	TGLQX	10	—	10	—	ns
Output High Z from $\overline{G}$	TGHQZ	—	40	—	50	ns
Output Low Z from $\overline{W}$	TWHQX	15	—	15	—	ns
Output High Z from $\overline{W}$	TWLQZ	—	40	—	50	ns
Output Enable to Output Valid	TGLQV	—	50	—	60	ns
Address Set Up Time	TAVEL, TAVWL	0	—	0	—	ns
Read Set Up Time	TWHEL, TWHAV	0	—	0	—	ns
Read Hold Time	TAXWL, TEHWL	0	—	0	—	ns
Write Set Up Time	TWLEL	0	—	0	—	ns
Write Hold Time	TEHWH	0	—	0	—	ns
Address Valid to End of Write	TAVWH	100	—	120	—	ns
Chip Enabled to End of Write	TELEH	100	—	120	—	ns
Write Pulse Width	TWLWH	70	—	90	—	ns
Write Recovery Time	TWHAX, TEHAX	5	—	5	—	ns
Data Set Up Time	TDVEH, TDVWH	35	—	40	—	ns
Data Hold Time	TWHDX, TEHDX	0	—	0	—	ns

Mode 1 — $\overline{W}$ Controlled
($\overline{E}$ = Low, $\overline{G}$ = Low)

Read Cycle Timing Diagram

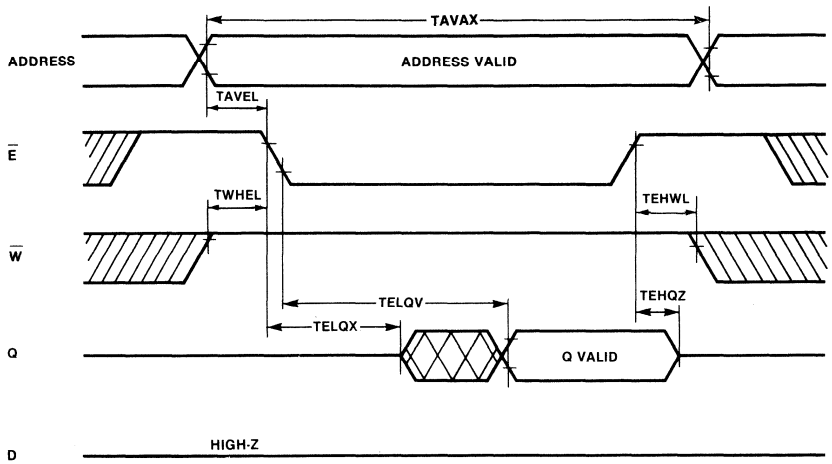


Write Cycle Timing Diagram

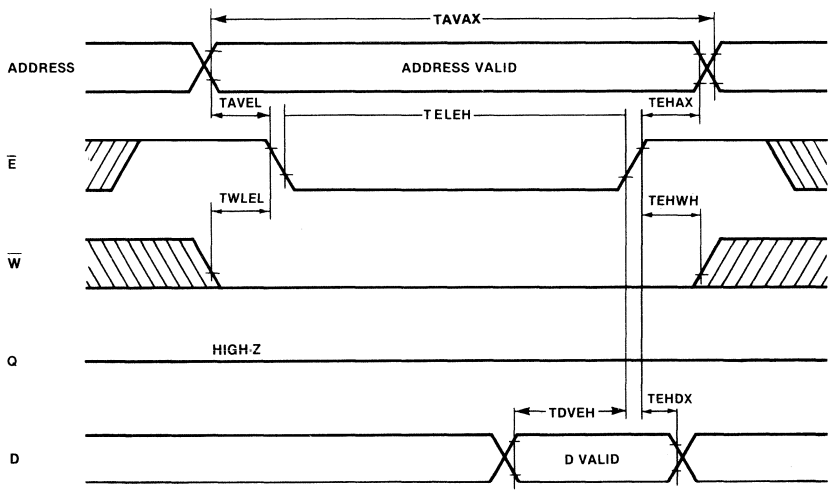


Mode 2 — $\overline{E}$ Controlled
($\overline{G}$ = Low)

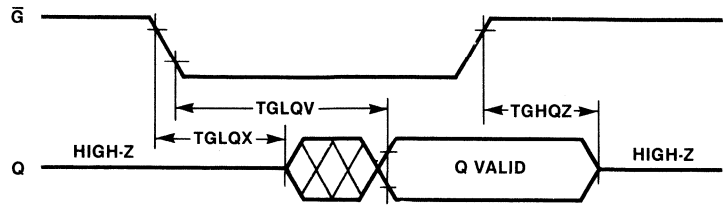
Read Cycle Timing Diagram



Write Cycle Timing Diagram



Mode 3 — $\overline{G}$ Controlled
($\overline{E}$ = Low, $\overline{W}$ = High, Address Valid)

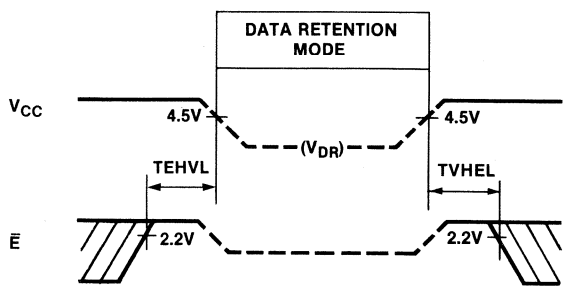


Data Retention Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8416A-12/15 Min	MB8416A-12/15 Max	MB8416A-12L/15L Min	MB8416A-12L/15L Max	Unit	Test Condition
Data Retention Supply Voltage	V_{DR}	2.0	5.5	2.0	5.5	V	Note 1
Data Retention Supply Current	I_{DR}	—	0.5	—	0.03	mA	Note 2
Data Retention Set Up Time	TEHVL	0	—	0	—	ns	Note 3
Recovery Time	TVHEL	40	—	40	—	ns	Note 3

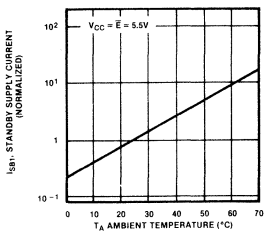
Note 1. $\overline{E}$ = 2.2V to VDR + 0.3V when VDR = 2.5V to 5.5V, $\overline{E}$ = VDR ± 0.3V when VDR = 2.0 to 2.5V.
Note 2. $V_{CC} = V_{DR}$ = 3.0V, $\overline{E} = V_{DR} - 0.2V$ to $V_{DR} + 0.2V$, $V_{IN} = -0.2V$ to $V_{DR} + 0.2V$.
Note 3. V_L = 4.5V on the falling transition, V_H = 4.5V on the rising transition.

Data Retention Timing Diagram

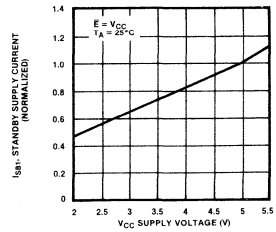


Typical Characteristics Curves

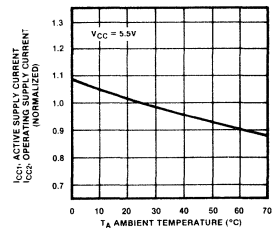
Standby Supply Current vs. Ambient Temp



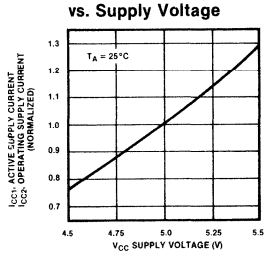
Standby Supply Current vs. Supply Voltage



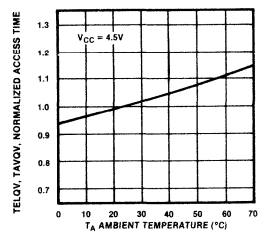
Supply Current (Active/Operating) vs. Ambient Temp



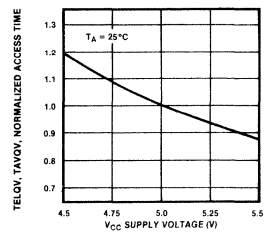
Supply Current (Active/Operating) vs. Supply Voltage



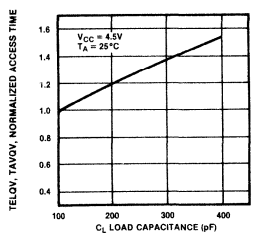
Access Times vs. Ambient Temp



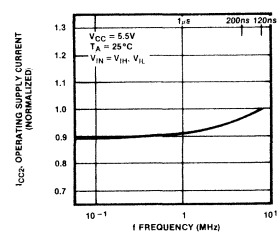
Access Times vs. Supply Voltage



Access Times vs. Load Capacitance

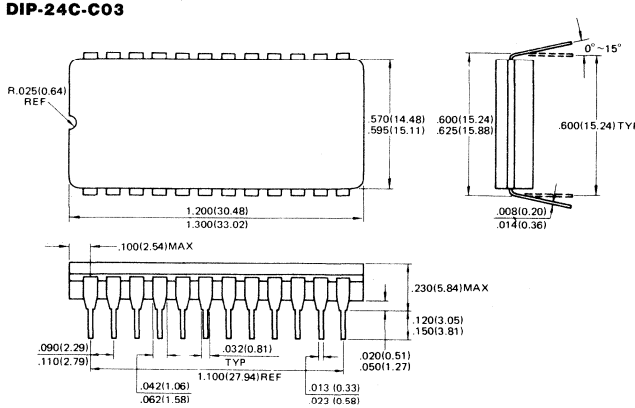


Supply Current vs. Frequency

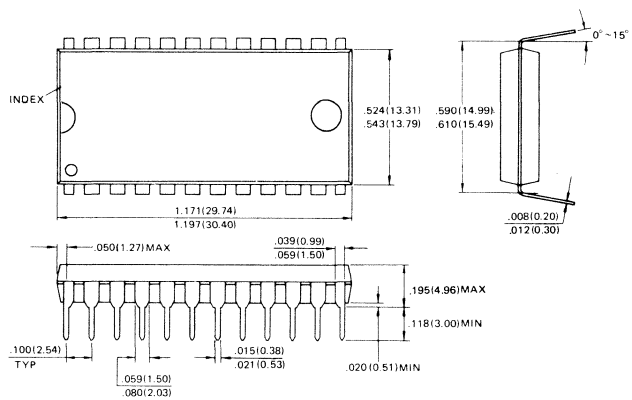


Package Dimensions
Dimensions in inches
(millimeters)

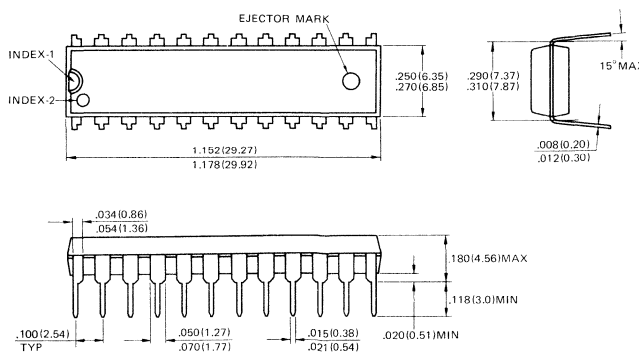
24-Lead Ceramic (Cerdip)
Dual In-Line Package
DIP-24C-C03



24-Lead Plastic
Dual In-Line Package
DIP-24P-M02



24-Lead Plastic
Dual In-Line Package
DIP-24P-M03



FUJITSU

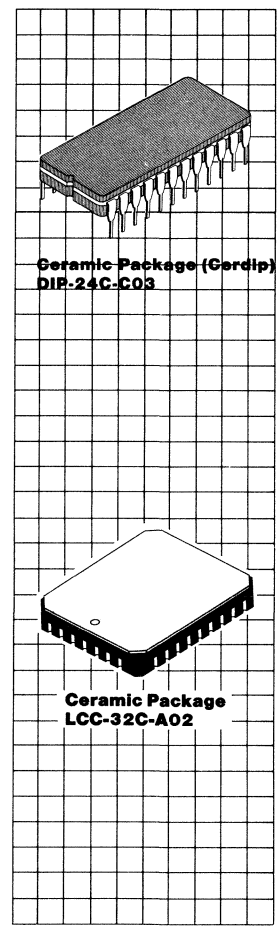
■ MB8416-25-W

CMOS 16,384-Bit Static Random Access Memory

Description

The Fujitsu MB8416 is a 2048-word by 8-bit static random access memory fabricated with a CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL-compatible, and a single 5 volt power supply is required.

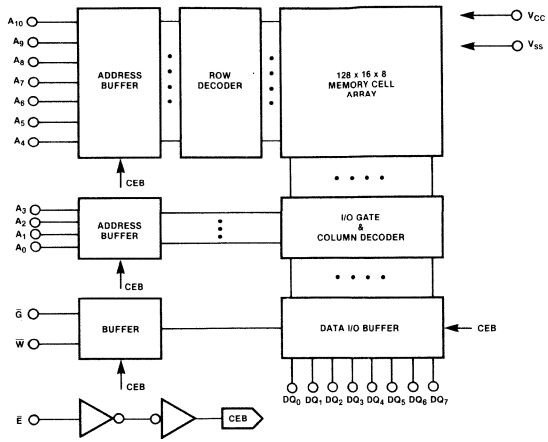
The MB8416 is ideally suited for use in microcomputer systems and other applications where fast access time and ease of use are required. This device offers the advantages of low power dissipation, low cost, and high performance.

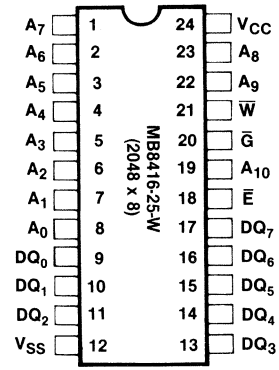


Features

- Organized as 2048 words x 8 bits
- Fast Access Time: 250 ns max.
- Completely static operation: No clock required
- TTL compatible input/output
- Three-state output
- Common data input/output
- Single +5 V power supply
- Low standby power
- Data retention: 2.0 V min.
- Standard 24-pin DIP (Ceramic Cerdip)
- Standard 32-pad leadless chip carrier
- Wide Temperature Range: $T_A = -55°C$ to $+125°C$

MB8416 Block Diagram and Pin Assignment





Functions and Pin Connections

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	Supply Current	DQ Pin	A_{IN}	V_{CC}	GND
Standby	H	X	X	I_{SB}	High-Z	Don't Care	V_{CC}	V_{SS}
Output Disable	L	H	H	I_{CC}	High-Z	Don't Care	V_{CC}	V_{SS}
Read	L	L	H	I_{CC}	D_{OUT}	A_{IN}	V_{CC}	V_{SS}
Write	L	X	L	I_{CC}	D_{IN}	A_{IN}	V_{CC}	V_{SS}
Data Retention	H	X	X	IDR	High-Z	Don't Care	V_{DR}	V_{SS}

Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Storage Temperature Range	Ceramic	T_{stg}	−65 to +150	°C
Temperature Under Bias		T_{bias}	−55 to +125	°C
Supply Voltage		V_{CC}	−0.5 to +8.0	V
Input Voltage		V_{IN}	−0.5 to V_{CC} + 0.5	V
Output Voltage		V_{OUT}	−0.5 to V_{CC} + 0.5	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

Capacitance
(T_A = 25 °C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$	—	—	10	pF
Input Capacitance ($V_{I/O}$ = 0V)	C_{IN}	—	—	7	pF

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−0.3	—	0.7	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Ambient Temperature	T_A	−55	—	125	°C

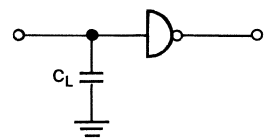
DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby Supply Current	I_{SB1}		300	μA	$\overline{E} = V_{CC} - 0.2V$ to $V_{CC} + 0.2V$, $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$
	I_{SB2}		2	mA	$\overline{E} = V_{IH}$, $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$
Active Supply Current	I_{CC1}		65	mA	$\overline{E} = V_{IL}$, $V_{IN} = V_{IL}$ or V_{IH}, $I_{OUT} = 0$
Operating Supply Current	I_{CC2}		65	mA	Cycle = Min, Duty = 100%, $I_{OUT} = 0$
Input Leakage Current	I_{LI}	−5	5	μA	$V_{IN} = 0V$ to V_{CC}
Output Leakage Current	I_{LO}	−5	5	μA	$V_{I/O} = 0V$ to V_{CC}, $\overline{E} = V_{IH}$
Output High Voltage	V_{OH}	2.4		V	$I_{OUT} = -1.0$ mA
Output Low Voltage	V_{OL}		0.45	V	$I_{OUT} = 4.0$ mA

Note: All voltages are referenced to V_{SS}.

AC Test Conditions

Input Pulse Levels: 0.6 V to 2.4 V
Input Pulse Rise and Fall Times: 10 ns (Transient Time between 0.8 V and 2.2 V)
Timing Reference Levels: Input: $V_{IL} = 0.8$ V, $V_{IH} = 2.2$ V
Output: $V_{OL} = 0.8$ V, $V_{OH} = 2.2$ V
Output Load: 1 TTL Gate and $C_L = 100$ pF for all AC parameters except TEHQZ and TWLQZ, TGHQZ
$C_L = 5$pF for TEHQZ, TWLQZ and TGHQZ

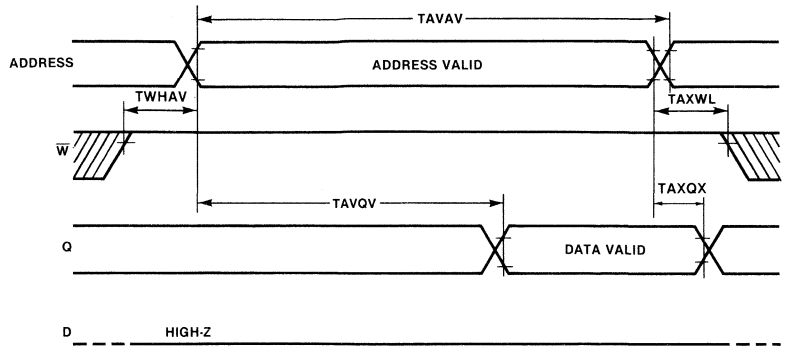


AC Characteristics
(Recommended operating conditions unless otherwise noted.)

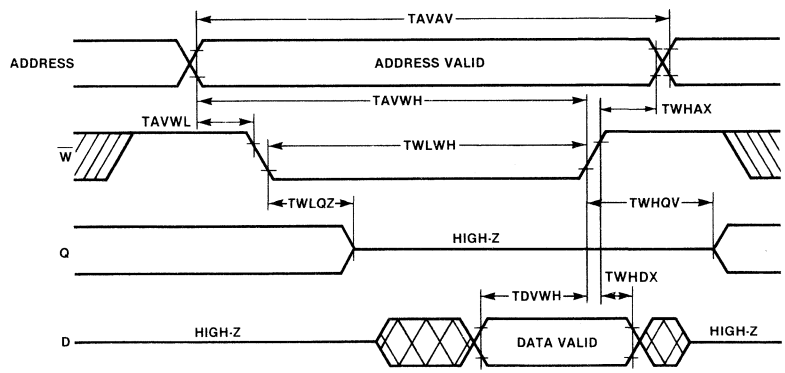
Parameter	Symbol	Min	Max	Unit
Read Cycle Time	TAVAX	250		ns
Write Cycle Time	TAVAX	250		ns
Address Access Time	TAVQV		250	ns
Chip Select Access Time	TELQV		250	ns
Output Hold from Address Change	TAXQX	15		ns
Output Low Z from $\overline{E}$	TELQX	15		ns
Output High Z from $\overline{E}$	TEHQZ		70	ns
Output Low Z from $\overline{G}$	TGLQX	15		ns
Output High Z from $\overline{G}$	TGHQZ		70	ns
Output Low Z from $\overline{W}$	TWHQV	15		ns
Output High Z from $\overline{W}$	TWLQZ		70	ns
Output Enable to Output Valid	TGLQV		120	ns
Address Set Up Time	TAVEL/TAVWL	0		ns
Read Set Up Time	TWHEL/TWHAV	0		ns
Read Hold Time	TAXWL/TEHWL	0		ns
Write Set Up Time	TWLEL	0		ns
Write Hold Time	TEHWH	0		ns
Address Valid to End of Write	TAVWH	200		ns
Chip Selection to End of Write	TELEH	200		ns
Write Pulse Width	TWLWH	160		ns
Write Recovery Time	TWHAX/TEHAX	10		ns
Data Set Up Time	TDVEH/TDVWH	70		ns
Data Hold Time	TWHDX/TEHDX	0		ns

Mode 1 — $\overline{W}$ Controlled ($\overline{E}$ = Low, $\overline{G}$ = Low)

Read Cycle Timing Diagram

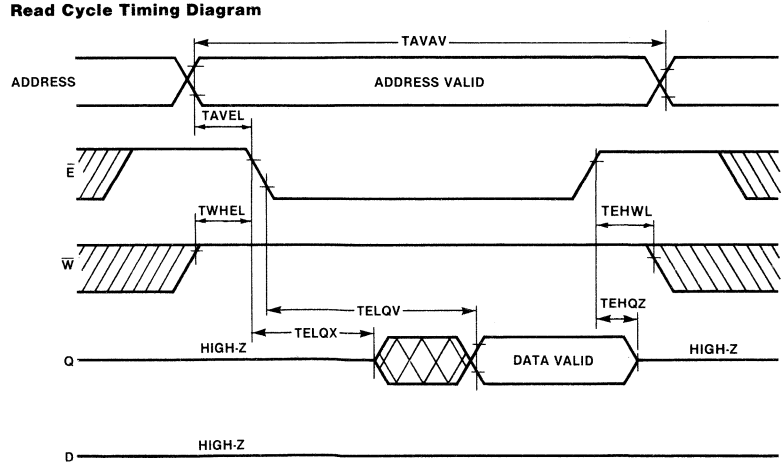


Write Cycle Timing Diagram



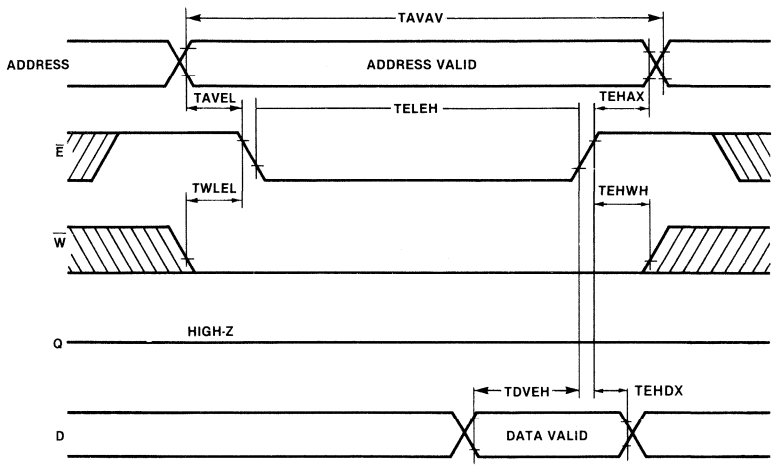
Mode 2 — $\overline{E}$ Controlled ($\overline{G}$ = Low)

Read Cycle Timing Diagram



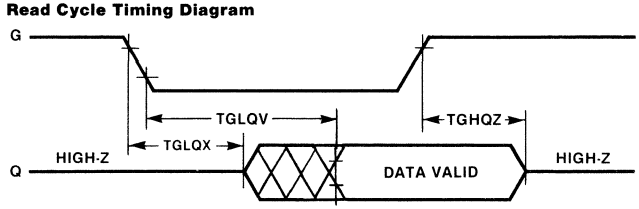
Mode 2 — $\overline{E}$ Controlled ($\overline{G}$ = Low), (continued)

Write Cycle Timing Diagram



Mode 3 — $\overline{G}$ Controlled ($\overline{E}$ = Low, $\overline{W}$ = High, ADDRESS VALID)

Read Cycle Timing Diagram

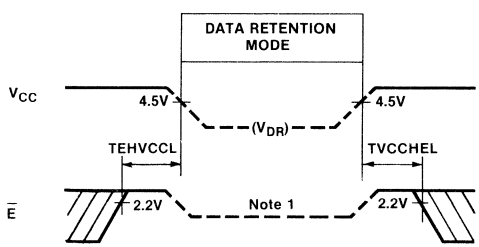


Data Retention Characteristics

Parameter	Symbol	Min	Max	Unit	Test Conditions
Data Retention Supply Voltage	VDR	2.0	5.5	V	Note 1
Data Retention Supply Current	IDR		300	μA	Note 2
Data Retention Set Up Time	TEHVCCL	0		ns	
Recovery Time	TVCCHEL	60		ns	

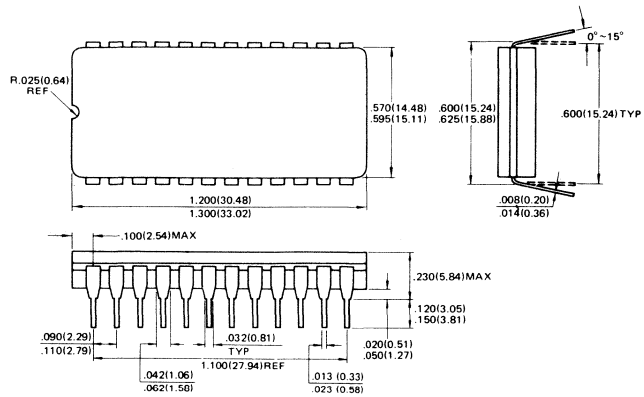
Note 1: $\overline{E}$ = 2.2V to VDR + 0.3V when VDR = 2.5V to 5.5V.
$\overline{E}$ = VDR ± 0.3V when VDR = 2.0 to 2.5V.
Note 2: V_{CC} = VDR, E = VDR ± 0.2V, V_{IN} = −0.2V to VDR + 0.2V.

Data Retention Timing Diagram

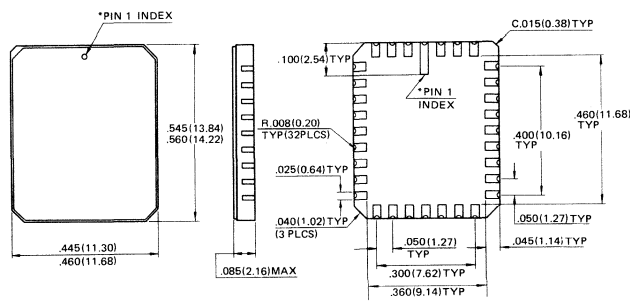


Package Dimensions
Dimensions in inches
(millimeters)

24-Lead Ceramic (Cerdip)
Dual In-Line Package
DIP-24C-C03



32-Pad Ceramic (Metal Seal)
Leadless Chip Carrier
LCC-32C-A02



*Shape of Pin 1 index : Subject to change without notice

FUJITSU
MICROELECTRONICS, INC.

MB8417-20
MB8417-20L

CMOS 16,384-BIT STATIC RANDOM ACCESS MEMORY

DESCRIPTION

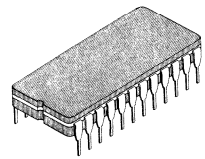
The Fujitsu MB8417 is a 2048 word by 8-bit static random access memory fabricated with high density, high reliability Complementary MOS silicon-gate technology.

The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All input and output pins are TTL-compatible, and a single 5 volt power supply is used. It is possible to retain data at low power supply voltage.

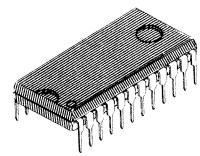
The MB8417 can be optimized for high performance applications such as microcomputer systems where fast access time and ease of use are required. Chip Select $\overline{E}^*$ permits the fast access time. The MB8417 is packaged in an industry standard 24-pin dual in-line package or 32-pin leadless chip carrier.

FEATURES

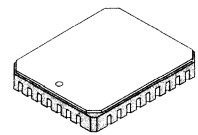
- **Extended temperature range:**
  MB8417-20: −40°C to +85°C
  MB8417-20L: −40°C to +70°C
- **Organized as 2048 words by 8-bits**
- **Fast Access Time:**
  200 ns Max. ($\overline{E}$ Controlled)
  100 ns Max. ($\overline{E}^*$ Controlled)
- **Low Standby Power:**
  MB8417-20: 55 μW
  MB8417-20L: 5.5 μW
- **Completely Static Operation, no clocks required**
- **Single +5 Volt Power Supply**
- **TTL Compatible Inputs/Outputs**
- **Low Data Retention Voltage: 2.0V Min.**
- **Pin compatible with TC5516 and μPD447**



CERDIP PACKAGE
DIP-24C-C03

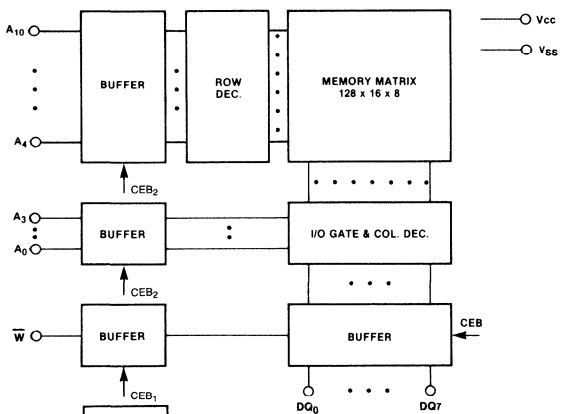


PLASTIC PACKAGE
DIP-24P-M02



LEADLESS CHIP CARRIER
LCC-32C-A02

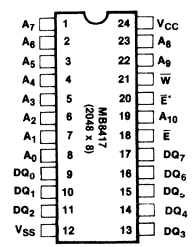
MB8417 BLOCK DIAGRAM

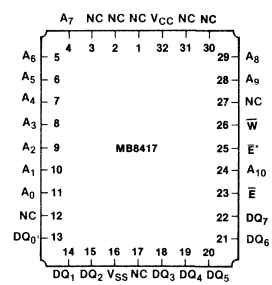


TRUTH TABLE

$\overline{E}$	$\overline{E}^*$	$\overline{W}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	Not Selected	I_{SB}	High-Z
L	H	X	Not Selected	I_{CC}	High-Z
L	L	H	Read	I_{CC}	D_{OUT}
L	L	L	Write	I_{CC}	D_{IN}

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Unit
Storage Temperature	Ceramic	T_{stg}	−65	150	°C
	Plastic		−45	125	
Temperature Under Bias		T_{bias}	−40	85	°C
Supply Voltage		V_{CC}	−0.5	8.0	V
Input Voltage		V_{IN}	−0.5	V_{CC} + 0.5	V
Input/Output Voltage		$V_{I/O}$	−0.5	V_{CC} + 0.5	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS, V_{SS} = GND

Parameter	Symbol		MB8417 Min	MB8417 Typ	MB8417 Max	Unit
Ambient Temperature	T_A	MB8417-20L	−40	—	+70	°C
		MB8417-20	−40	—	+85	
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Input High Voltage	V_{IH}		2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		−0.3	—	0.8	V

CAPACITANCE

(T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit	Condition
Input Capacitance	C_{IN}	—	7	pF	V_{IN} = 0V
Input / Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

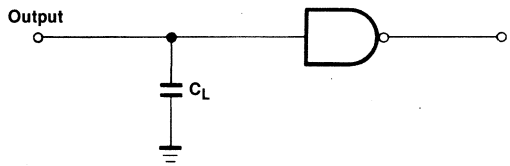
STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol		Min	Max	Units
Standby Supply Current	$\overline{E} = V_{CC} - 0.2V$ to V_{CC} + 0.2V V_{IN} = −0.2V to V_{CC} +0.2V	I_{SB1}	MB8417-20L	—	1	μA
			MB8417-20	—	10	
Standby Supply Current	$\overline{E} = V_{IH}$ V_{IN} = −0.2V to V_{CC} +0.2V	I_{SB2}		—	2	mA
Active Supply Current	$\overline{E} = V_{IL}$ $V_{IN} = V_{IL}$ or V_{IH}; I_{OUT} = 0	I_{CC1}		—	60	mA
Operating Supply Current	Cycle = Min, Duty = 100% I_{OUT} = 0	I_{CC2}		—	60	mA
Input Leakage Current	V_{IN} = 0V to V_{CC}	I_{LI}		−1.0	1.0	μA
Output Leakage Current	$V_{I/O}$ = 0V to V_{CC} $\overline{E} = V_{IH}$ or $\overline{E}^* = V_{IH}$	I_{LO}		−1.0	1.0	μA
Output High Voltage	I_{OUT} = −1.0 mA	V_{OH}		2.4	—	V
Output Low Voltage	I_{OUT} = 4.0 mA	V_{OL}		—	0.4	V

AC TEST CONDITIONS

Input Pulse Levels:	**0.6V to 2.4V**
Input Pulse Rise and Fall Times:	**10 ns**
Input Timing Reference Level:	**0.8V to 2.2V**
Output Timing Reference Level:	**0.8V to 2.2V**
Output Load:	**1 TTL Gate and C_L = 100 pF for all others.**



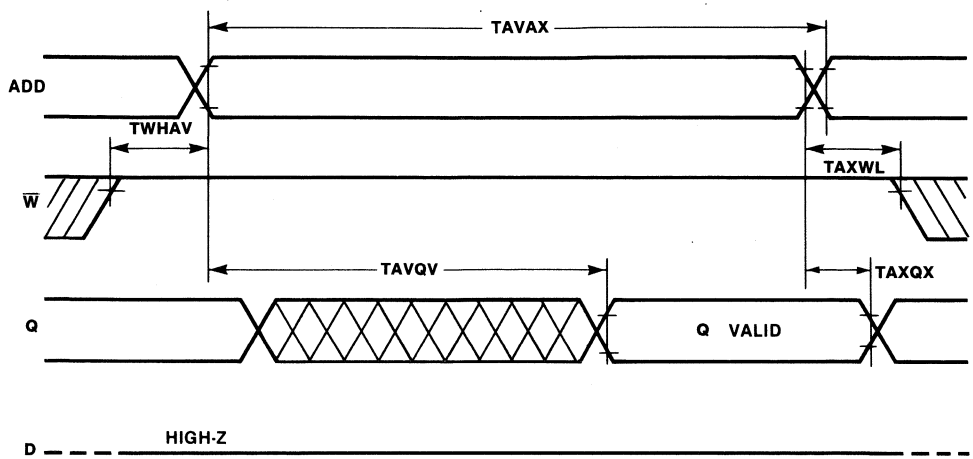
DYNAMIC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	TAVAX	200	—	ns
Write Cycle Time	TAVAX	200	—	ns
Address Access Time	TAVQV	—	200	ns
Chip Enable Access Time	TELQV	—	200	ns
Chip Select Access Time	TSLQV	—	100	ns
Output Hold from Address Change	TAXQX	15	—	ns
Output Low Z from $\overline{E}$ or $\overline{E}^*$	TELQX, TSLQX	15	—	ns
Output High Z from $\overline{E}$ or $\overline{E}^*$	TEHQZ, TSHQZ	—	60	ns
Output Low Z from $\overline{W}$	TWHQX	15	—	ns
Output High Z from $\overline{W}$	TWLQZ	—	60	ns
Address Set Up Time	TAVWL, TAVSL, TAVEL	0	—	ns
Read Set Up Time	TWHAV, TWHEL, TWHSL	0	—	ns
Read Hold Time	TEHWL, TAXWL, TSHWL	0	—	ns
Write Set Up Time	TWLSL, TWLEL	0	—	ns
Write Hold Time	TSHWH, TEHWH	0	—	ns
Address Valid to End of Write	TAVSH, TAVWH	160	—	ns
Chip Enable to End of Write	TELEH	160	—	ns
Chip Selection to End of Write	TELEH*	100	—	ns
Write Pulse Width	TWLWH	140	—	ns
Write Recovery Time	TEHAX, TWHAX, TSHAX	10	—	ns
Data Set Up Time	TDVWH, TDVEH, TDVSH	60	—	ns
Data Hold Time	TEHDX, TWHDX, TSHDX	0	—	ns

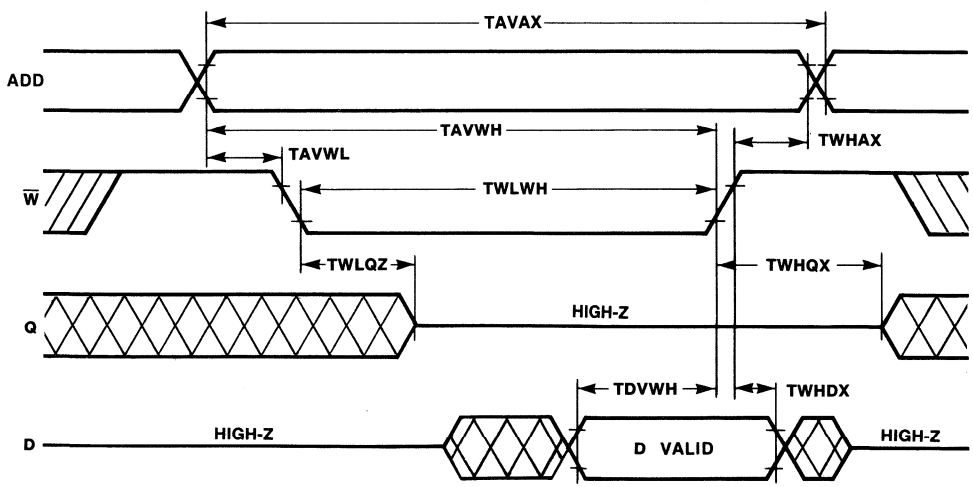
WAVEFORMS

MODE 1: $\overline{W}$ Controlled: ($\overline{E}$ = Low, $\overline{E}^*$ = Low)

Read Cycle



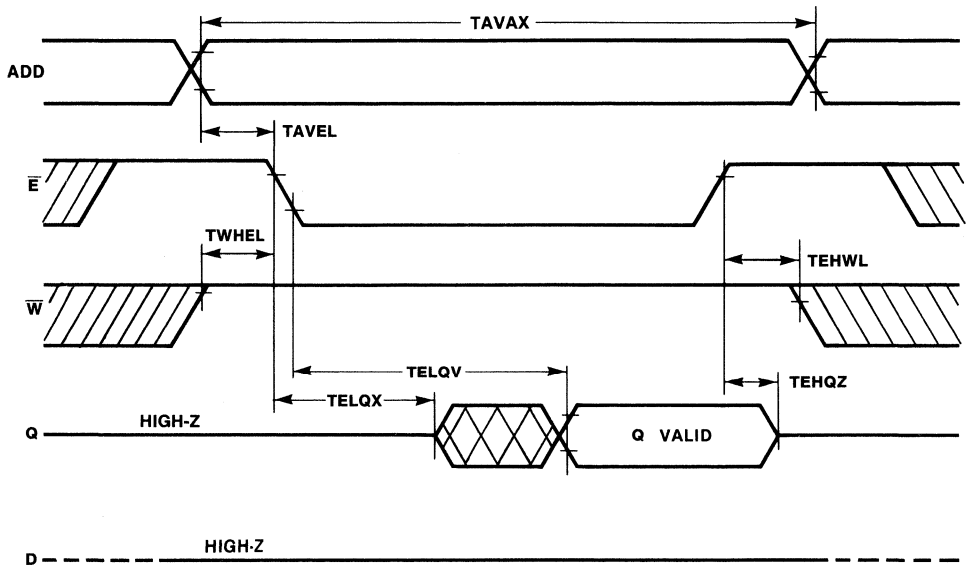
Write Cycle



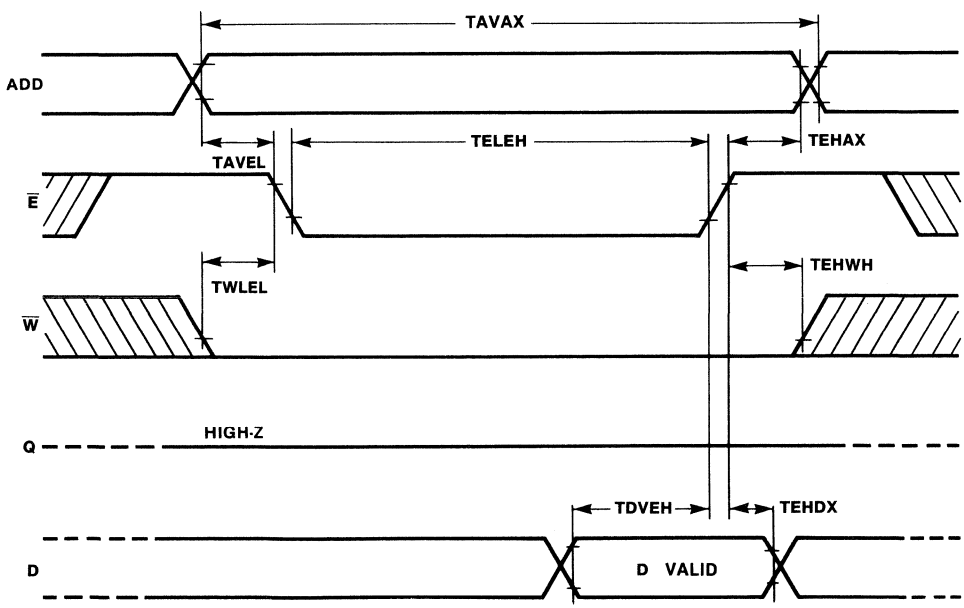
WAVEFORMS (Continued)

MODE 2: $\overline{E}$ Controlled, ($\overline{E}^*$ = Low)

Read Cycle

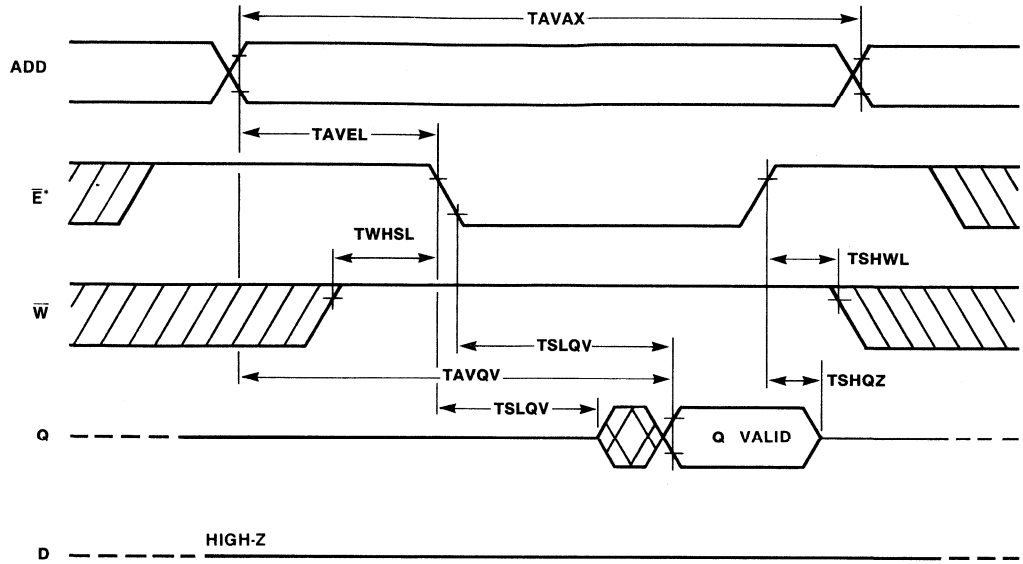


Write Cycle

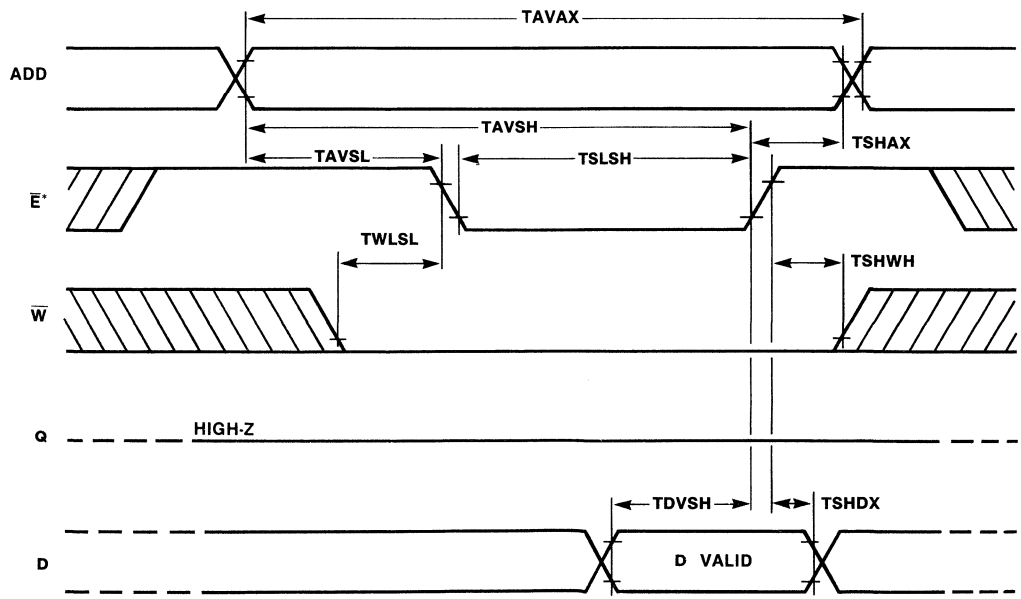


WAVEFORMS (Continued)
MODE 3: $\overline{E}^*$ Controlled, ($\overline{E}$ = Low)

Read Cycle



Write Cycle



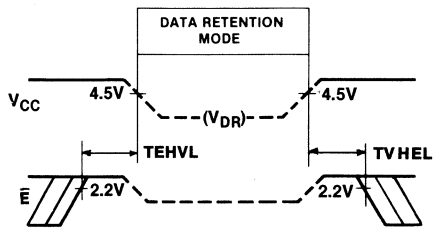
DYNAMIC CHARACTERISTICS

Data Retention Characteristics, NOTES 1, 2, 3 (Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol		Min	Max	Unit
Data Retention Supply Voltage	1	VDR		2.0	5.5	V
Data Retention Supply Current	2	IDR	MB8417-20	—	10	μA
			MB8417-20L	—	1	μA
Data Retention Set Up Time	3	TEHVL		0	—	ns
Recovery Time	3	TVHEL		60	—	ns

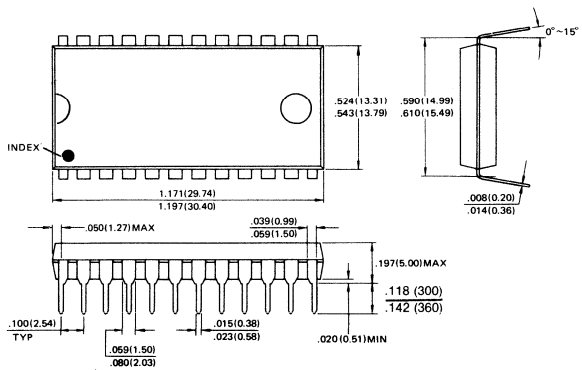
NOTES:

1. $\overline{E}$ = 2.2V to VDR + 0.3V when VDR = 2.5V to 5.5V, $\overline{E}$ = VDR ± 0.3V when VDR = 2.0 to 2.5V.
2. V_{CC} = VDR = 2.0V, $\overline{E}$ = VDR ± 0.2V V_{IN} = −0.2V to VDR + 0.2V.
3. V_L = 4.5V on the falling transition, V_H = 4.5V on the rising transition.



PACKAGE DIMENSIONS Dimensions in inches (millimeters)

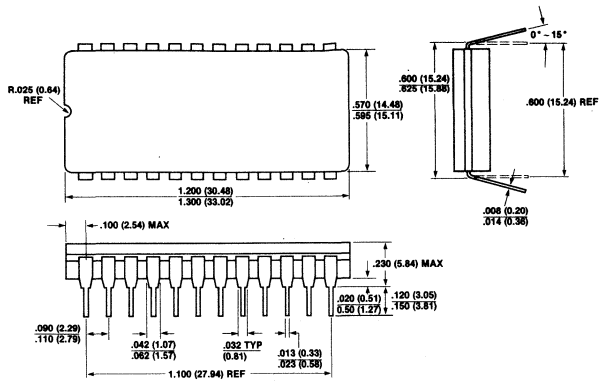
24-LEAD PLASTIC DUAL IN-LINE PACKAGE
DIP-24P-M02



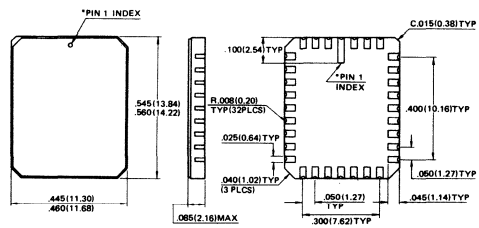
***Symbols in extra bold type are industry standards. See IEEE STD 662 for details.**

PACKAGE DIMENSIONS Dimensions in inches (millimeters) (Continued)

24-LEAD CERAMIC DUAL IN-LINE PACKAGE
DIP-24C-C03



LEADLESS CHIP CARRIER
LCC-32C-A02



*Shape of Pin 1 index : Subject to change without notice

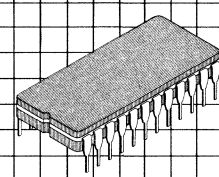
MB8417A-12, MB8417A-12L, MB8417A-15, MB8417A-15L

CMOS 16,384-Bit Static Random Access Memory

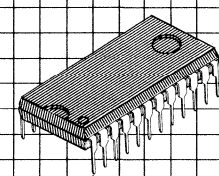
Description

The Fujitsu MB8417A is a 2048-word by 8-bit static random access memory fabricated with CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single 5 volt power supply is required.

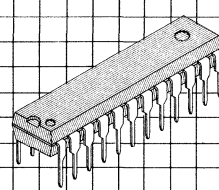
The MB8417A is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost, and high performance.



24-Lead Ceramic (Cerdip)
DIP-24C-C03



24-Lead Plastic DIP
DIP-24P-M02

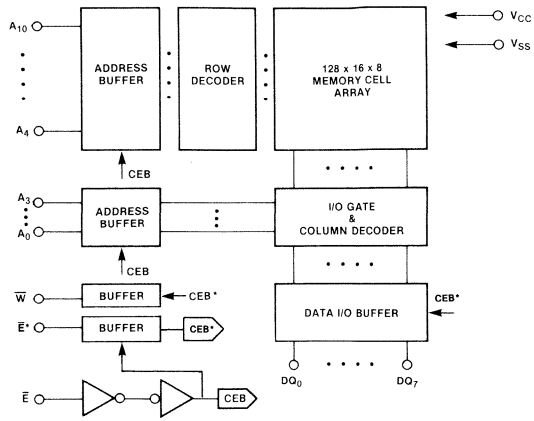


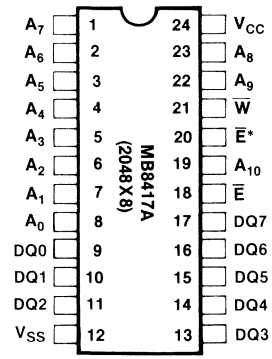
24-Lead Plastic DIP
DIP-24P-M03

Features

- Organization: 2048 words x 8-bits
- Fast Access Time:
  - $\overline{E}$ Controlled:
    - 120 ns max. (MB8417A-12/12L)
    - 150 ns max. (MB8417A-15/15L)
  - $\overline{E}$* Controlled:
    - 50 ns max. (MB8417A-12/12L)
    - 60 ns max. (MB8417A-15/15L)
- Completely static operation: No clocks required
- TTL compatible inputs/outputs
- Three-state output
- Common data input/output
- Single +5V power supply
- Low power standby:
  - 5.5 mW max. (MB8417A-12/15)
  - 275μW max. (MB8417A-12L/15L)
- Data retention: 2.0V min.
- Jedec Standard 24-pin DIP (Ceramic Cerdip/Plastic Mold)
- Pin compatible with TC5516

MB8417A Block Diagram and Pin Assignment





Truth Table

$\overline{E}$	E	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	I_{SB}	High-Z
L	H	X	Not Selected	I_{CC}	High-Z
L	L	H	Read	I_{CC}	D_{OUT}
L	L	L	Write	I_{CC}	D_{IN}

Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Storage Temperature	Ceramic	T_{stg}	−65 to +150	°C
	Plastic		−45 to +125	
Temperature Under Bias		T_{bias}	−10 to +85	°C
Supply Voltage		V_{CC}	−0.5 to +7.0	V
Input Voltage		V_{IN}	−0.5 to V_{CC} + 0.5	V
Output Voltage		$V_{I/O}$	−0.5 to V_{CC} + 0.5	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$	—	—	10	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}	—	—	7	pF

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Ambient Temperature	T_A	0	—	70	°C

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol	MB8417A-12/15 Min	MB8417A-12/15 Max	MB8417A-12L/15L Min	MB8417A-12L/15L Max	Unit
Standby Supply Current 1	$\overline{E} = V_{CC} - 0.2V$ to $V_{CC} + 0.2V$, $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	I_{SB1}	—	1	—	0.05	mA
Standby Supply Current 2	$\overline{E} = V_{IH}$, $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	I_{SB2}	—	2	—	1	mA
Active Supply Current	$\overline{E} = V_{IL}$ $V_{IN} = V_{IL}$ or V_{IH}; $I_{OUT} = 0$ mA	I_{CC1}	—	60	—	60	mA
Operating Supply Current	Cycle = Min, Duty = 100% $I_{OUT} = 0$ mA	I_{CC2}	—	60	—	60	mA
Input Leakage Current	$V_{IN} = 0V$ to V_{CC}	I_{LI}	−1.0	1.0	−1.0	1.0	μA
Output Leakage Current	$V_{I/O} = 0V$ to V_{CC} $\overline{E} = V_{IH}$ or $\overline{E}^* = V_{IH}$	I_{LO}	−1.0	1.0	−1.0	1.0	μA
Output High Voltage	$I_{OUT} = -1.0$ mA	V_{OH}	2.4	—	2.4	—	V
Output Low Voltage	$I_{OUT} = 4.0$ mA	V_{OL}	—	0.4	—	0.4	V

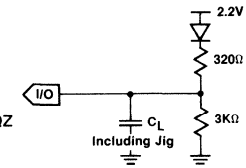
Note: All voltages are referenced to GND.

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8417A-12/12L Min	MB8417A-12/12L Max	MB8417A-15/15L Min	MB8417A-15/15L Max	Unit
Read Cycle Time	TAVAX	120	—	150	—	ns
Write Cycle Time	TAVAX	120	—	150	—	ns
Address Access Time	TAVQV	—	120	—	150	ns
Chip Enable Access Time	TELQV	—	120	—	150	ns
Output Hold from Address Change	TAXQX	15	—	15	—	ns
Output Low Z from $\overline{E}$	TELQX	15	—	15	—	ns
Output High Z from $\overline{E}$	TEHQZ	—	40	—	50	ns
Output Low Z from $\overline{E}$*	TSLQX, TELQX*	10	—	10	—	ns
Output High Z from $\overline{E}$*	TSHQZ, TEHQZ*	—	40	—	50	ns
Output Low Z from $\overline{W}$	TNHQX	15	—	15	—	ns
Output High Z from $\overline{W}$	TWLQZ	—	40	—	50	ns
Chip Select to Output Valid	TSLQV, TELQV*	—	50	—	60	ns
Address Set Up Time	TAVEL, TAVWL	0	—	0	—	ns
Address Set Up Time	TAVSL, TAVEL*	20	—	20	—	ns
Read Set Up Time	TWHEL, TWHAV, TWHSL, TWHEL*	0	—	0	—	ns
Read Hold Time	TAXWL, TEHWL, TSHWL, TEHWL*	0	—	0	—	ns
Write Set Up Time	TWLEL, TWLSL, TWLEL*	0	—	0	—	ns
Write Hold Time	TEHWH, TSHWH, TEHWH*	0	—	0	—	ns
Address Valid to End of Write	TAVWH, TAVSH	100	—	120	—	ns
Chip Enabled to End of Write	TELEH, TAVEH	100	—	120	—	ns
Chip Selection to End of Write	TSLSH, TELEH*	50	—	60	—	ns
Write Pulse Width	TWLWH, TWLSH, TWLEH*	70	—	90	—	ns
Write Recovery Time	TSHAX, TWHAX, TEHAX, TEHAX*	5	—	5	—	ns
Data Set Up Time	TDVSH, TDVEH, TDVWH, TDVEH*	35	—	40	—	ns
Data Hold Time	TSHDX, TWHDX, TEHDX, TEHDX*	0	—	0	—	ns

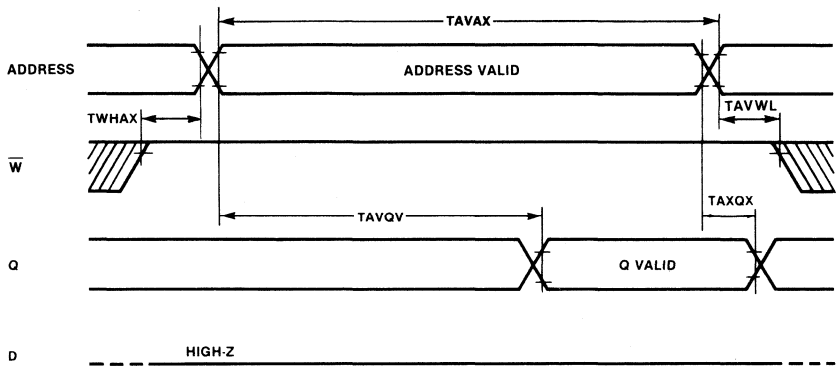
AC Test Conditions

Input Pulse Levels:	0.6V to 2.4V
Input Pulse Rise and Fall Times:	5ns (Transient Time between 0.8V and 2.2V)
Timing Reference Levels:	Input: $V_{IL} = 0.8V$, $V_{IH} = 2.2V$ Output: $V_{OL} = 0.8V$, $V_{OH} = 2.2V$
Output Load:	$C_L = 5_{pF}$ for TEHQZ, TEHQZ* and TWLQZ $C_L = 100$ pF for all others.

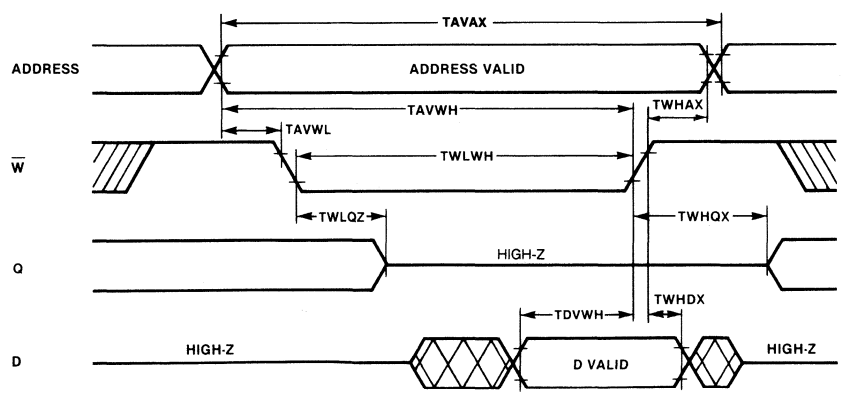


Mode 1 — $\overline{W}$ Controlled
($\overline{E}$ = Low, $\overline{E}^*$ = Low)

Read Cycle Timing Diagram

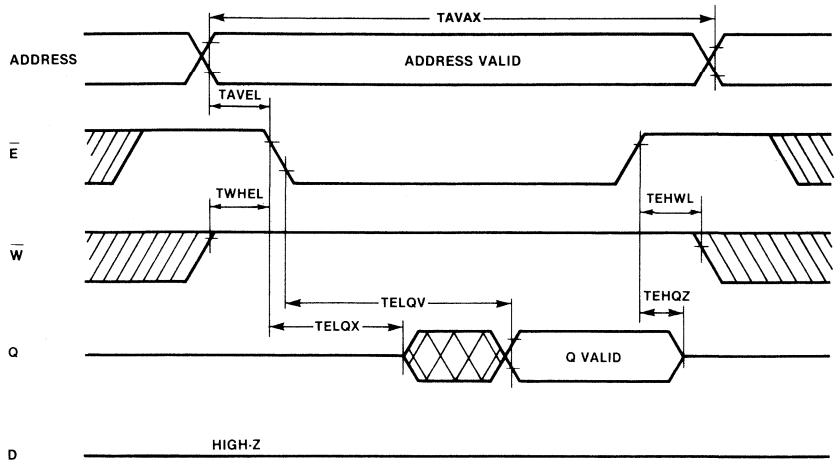


Write Cycle Timing Diagram

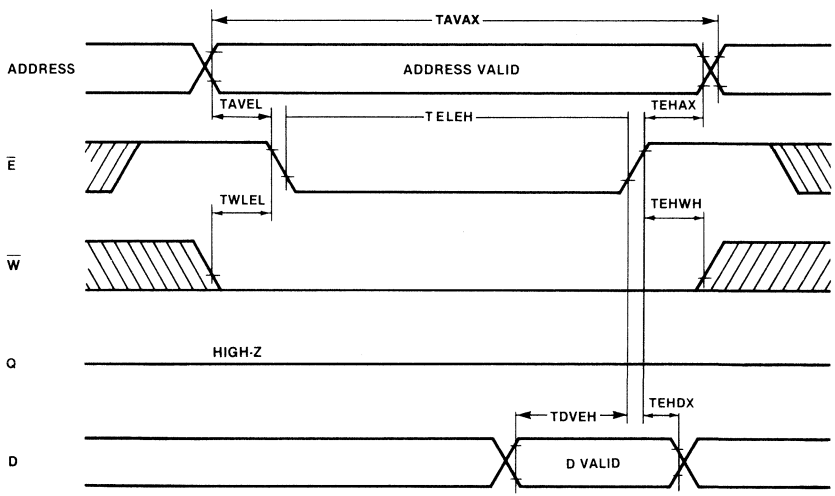


Mode 2 — $\overline{E}$ Controlled
($\overline{E}$* = Low)

Read Cycle Timing Diagram

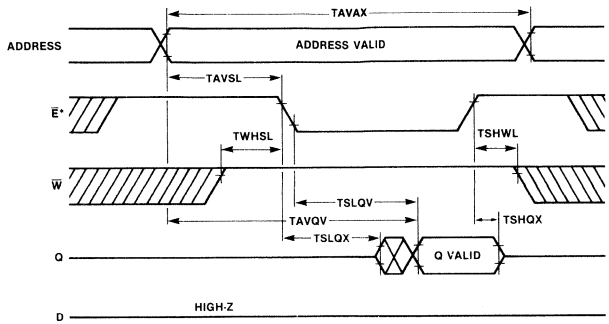


Write Cycle Timing Diagram

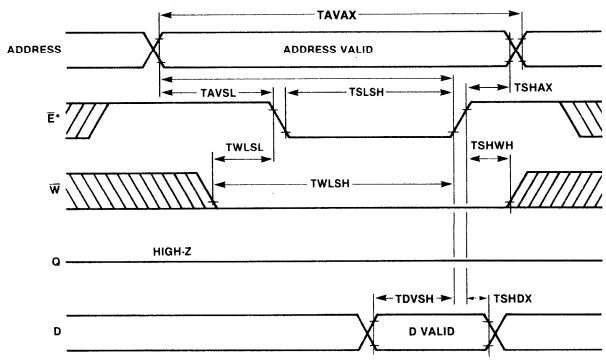


Mode 3 — $\overline{E}$* Controlled
($\overline{E}$ = Low, $\overline{W}$ = High, Address Valid)

Read Cycle Timing Diagram



Write Cycle Timing Diagram

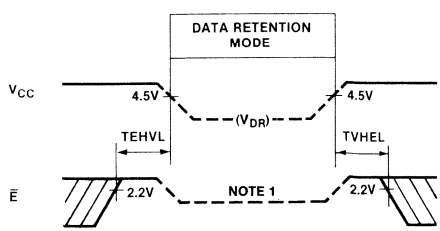


Data Retention Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8417A-12/15 Min	MB8417A-12/15 Max	MB8417A-12L/15L Min	MB8417A-12L/15L Max	Unit	Test Condition
Data Retention Supply Voltage	V_{DR}	2.0	5.5	2.0	5.5	V	Note 1
Data Retention Supply Current	I_{DR}	—	0.5	—	0.03	mA	Note 2
Data Retention Set Up Time	TEHVL	0	—	0	—	ns	Note 3
Recovery Time	TVHEL	40	—	40	—	ns	Note 3

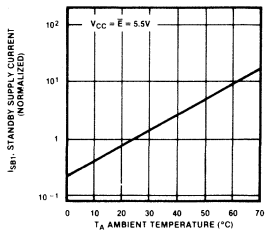
Note 1. $\overline{E}$ = 2.2V to VDR + 0.3V when VDR = 2.5V to 5.5V, $\overline{E}$ = VDR ± 0.3V when VDR = 2.0 to 2.5V.
Note 2. $V_{CC} = V_{DR} = 3.0V$, $\overline{E} = V_{DR} - 0.2V$ to $V_{DR} + 0.2V$, $V_{IN} = -0.2V$ to $V_{DR} + 0.2V$.
Note 3. $V_L = 4.5V$ on the falling transition, $V_H = 4.5V$ on the rising transition.

Data Retention Timing Diagram

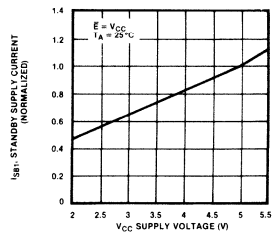


Typical Characteristics Curves

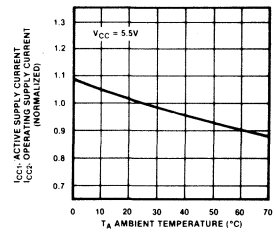
Standby Supply Current vs. Ambient Temp



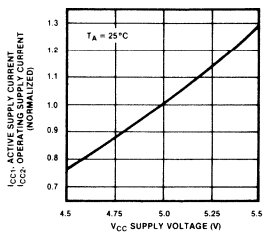
Standby Supply Current vs. Supply Voltage



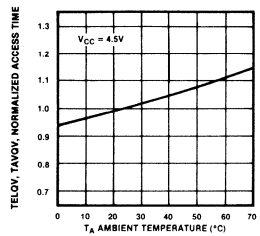
Supply Current (Active/Operating) vs. Ambient Temp



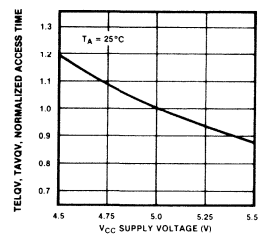
Supply Current (Active/Operating) vs. Supply Voltage



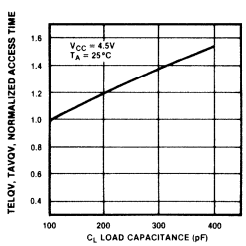
Access Time vs. Ambient Temp



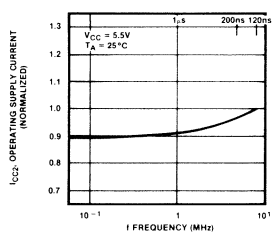
Access Time vs. Supply Voltage



Access Times vs. Load Capacitance

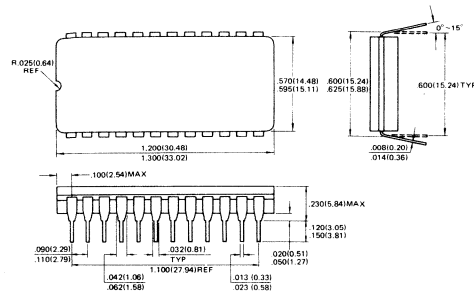


Supply Current vs. Frequency

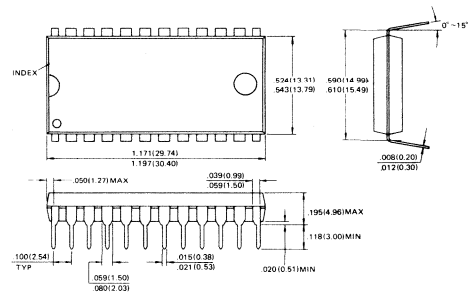


Package Dimensions
Dimensions in inches
(millimeters)

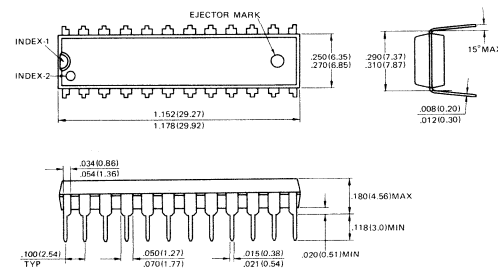
24-Lead Ceramic (Cerdip)
Dual In-Line Package
DIP-24C-C03



24-Lead Plastic
Dual In-Line Package
DIP-24P-M02



24-Lead Plastic
Dual In-Line Package
DIP-24P-M03



FUJITSU
MICROELECTRONICS, INC.

MB8418-20
MB8418-20L

CMOS 16,384-BIT STATIC RANDOM ACCESS MEMORY

DESCRIPTION

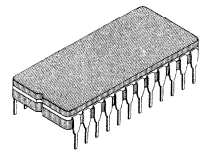
The Fujitsu MB8418 is a 2048 word by 8-bit static random access memory fabricated with high density, high reliability Complementary MOS silicon-gate technology.

The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All input and output pins are TTL-compatible, and a single 5 volt power supply is used. It is possible to retain data at low power supply voltage.

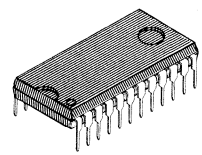
The MB8418 can be optimized for high performance applications such as microcomputer systems where fast access time and ease of use are required. Two Chip Enables ($\overline{E}_1$ and $\overline{E}_2$) permit the selection of an individual device when the outputs are OR-tied. $\overline{E}_2$ controls minimum power consumption. The MB8418 is packaged in an industry standard 24-pin dual in-line package, or 32-pin leadless chip carrier.

FEATURES

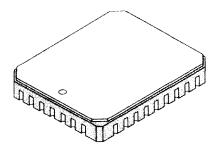
- **Extended temperature range:**
  MB8418-20: −40°C to +85°C
  MB8418-20L: −40°C to +70°C
- **Organized as 2048 words by 8-bits**
- **Fast Access Time: 200 ns Max.**
- **Low Standby Power:**
  MB8418-20: 55μW
  MB8418-20L: 5.5μW
- **Completely Static Operation, no clocks required**
- **Single +5 Volt Power Supply**
- **TTL Compatible Inputs/Outputs**
- **Low Data Retention Voltage: 2.0V Min.**
- **Pin compatible with HM6117 TC5518 and μPD449**



CERDIP PACKAGE
DIP-24C-C03

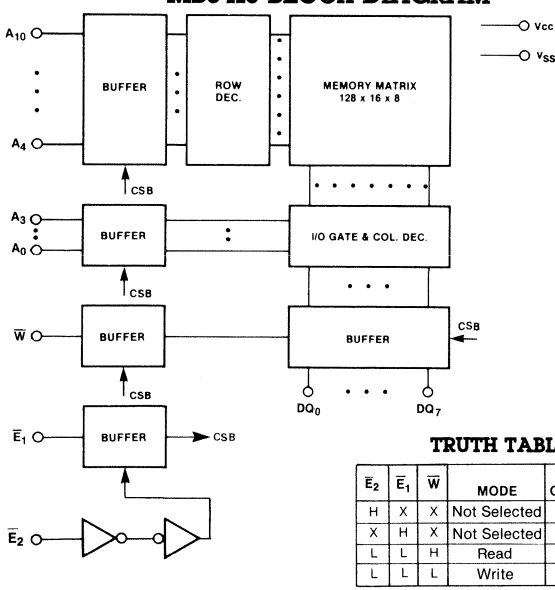


PLASTIC PACKAGE
DIP-24P-M02



LEADLESS CHIP CARRIER
LCC-32-A02

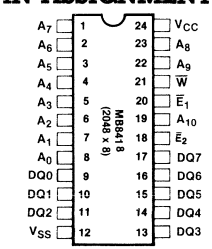
MB8418 BLOCK DIAGRAM

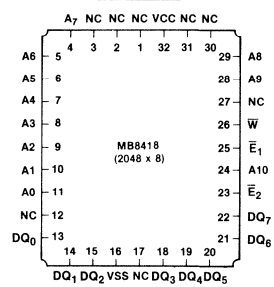


TRUTH TABLE

$\overline{E}_2$	$\overline{E}_1$	$\overline{W}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	Not Selected	I_{SB}	High-Z
X	H	X	Not Selected	I_{SB}	High-Z
L	L	H	Read	I_{CC}	D_{OUT}
L	L	L	Write	I_{CC}	D_{IN}

PIN ASSIGNMENTS





ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Unit
Storage Temperature	Ceramic	T_{stg}	−65	150	°C
	Plastic		−45	125	
Temperature Under Bias		T_{bias}	−40	85	°C
Supply Voltage		V_{CC}	−0.5	8.0	V
Input Voltage		V_{IN}	−0.5	V_{CC} + 0.5	V
Input/Output Voltage		$V_{I/O}$	−0.5	V_{CC} + 0.5	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS, (Referenced to V_{SS} = GND)

Parameter	Symbol		MB8418 Min	MB8418 Typ	MB8418 Max	Unit
Ambient Temperature	T_A	MB8418-20L	−40	—	+70	°C
		MB8418-20	−40	—	+85	
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Input High Voltage	V_{IH}		2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		−0.3	—	0.8	V

CAPACITANCE

(T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit	Condition
Input Capacitance	C_{IN}	—	7	pF	V_{IN} = 0V
Input / Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

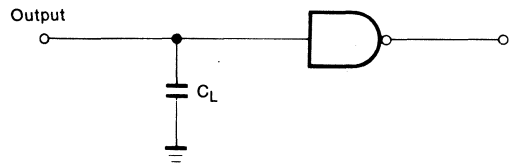
STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol		Min	Max	Units
Standby Supply Current	$\overline{E}_2 = V_{CC} \pm 0.2$ OR V_{IN} = −0.2V to V_{CC} + 0.2V	I_{SB1}	MB8418-20L	—	1	μA
			MB8418-20	—	10	
Standby Supply Current	$\overline{E}_2$ or $\overline{E}_1 = V_{IH}$ V_{IN} = −0.2V to V_{CC} + 0.2V	I_{SB2}		—	2	mA
Active Supply Current	$\overline{E}_2 = V_{IL}$ $V_{IN} = V_{IL}$ or V_{IH}; I_{OUT} = 0	I_{CC1}		—	60	mA
Operating Supply Current	Cycle = Min, Duty = 100% I_{OUT} = 0	I_{CC2}		—	60	mA
Input Leakage Current	V_{IN} = 0V to V_{CC}	I_{LI}		−1.0	1.0	μA
Output Leakage Current	$V_{I/O}$ = 0V to V_{CC} $\overline{E}_2 = V_{IH}$ or $\overline{E}_1 = V_{IH}$	I_{LO}		−1.0	1.0	μA
Output High Voltage	I_{OUT} = −1.0 mA	V_{OH}		2.4	—	V
Output Low Voltage	I_{OUT} = 4.0 mA	V_{OL}		—	0.4	V

AC TEST CONDITIONS

Input Pulse Levels:	**0.6V to 2.4V**
Input Pulse Rise and Fall Times:	**10 ns (0.8V to 2.2 V)**
Input Timing Reference Level:	**0.8V to 2.2V**
Output Timing Reference Level:	**0.8V to 2.2V**
Output Load:	**1 TTL Gate and $C_L = 100_{PF}$**



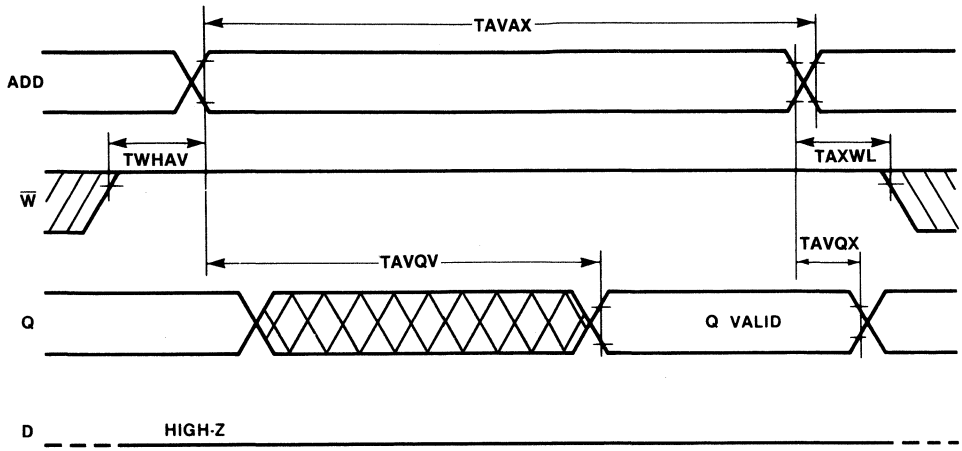
DYNAMIC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	TAVAX	200	—	ns
Write Cycle Time	TAVAX	200	—	ns
Address Access Time	TAVQV	—	200	ns
Chip Enable Access Time	TELQV	—	200	ns
Output Hold from Address Change	TAVQX	15	—	ns
Output Low Z from $\overline{E}_2$ or $\overline{E}_1$	TELQX	15	—	ns
Output High Z from $\overline{E}_2$ or $\overline{E}_1$	TEHQZ	—	60	ns
Output Low Z from $\overline{W}$	TWHQV	15	—	ns
Output High Z from $\overline{W}$	TWLQZ	—	60	ns
Address Set Up Time	TAVEL, TAVWL	0	—	ns
Read Set Up Time	TWHEL, TWHAV	0	—	ns
Read Hold Time	TAXWL, TEHWL	0	—	ns
Write Set Up Time	TWLEL	0	—	ns
Write Hold Time	TEHWH	0	—	ns
Address Valid to End of Write	TAVWH	160	—	ns
Chip Enable to End of Write	TELEH	160	—	ns
Write Pulse Width	TWLWH	140	—	ns
Write Recovery Time	TWHAX, TEHAX	10	—	ns
Data Set Up Time	TDVEH, TDVWH	60	—	ns
Data Hold Time	TWHDX, TEHDX	0	—	ns

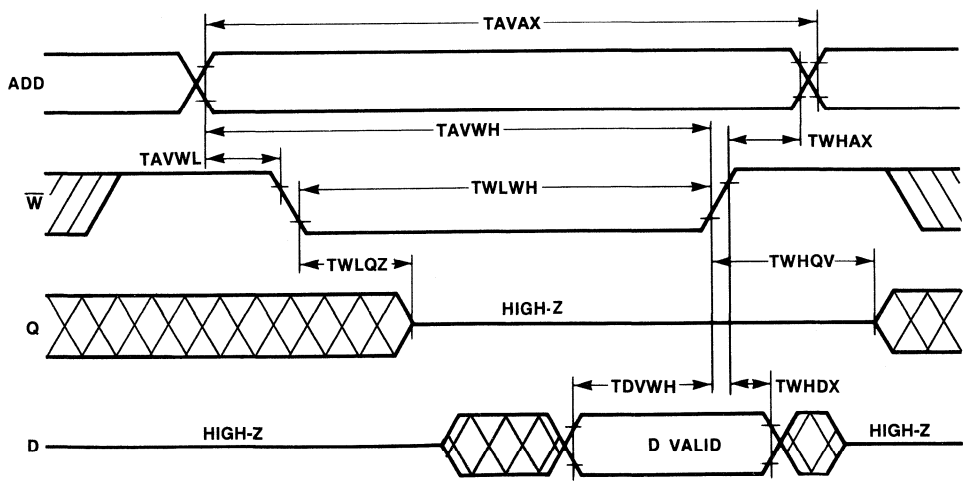
WAVEFORMS

MODE 1: W Controlled: ($\overline{E}_1 = \overline{E}_2$ = LOW)

Read Cycle



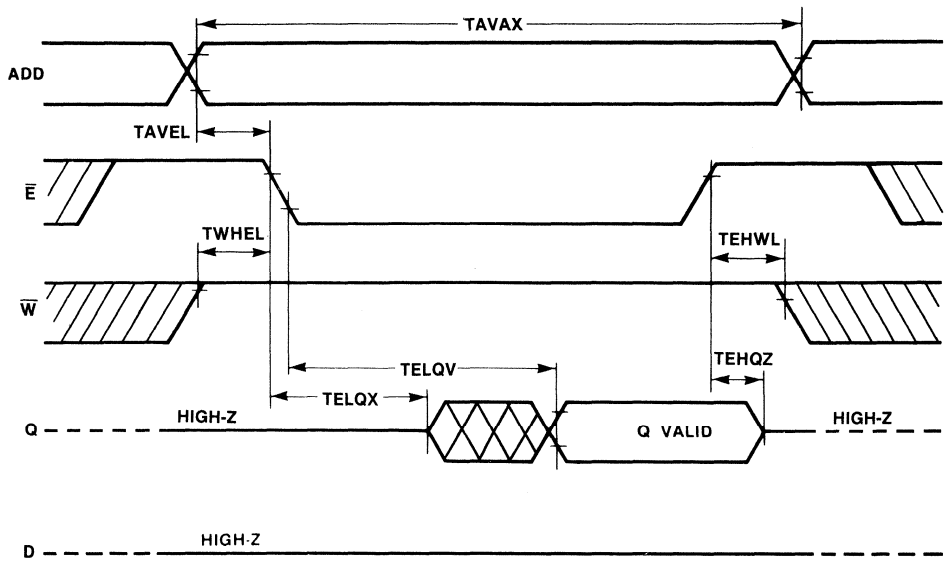
Write Cycle



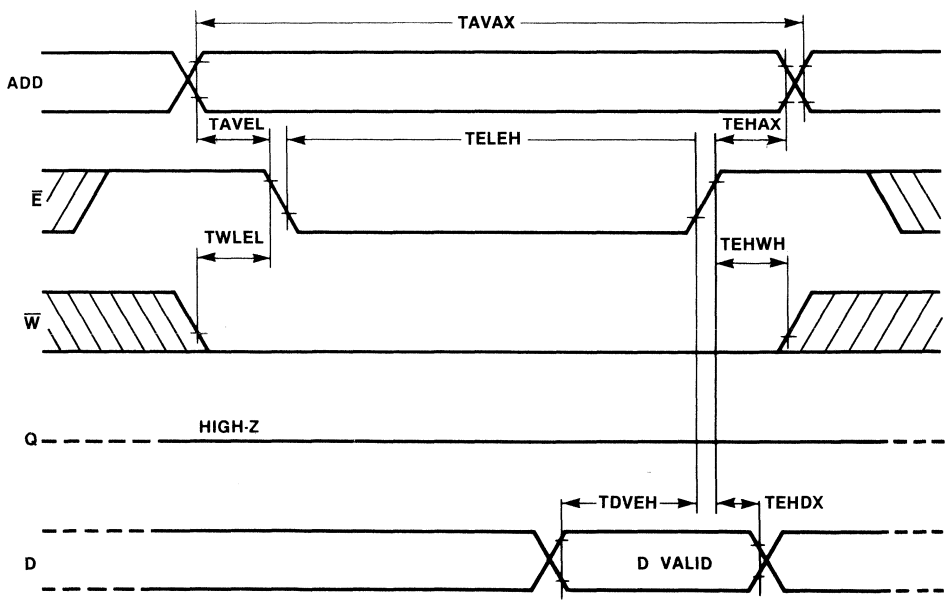
WAVEFORMS (Continued)

MODE 2: ($\overline{E}_1$ or $\overline{E}_2$ Controlled ($\overline{E}_2$ = Low or $\overline{E}_1$ = Low)

Read Cycle



Write Cycle



DYNAMIC CHARACTERISTICS

Data Retention Characteristics, NOTES [1, 2, 3] (Recommended operating conditions unless otherwise noted.)

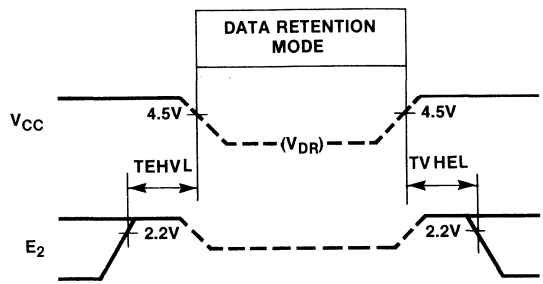
Parameter	Notes	Symbol		Min	Max	Unit
Data Retention Supply Voltage	[1]	VDR		2.0	5.5	V
Data Retention Supply Current	[2]	IDR	MB8418-20	—	10	μA
			MB8418-20L	—	1	μA
Data Retention Set Up Time	[3]	TEHVCL		0	—	ns
Recovery Time	[3]	TVHEL		60	—	ns

Notes:

[1.] $\overline{E}_2 = 2.2V$ to $V_{CC} \pm 0.3V$ for VDR = 2.5V to 5.5V
$\overline{E}_2 = V_{CC} \pm 0.3V$ for VDR = 2.0 to 2.5V.

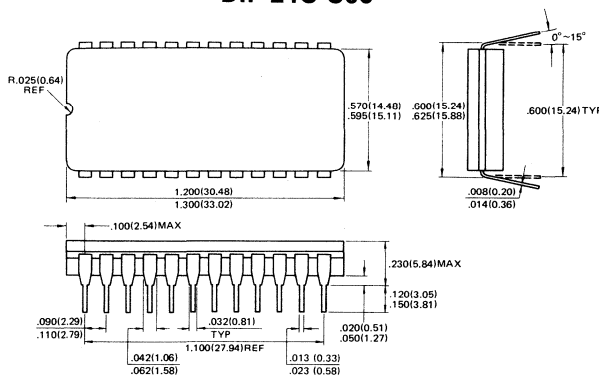
[2.] $V_{CC} = V_{DR}$, $\overline{E}_2 = V_{DR} - 0.2V$ to $V_{DR} + 0.2V$, $V_{IN} = -0.2V$ to $V_{DR} + 0.2V$.

[3.] $V_L = 4.5V$ on the falling transition, $V_H = 4.5V$ on the rising transition.

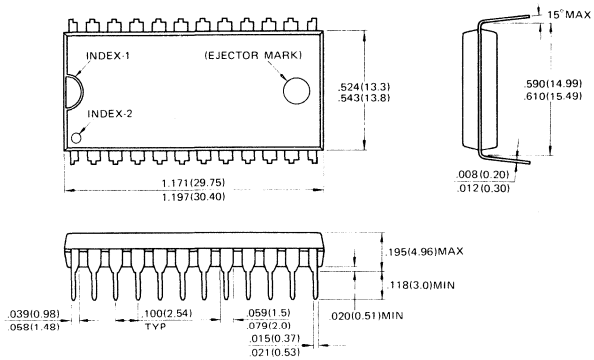


PACKAGE DIMENSIONS Dimensions in inches (millimeters)

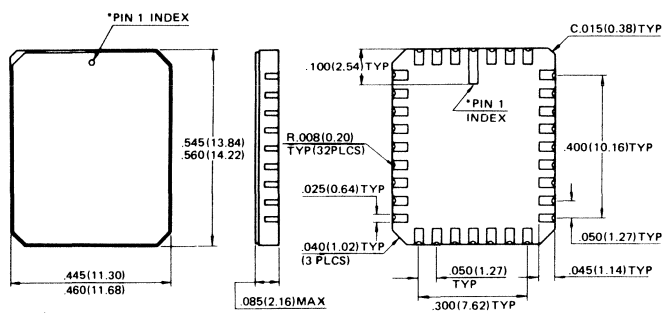
24-LEAD CERDIP DUAL IN-LINE PACKAGE
DIP-24C-C03



24-LEAD PLASTIC DUAL IN-LINE PACKAGE
DIP-24P-M02



32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
LCC-32-A02



*Shape of Pin 1 index : Subject to change without notice

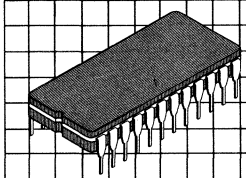
■ MB8418A-12, MB8418A-12L, MB8418A-15, MB8418A-15L

CMOS 16,384-Bit Static Random Access Memory

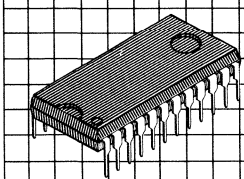
Description

The Fujitsu MB8418A is a 2048-word by 8-bit static random access memory fabricated with CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single 5 volt power supply is required.

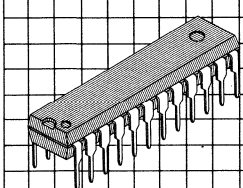
The MB8418A is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost, and high performance.



Ceramic Package (Cerdip)
DIP-24C-C03



Plastic Package
DIP-24P-M02

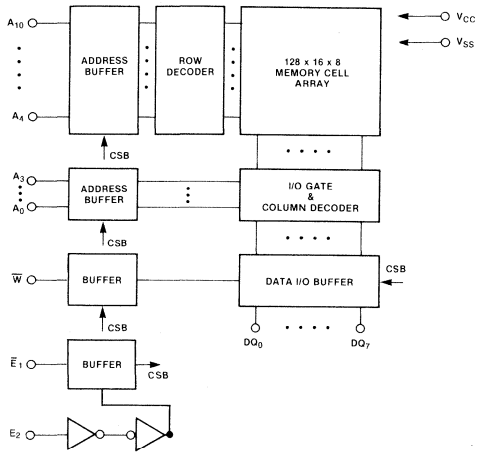


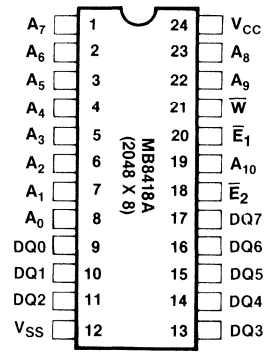
Plastic Package
DIP-24P-M03

Features

- Organization: 2048 words x 8-bits
- Fast Access Time:
  120 ns max. (MB8418A-12/12L)
  150 ns max. (MB8418A-15/15L)
- Completely static operation: No clocks required
- TTL compatible inputs/outputs
- Three-state output
- Common data input/output
- Single +5V power supply
- Low power standby:
  5.5 mW max. (MB8418A-12/15)
  275 μW max. (MB8418A-12L/15L)
- Data retention: 2.0V min.
- Standard 24-pin DIP (Ceramic Cerdip/Plastic Mold)
- Dual chip enable inputs for battery back-up use.

MB8418A Block Diagram and Pin Assignment





Truth Table

$\overline{E}_2$	$\overline{E}_1$	W	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	I_{SB}	High-Z
X	H	X	Not Selected	I_{SB}	High-Z
L	L	H	Read	I_{CC}	D_{OUT}
L	L	L	Write	I_{CC}	D_{IN}

Absolute Maximum Ratings
(See Note)

Parameter		Symbol	Value	Unit
Storage Temperature	Ceramic Plastic	T_{stg}	−65 to +150 −45 to +125	°C
Temperature Under Bias		T_{bias}	−10 to +85	°C
Supply Voltage		V_{CC}	−0.5 to +7.0	V
Input Voltage		V_{IN}	−0.5 to V_{CC} + 0.5	V
Input/Output Voltage		$V_{I/O}$	−0.5 to V_{CC} + 0.5	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

Capacitance
(f = 1 MHz, T_A = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit
I/O Capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$	—	—	10	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}	—	—	7	pF

Recommended Operating Conditions
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Ambient Temperature	T_A	0	—	70	°C

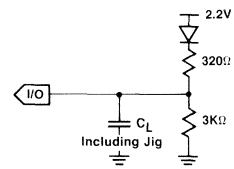
DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol	MB8418A-12/15 Min	MB8418A-12/15 Max	MB8418A-12L/15L Min	MB8418A-12L/15L Max	Unit
Standby Supply Current 1	$\overline{E}_2 = V_{CC} \pm 0.2$ OR $\overline{E}_1 = V_{CC} + 0.2V$ and $E_2 = V_{SS} \pm 0.2V$ $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	I_{SB1}	—	1	—	0.05	mA
Standby Supply Current 2	$\overline{E}_2$ or $\overline{E}_1 = V_{IH}$, $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	I_{SB2}	—	2	—	1	mA
Active Supply Current	$\overline{E}_1 = \overline{E}_2 = V_{IL}$ $V_{IN} = V_{IL}$ or V_{IH}; $I_{OUT} = 0$ mA	I_{CC1}	—	60	—	60	mA
Operating Supply Current	Cycle = Min, Duty = 100% $I_{OUT} = 0$ mA	I_{CC2}	—	60	—	60	mA
Input Leakage Current	$V_{IN} = 0V$ to V_{CC}	I_{LI}	−1.0	1.0	−1.0	1.0	μA
Output Leakage Current	$V_{I/O} = 0V$ to V_{CC} $\overline{E}_2 = V_{IH}$ or $\overline{E}_1 = V_{IH}$	I_{LO}	−1.0	1.0	−1.0	1.0	μA
Output High Voltage	$I_{OUT} = -1.0$ mA	V_{OH}	2.4	—	2.4	—	V
Output Low Voltage	$I_{OUT} = 4.0$ mA	V_{OL}	—	0.4	—	0.4	V

Note: All voltages are referenced to GND.

AC Test Conditions

Input Pulse Levels:	0.6V to 2.4V
Input Pulse Rise and Fall Times:	5ns (Transient Time between 0.8V and 2.2V)
Timing Reference Levels:	Input: $V_{IL} = 0.8V$, $V_{IH} = 2.2V$ Output: $V_{OL} = 0.8V$, $V_{OH} = 2.2V$
Output Load:	$C_L = 5_{PF}$ for TEHQZ and TWHQZ $C_L = 100$ pF for all others.

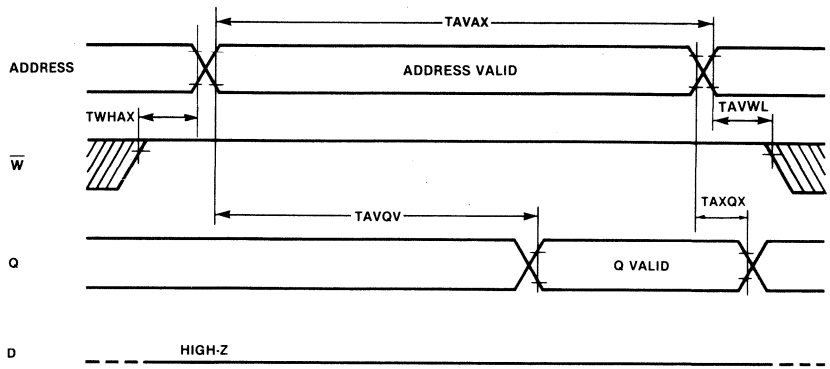


AC Characteristics
(Recommended operating conditions unless otherwise noted.)

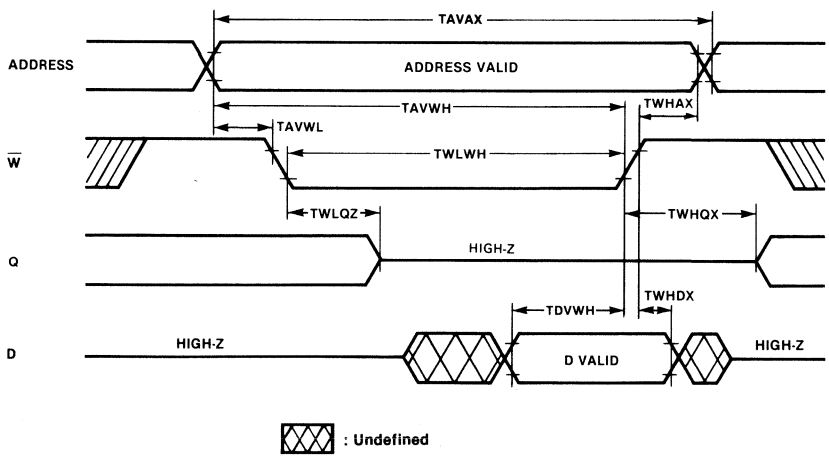
Parameter	Symbol	MB8418A-12/12L Min	MB8418A-12/12L Max	MB8418A-15/15L Min	MB8418A-15/15L Max	Unit
Read Cycle Time	TAVAX	120	—	150	—	ns
Write Cycle Time	TAVAX	120	—	150	—	ns
Address Access Time	TAVQV	—	120	—	150	ns
Chip Enable Access Time	TELQV	—	120	—	150	ns
Output Hold from Address Change	TAXQX	15	—	15	—	ns
Output Low Z from $\overline{E}_2$ or $\overline{E}_1$	TELQX	15	—	15	—	ns
Output High Z from $\overline{E}_2$ or $\overline{E}_1$	TEHQZ	—	40	—	50	ns
Output Low Z from $\overline{W}$	TWHQX	15	—	15	—	ns
Output High Z from $\overline{W}$	TWLQZ	—	40	—	50	ns
Address Set Up Time	TAVEL, TAVWL	0	—	0	—	ns
Read Set Up Time	TWHEL, TWHAV	0	—	0	—	ns
Read Hold Time	TAXWL, TEHWL	0	—	0	—	ns
Write Set Up Time	TWLEL	0	—	0	—	ns
Write Hold Time	TEHWH	0	—	0	—	ns
Address Valid to End of Write	TAVWH	100	—	120	—	ns
Chip Enabled to End of Write	TELEH	100	—	120	—	ns
Write Pulse Width	TWLWH	70	—	90	—	ns
Write Recovery Time	TWHAX, TEHAX	5	—	5	—	ns
Data Set Up Time	TDVEH, TDVWH	35	—	40	—	ns
Data Hold Time	TWHDX, TEHDX	0	—	0	—	ns

Mode 1 — $\overline{W}$ Controlled
($\overline{E}_1$ = $\overline{E}_2$ = Low)

Read Cycle Timing Diagram

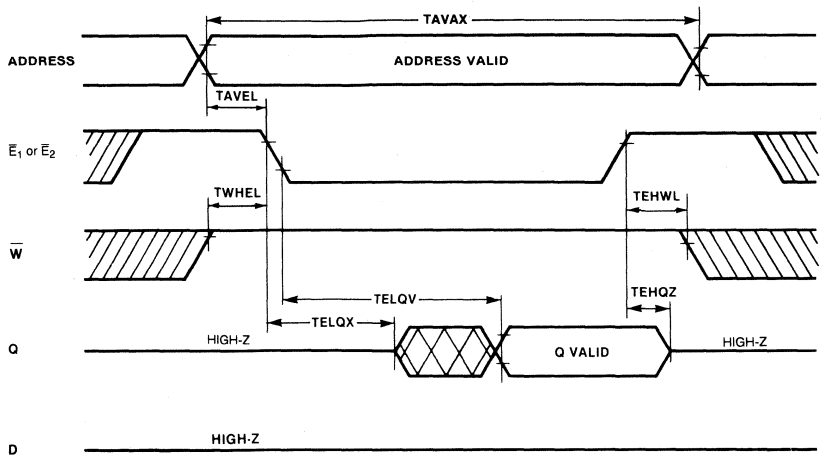


Write Cycle Timing Diagram

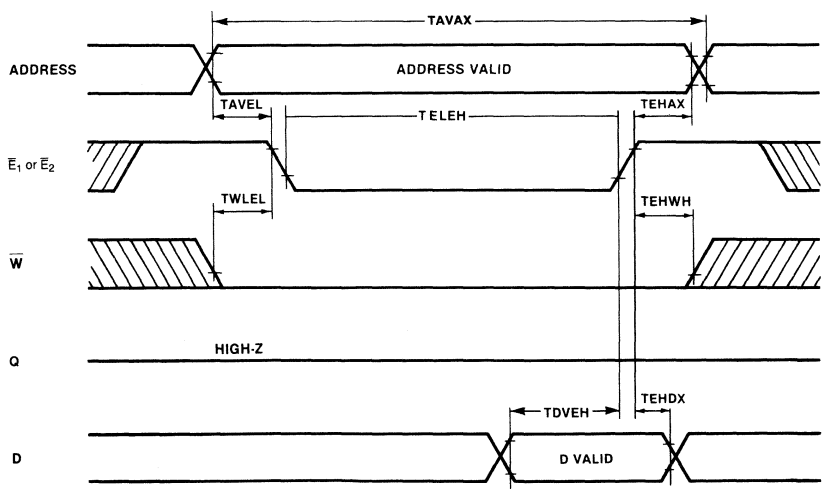


Mode 2 — $\overline{E}_2$ or $\overline{E}_1$ Controlled
($\overline{E}_1$ = Low or $\overline{E}_2$ = Low)

Read Cycle Timing Diagram



Write Cycle Timing Diagram



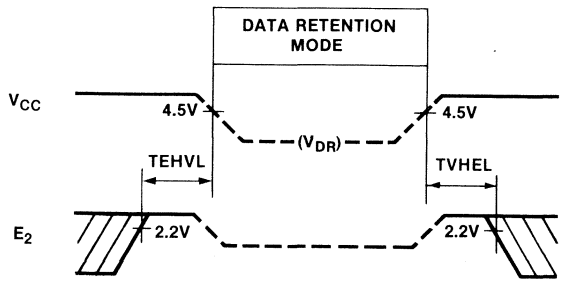
: Undefined

Data Retention Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8418A-12/15 Min	MB8418A-12/15 Max	MB8418A-12L/15L Min	MB8418A-12L/15L Max	Unit	Test Condition
Data Retention Supply Voltage	V_{DR}	2.0	5.5	2.0	5.5	V	Note 1
Data Retention Supply Current	I_{DR}	—	0.5	—	0.03	mA	Note 2
Data Retention Set Up Time	TEHVL	0	—	0	—	ns	Note 3
Recovery Time	TVHEL	40	—	40	—	ns	Note 3

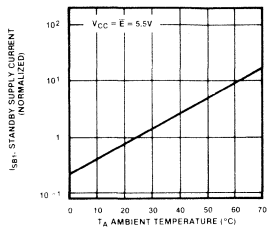
Note 1. $\overline{E}_2 = 2.2V$ to $V_{CC} + 0.3V$ for VDR = 2.5V to 5.5V
$\overline{E}_2 = V_{CC} \pm 0.3V$ for VDR = 2.0 to 2.5V.
Note 2. $V_{CC} = V_{DR} = 3.0V$, $\overline{E}_2 = V_{DR} - 0.2V$ to $V_{DR} + 0.2V$, $V_{IN} = -0.2V$ to $V_{DR} + 0.2V$.
Note 3. $V_L = 4.5V$ on the falling transition, $V_H = 4.5V$ on the rising transition.

Data Retention Timing Diagram

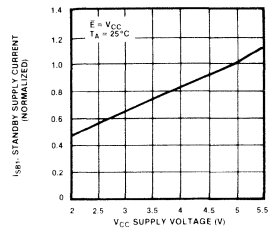


Typical Characteristics Curves

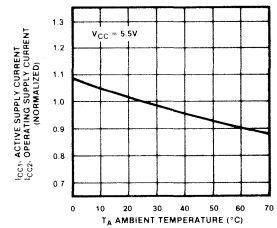
Standby Supply Current vs. Ambient Temp



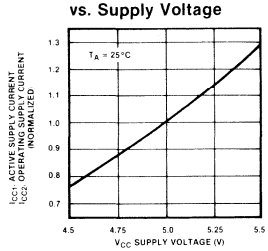
Standby Supply Current vs. Supply Voltage



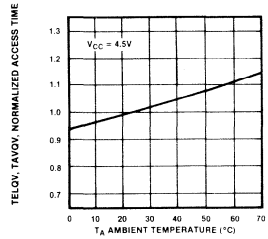
Supply Current (Active/Operating) vs. Ambient Temp



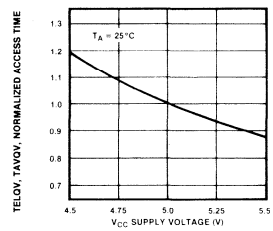
Supply Current (Active/Operating) vs. Supply Voltage



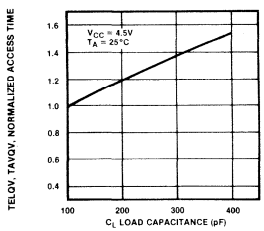
Access Time vs. Ambient Temp



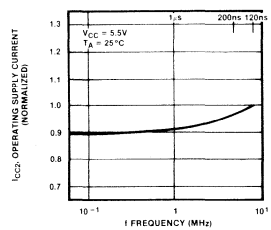
Access Time vs. Supply Voltage



Access Time vs. Load Capacitance



Supply Current vs. Frequency



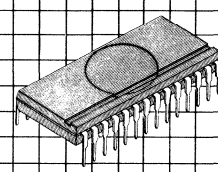
■ MB8464-12, MB8464-12L, MB8464-15, MB8464-15L, MB8464-12LL, MB8464-15LL

CMOS 65,536-Bit Static Random Access Memory with Data Retention Mode

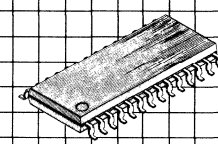
Description

The Fujitsu MB8464 is a 8,192-word by 8-bit static random access memory fabricated with a CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5 volt power supply is required.

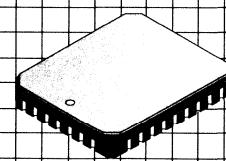
The MB8464 is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost, and high performance.



Plastic Package
DIP-28P-M02



Plastic Package
FPT-28P-M01

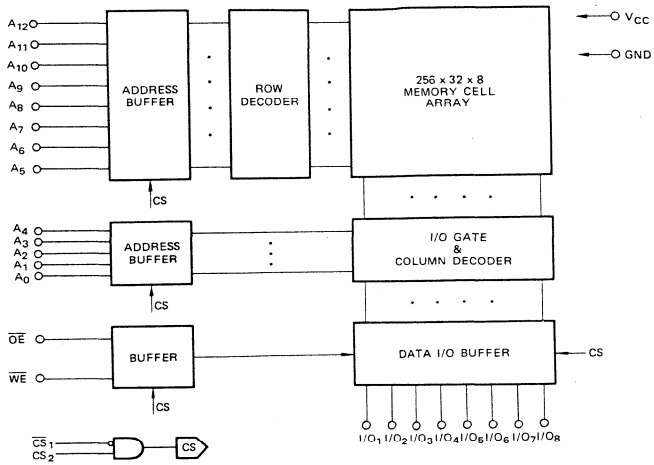


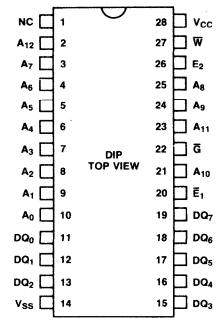
Ceramic Package
LCC-32C-A02

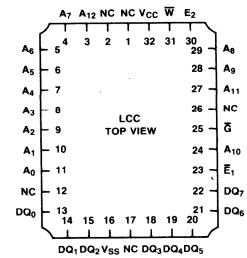
Features

- Organization: 8,192 words x 8-bits
- Fast access times: TAVQV = TELQV = 120 ns max. MB8464-12/-12L/-12LL TAVQV = TELQV = 150 ns max. MB8464-15/-15L/-15LL
- Completely static operation: No clock required
- TTL compatible input/output
- Three-state output
- Common data input/output
- Single +5V power supply, ±10% tolerance
- Low power standby: 11 mW max. MB8464-12/-15 0.55 mW max. MB8464-12L/-15L/-12LL/-15LL
- Data retention: 2.0V min.
- Standard 28-pin flat package
- Standard 32-pad LCC
- Standard 28-pin DIP

MB8464 Block Diagram and Pin Assignments







TRUTH TABLE

$\overline{CS}_1$	CS_2	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	X	NOT SELECTED	I_{SB}	HIGH-Z
X	L	X	X	NOT SELECTED	I_{SB}	HIGH-Z
L	H	H	H	D_{OUT} DISABLE	I_{CC}	HIGH-Z
L	H	L	H	READ	I_{CC}	D_{OUT}
L	H	X	L	WRITE	I_{CC}	D_{IN}

Absolute Maximum Ratings

Rating		Symbol	Value	Unit
Storage temperature	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−45 to +125	
Temperature under bias		T_{BIAS}	−10 to +85	°C
Supply voltage		V_{CC}	−0.5 to +7.0	V
Input voltage		V_{IN}	−0.5 to V_{CC} + 0.5	V
Output voltage		V_{OUT}	−0.5 to V_{CC} + 0.5	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

Capacitance

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
DQ capacitance (V_{DQ} = 0V)	C_{DQ}			10	pF
Input capacitance (V_{IN} = 0V)	C_{IN}			7	pF

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−2.0*	—	0.8	V
Input High Voltage	V_{IH}	2.2	—	$V_{CC}+0.3$	V
Ambient Temperature	T_A	0	—	70	°C

*For pulse width less than 20 ns. (V_{IL} Min. = −0.3V at DC level)

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

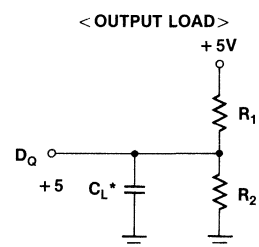
Parameter	Symbol	MB8464-12/15 Min	MB8464-12/15 Max	MB8464-12L/15L 12LL/15LL Min	MB8464-12L/15L 12LL/15LL Max	Unit	Test Conditions
Standby Supply Current	I_{SB1}		2		0.1	mA	$E_2 \leqslant 0.2V$, $\overline{E}_1 \geqslant V_{CC}-0.2V$ ($E_2 \leqslant 0.2V$ or $E_2 \geqslant V_{CC}-0.2V$)
	I_{SB2}		5		3		$\overline{E}_1 = V_{IH}$ or $E_2 = V_{IL}$
Active Supply Current	I_{CC1}		30		25	mA	$\overline{E}_1 = V_{IL}$, $E_2 = V_{IH}$ $V_{IN} = V_{IH}$ or V_{IL}, $I_{OUT} = 0mA$
Operating Supply Current	I_{CC2}		90		60	mA	Cycle = Min, Duty = 100%, $I_{OUT} = 0mA$
Input Leakage Current	I_{LI}	−1	1	−1	1	μA	$V_{IN} = 0V$ to V_{CC}
Output Leakage Current	$I_{LI/O}$	−10	10	−10	10	μA	$V_{I/O} = 0V$ to V_{CC} $\overline{E}_1 = V_{IH}$ or $E_2 = V_{IL}$ or $\overline{G} = V_{IH}$ or $\overline{W} = V_{IL}$
Output High Voltage	V_{OH}	2.4		2.4		V	$I_{OH} = -1.0$ mA
Output Low Voltage	V_{OL}		0.4		0.4	V	$I_{OL} = 2.1$ mA

Note: All voltages are referenced to V_{SS}

AC Test Conditions

Input Pulse Levels: 0.6V to 2.4V
Input Pulse Rise and Fall Times: 5 ns (Transient Time between 0.8V and 2.2V)
Timing Reference Level: Input = 0.8V, V_{IH} = 2.2V
Output: V_{OL} = 0.8V, V_{OH} = 2.0V
Output Load:

	R_1	R_2	C_L	Parameters Measured
Load I	1.8KΩ	990Ω	100 pF	except TE1LQX, TE2HQX, TG1QZ, TE1HQZ, TE2HQZ, TEHQZ, TWHQZ, TWLQX
Load II	1.8KΩ	990Ω	5 pF	TE1LQX, TE2HQX, TGTQZ, TE1HQZ, TE2HQZ, TGHQZ, TWHQX, TWLQX



*Including probe and stray capacitance

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Read Cycle *1

Parameter	Symbol	MB8464-12/12L Min	MB8464-12/12L Max	MB8464-15/15L Min	MB8464-15/15L Max	Unit
Read cycle time	TAVAX	120		150		ns
Address access time *2	TAVQV		120		150	ns
$\overline{E}_1$ access time	TE1LQV		120		150	ns
E_2 access time	TE2HQV		120		150	ns
Output enable to output valid	TGLQV		50		60	ns
Output hold from address change	TAXQX	10		10		ns
Chip enable to output low-Z *3	TE1LQX, TE2HQX	10		10		ns
Output enable to output low-Z *3	TGLQZ	5		5		ns
Chip enable to output high-Z *3	TE1HQZ, TE2LQZ		40		50	ns
Output enable to output high-Z *3	TGHQZ		40		50	ns

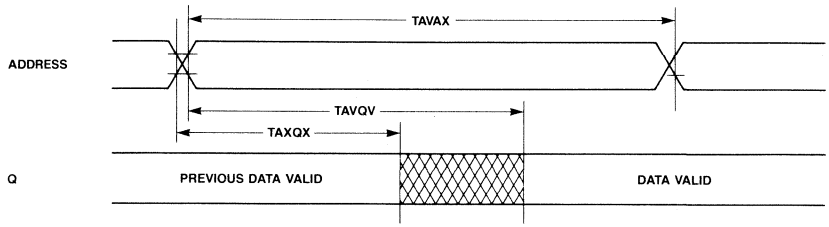
Write Cycle

Parameter	Symbol	MB8464-12/12L Min	MB8464-12/12L Max	MB8464-15/15L Min	MB8464-15/15L Max	Unit
Write cycle time	TAVAV	120		150		ns
Address valid to end of write	TAVWH, TAVE1L, TAVE2H	85		100		ns
Chip enable to end of write	TE1LE1H, TE2HE2L	85		100		ns
Data valid to end of write	TDVWH, TDVE1L, TDVE2L	40		50		ns
Data hold time	TWHDX, TE1HDX, TE2LDX	0		0		ns
Write pulse width	TWLWH	70		90		ns
Address setup time	TAVWL, TAVE1L, TAVE2H	0		0		ns
Write recovery time	TWHAX, TE1HAX, TE2LAX	0		0		ns
Write enable to output low-Z	TWHQX *3*4	5		5		ns
Write enable to output high-Z	TWLQZ *3*4		40		50	ns

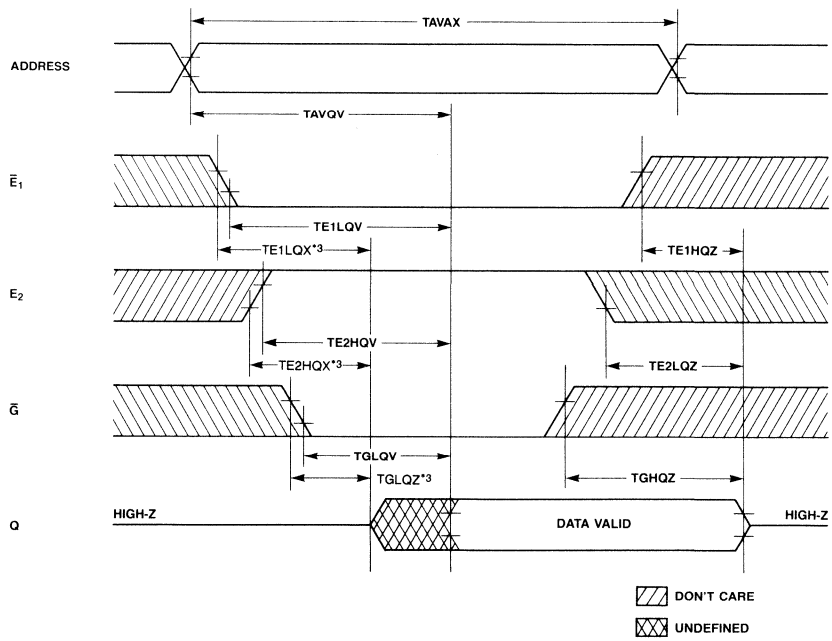
NOTE: *1 $\overline{WE}$ IS HIGH FOR READ CYCLE.
*2 DEVICE IS CONTINUOUSLY SELECTED, $\overline{CS}_1 = \overline{OE} = V_{IL}$, $CS_2 = V_{IH}$.
*3 TRANSITION IS MEASURED AT THE POINT OF ±500 mV FROM STEADY STATE VOLTAGE.
*4 If $\overline{OE}$, $\overline{CS}_1$ AND CS_2 ARE IN THE **READ** MODE DURING THIS PERIOD, I/O PINS ARE IN THE OUTPUT STATE SO THAT THE INPUT SIGNALS OF OPPOSITE PHASE TO THE OUTPUTS MUST NOT BE APPLIED.

Read Cycle Timing Diagrams

Read Cycle I *1,2



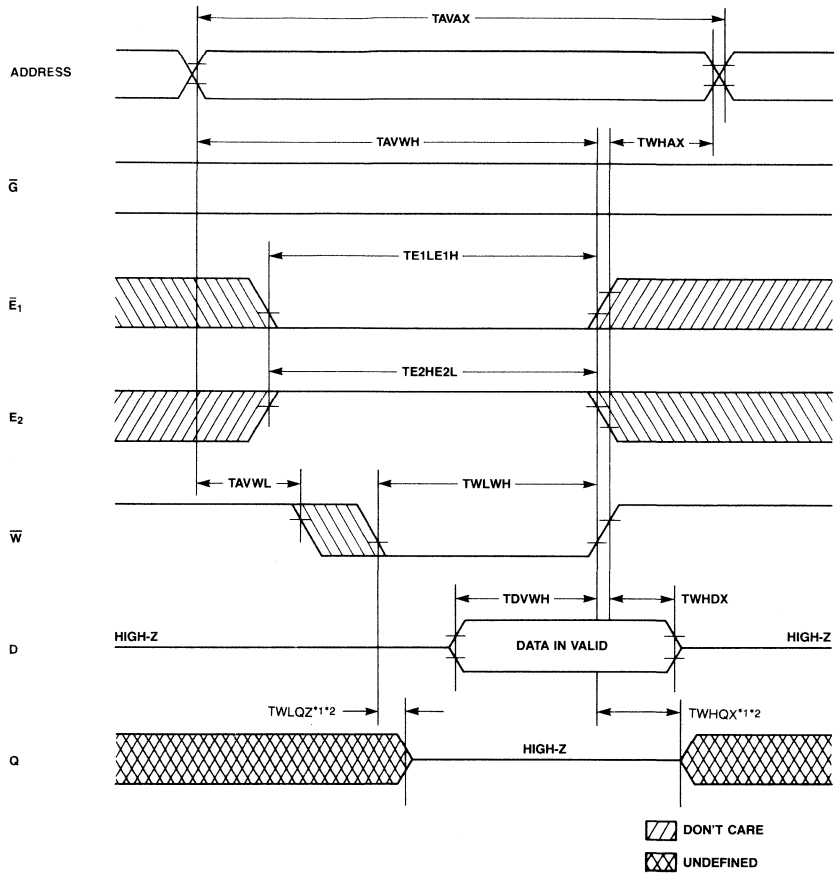
Read Cycle II *1



NOTE: *1 $\overline{W}$ IS HIGH FOR READ CYCLE.
*2 DEVICE IS CONTINUOUSLY SELECTED, $\overline{E}_1 = \overline{G} = V_{IL}$, $E_2 = V_{IH}$.
*3 TRANSITION IS MEASURED AT THE POINT OF ±500 mV FROM STEADY STATE VOLTAGE.

Write Cycle Timing Diagrams

Write Cycle I ($\overline{W}$ Controlled)

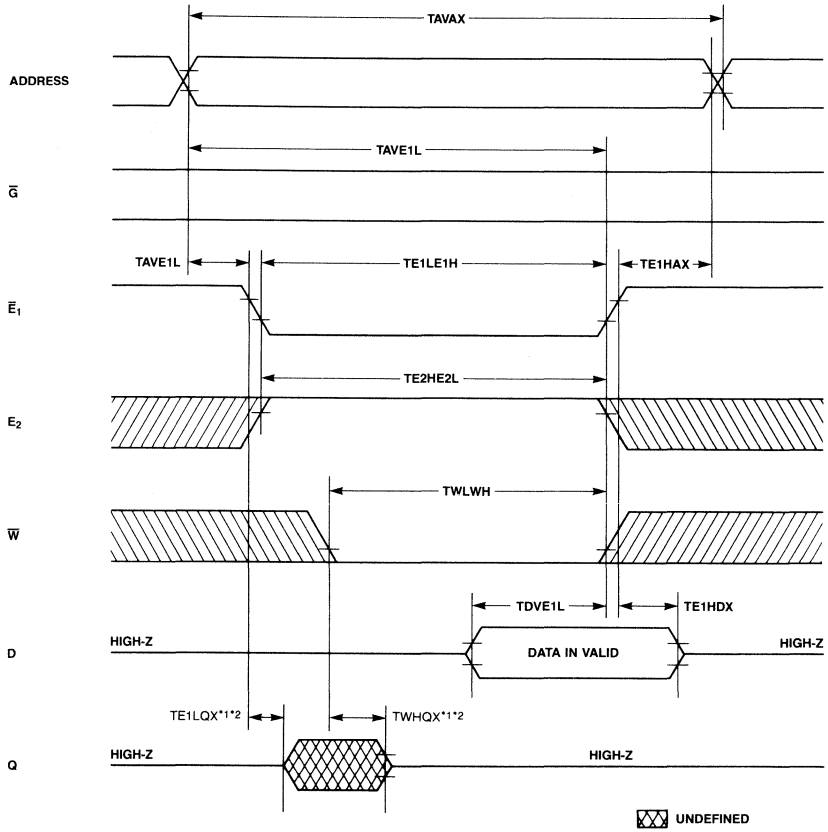


NOTE: *1 IF $\overline{G}$, $\overline{E}_1$, AND E_2 ARE IN THE READ MODE DURING THIS PERIOD, I/O PINS ARE IN THE OUTPUT STATE SO THAT THE INPUT SIGNALS OF OPPOSITE PHASE TO THE OUTPUTS MUST NOT BE APPLIED

*2 TRANSITION IS MEASURED AT THE POINT OF ±500 mV FROM STEADY STATE VOLTAGE.

Write Cycle Timing Diagrams (Continued)

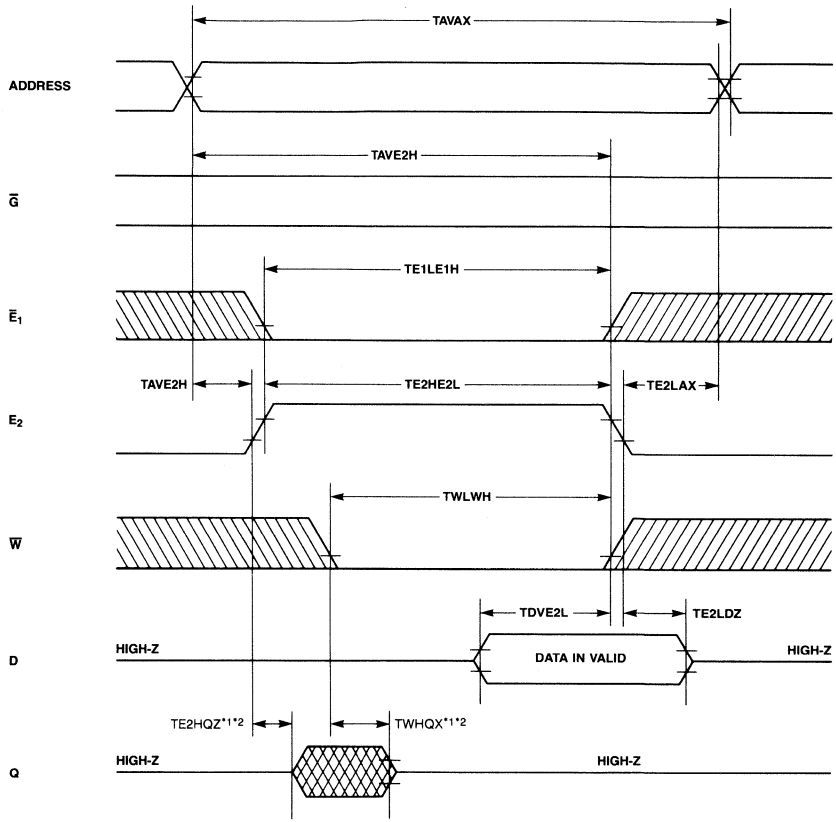
Write Cycle II ($\overline{E}_1$ Controlled)



NOTE: *1 IF $\overline{OE}$, CS_2 AND $\overline{WE}$ ARE IN THE **READ** MODE DURING THIS PERIOD, I/O PINS ARE IN THE OUTPUT STATE SO THAT THE INPUT SIGNALS OF OPPOSITE PHASE TO THE OUTPUTS MUST NOT BE APPLIED.
*2 TRANSITION IS MEASURED AT THE POINT OF ±500 mV FROM STEADY STATE VOLTAGE.

Write Cycle Timing Diagrams (Continued)

Write Cycle III (E_2 Controlled)



NOTE: *1 IF $\overline{G}$, E_2 AND $\overline{W}$ ARE IN THE READ MODE DURING THIS PERIOD, D/Q PINS ARE IN THE OUTPUT STATE SO THAT THE INPUT SIGNALS OF OPPOSITE PHASE TO THE OUTPUTS MUST NOT BE APPLIED.

*2 TRANSITION IS MEASURED AT THE POINT OF ±500 mV FROM STEADY STATE VOLTAGE.

UNDEFINED

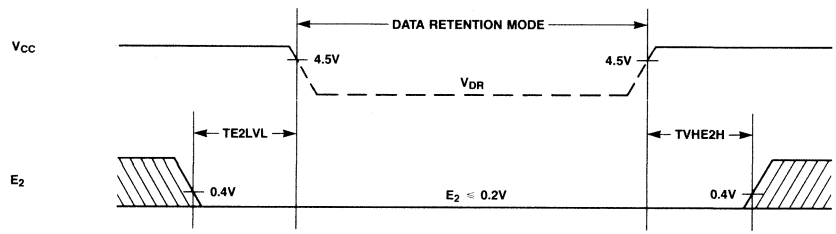
Data Retention Characteristics
(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Data Retention Supply Voltage *1		V_{DR}	2.0	5.5	V
Data Retention Supply Current *2	Standard	I_{DR}		1.0*3	mA
	L Version	I_{DR}		25*3	μA
	LL Version	I_{DR}		25*3/2*4	μA
Data Retention Setup Time		t_{DRS}	0		ns
Operation Recovery Time		t_R	t_{RC}		ns

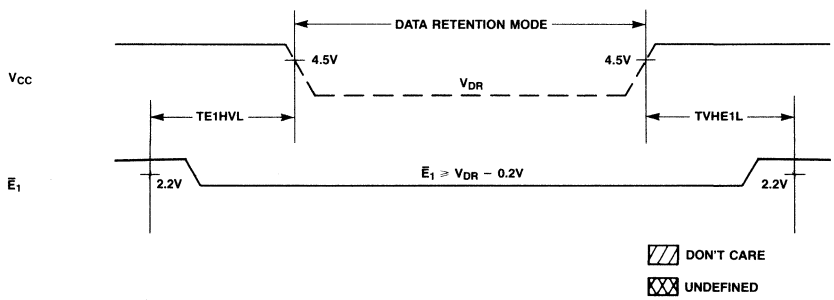
Note: *1 $\overline{E}_1$ controlled: $E_2 \leq 0.2V$
$\overline{E}_1$ controlled: $\overline{E}_1 \geq V_{DR} - 0.2V$ ($E_2 \leq 0.2V$ or $E_2 \geq V_{DR} - 0.2V$)
*2 E_2 controlled: $V_{DR} = 3.0V$, $E_2 \leq 0.2V$
$\overline{E}_1$ controlled: $V_{DR} = 3.0V$, $\overline{E}_1 \geq V_{DR} - 0.2V$ ($E_2 \leq 0.2V$ or $E_2 \geq V_{DR} - 0.2V$)
*3 For TA = 0° to 70°C
*4 For T_A = 0° to +40°C

Data Retention Timing

Data Retention I (E_2 Controlled)



Data Retention II ($\overline{E}_1$ Controlled)



Typical Characteristics Curves

Fig. 3.—NORMALIZED ACCESS TIME vs V_{CC} SUPPLY VOLTAGE

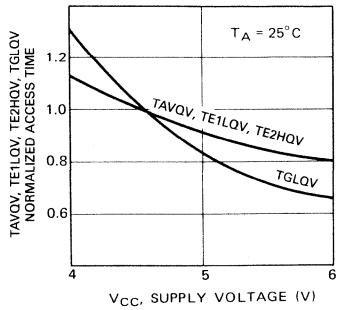


Fig. 4.—NORMALIZED ACCESS TIME vs AMBIENT TEMPERATURE

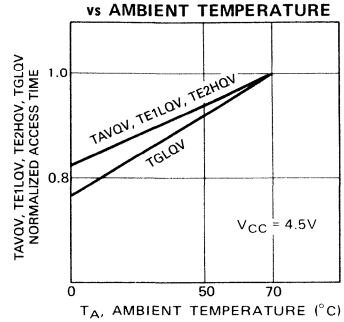


Fig. 5.—NORMALIZED POWER SUPPLY CURRENT vs V_{CC} SUPPLY VOLTAGE

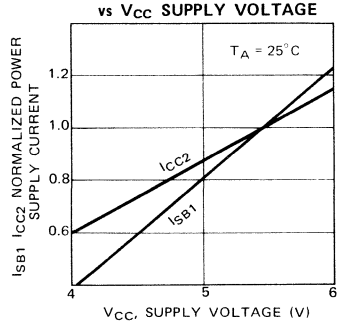


Fig. 6.—NORMALIZED POWER SUPPLY CURRENT vs AMBIENT TEMPERATURE

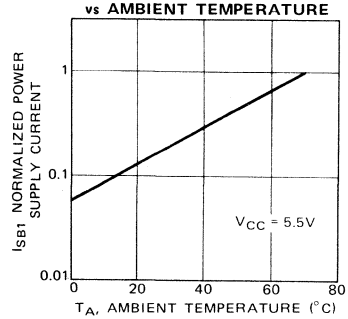


Fig. 7.—NORMALIZED POWER SUPPLY CURRENT vs AMBIENT TEMPERATURE

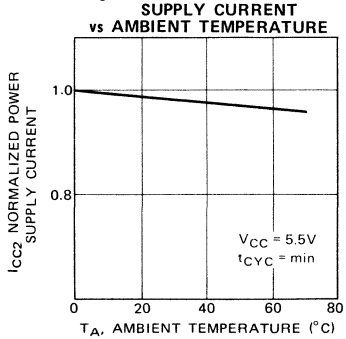
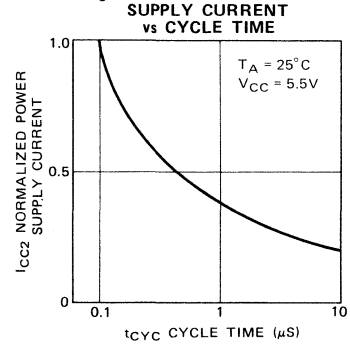
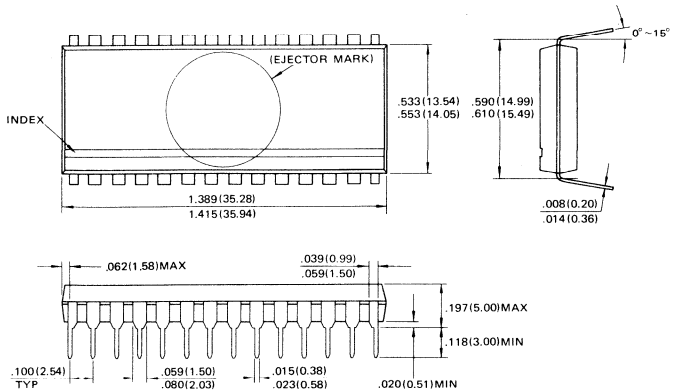


Fig. 8.—NORMALIZED POWER SUPPLY CURRENT vs CYCLE TIME

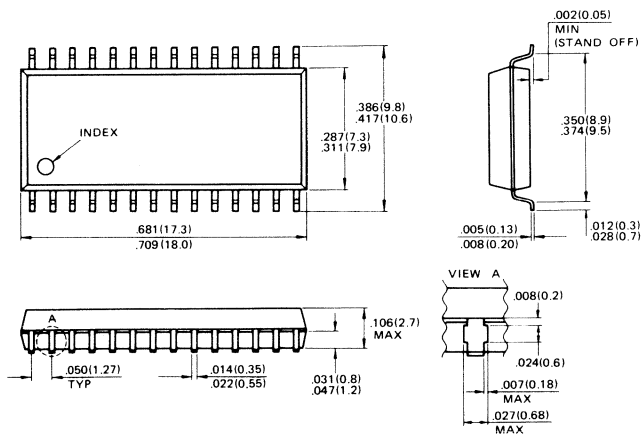


Package Dimensions
In inches (millimeters)

28-Lead Plastic
Dual In-Line Package
DIP-28P-M02

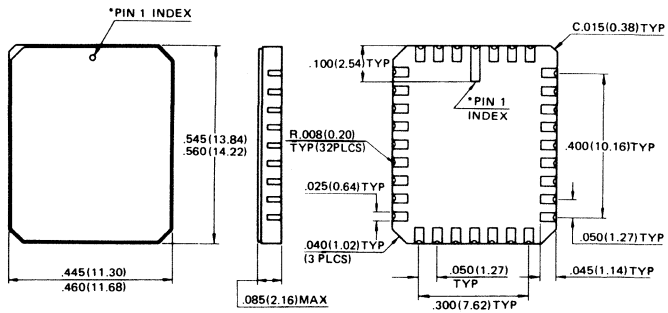


28-Lead Plastic Flat Package
FPT-28-M01



Package Dimensions
Continued

32-Pad Ceramic (Metal Seal)
Leadless Chip Carrier
LCC-32-A02



*Shape of Pin 1 index : Subject to change without notice

Preliminary

MOS Memories

FUJITSU

■ MB8464-15-X, MB8464-15-W, MB8464-20-W

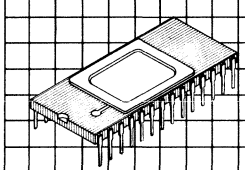
CMOS 65,536-Bit Static Random Access Memory
with Data Retention Mode

Description

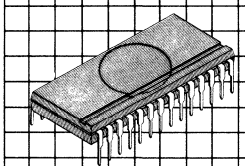
The Fujitsu MB8464-X/W is a 8,192 word by 8-bit static random access memory fabricated with a CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5 volt power supply is required.

Features

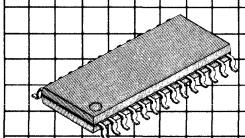
- **Organization: 8,192 words x 8-bits**
- **Fast access time: TAVQV = TELQV = 150 ns max. (MB8464-15X/W) TAVQV = TELQV = 200 ns max. (MB8464-20W)**
- **Completely static operation: No clock required**
- **TTL compatible input/output**
- **Three-state output**
- **Wide temperature range: −55 to +125°C (MB8464-15/20-W) −40 to +85°C (MB8464-15-X)**
- **Common data input/output**
- **Single +5V power supply, ±10% tolerance**
- **Low power standby: 11 mW max.**
- **Data retention: 2.0V min.**
- **Ceramic Package (28-pin) (-X, -W), LCC (32-pad) (-X, -W) Standard 28 Pin Plastic DIP (-X), and Plastic Flatpack (-X)**



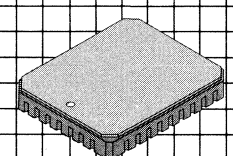
Ceramic Package DIP-28C-A07



Plastic Package DIP-28P-M02



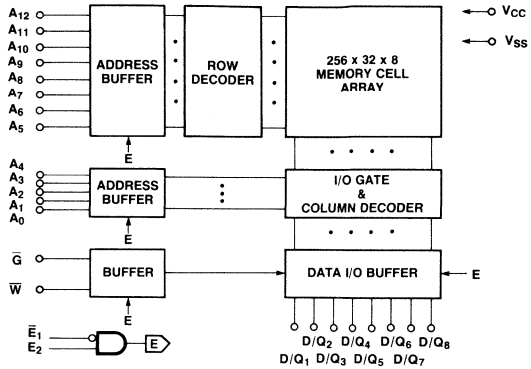
Plastic Package FPT-28P-M01

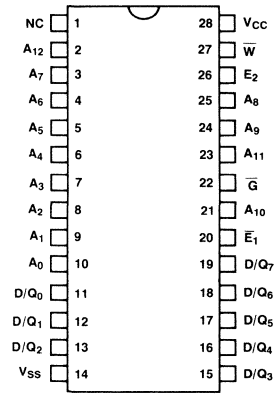


Ceramic Package (LCC-32C-A02)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

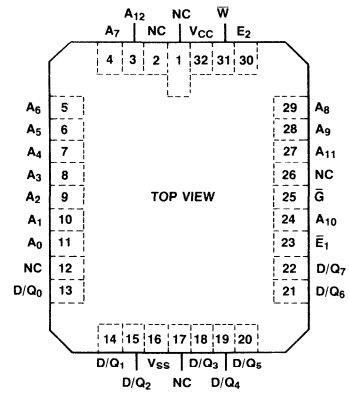
MB8464 Block Diagram and Pin Assignments





TRUTH TABLE

$\overline{E}_1$	E_2	$\overline{G}$	$\overline{W}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	X	NOT SELECTED	I_{SB}	HIGH-Z
X	L	X	X	NOT SELECTED	I_{SB}	HIGH-Z
L	H	H	H	OUT DISABLE	I_{CC}	HIGH-Z
L	H	L	H	READ	I_{CC}	Q_{OUT}
L	H	X	L	WRITE	I_{CC}	D_{IN}



Absolute Maximum Ratings
(See Note)

Rating	Symbol		Value	Unit
Storage temperature range	T_{STG}	Ceramic	−65 to +150	°C
		Plastic	−45 to +125	
Temperature under bias	T_{BIAS}	−W	−55 to +125	°C
		−X	−40 to +85	
Supply voltage	V_{CC}		−0.5 to +7.0	V
Input voltage	V_{IN}		−0.5 to V_{CC} +0.5	V
Output voltage	V_{OUT}		−0.5 to V_{CC} +0.5	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol		Min	Typ	Max	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
Input low voltage	V_{IL}		−0.3		0.6	V
Input high voltage	V_{IH}		2.4		V_{CC} +0.3	V
Ambient temperature	T_A	MB8464-15-W / MB8464-20-W	−55		+125	°C
	T_A	MB8464-15-X	−40		+85	°C

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$			10	pF
Input capacitance (V_{IN} = 0V)	C_{IN}			7	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8464 -15-X Min	MB8464 -15-X Max	MB8464 -15-X/-15-W Min	MB8464 -15-X/-15-W Max	Unit	Test Conditions
Standby supply current	I_{SB1}		0.2		2	mA	$E_2 \leq 0.2V$, $\overline{E}_1 \geq V_{CC} - 0.2V$ ($E_2 \leq 0.2V$ or $E_2 \geq V_{CC} - 0.2V$
	I_{SB2}		5		5		$\overline{E}_1 = V_{IH}$ or $E_2 = V_{IL}$
Active supply current	I_{CC1}		30		30	mA	$\overline{E}_1 = V_{IL}$, $E_2 = V_{IH}$ $V_{IN} = V_{IH}$ or V_{IL}, I_{OUT} = 0 mA
Operating supply current	I_{CC2}		70		90	mA	Cycle = min., duty = 100%, I_{OUT} = 0 mA
Input leakage current	I_{LI}	−10	10	−10	10	μA	V_{IN} = 0V to V_{CC}
Output leakage current	$I_{LI/O}$	−50	50	−50	50	μA	$V_{I/O}$ = 0V to V_{CC} $\overline{E}_1 = V_{IH}$ or $E_2 = V_{IL}$ or $\overline{G} = V_{IH}$ or $\overline{W} = V_{IL}$
Output high voltage	V_{OH}	2.4		2.4		V	I_{OH} = −1.0 mA
Output low voltage	V_{OL}		0.4		0.4	V	I_{OL} = 2.1 mA

Note: All voltages are referenced to GND.

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

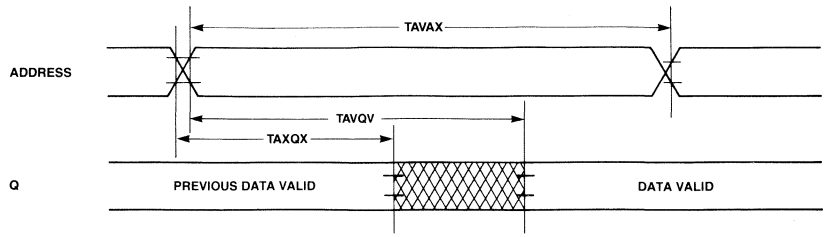
Read Cycle

Parameter	Symbol	MB8464-15-X MB8464-15-W Min	MB8464-15-X MB8464-15-W Max	MB8464-20-W Min	MB8464-20-W Max	Unit
Read cycle time	TAVAX	150		200		ns
Address access time	TAVQV		150		200	ns
$\overline{E}_1$ access time	TE1LQV		150		200	ns
E_2 access time	TE2HQV		150		200	ns
Output enable to output valid	TGLQV		60		70	ns
Output hold from address change	TAXQX	10		10		ns
Chip enable to output low-Z	TE1LQX, TE2HQX	10		10		ns
Output enable to output low-Z	TGLQZ	5		5		ns
Chip enable to output high-Z	TE1HQZ, TE2LQZ		50		60	ns
Output enable to output high-Z	TGHQZ		50		60	ns

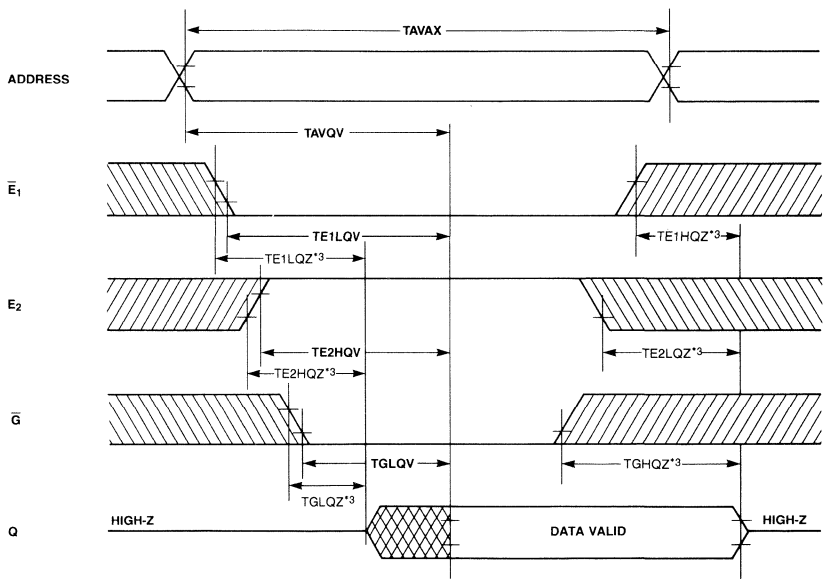
AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Read Cycle Timing Diagrams

Read Cycle I*1,2



Read Cycle II*1



NOTES: *1 $\overline{W}$ IS HIGH FOR READ CYCLE.
*2 DEVICE IS CONTINUOUSLY SELECTED, $\overline{E}_1 = \overline{G} = V_{IL}$, $E_2 = V_{IH}$.
*3 TRANSITION IS MEASURED AT THE POINT OF ±500 mV STEADY STATE VOLTAGE.

DON'T CARE
UNDEFINED

Write Cycle

Parameter	Symbol	MB8464-15-X/ MB8464-15-W Min	MB8464-15-X/ MB8464-15-W Max	MB8464-20-W Min	MB8464-20-W Max	Unit
Write cycle time	TAVAV	150		200		ns
Address valid to end of write	TAVWH TAVE1L, TAVE2H	100		140		ns
Chip enable to end of write	TE1LE1H, TE2HE2L	100		140		ns
Data valid to end of write	TDVWH TDVE1L, TDVE2H	50		60		ns

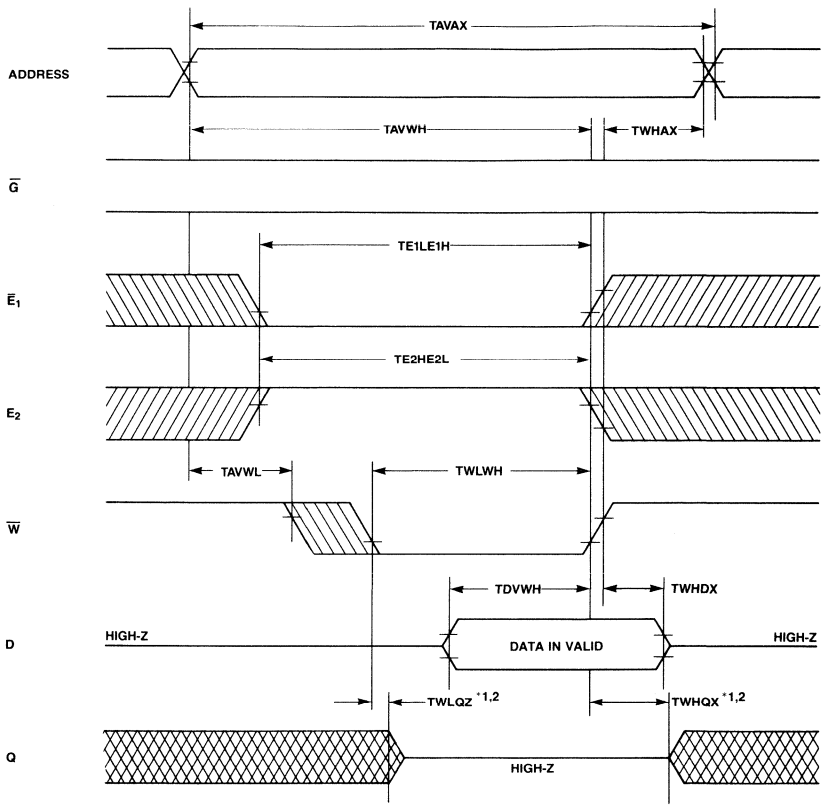
AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle (Continued)

Parameter	Symbol	MB8464-15-X/ MB8464-15-W Min	MB8464-15-X/ MB8464-15-W Max	MB8464-20-W Min	MB8464-20-W Max	Unit
Data hold time	TWHDX, TE1HDX, TE2LDX	0		0		ns
Write pulse width	TWLWH	90		100		ns
Address setup time	TAVWL, TAVE1L TAVE2H	0		10		ns
Write recovery time	TWHAX TE1HAX TE2LAX	5		5		ns
Write enable to output low-Z	TWHQX	5		5		ns
Write enable to output high-Z	TWLQZ		50		60	ns

Write Cycle Timing Diagrams

Write Cycle I ($\overline{W}$ Controlled)



NOTE: *1 IF $\overline{G}$, $\overline{E}_1$ AND E_2 ARE IN THE READ MODE DURING THIS PERIOD, DQ PINS ARE IN THE OUTPUT STATE SO THAT THE INPUT SIGNALS OF OPPOSITE PHASE TO THE OUTPUTS MUST NOT BE APPLIED.

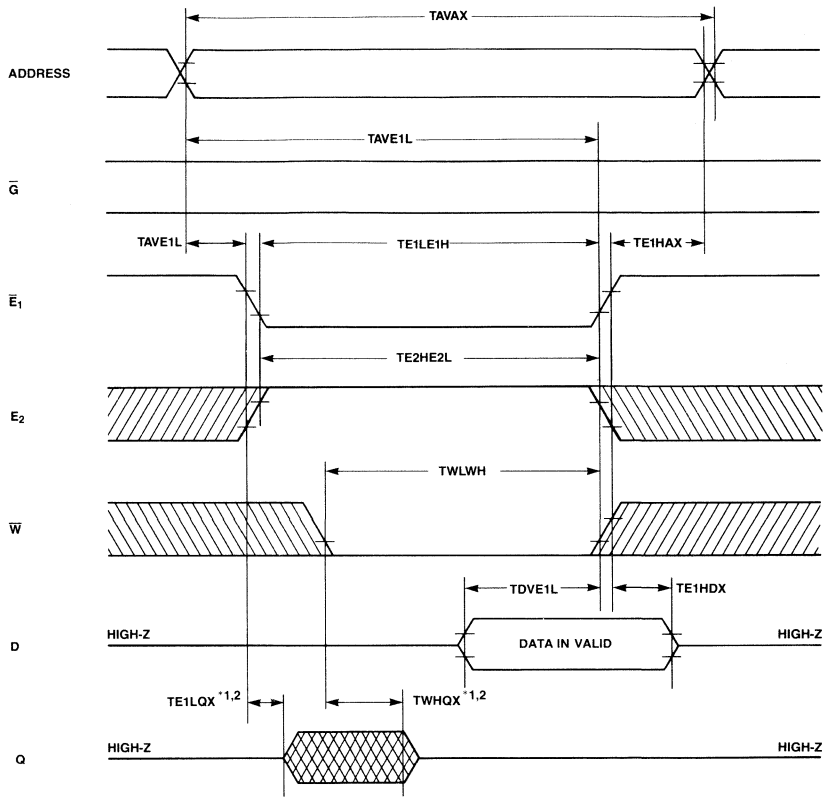
*2 TRANSITION IS MEASURED AT THE POINT OF ±500 mV FROM STEADY STATE VOLTAGE.

DON'T CARE
UNDEFINED

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle Timing Diagrams (Continued)

Write Cycle II ($\overline{E}_1$ Controlled)



NOTE: *1 IF $\overline{G}$, $\overline{E}_2$ AND $\overline{W}$ ARE IN THE READ MODE DURING THIS PERIOD,D/Q PINS ARE IN THE OUTPUT STATE SO THAT THE INPUT SIGNALS OF OPPOSITE PHASE TO THE OUTPUTS MUST NOT BE APPLIED.

*2 TRANSITION IS MEASURED AT THE POINT OF ±500 mV FROM STEADY STATE VOLTAGE.

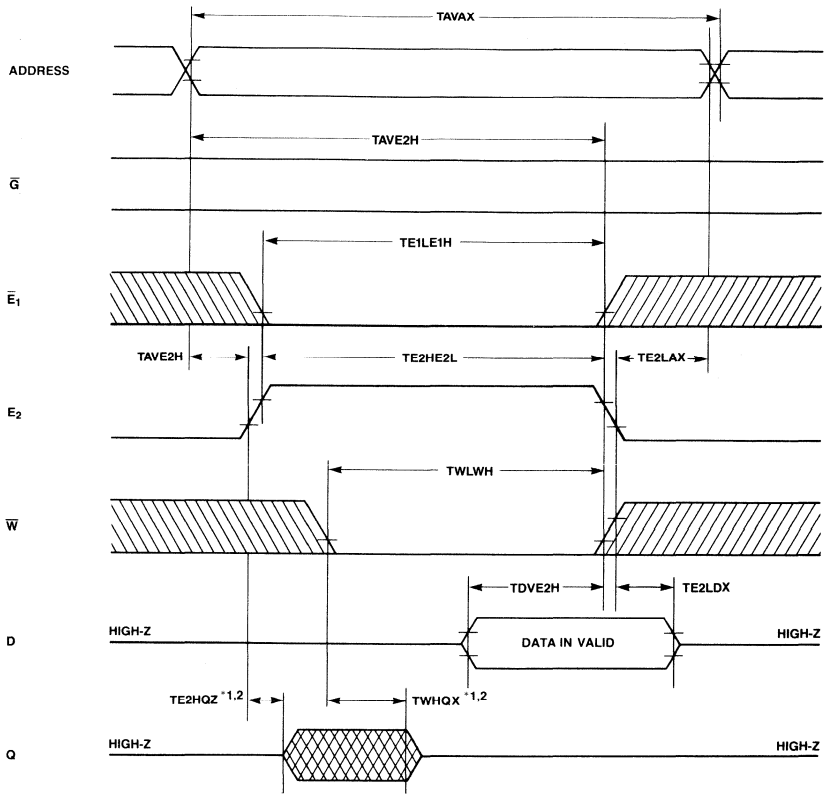
DON'T CARE

UNDEFINED

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle Timing Diagrams (Continued)

Write Cycle III (E_2 Controlled)



NOTE: *1 IF $\overline{G}$, E_2, AND $\overline{W}$ ARE IN THE READ MODE DURING THIS PERIOD, DQ PINS ARE IN THE OUTPUT STATE SO THAT THE INPUT SIGNALS OF OPPOSITE PHASE TO THE OUTPUTS MUST NOT BE APPLIED.

*2 TRANSITION IS MEASURED AT THE POINT OF ±500 mV FROM STEADY STATE VOLTAGE.

DON'T CARE

UNDEFINED

Data Retention Characteristics

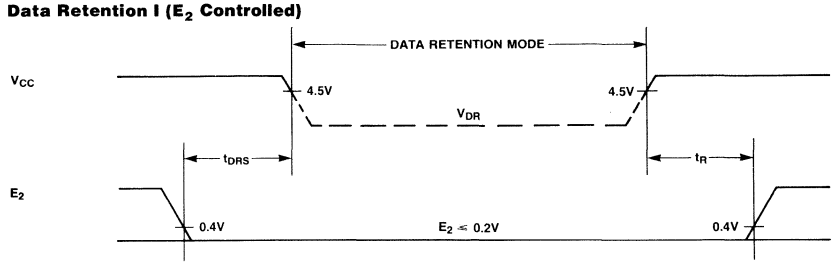
(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Max	Unit
Data retention supply voltage*1	V_{DR}	2.0	5.5	V
Data retention supply current*2	MB8464-15/20-W		0.5	mA
	MB8464-15-X		0.05	mA
Data retention setup time	TE1HVL TE2LVL	0		ns
Operation recovery time	TVHE1L TVHE2H	TAVAX		ns

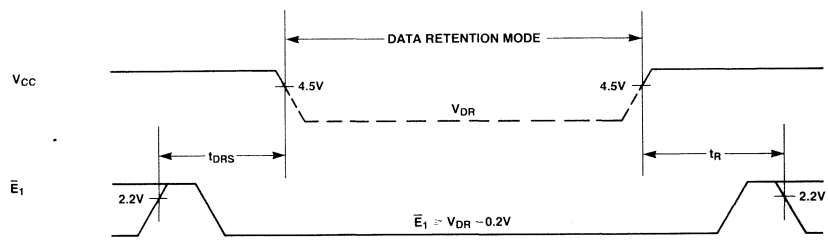
Notes: *1 E_2 controlled: $E_2 \leq 0.2V$
$\overline{E}_1$ controlled: $\overline{E}_1 \geq V_{DR} - 0.2V$ ($E_2 \leq 0.2V$ or $E_2 \geq V_{DR} - 0.2V$)
*2 E_2 controlled: $V_{DR} = 3.0V$, $E_2 \leq 0.2V$
$\overline{E}_1$ controlled: $V_{DR} = 3.0V$, $\overline{E}_1 \geq V_{DR} - 0.2V$ ($E_2 \leq 0.2V$ or $E_2 \geq V_{DR} - 0.2V$)

Data Retention Timing

Data Retention I (E_2 Controlled)



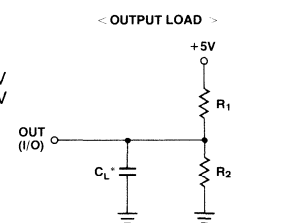
Data Retention II ($\overline{E}_1$ Controlled)



AC Test Conditions

Input Pulse Levels: 0.4V to 2.6V
Input Pulse Rise and Fall Times: 5 ns (Transient Time between 0.6V and 2.4V)
Timing Reference Levels: Input: $V_{IL} = 0.6V$, $V_{IH} = 2.4V$
Output: $V_{OL} = 0.8V$, $V_{OH} = 2.0V$
Output Load:

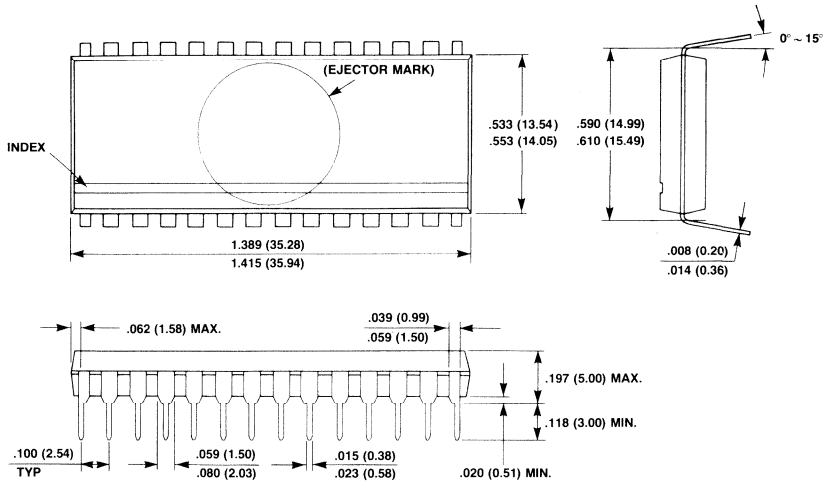
	R_1	R_2	C_L	Parameters Measured
Load I	1.8KΩ	990Ω	100 pF	except TE1LQX TE1HQZ, TE2LQZ, TGHQZ, TWLQZ, and TWHQX
Load II	1.8KΩ	990Ω	5 pF	TE1LQX, TE1HQZ, TE2LQZ, TGHQZ, TWLQZ, and TWHQX



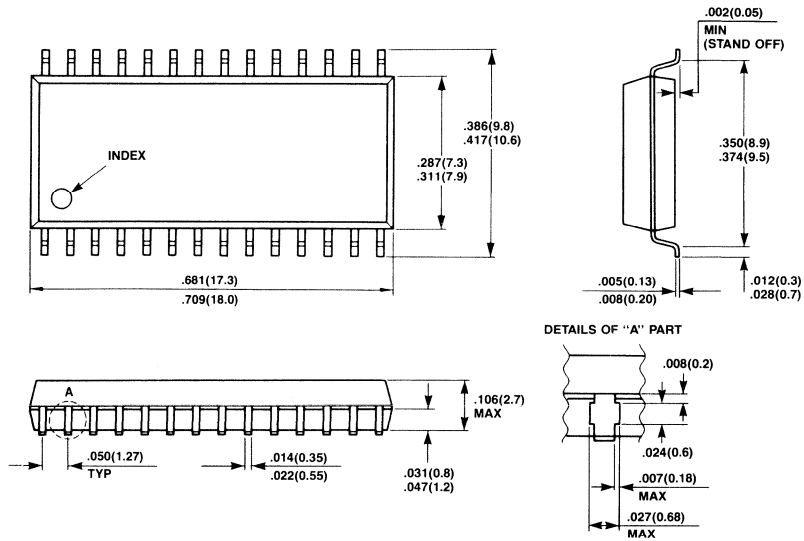
*INCLUDING PROBE AND STRAY CAPACITANCE

Package Dimensions
Dimensions in inches
(millimeters)

28-Lead Plastic Dual-In-Line Package
(Case No.: DIP-28P-M02)

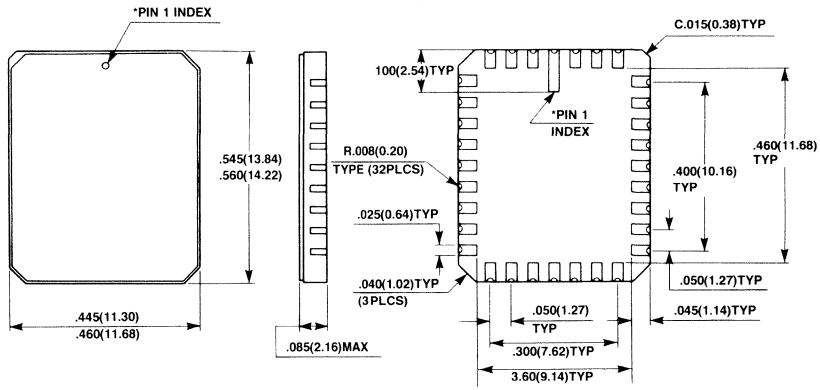


28-Lead Plastic Flat Package
(Case No.: FPT-28P-M01)

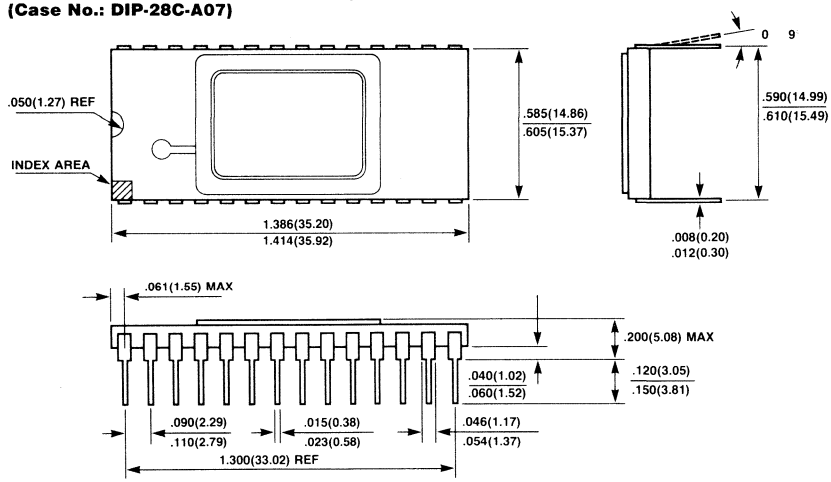


Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

32-Pad Ceramic (Metal Seal) Leadless Chip Carrier
(Case No.: LCC-32C-A02)



28-Lead Ceramic Dual-In-Line Package
(Case No.: DIP-28C-A07)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

Preliminary

MOS Memories

FUJITSU

■ MB8464A-70, MB8464A-70L, MB8464A-70LL
MB8464A-10, MB8464A-10L, MB8464A-10LL
MB8464A-15, MB8464A-15L, MB8464A-15LL

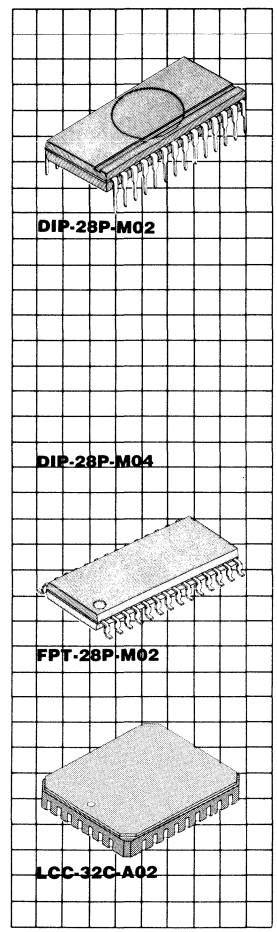
8,192 Words x 8-Bit CMOS
Static RAM with Low Power
and Data Retention

Description

The Fujitsu MB8464A is a 8,192-word by 8-bit static random access memory fabricated with a CMOS silicon gate process.

The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5V volt power supply is required.

The MB8464A is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. The MB8464A offers the advantages of low power dissipation, low cost, and high performance.

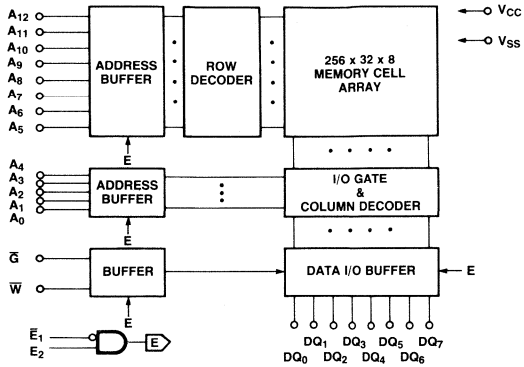


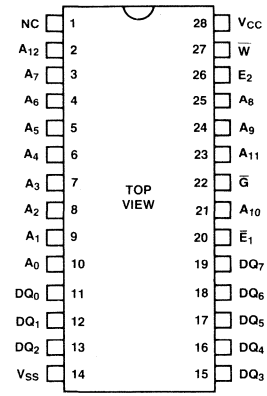
Features

- **Organization: 8,192 words x 8-bits**
- **Fast access time: TAVQV = TELQV = 70 ns max. (MB8464A-70/70L/70LL) TAVQV = TE1QV = 100 ns max. (MB8464A-10/10L/10LL) TAVQV=TELQV=150 ns max. (MB8464A-15/15L/15LL)**
- **Completely static operation: No clock required**
- **TTL compatible input/output**
- **Three-state output**
- **Common data input/output**
- **Single +5V power supply, ±10% tolerance**
- **Low power standby: 11 mW max. (70/10/15) 0.55 mW max. (70L/10L/15L) (70LL/10LL/15LL)**
- **Data retention: 2.0V min.**
- **Package 28 pin DIP 600 mil, 300 mil 28 pin plastic flatpak 32 pin LCC**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

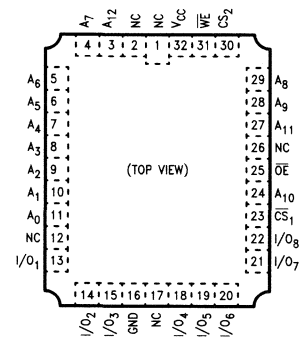
MB8464A Block Diagram and Pin Assignments





TRUTH TABLE

$\overline{E_1}$	E_2	$\overline{G}$	$\overline{W}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	X	NOT SELECTED	I_{SB}	HIGH-Z
X	L	X	X	NOT SELECTED	I_{SB}	HIGH-Z
L	H	H	H	OUT DISABLE	I_{CC}	HIGH-Z
L	H	L	H	READ	I_{CC}	Q_{OUT}
L	H	X	L	WRITE	I_{CC}	IN



Absolute Maximum Ratings
(See Note)

Rating	Symbol		Value	Unit
Storage temperature range	t_{STG}	Ceramic	−65 to +150	°C
		Plastic	−45 to +125	
Temperature under bias	t_{BIAS}		−10 to +85	°C
Supply voltage	V_{CC}		−0.5 to +7.0	V
Input voltage	V_{IN}		−0.5* to V_{CC} +0.5	V
Output voltage	V_{OUT}		−0.5 to V_{CC} +0.5	V

* −2.0 V for pulse width less than 20 ns.

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	+5.0	5.5	V
Input low voltage	V_{IL}	−2.0*		0.8	V
Input high voltage	V_{IH}	2.2		V_{CC} +0.3	V
Ambient temperature	t_A	0		70	°C

* −2.0 V Min. for pulse width less than 20 ns. (V_{IL} Min. = −0.3 V at DC level)

Capacitance

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$			8	pF
Input capacitance (V_{IN} = 0V)	C_{IN}			6	pF

DC Characteristics

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8464A-70/10 Min	MB8464A-70/10 Max	MB8464A-70L/10L/15L 70LL/10LL/15LL Min	MB8464A-70L/10L/15L 70LL/10LL/15LL Max	Unit	Test Conditions
Standby supply current	I_{SB1}		2		0.1	mA	$E_2 \leqslant 0.2V$, $\overline{E}_1 \geqslant V_{CC} - 0.2V$ ($E_2 \leqslant 0.2V$ or $E_2 \geqslant V_{CC} - 0.2V$)
	I_{SB2}		3		3		$\overline{E}_1 = V_{IH}$ or $E_2 = V_{IL}$
Active supply current	I_{CC1}		55		55	mA	$\overline{E}_1 = V_{IL}$, $E_2 = V_{IH}$ $V_{IN} = V_{IH}$ or V_{IL}, I_{OUT} = 0 mA
Operating supply current	I_{CC2}		65		65	mA	Cycle = min., Duty = 100%, I_{OUT} = 0 mA
Input leakage current	I_{LI}	−1	1	−1	1	μA	V_{IN} = 0V to V_{CC}
Output leakage current	$I_{LI/O}$	−2	2	−2	2	μA	$V_{I/O}$ = 0V to V_{CC} $\overline{E}_1 = V_{IH}$ or $E_2 = V_{IL}$ or $\overline{G} = V_{IH}$ or $\overline{W} = V_{IL}$
Output high voltage	V_{OH}	2.4		2.4		V	I_{OH} = −1.0 mA
Output low voltage	V_{OL}		0.4		0.4	V	I_{OL} = 2.1 mA

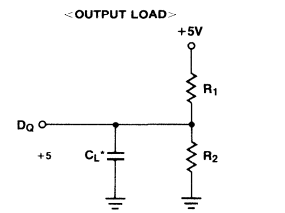
Note: All voltages are referenced to V_{SS}

AC Test Conditions

Input pulse levels: 0.6V to 2.4V
Input pulse rise and fall times: 6 ns (transient time between 0.8V and 2.2V)
Timing reference levels: Input: V_{IL} = 0.8V, V_{IH} = 2.2V
Output: V_{OL} = 0.8V, V_{OH} = 2.0V

Output load:

	R_1	R_2	C_L	Parameters Measured
Load 1	1.8Ω	990Ω	100 pF	except TE1LQX, TE2HQX, TE1HQZ, TE2LQZ, TGHQZ TWHQK, TWLQZ
Load II	1.8Ω	990Ω	5 pF	TE1LQX, TE1LQZ, TELQZ, TE1HQZ, TE2LQZ, TGHQZ, TWLQZ, TWHQX



*INCLUDING PROBE AND STRAY CAPACITANCE

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

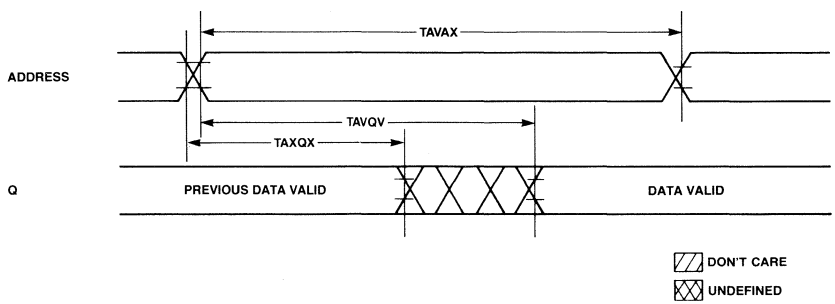
Read Cycle

Parameter	Symbol	MB8464A -70/70L/70LL Min	MB8464A -70/70L/70LL Max	MB8464A -100/100L/100LL Min	MB8464A -100/100L/100LL Max	MB8464A -150/150L/150LL Min	MB8464A -150/150L/150LL Max	Unit
Read cycle time	TAVAX	70		100		150		ns
Address access time	TAVQV		70		100		150	ns
$\overline{E}_1$ access time	TE1LQV		70		100		150	ns
E_2 access time	TE2HQV		70		100		150	ns
Output enable to output valid	TGLQV		35		45		55	ns
Output hold from address change	TAXQX	10		10		10		ns
Chip enable to output low-Z*	TE1LQX TE2HQX	10		10		10		ns
Output enable to output low-Z*	TGLQZ	5		5		5		ns
Chip enable to output high-Z*	TE1HQZ TE2LQZ		35		35		40	ns
Output enable to output high-Z*	TGHQZ		30		35		40	ns

Note: * Transition is measured at the point of ±500 mV from steady.

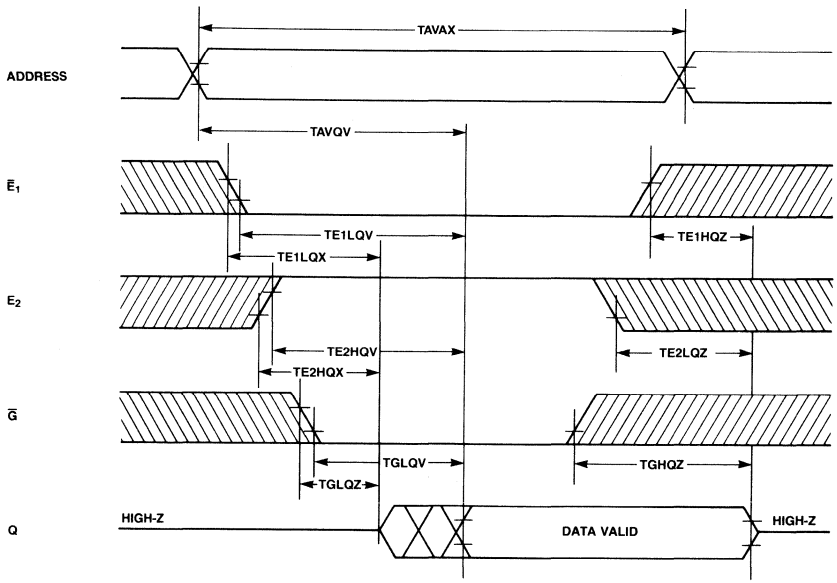
Read Cycle Timing Diagrams

Read Cycle I*[1,2]



AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Read Cycle II[*1]



Notes: *1 $\overline{W}$ IS HIGH FOR READ CYCLE.
*2 DEVICE IS CONTINUOUSLY SELECTED, $\overline{E}_1 = \overline{G} = V_{IL}$, $E_2 = V_{IH}$.

DON'T CARE
UNDEFINED

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle

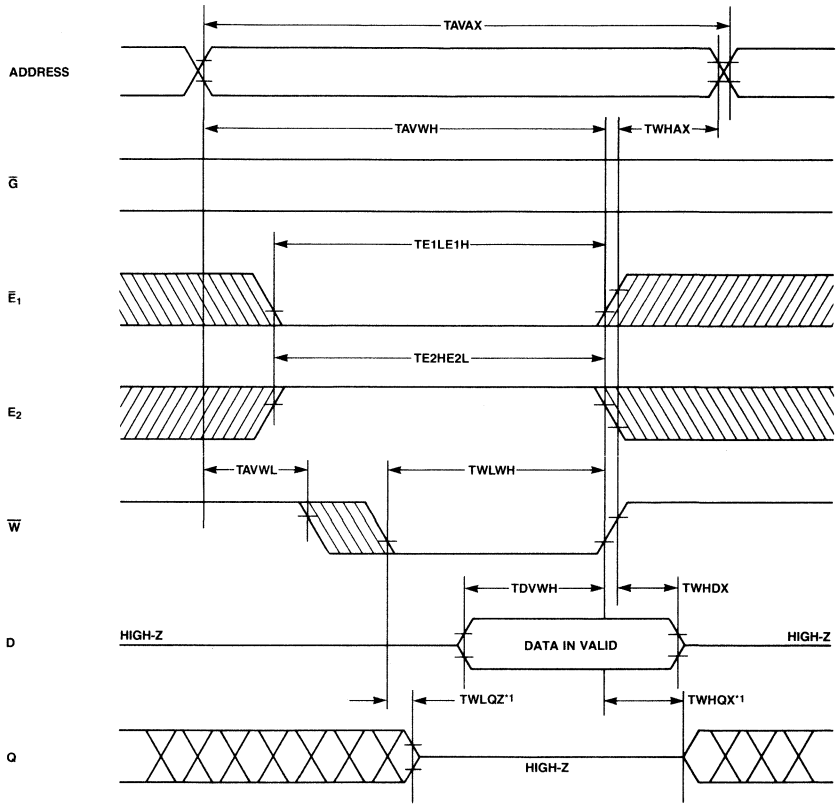
Parameter	Symbol	MB8464A -70/70L/70LL Min	MB8464A -70/70L/70LL Max	MB8464A -100/100L/100LL Min	MB8464A -100/100L/100LL Max	MB8464A -150/150L/150LL Min	MB8464A -150/150L/150LL Max	Unit
Write cycle time	TAVAX	70		100		150		ns
Address valid to end of write	TAVWH TAVE1L TAVE2H	60		80		100		ns
Chip enable to end of write	TE1LE1H TE2HE2L	60		80		100		ns
Data valid to end of write	TDVWH TDVE1L TDVE2H	30		35		40		ns
Data hold time	TWHDX TE1HDX TE2LDX	5		5		5		ns
Write pulse width	TWLWH	60		70		90		ns
Address setup time	TAVWL TAVE1L TAVE2H	0		0		0		ns
Write recovery time	TWHAX TE1HAX TE2LAX	10		10		10		ns
Write enable to output low-Z*	TWHQX	5		5		5		ns
Write enable to output high-Z*	TWLQZ		30		35		40	ns

*Transition is measured at the point of ±500 mV steady state voltage.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle Timing Diagrams

Write Cycle I ($\overline{W}$ Controlled)

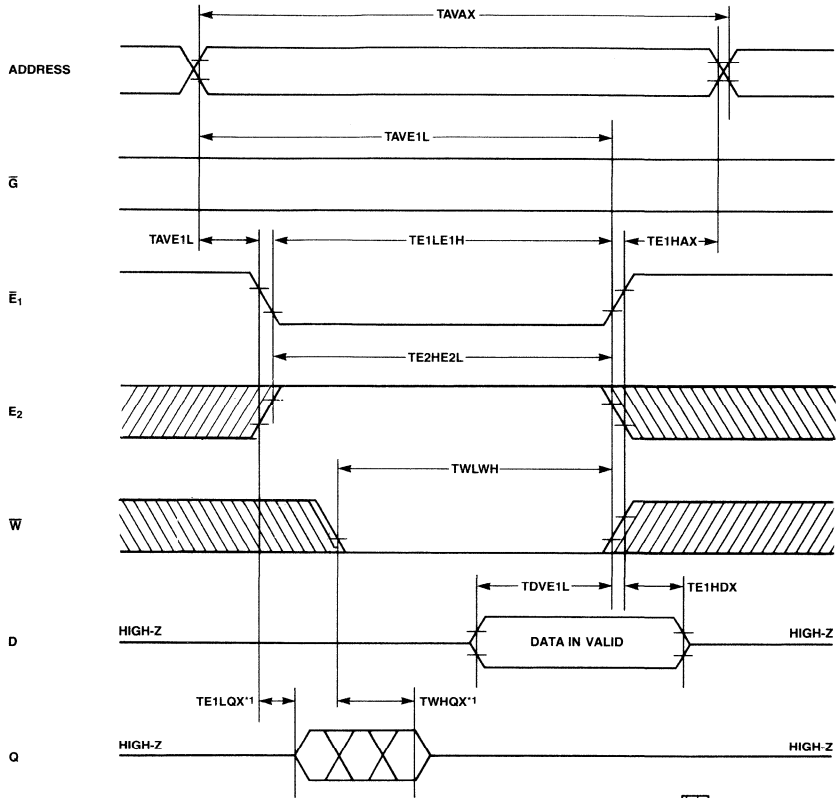


Note: *1 IF $\overline{G}$, $\overline{E}_1$ AND E_2 ARE IN THE READ MODE DURING THIS PERIOD, DQ PINS ARE IN THE OUTPUT STATE SO THAT THE INPUT SIGNALS OF OPPOSITE PHASE TO THE OUTPUTS MUST NOT BE APPLIED.

DON'T CARE
UNDEFINED

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

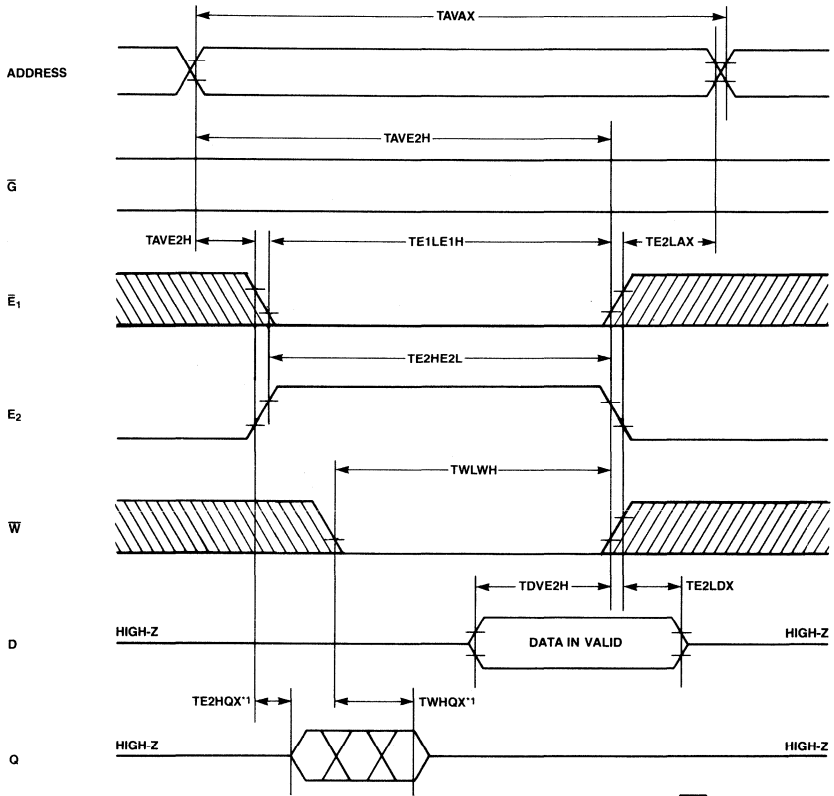
Write Cycle II ($\overline{E}_1$ Controlled)



Note: *1 IF $\overline{G}$, E_2 AND $\overline{W}$ ARE IN THE READ MODE DURING THIS PERIOD, DQ PINS ARE IN THE OUTPUT STATE SO THAT THE INPUT SIGNALS OF OPPOSITE PHASE TO THE OUTPUTS MUST NOT BE APPLIED.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle III (E_2 Controlled)



Note: *1 IF $\overline{G}$, $\overline{E}_1$ AND $\overline{W}$ ARE IN THE READ MODE DURING THIS PERIOD, DQ PINS ARE IN THE OUTPUT STATE SO THAT THE INPUT SIGNALS OF OPPOSITE PHASE TO THE OUTPUTS MUST NOT BE APPLIED.

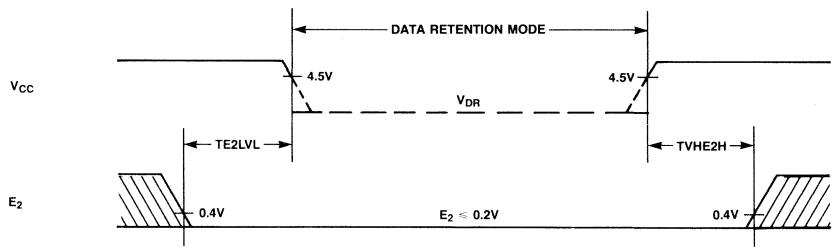
Data Retention Characteristics
(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Typ	Max	Unit
Data retention supply voltage*1		V_{DR}	2.0		5.5	V
Data retention supply current*2	Standard	I_{DR}			1.0	ma
	L-Version*3/LL*4			1.0	25/2	μA
Data retention setup time		TE1HVL TE2LVL	0			ns
Operation recovery time		TVHE1L TVHE2H	TAVAX			

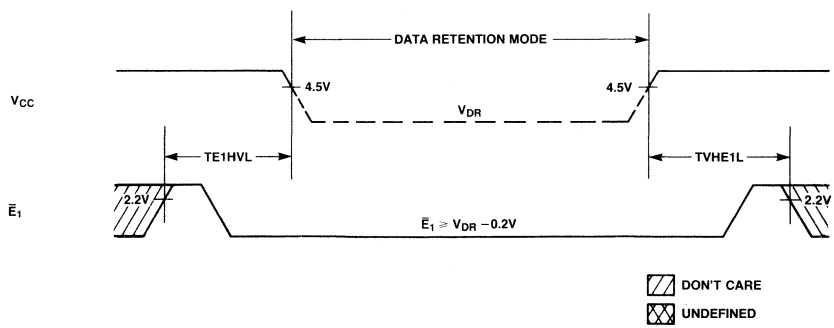
Notes: *1 E_2 controlled: $E_2 \leq 0.2V$
$\bar{E}_1$ controlled: $\bar{E}_1 \geq V_{DR} - 0.2V$ ($E_2 \leq 0.2V$ or $E_2 \geq V_{DR} - 0.2V$)
*2 E_2 controlled: $V_{DR} = 3.0V$, $E_2 \leq 0.2V$
$\bar{E}_1$ controlled: $V_{DR} = 3.0V$, $\bar{E}_1 \geq V_{DR} - 0.2V$ ($E_2 \leq 0.2V$ or $E_2 \geq V_{DR} - 0.2V$)
*3 For $T_A = 0°$ to $70°C$
*4 For $T_A = 0°C$ to $40°C$, $V_{DR} = 3.0$ V

Data Retention Timing

Data Retention I (E_2 Controlled)

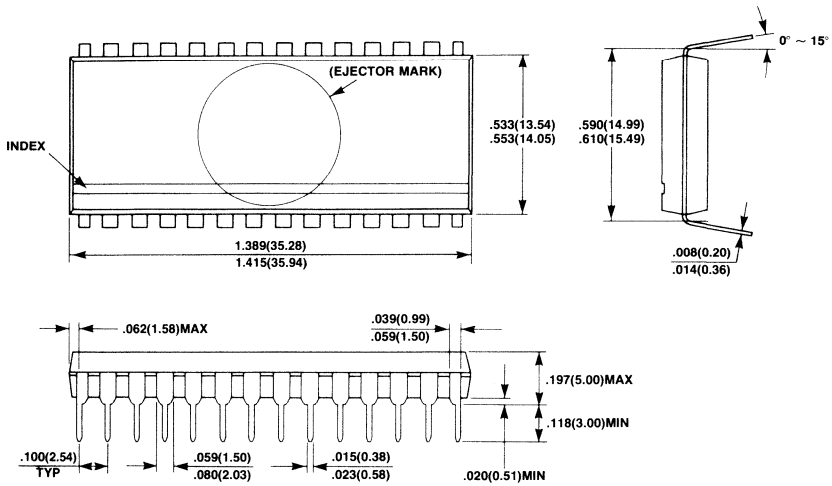


Data Retention II ($\bar{E}_1$ Controlled)

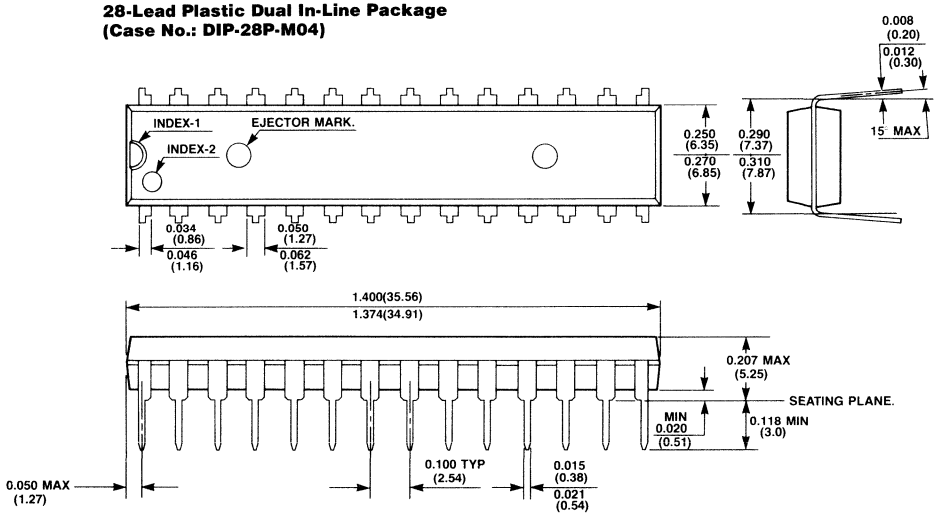


Package Dimensions
Dimensions in inches
(millimeters)

28-Lead Plastic Dual In-Line Package
(Case No.: DIP-28P-M02)

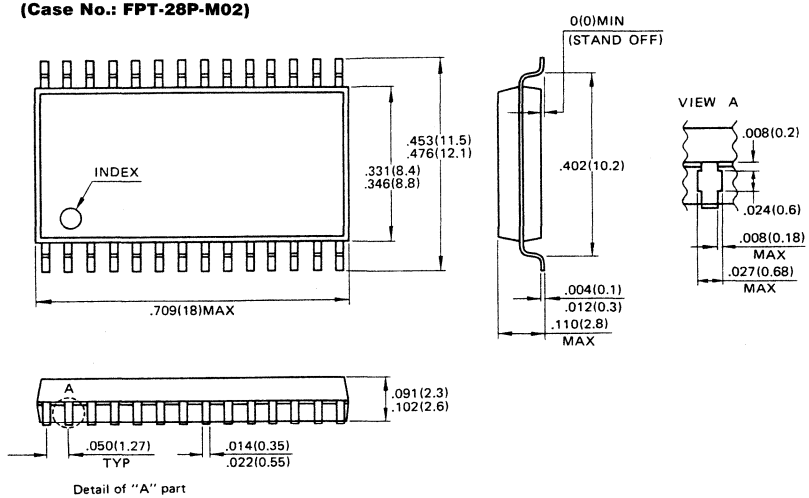


28-Lead Plastic Dual In-Line Package
(Case No.: DIP-28P-M04)

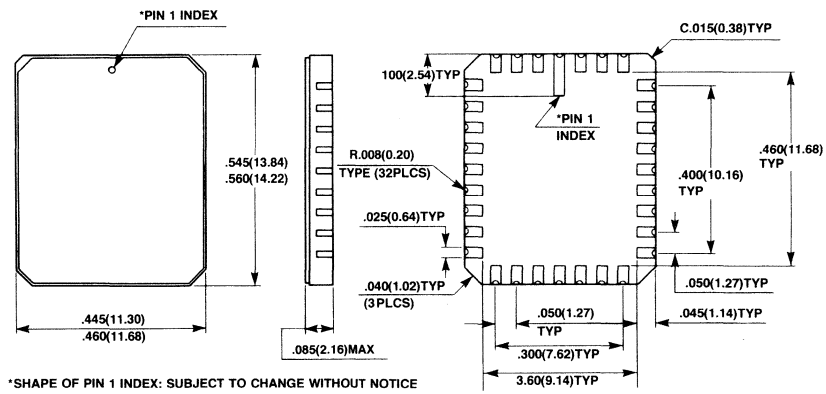


Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

28-Lead Plastic Flat Package
(Case No.: FPT-28P-M02)



32-Pad Ceramic (Metal Seal) Leadless Chip Carrier
(Case No.: LCC-32C-A02)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

Preliminary

MOS Memories

FUJITSU

■ MB8464A-10-W, MB8464A-15-W

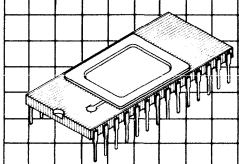
CMOS 65,536-Bit Static
Random Access Memory
with Data Retention Mode

Description

The Fujitsu MB8464A-W is a 8,192-word by 8-bit static random access memory fabricated with a CMOS silicon gate process.

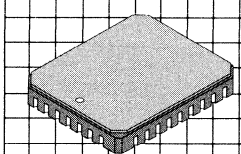
The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5 volt power supply is required.

The MB8464A-W is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost, and high performance.



DIP-28C-A07

DIP-28C-A08

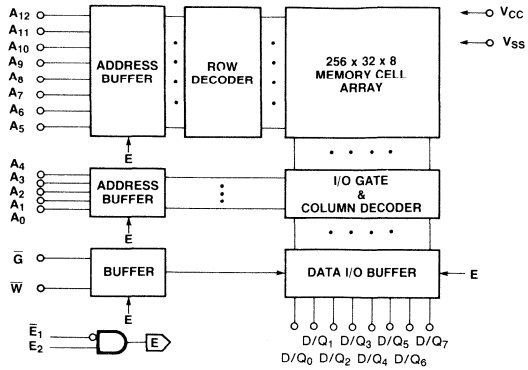


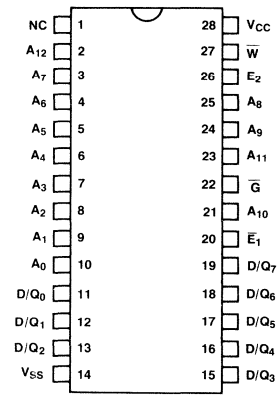
LCC-32C-A02

Features

- **Organization: 8,192 words x 8-bits**
- **Fast access time:**
  TAVQV = TELQV = 100 ns max. (MB8464A-10-W)
  TAVQV = TELQV = 150 ns max. (MB8464A-15-W)
- **Completely static operation: No clock required**
- **TTL compatible input/output**
- **Three-state output**
- **Common data input/output**
- **Single +5V power supply, ±10% tolerance**
- **Low power standby: 11 mW max.**
- **Data retention: 2.0V min.**
- **28-pin ceramic package (300 mil width) (600 mil width)**
- **32-pad leadless chip carrier**
- **Pin compatible with MB8464-W**

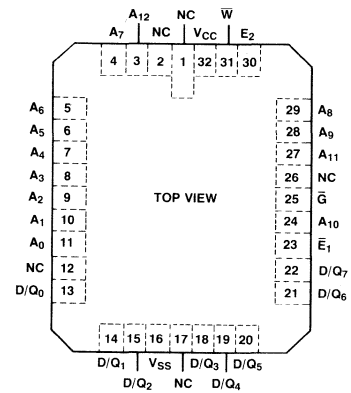
MB8464A-W Block Diagram and Pin Assignment





TRUTH TABLE

$\overline{E}_1$	E_2	$\overline{G}$	$\overline{W}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	X	NOT SELECTED	I_{SB}	HIGH-Z
X	L	X	X	NOT SELECTED	I_{SB}	HIGH-Z
L	H	H	H	OUT DISABLE	I_{CC}	HIGH-Z
L	H	L	H	READ	I_{CC}	Q_{OUT}
L	H	X	L	WRITE	I_{CC}	IN



Absolute Maximum Ratings
(See note)

Rating	Symbol	Value	Unit
Storage temperature range	T_{STG}	−65 to +150	°C
Temperature under bias	T_{BIAS}	−55 to +125	°C
Supply voltage	V_{CC}	−0.5 to +7.0	V
Input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
Output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low voltage	V_{IL}	−0.3		0.6	V
Input high voltage	V_{IH}	2.4		V_{CC} + 0.3	V
Ambient temperature	T_A	−55		+125	°C

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
I/O capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$			8	pF
Input capacitance (V_{IN} = 0V)	C_{IN}			6	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8464A-10-W MB8464A-15-W Min	Max	Unit	Test Condition
Standby supply current	I_{SB1}		2	mA	$E_2 \leq 0.2V$, $\overline{E}_1 \geq V_{CC} - 0.2V$ ($E_2 \leq 0.2V$ or $E_2 \geq V_{CC} - 0.2V$)
	I_{SB2}		5	mA	$\overline{E}_1 = V_{IH}$ or $E_2 = V_{IL}$
Active supply current	I_{CC1}		70	mA	$\overline{E}_1 = V_{IL}$, $E_2 = V_{IH}$ $V_{IN} = V_{IH}$ or V_{IL}, I_{OUT} = 0 mA
Operating supply current	I_{CC2}		90	mA	Cycle = min., duty = 100%, I_{OUT} = 0 mA
Input leakage current	I_{LI}	−10	10	μA	V_{IN} = 0V to V_{CC}
Output leakage current	$I_{LI/O}$	−50	50	μA	$V_{I/O}$ = 0V to V_{CC} $\overline{E}_1 = V_{IH}$ or $E_2 = V_{IL}$ or $\overline{G} = V_{IH}$ or $\overline{W} = V_{IL}$
Output high voltage	V_{OH}	2.4		V	I_{OH} = −1.0 mA
Output low voltage	V_{OL}		0.4	V	I_{OL} = 2.1 mA

Note: All voltages are referenced to V_{SS}

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Read Cycle

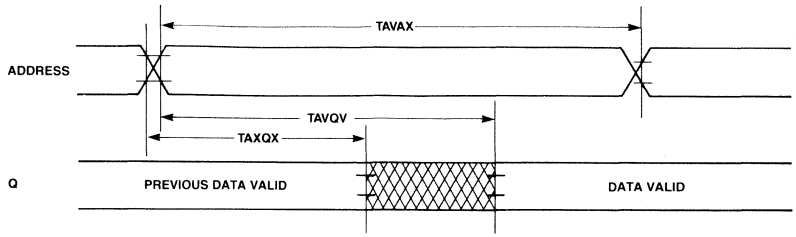
Parameter	Symbol	MB8464A-10-W Min	MB8464A-10-W Max	MB8464A-15-W Min	MB8464A-15-W Max	Unit
Read cycle time	TAVAX	100		150		ns
Address access time	TAVQV		100		150	ns
$\overline{E}_1$ access time	TE1LQV		100		150	ns
E_2 access time	TE2HQV		100		150	ns
Output enable to output valid	TGLQV		45		60	ns
Output hold from address change	TAXQX	10		10		ns
Chip enable to output low-Z*	TE1LQX TE2HQX	10		10		ns
Output enable to output low-Z*	TGLQZ	5		5		ns
Chip enable to output high-Z*	TE1HQZ TE2LQZ		40		50	ns
Output enable to output high-Z*	TGHQZ		40		50	ns

Note: * Transition is measured at the point of +500 mV from steady state voltage.

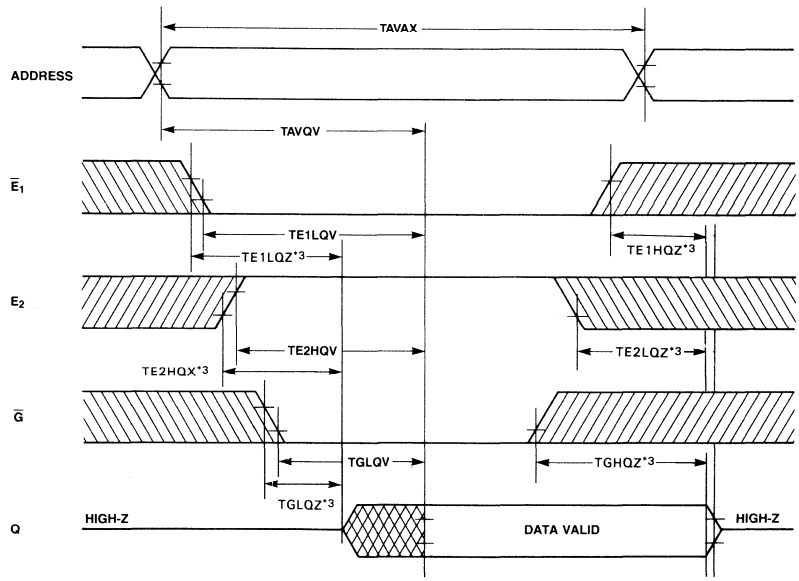
AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted)

Read Cycle Timing Diagrams

Read Cycle I*1,2



Read Cycle II*1



NOTES: *1 $\overline{W}$ IS HIGH FOR READ CYCLE.
*2 DEVICE IS CONTINUOUSLY SELECTED, $\overline{E}_1 = \overline{G} = V_{IL}$, $E_2 = V_{IH}$.
*3 TRANSITION IS MEASURED AT THE POINT OF ±500 mV STEADY STATE VOLTAGE.

DON'T CARE
UNDEFINED

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted)

Write Cycle

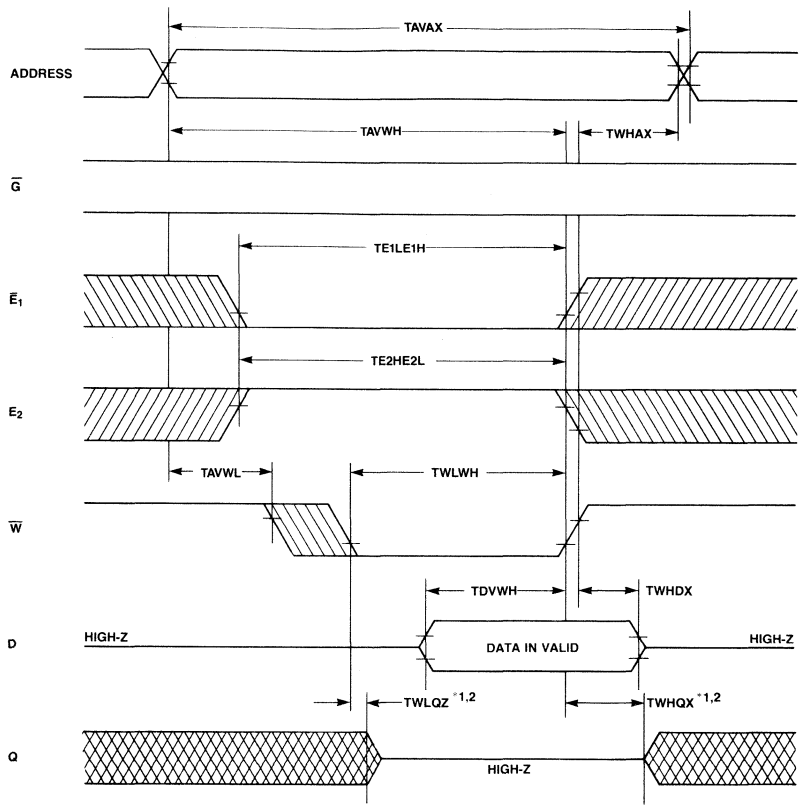
Parameter	Symbol	MB8464A-10-W Min	MB8464A-10-W Max	MB8464A-15-W Min	MB8464A-15-W Max	Unit
Write cycle time	TAVAX	100		150		ns
Address valid to end of write	TAVWH, TAVE1L, TAVE2H	80		100		ns
Chip enable to end of write	TE1LE1H, TE2H2EL	80		100		ns
Data valid to end of write	TDVWH, TDVE1L, TDVE2H	40		50		ns
Data hold time	TWHDX, TE1HDX, TE2LDX	5		5		ns
Write pulse width	TWLWH	60		70		ns
Address setup time	TAVWL, TAVE1L, TAVE2H	0		10		ns
Write recovery time	TWHAX, TE1HAX, TE2LAX	10		10		ns
Write enable to output low-Z*	TWHQX	5		5		ns
Write enable to output high-Z*	TWLQZ		40		50	ns

*TRANSITION IS MEASURED AT THE POINT OF ±500 mV STEADY STATE VOLTAGE.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted)

Write Cycle Timing Diagrams

Write Cycle I ($\overline{W}$ Controlled)



NOTE: *1 IF $\overline{G}$, $\overline{E}_1$ AND E_2 ARE IN THE READ MODE DURING THIS PERIOD, DQ PINS ARE IN THE OUTPUT STATE SO THAT THE INPUT SIGNALS OF OPPOSITE PHASE TO THE OUTPUTS MUST NOT BE APPLIED.

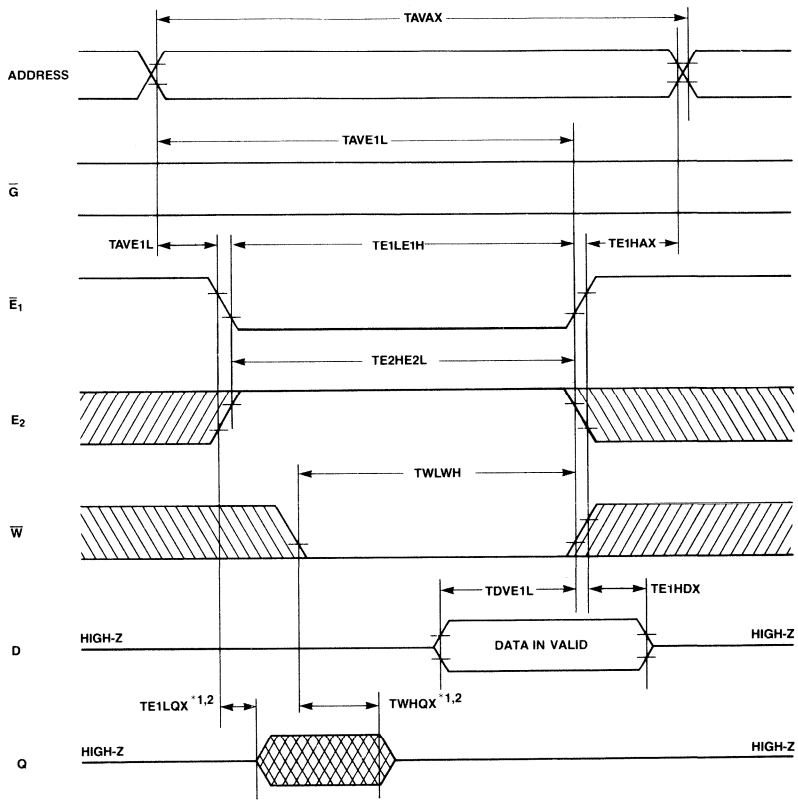
*2 TRANSITION IS MEASURED AT THE POINT OF ±500 mV FROM STEADY STATE VOLTAGE.

DON'T CARE

UNDEFINED

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted)

Write Cycle II ($\overline{E}_1$ Controlled)



NOTE: *1 IF $\overline{G}$, $\overline{E}_2$ AND $\overline{W}$ ARE IN THE READ MODE DURING THIS PERIOD, D/Q PINS ARE IN THE OUTPUT STATE SO THAT THE INPUT SIGNALS OF OPPOSITE PHASE TO THE OUTPUTS MUST NOT BE APPLIED.

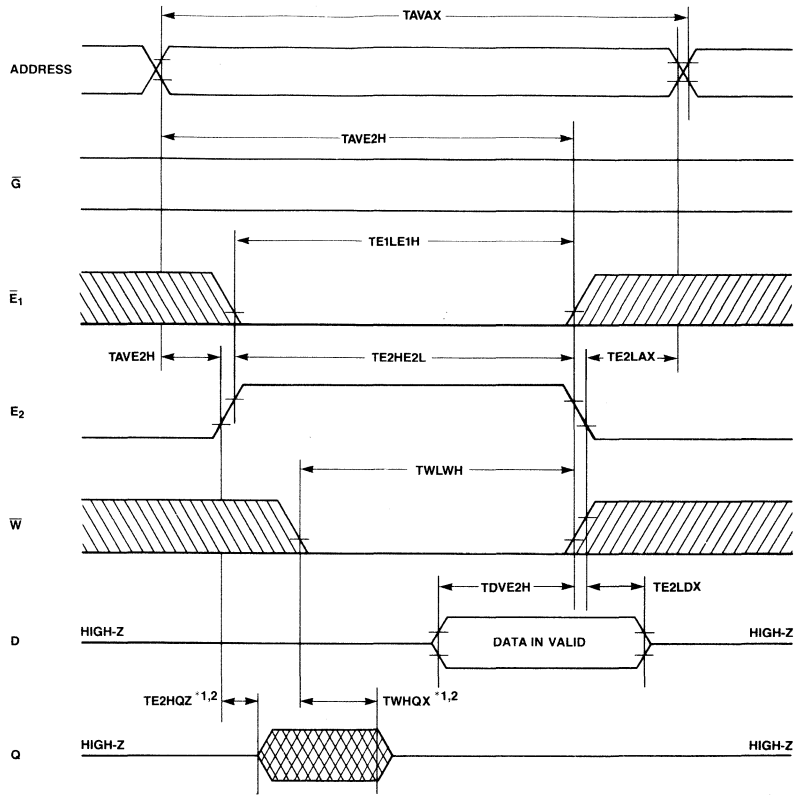
*2 TRANSITION IS MEASURED AT THE POINT OF ±500 mV FROM STEADY STATE VOLTAGE.

DON'T CARE

UNDEFINED

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted)

Write Cycle III (E_2 Controlled)



NOTE: *1 IF $\overline{G}$, E_2, AND $\overline{W}$ ARE IN THE READ MODE DURING THIS PERIOD, DQ PINS ARE IN THE OUTPUT STATE SO THAT THE INPUT SIGNALS OF OPPOSITE PHASE TO THE OUTPUTS MUST NOT BE APPLIED.

*2 TRANSITION IS MEASURED AT THE POINT OF ±500 mV FROM STEADY STATE VOLTAGE.

DON'T CARE

UNDEFINED

Data Retention Characteristics
(Recommended operating conditions unless otherwise noted)

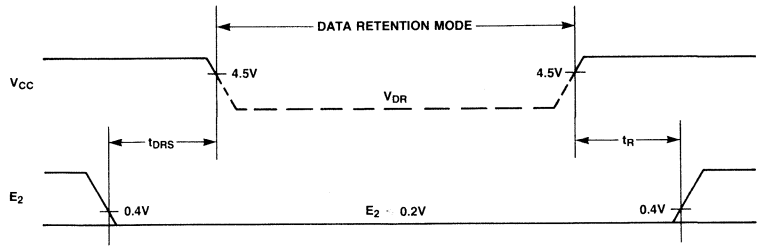
Parameter		Symbol	Min	Max	Unit
Data retention supply voltage*1		V_{DR}	2.0	5.5	V
Data retention supply current*2	Standard	I_{DR}		0.5	mA
Data retention setup time		TE1HVL, TE2LVL	0		ns
Operation recovery time		TVHE1L, TVHE2H	TAVAX		

Notes: *1 E_2 controlled: $E_2 \leqslant 0.2V$
$\overline{E}_1$ controlled: $\overline{E}_1 \geqslant V_{DR} - 0.2V$ ($E_2 \leqslant 0.2V$ or $E_2 \geqslant V_{DR} - 0.2V$)
*2 E_2 controlled: $V_{DR} = 3.0V$, $E_2 \leqslant 0.2V$
$\overline{E}_1$ controlled: $V_{DR} = 3.0V$, $\overline{E}_1 \geqslant V_{DR} - 0.2V$ ($E_2 \leqslant 0.2V$ or $E_2 \geqslant V_{DR} - 0.2V$)

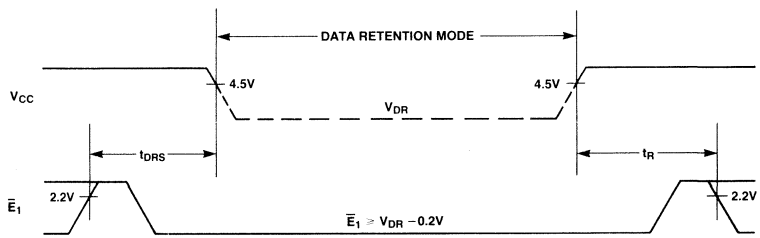
Data Retention Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted)

Data Retention Timing

Data Retention I (E_2 Controlled)



Data Retention II ($\overline{E}_1$ Controlled)

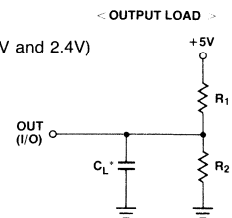


AC Test Conditions

Input Pulse Levels: 0.4V to 2.6V
Input Pulse Rise and Fall Times: 5 ns (Transition time between 0.6V and 2.4V)
Timing Reference Levels: Input: V_{IL} = 0.6V, V_{IH} = 2.4V
Output: V_{OL} = 0.8V, V_{OH} = 2.0V

Output Load:

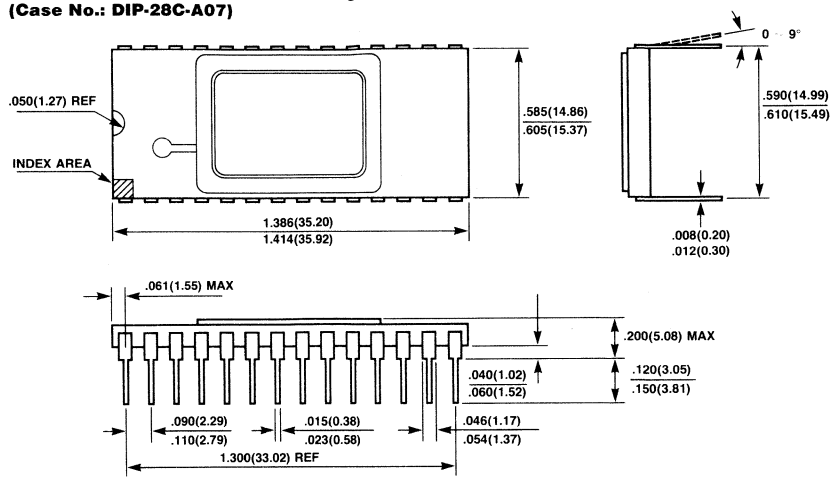
	R_1	R_2	C_L	PARAMETERS MEASURED
LOAD I	1.8 KΩ	990 Ω	100 pF	EXCEPT TEHQX, TGLQZ, TE1HQZ, TGHQZ, TWHQX AND TWLQZ
LOAD II	1.8 KΩ	990 Ω	5 pF	TE1LQX, TGLQZ, TE1HQZ, TGHQZ, TWHQX AND TWLQZ



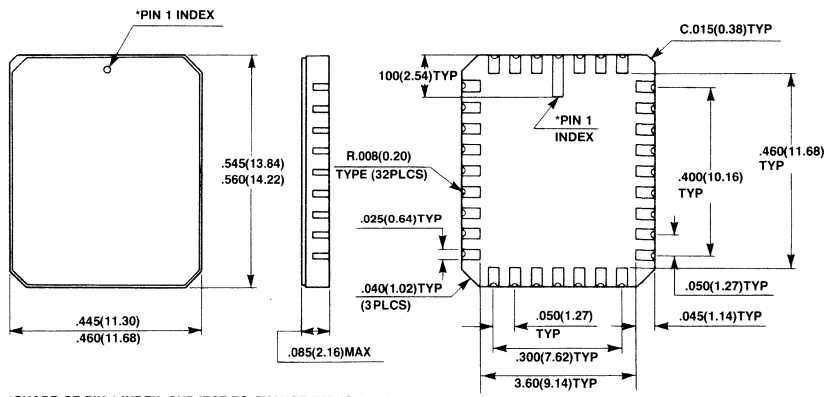
*INCLUDING PROBE AND STRAY CAPACITANCE

Package Dimensions
Dimensions in inches
(millimeters)

28-Lead Ceramic Dual-In-Line Package
(Case No.: DIP-28C-A07)



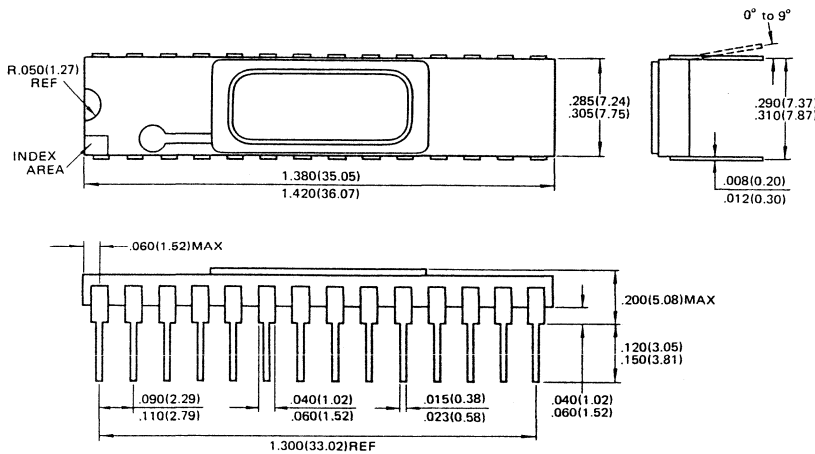
32-PAD Ceramic (Metal Seal) Leadless Chip Carrier
(Case No. LCC-32C-A02)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

Package Dimensions
(Continued)
Dimensions in inches
(millimeter)

28-Lead Ceramic (Metal Seal) Dual In-Line Package
(Case No.: DIP-28C-A08)



Preliminary

MOS Memories

FUJITSU

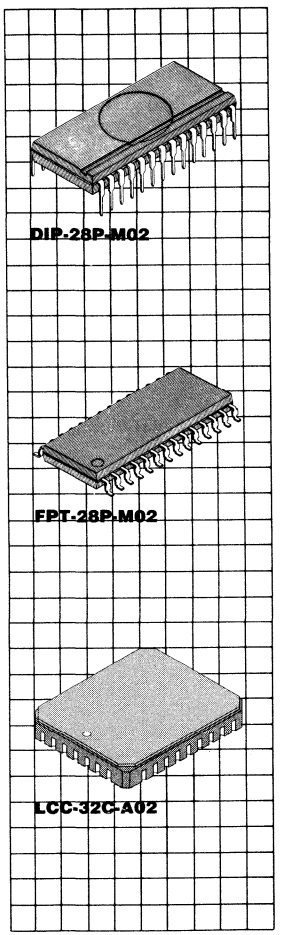
■ MB84256-10, MB84256-10L, MB84256-15, MB84256-15L

CMOS 262,144-Bit Static Random Access Memory with Data Retention Mode

Description

The Fujitsu MB84256 is a 32,768-words by 8-bits static random access memory fabricated with a CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5 volt power supply is required.

The MB84256 is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

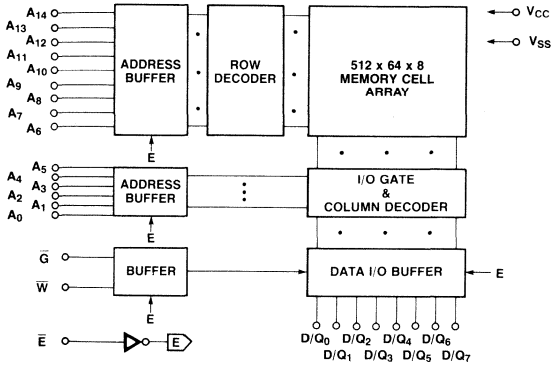


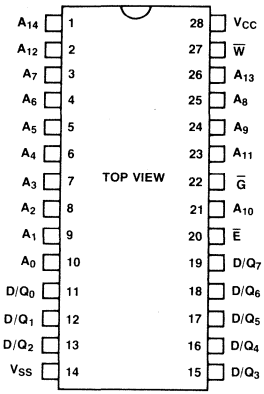
Features

- **Organization: 32,768 words x 8-bits**
- **Fast access time: TAVQV = TELQV = 100 ns max. (MB84256-10/10L) TAVQV = TELQV = 150 ns max. (MB84256-15/15L)**
- **Completely static operation: No clock required TTL compatible input/output**
- **Three-state output**
- **Common data input/output**
- **Single +5V power supply ±10% tolerance**
- **Low power standby: 5.5 mW max. (MB84256-10/15) 1.1 mW max. (MB84256-10L/15L)**
- **Data retention: 2.0V min.**
- **Standard 28-pin DIP (600 mil)**
- **Standard 28-pin Plastic Flat pack (450 mil)**
- **Standard 32-pad LCC**

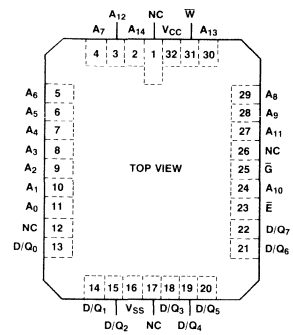
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB84256 Block Diagram and Pin Assignments





TRUTH TABLE					
$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	NOT SELECTED	I_{SB}	HIGH-Z
L	H	H	OUT DISABLE	I_{CC}	HIGH-Z
L	L	H	READ	I_{CC}	QOUT
L	X	L	WRITE	I_{CC}	IN



Absolute Maximum Ratings
(See note)

Rating		Symbol	Value	Unit
Storage Temperature range	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−40 to +125	
Temperature under bias		T_{BIAS}	−10 to +85	°C
Supply voltage		V_{CC}	−0.5 to +7.0	V
Input voltage		V_{IN}	−0.5 to V_{CC} + 0.5	V
Output voltage		V_{OUT}	−0.5 to V_{CC} + 0.5	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low voltage	V_{IL}	2.0*		0.8	V
Input high voltage	V_{IH}	2.2		V_{CC} + 0.3	V
Ambient temperature	T_A	0		70	°C

* −2.0 V Min. for pulse width less than 20 ns (V_{IL} Min. = −0.3 V at DC level)

Capacitance

(T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
D/Q capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$			8	pF
Input capacitance (V_{IN} = 0V)	C_{IN}			7	pF

DC Characteristics

(Recommended operating conditions otherwise noted.)

Parameter	Symbol	MB84256-10/15 Min	MB84256-10/15 Max	MB84256-10L/15L Min	MB84256-10L/15L Max	Unit	Test Conditions
Standby supply current	I_{SB1}		1		0.2	mA	$\overline{E} \geqslant V_{CC} - 0.2$
	I_{SB2}		3		3		$\overline{E} = V_{IH}$
Active supply current	I_{CC1}		45		45	mA	$\overline{E} = V_{IL}$, $V_{IN} = V_{IH}$ or V_{IL}, I_{OUT} = 0 mA
Operating supply current	I_{CC2}		70		70		Cycle = min., Duty = 100%, I_{OUT} = 0 mA
Input leakage current	I_{LI}	−1	1	−1	1	μA	V_{IN} = 0V to V_{CC}
Output leakage current	$I_{LI/O}$	−1	1	−1	1	μA	$V_{I/O}$ = 0V to V_{CC} $\overline{E} = V_{IH}$ $\overline{G} = V_{IH}$ or $\overline{W} = V_{IL}$
Input high voltage	V_{OH}	2.4		2.4		V	I_{OH} = −1.0 mA
Output low voltage	V_{OL}		0.4		0.4	V	I_{OL} = 2.1 mA

Note: All voltages are referenced to V_{SS}

AC Characteristics

(Recommended operating conditions unless otherwise noted)

Read Cycle*1

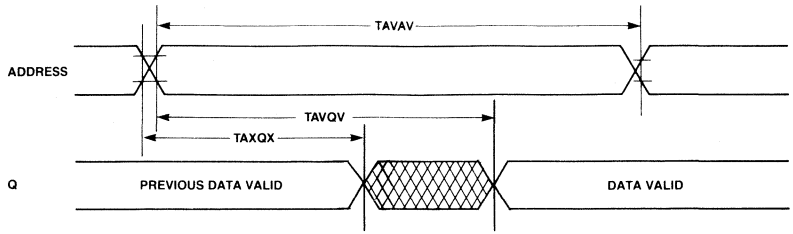
Parameter	Symbol	MB84256-10/10L Min	MB84256-10/10L Max	MB84256-15/15L Min	MB84256-15/15L Max	Unit
Read cycle time	TAVAV	100		150		ns
Address access time*2	TAVQV		100		150	ns
$\overline{E}$ access time*3	TELQV		100		150	ns
Output enable to output valid	TGLQV		40		60	ns
Output hold from address change	TAXQX	20		20		ns
Chip select to output low-Z*4,5	TELQX	10		10		ns
Output enable to output low-Z*4,5	TGLQZ	5		5		ns
Chip select to output high-Z*4,5	TEHQZ		40		50	ns
Output enable to output high-Z*4,5	TGHQZ		40		50	ns

Note: *1 $\overline{W}$ is high for Read cycle.
*2 Device is continuously selected, $\overline{E} = \overline{G} = V_{IL}$.
*3 Address valid prior or coincident with as transition low.
*4 Transition is measured at the point of ±500 mV from steady state voltage.
*5 This parameter is measured with specified loading Load II in AC Test Conditions Diagram.

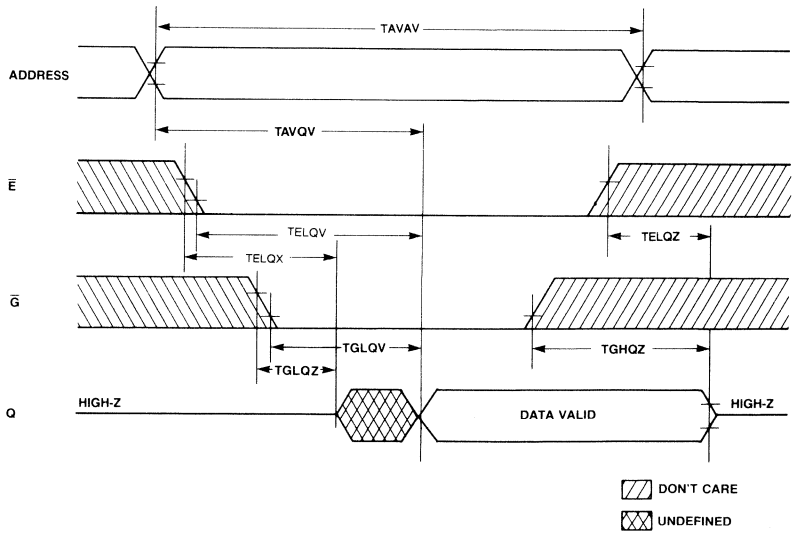
AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Read Cycle Timing Diagrams

Read Cycle I: Address Controlled



Read Cycle II: $\overline{E}$ Controlled



AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle[*1,2]		**MB84256-10/10L**		**MB84256-15/15L**		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Write cycle time[*3]	TAVAV	100		150		ns
Address valid to end of write	TAVWH TAVEL	80		100		ns
Chip select to end of write	TELEH	80		100		ns
Data valid to end of write	TDVWH	40		50		ns
Data hold time	TWHDX	0		0		ns
Write pulse width	TWLWH	60		90		ns
Address setup time	TAVWL TAVEL	0		0		ns
Write recovery time[*4]	TWHAX TEHAX	5		5		ns
Write enable to output low-Z[*5,6]	TWHQX	5		5		ns
Write enable to output high-Z[*5,6]	TWLQZ		40		50	ns

Note: *1 If $\overline{G}$, $\overline{E}$ are in the Read Mode during this period, D/Q pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*2 If $\overline{E}$ goes high simultaneously with $\overline{W}$ high the output remain in high impedance state.

*3 All write cycles are determined from last address transition to the first address transition of the next address.

*4 TWHAX is defined from the end point of write mode.

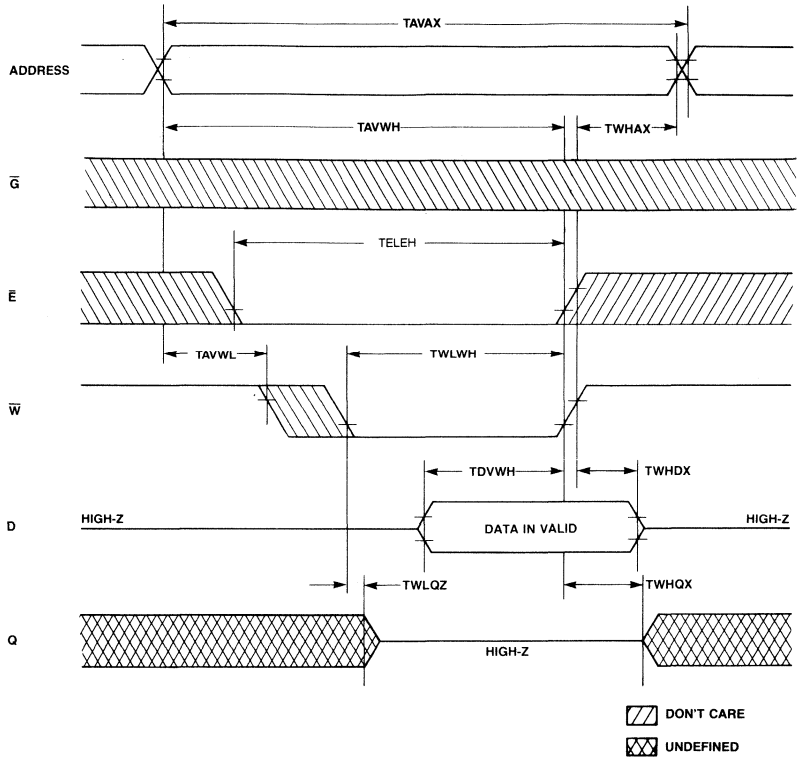
*5 Transition is measured at the point of ±500 mV from steady state voltage.

*6 This parameter is measured with specified loading Load II in Fig. 2.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

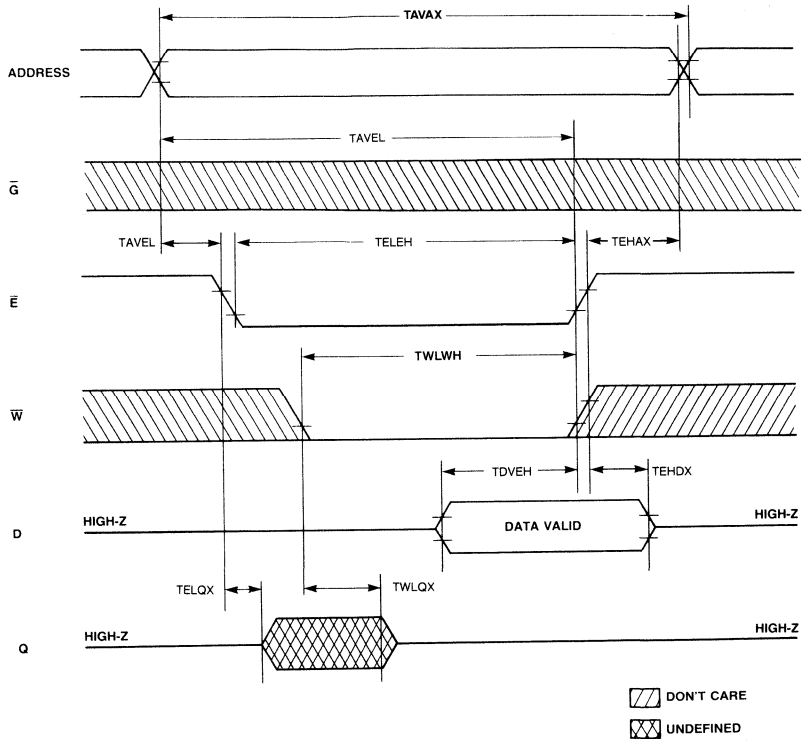
Write Cycle Timing Diagram

Write Cycle I ($\overline{W}$ Controlled)



AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle II ($\overline{E}$ controlled)

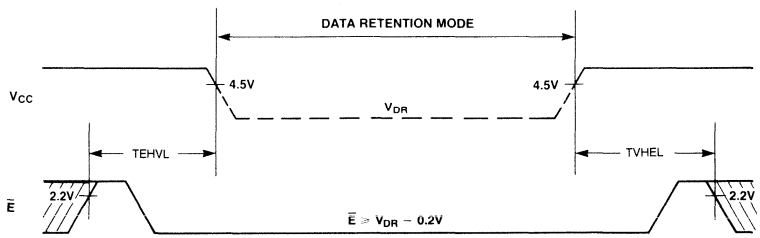


Data Retention Characteristics

(Recommended operating conditions unless otherwise noted)

Parameter		Symbol	Min	Max	Unit
Data retention*1 supply voltage		V_{DR}	2.0	5.5	V
Data retention*2 supply current	Standard	I_{DR}		1	mA
	L-version			50	μA
Data retention setup time		TEHVL	0		ns
Operation recovery time		TVHEL	TAVAX		ns

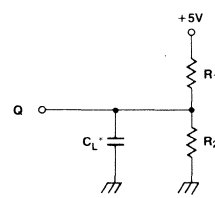
Note: *1 $\overline{E} \geq V_{DR} - 0.2V$
*2 $V_{DR} = 3.0V$, $E \geq V_{DR} - 0.2V$



AC Test Conditions

Input Pulse Levels: 0.6V to 2.4V
Input Pulse Rise and Fall Times: 5 ns (Transient between 0.8V and 2.2V)
Timing Reference Levels: Input: $V_{IL} = 0.8V$, $V_{IH} = 2.2V$
Output: $V_{OL} = 0.8V$, $V_{OH} = 2.2V$

Output Load OUTPUT LOAD

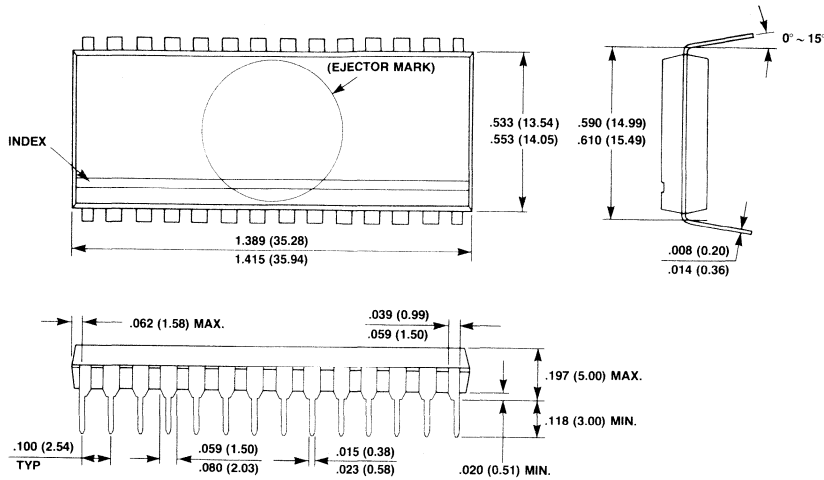


*INCLUDING PROBE AND STRAY CAPACITANCE

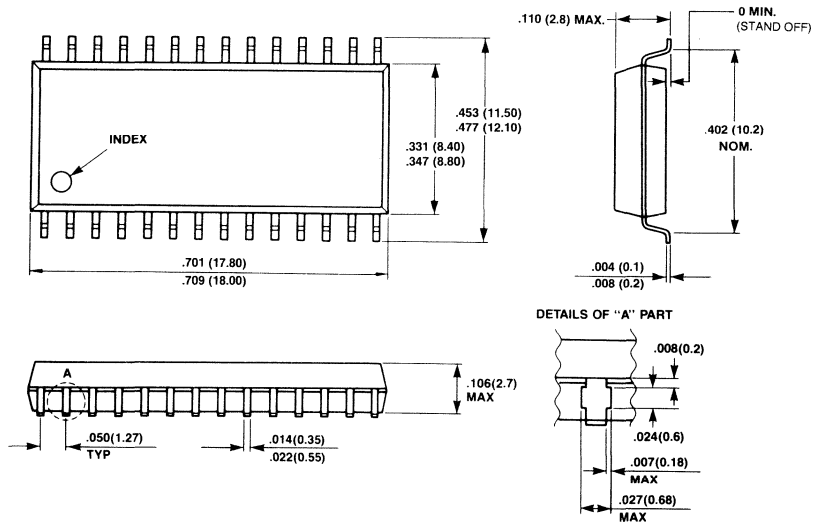
	R_1	R_2	C_L	Parameters Measured
Load I	1.8KΩ	990Ω	100 pF	Except TE1LQX, TGLQZ, TE1HQZ, TWHQX and TWLQZ
Load II	1.8KΩ	990Ω	5 pF	TE1LQX, TGLQZ, TE1HQZ, TGHQZ, TWHQX and TWLQZ

Package Dimensions
Dimensions in inches
(millimeters)

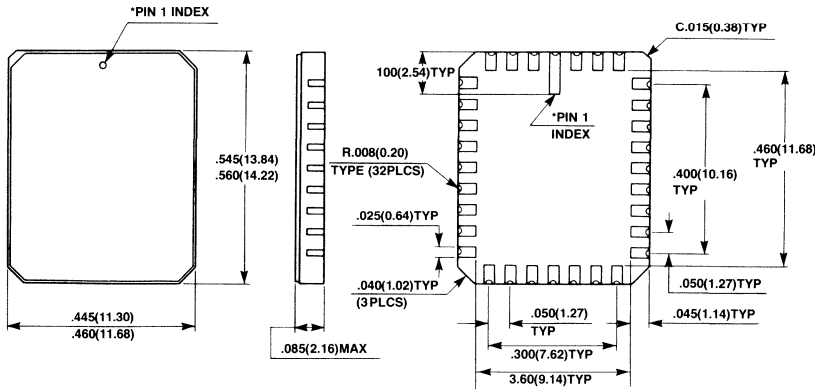
28-Lead Plastic Dual In-Line Package
(Case No.: DIP-28P-M02)



28-Lead Plasic Flat Package
(Case No.: FPT-28P-MO2)



32-Pad Ceramic (Metal Seal) Leadless Chip Carrier (Case No.: LCC-32C-A02)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

NMOS Static RAMs

MB8128 4-2
MB8167A 4-10
MB8168 4-16
MB8171 4-22

FUJITSU

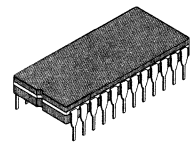
MOS 16384-BIT STATIC RANDOM ACCESS MEMORY

MB 8128-10
MB 8128-15

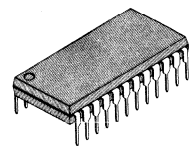
16384-BIT STATIC RANDOM ACCESS MEMORY WITH AUTOMATIC POWER DOWN

The Fujitsu MB 8128 is a 16384 bit static random access memory organized as 2048 words by 8 bits. The MB 8128 is fabricated using N-channel silicon gate MOS technology. It uses fully static circuitry throughout and therefore requires no clocks or refreshing to operate.

MB 8128 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are required. The MB 8128 is compatible with TTL logic families in all respects; inputs, outputs and a single +5V supply.



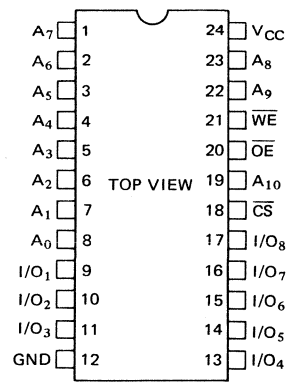
CERAMIC PACKAGE
(CERDIP)
DIP-24C-C01



PLASTIC PACKAGE
DIP-24P-M01

- 2048 words x 8 bits organization
- Static operation: no clocks or refresh required
- Fast access time : 100ns max. (MB 8128-10)
  : 150ns max. (MB 8128-15)
- Single +5V supply, ±10% tolerance
- Common data input/output
- TTL compatible inputs/outputs
- Three-state output with OR-tie capability
- Chip select for simplified memory expansion, automatic power down
- All inputs and outputs have protection against static charge
- Standard 24 pin DIP package

PIN ASSIGNMENT



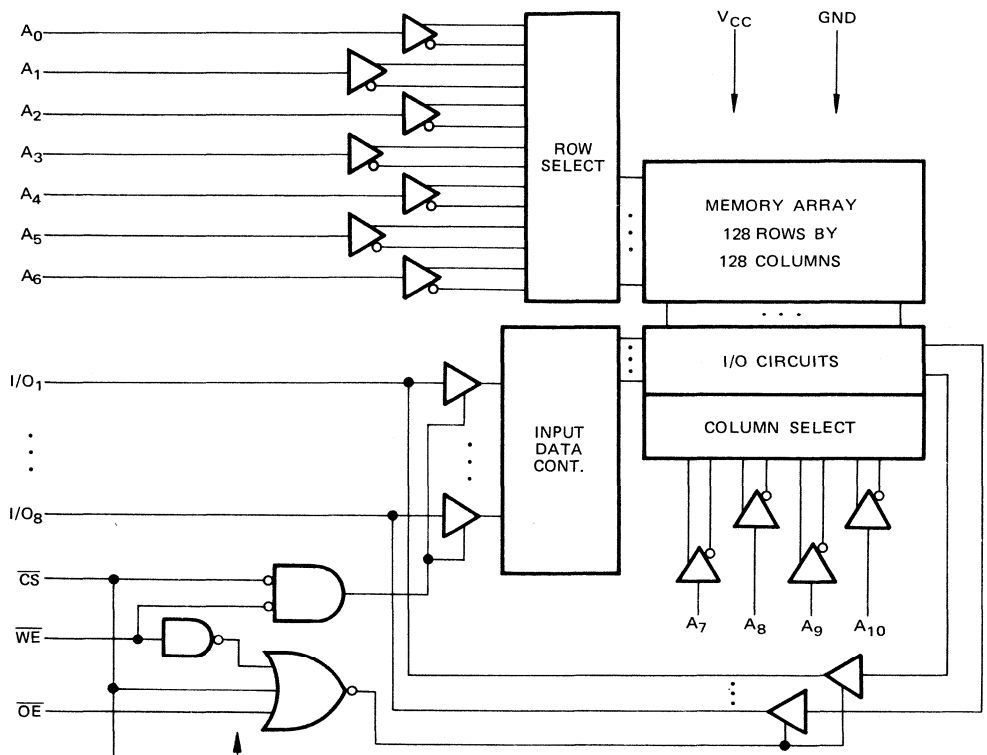
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Voltage on Any Pin with respect to GND		V_{IN}, V_{OUT}, V_{CC}	-3.5 to +7	V
Temperature under Bias		T_{BIAS}	-10 to +85	°C
Storage Temperature	CERAMIC	T_{STG}	-65 to +150	°C
	PLASTIC		-40 to +125	
Power Dissipation		P_D	1.2	W

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 — MB 8128 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	NOT SELECTED	I_{SB}	HIGH-Z
L	H	H	D_{OUT} DISABLE	I_{CC}	HIGH-Z
L	L	H	READ	I_{CC}	D_{OUT}
L	X	L	WRITE	I_{CC}	D_{IN}

CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)*	C_{IN}	—	5	pF
Input/Output Capacitance ($V_{I/O}$ = 0V)*	$C_{I/O}$	—	7	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit	Ambient[1] Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
Input Low Voltage	V_{IL}	−3.0[2]	–	0.8	V	
Input High Voltage	V_{IH}	2.2	–	6.0	V	

Note: 1) The operating ambient temperature range is guaranteed with transverse airflow exceeding 2m/sec.
2) −3.0 V Min. for pulse width less than 20 ns. (V_{IL} Min. = −0.5 V at DC level).

DC CHARACTERISTICS

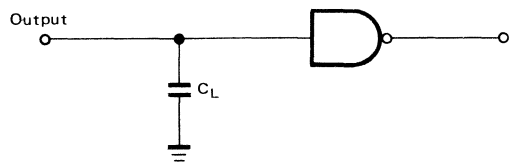
(Recommended operating conditions unless otherwise noted.)

Parameter			Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = GND to V_{CC}, V_{CC} = Max.)			$\|I_{LI}\|$			10	μA
Input/Output Leakage Current ($\overline{CS}$ or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}, V_{CC} = Max.)			$\|I_{LO}\|$			10	μA
Power Supply Current (V_{CC} = Max., $\overline{CS}$ = V_{IL}, $I_{I/O}$ = Open)	T_A = 25°C	MB 8128-10	I_{CC}		70		mA
		MB 8128-15			50		
	T_A = 0°C	MB 8128-10				100	
		MB 8128-15				70	
Output Low Voltage (I_{OL} = 2.1 mA)			V_{OL}			0.4	V
Output High Voltage (I_{OH} = -1.0 mA)			V_{OH}	2.4			V
Standby Current (V_{CC} = Min. to Max., $\overline{CS}$ = V_{IH})		MB 8128-10	I_{SB}		8	20	mA
		MB 8128-15			6	15	
Peak Power-On Current (V_{CC} = GND to V_{CC} Min., $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min.)		MB 8128-10	I_{PO}			20	mA
		MB 8128-15				15	

Note: A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselacted. Otherwise, power-on current approaches I_{CC} active.

Fig. 2 – AC TEST CONDITIONS

Input Pulse Levels:	0.8V to 2.4V
Input Pulse Rise and Fall Times:	10 ns
Timing Measurement Reference Levels:	Input: 1.5V Output: 1.5V
Output Load :	1 TTL Gate and C_L = 100 pF



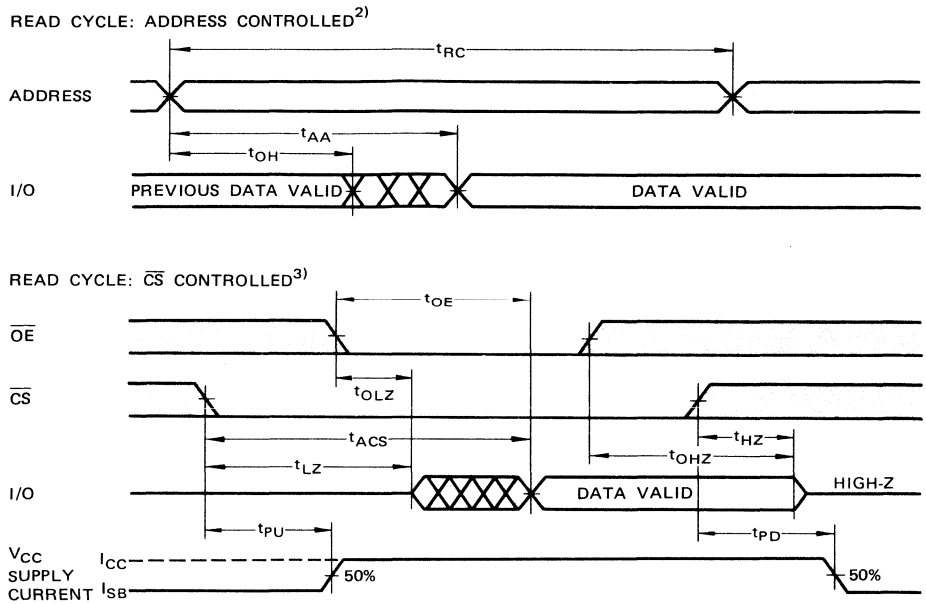
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE

Parameter	Symbol	MB 8128-10			MB 8128-15			Unit
		Min	Typ	Max	Min	Typ	Max	
Read Cycle Time	t_{RC}	100			150			ns
Address Access Time	t_{AA}			100			150	ns
Chip Select Access Time	t_{ACS}			100			150	ns
Output Hold from Address Change	t_{OH}	15			20			ns
Chip Select to Output Active	t_{LZ}	0			0			ns
Chip Select to Output in High Z	t_{HZ}			40			60	ns
Output Enable to Output Valid	t_{OE}			50			60	ns
Output Enable to Output Active	t_{OLZ}	10			10			ns
Output Enable to Output in High Z	t_{OHZ}			40			60	ns
Chip Select to Power Up Time	t_{PU}	0			0			ns
Chip Select to Power Down Time	t_{PD}			40			60	ns

READ CYCLE TIMING DIAGRAM[1)]



: Don't Care

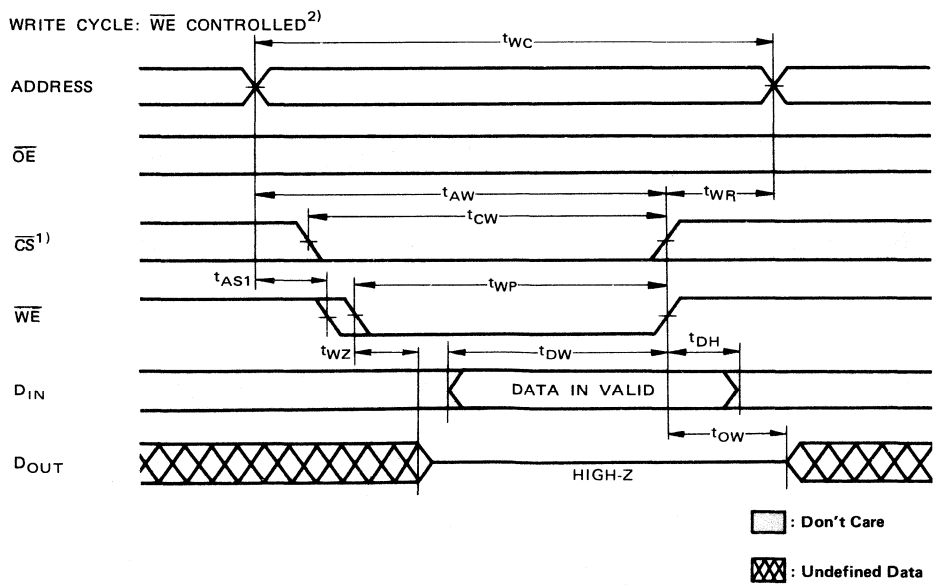
: Undefined Data

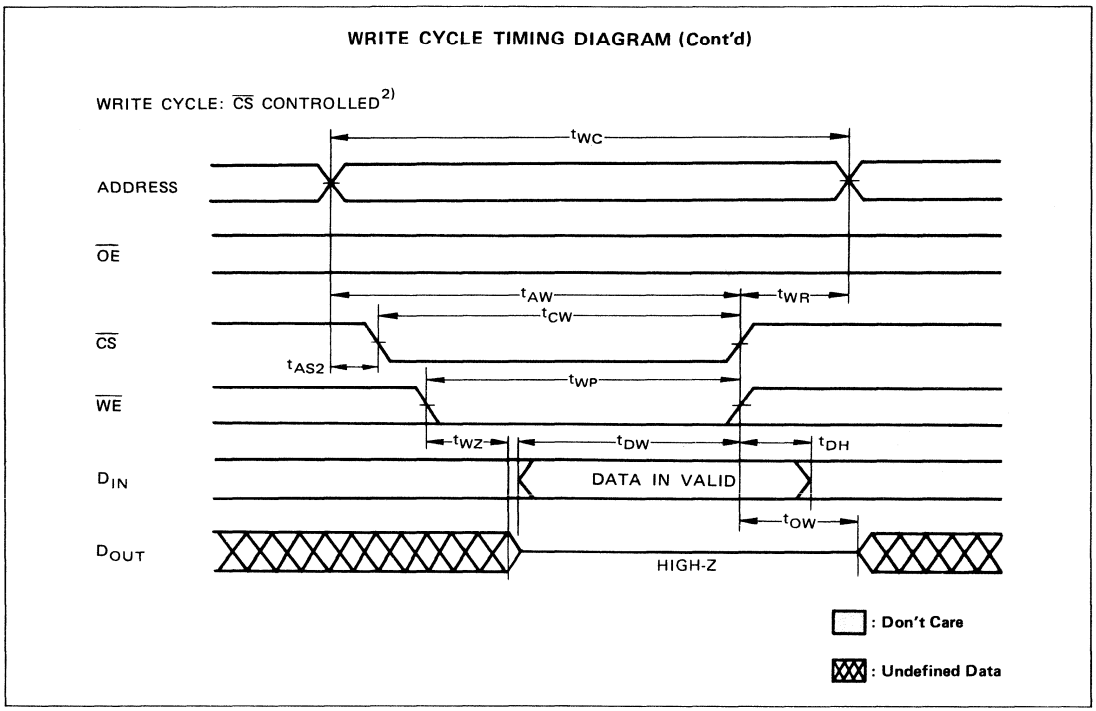
Note: 1) $\overline{WE}$ is high for Read Cycle.
2) Device is continuously selected, $\overline{CS} = V_{IL}$, $\overline{OE} = V_{IL}$.
3) Addresses valid prior to or coincident with $\overline{CS}$ transition low.

WRITE CYCLE

Parameter	Symbol	MB 8128-10			MB 8128-15			Unit
		Min	Typ	Max	Min	Typ	Max	
Write Cycle Time	t_{WC}	100			150			ns
Address Valid to End of Write	t_{AW}	95			140			ns
Chip Select to End of Write	t_{CW}	95			140			ns
Data Valid to End of Write	t_{DW}	40			60			ns
Data Hold Time	t_{DH}	5			5			ns
Write Pulse Width	t_{WP}	85			130			ns
Write Recovery Time	t_{WR}	5			10			ns
Address Setup Time	t_{AS1}	0			0			ns
	t_{AS2}	0			0			ns
Output Active From End of Write	t_{OW}	10			10			ns
Write Enabled to Output in High Z	t_{WZ}			40			60	ns

WRITE CYCLE TIMING DIAGRAM





Note: 1) If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ low, the outputs remain in a high impedance state.
2) $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.

DESCRIPTION

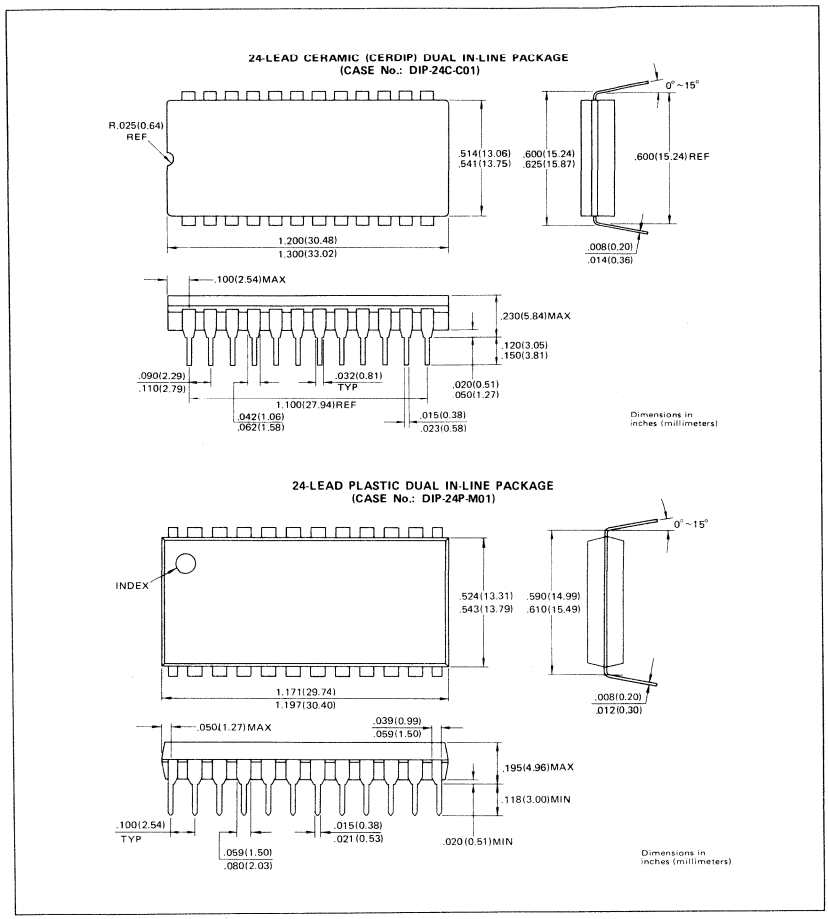
The MB 8128 from Fujitsu is high performance part. This is designed for high speed and low system power requirements.

The high speed is obtained by advanced NMOS processing. The low system power requirements are achieved by the use of the MB 8128 chip select (active low). The MB 8128 automatically enters standby drawing only I_{SB} whenever the chip select is high. Upon activation of chip select ($\overline{CS}$ = LOW) the MB 8128 automatically powers up and draws I_{CC}. This automatic power up/down is an extremely useful feature. However, care must be used as proper decoupling and PC board layout is required to minimize power line glitches.

PC board layout with proper V_{CC} decoupling will minimize power line glitches.

Input and data bus lines are an additional area of concern. Unless bus lines are properly designed and terminated, cross coupling, cross talk and reflections can occur. Of particular importance is the undershoot on address lines. Once again, careful attention to good PC board layout and proper termination techniques will yield a well designed and reliable memory system.

PACKAGE DIMENSIONS



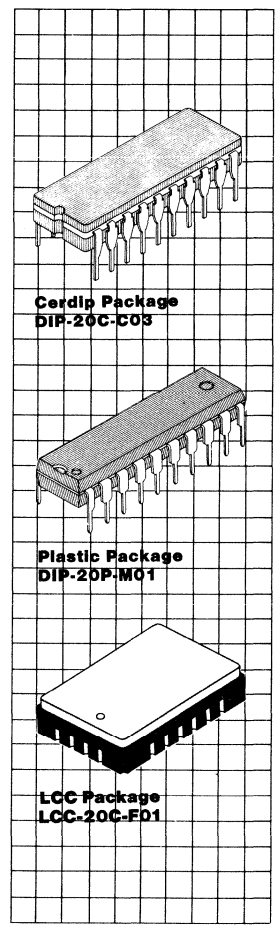
■ MB8167A-55, MB8167A-70

NMOS 16,384-Bit Static Random Access Memory

Description

The Fujitsu MB8167A is a 16,384 words by 1-bit static random access memory fabricated using N-channel silicon gate MOS technology. Separate input/output pins are provided. All devices are fully compatible with TTL logic families in all respects: inputs, output and the use of a single +5 V DC supply.

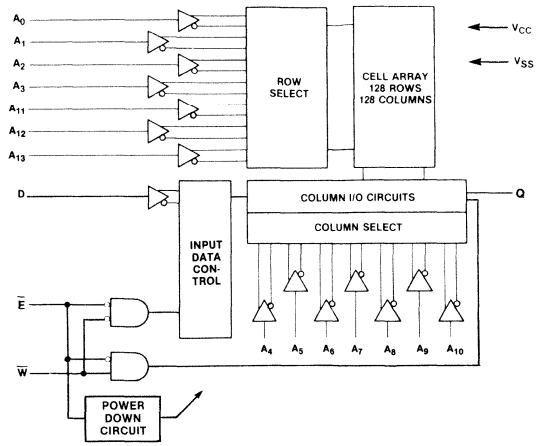
For ease of use, chip enable ($\overline{E}$) permits the selection of an individual package when outputs are OR-tied, and automatically powers down the MB8167A. This device offers the advantages of low power dissipation, low cost, and high performance.

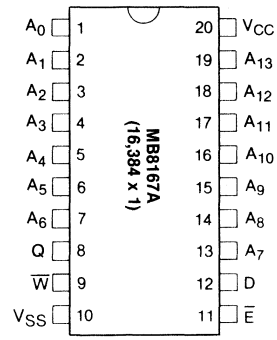


Features

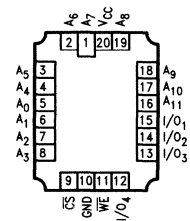
- Organized as 16,384 words x 1-bit
- Static operation: no clocks or refresh required
- Fast Access Time:
  MB8167A-55 55 ns Max.
  MB8167A-70 70 ns Max.
- Single +5 V DC supply voltage
- Separate data input and output
- TTL compatible inputs and output
- Three-state output with OR-tie capability
- Chip enable for simplified memory expansion and automatic power down
- All inputs and output have protection against static charge
- Standard 20-pin DIP package

MB8167A Block Diagram and Pin Assignment





TOP VIEW



(LCC-20C-F01)

Truth Table

$\overline{E}$	$\overline{W}$	Mode	Output	Power
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Voltage On Any Pin with Respect to V_{SS}		VIN, VOUT, VCC	−3.5 to +7	V
Temperature Under Bias		TA	−10 to +85	°C
Storage Temperature	Ceramic	TSTG	−65 to +150	°C
	Plastic	TSTG	−40 to +125	
Power Dissipation		PD	1.2	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance
(T_A = 25°C; f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (VIN = 0V)	CIN	—	5	pF
Output Capacitance (VOUT = 0V)	COUT	—	6	pF

Recommended Operating Conditions
(Referenced to VSS)

Parameter	Symbol	Min	Typ	Max	Unit	Ambient[1] Temperature
Supply Voltage	VCC	4.5	5.0	5.5	V	0°C to +70°C
Input Low Voltage	VIL	−3.0[2]	—	0.8	V	
Input High Voltage	VIH	2.0	—	6.0	V	

Note: (1) The operating ambient temperature range is guaranteed with transverse airflow exceeding 2 linear meters/second.
(2) −3.0 V Min. for pulse width less than 20 ns. (V_{IL} Min. = −0.5 at DC level)

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

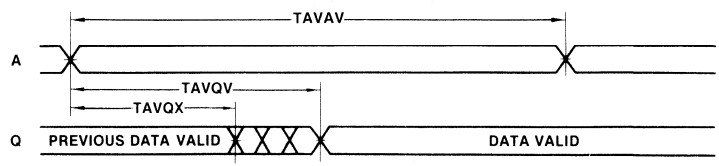
Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (VIN = VSS to VCC, VCC = Max)	ILI	—	0.01	10	μA
Output Leakage Current $\overline{E}$ = VIH, VOUT = VSS to VCC Min, VCC = Max)	I_{LO}	—	0.1	50	μA
Power Supply Current (VCC = Max, $\overline{E}$ = VIL, IOUT = 0mA)	ICC	—	90	120	mA
Output Low Voltage (IOL = 16mA)	VOL	—	—	0.45	V
Output High Voltage (IOH = −4mA)	VOH	2.4	—	—	V
Standby Current (VCC = Min to Max, $\overline{E}$ = VIH	ISB	—	15	25	mA
Peak Power-On Current (VCC = VSS to VCC Min, $\overline{E}$ = Lower of VCC or VIH Min)	IPO	—	—	25	mA

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

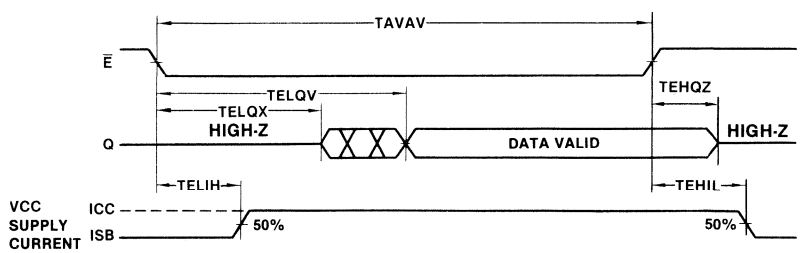
Read Cycle

Parameter	Notes	Symbol	MB8167A-55 Min	MB8167A-55 Max	MB8167A-70 Min	MB8167A-70 Max	Unit
Read Cycle Time		TAVAV	55	—	70	—	ns
Address Access Time		TAVQV		55		70	ns
Chip Enable Access Time		TELQV	—	55	—	70	ns
Output Hold from Address Change		TAVQX	5	—	5	—	ns
Chip Enable to Output Active	1 2	TELQX	10	—	10	—	ns
Chip Enable to Output in High Z	1 2	TEHQZ	0	30	0	40	ns
Chip Enable to Power Up Time		TELIH	0	—	0	—	ns
Chip Enable to Power Down Time		TEHIL	—	30	—	35	ns

Read Cycle: Address Controlled 3,4



Read Cycle: $\overline{E}$ Controlled 3, 5



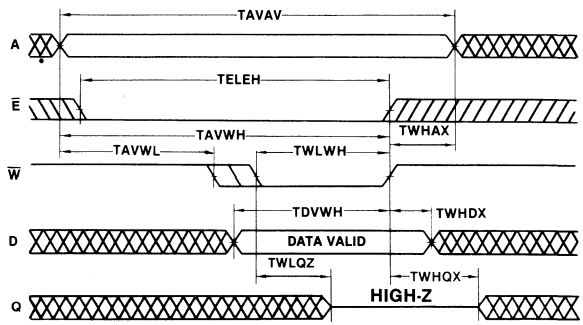
Notes:
1. Transition is measured at the point of ±500mV from steady state voltage.
2. This parameter is measured with specified loading in Fig.2.
3. $\overline{W}$ is high for Read Cycle.
4. Device is continuously selected, $\overline{E}$ = VIL.
5. Addresses valid prior to or coincident with $\overline{E}$ transition low.

AC Characteristics
(Recommended operating conditions unless otherwise noted.) (continued)

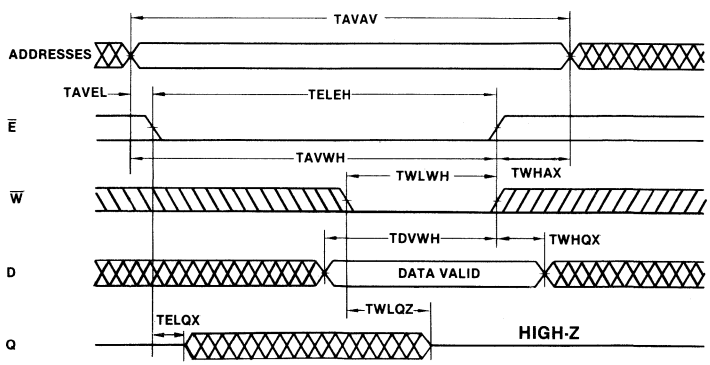
Write Cycle

Parameter	Notes	Symbol	MB8167A-55 Min	MB8167A-55 Max	MB8167A-70 Min	MB8167A-70 Max	Unit
Write Cycle Time		TAVAV	55	—	70	—	ns
Address Valid to End of Write		TAVWH	45	—	50	—	ns
Chip Enable to End of Write		TELEH	50	—	60	—	ns
Data Valid to End of Write		TDVWH	35	—	45	—	ns
Data Hold Time		TWHDX	0	—	0	—	ns
Write Pulse Width		TWLWH	35	—	45	—	ns
Write Recovery Time		TWHAX	5	—	10	—	ns
Address Setup Time		TAVWL	5	—	10	—	ns
		TAVEL	0	—	0	—	ns
Output Active From End of Write	7 8	TWHQX	0	—	0	—	ns
Write Enable to Output in High Z	7 8	TWLQZ	—	30	—	35	ns

Write Cycle: $\overline{W}$ Controlled[6,9]



Write Cycle: $\overline{E}$ Controlled[6,9]

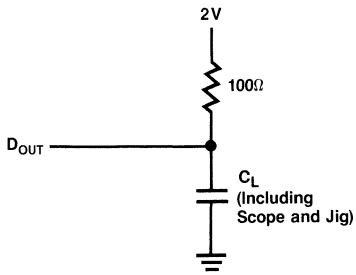


Notes:
6. If $\overline{E}$ goes high simultaneously with $\overline{W}$ high, the output remains in a high impedance state.
7. Transition is measured at the point of ±500mV from steady state voltage.
8. This parameter is measured with specified loading in Fig. 2.
9. $\overline{E}$ or $\overline{W}$ must be high during address transitions.

AC Test Conditions

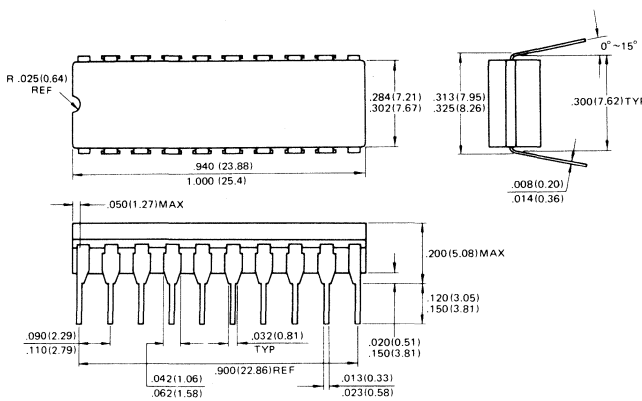
Input Pulse Levels:	0.8 V to 2.2 V
Input Pulse Rise and Fall Times:	5 ns
Timing Measurement Reference Levels:	Inputs: 1.5 V Output: 1.5 V
Load Capacitance:	5 pF for TEHQZ, TWLQZ, TELQX and TWHQX 30 pF for all others

Fig. 2: Output Load



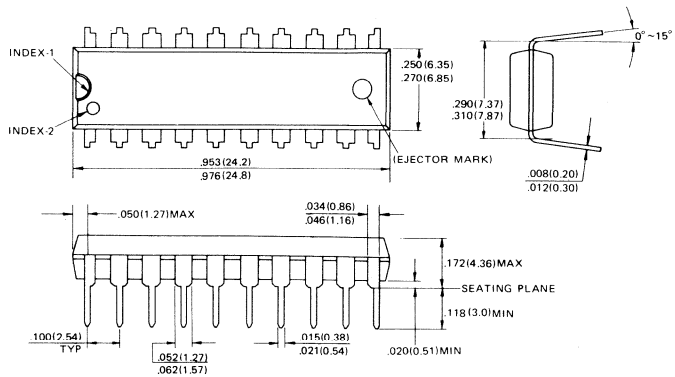
Package Dimensions
Dimensions in inches
(millimeters)

20-Lead Cerdip
Dual In-Line Package
DIP-20C-C03

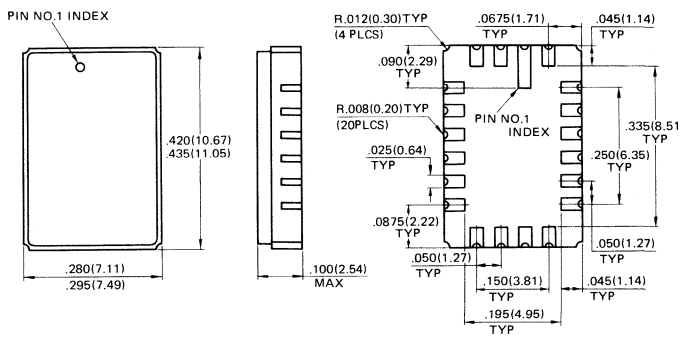


Package Dimensions
Dimensions in inches
(millimeters) (continued)

20-Lead Plastic
Dual In-Line Package
DIP-20P-M01



20-Pad Ceramic (Frit Seal)
Leadless Chip Carrier
(Case No.: LCC-20C-F01)



FUJITSU
MICROELECTRONICS, INC.

MB8168-55
MB8168-70

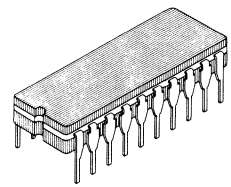
NMOS 16,384-BIT STATIC RANDOM ACCESS MEMORY

DESCRIPTION

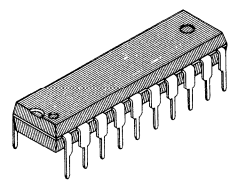
The Fujitsu MB8168 is a 4096 word by 4-bit static random access memory fabricated using N-channel silicon gate MOS technology. The memory is fully static and requires no clock or timing strobe. All pins are TTL compatible and a single 5V power supply is required.

A separate chip select $\overline{E}$ pin simplifies multipackage system design. It permits the selection of an individual package when outputs are OR-tied. Furthermore, when selecting a single package by $\overline{E}$, the other deselected packages automatically power down.

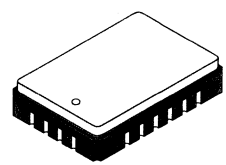
All Fujitsu devices offer the advantages of low power dissipation, low cost and high performance.



CERDIP PACKAGE
DIP-20C-C03



PLASTIC PACKAGE
DIP-20P-M01

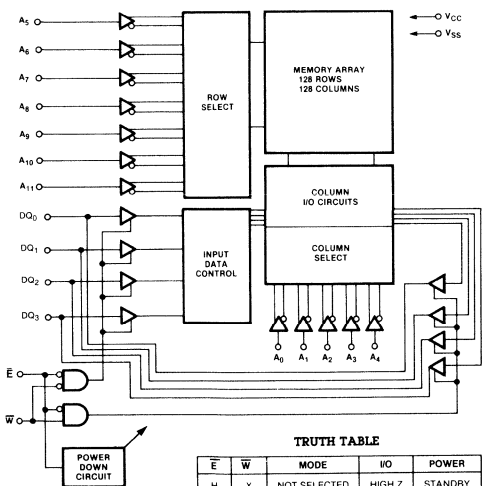


LCC PACKAGE
LCC-20C-F01

FEATURES

- **Organized as 4096 words x 4-bits**
- **Fully Static Operation, no clocks or timing strobe required**
- **Fast Access Time:**
  MB8168-55 55 ns Max.
  MB8168-70 70 ns Max.
- **Low Power Consumption:**
  I_{CC} = 150mA Max. (Active)
  I_{SB} = 40mA Max.(Standby)
- **Single +5V DC Supply Voltage, ±10% tolerance**
- **Common data input and output**
- **Three-state outputs with OR-tie capability**
- **Chip select for simplified memory expansion, automatic power-down**
- **Standard 20-pin DIP package**
- **Pin compatible with Intel 2168**

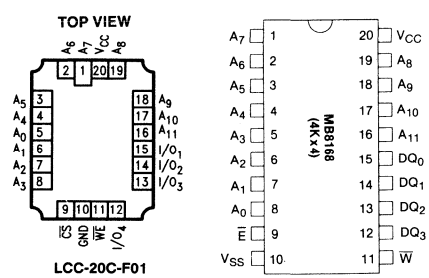
MB8168 BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}$	$\overline{W}$	MODE	I/O	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	D_{IN}	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

PIN ASSIGNMENTS



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage On Any Pin with Respect to V_{SS}	V_{IN}, V_{OUT}, V_{CC}	−3.5 to +7.0	V
Short Circuit Output Current	I_{SO}	20	mA
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature	Tstg Ceramic Plastic	−65 to +150 −40 to +125	°C
Power Dissipation	P_D	1.2	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient[1] Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
Input Low Voltage	V_{IL}	−3.0[2]	—	0.8	V	
Input High Voltage	V_{IH}	2.0	—	6.0	V	

Note: 1. The operating ambient temperature range is guaranteed with transverse airflow exceeding 2 linear meters/second.
2. −3.0 V Min. for Pulse width less than 20 ns. (V_{IL} Min. = −0.5 V at DC level)

CAPACITANCE (T_A = 25° C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance Address, $\overline{W}$: V_{IN} = 0V	C_{IN}	—	7	pF
Input Capacitance $\overline{E}$: V_{IN} = 0V	$C_{\overline{E}}$	—	8	pF
Output Capacitance Data I/O, V_{OUT} = 0V	$C_{I/O}$	—	8	pF

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (V_{IN} = V_{SS} to V_{CC}, V_{CC} = Max)	I_{LI}	−10	10	μA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{OUT} = V_{SS} to 4.5V, V_{CC} = Max)	I_{LO}	−50	50	μA
Power Supply Current (V_{CC} = Max, $\overline{E}$ = V_{IL}, I_{OUT} = 0mA)	I_{CC}	—	150	mA
Output Low Voltage (I_{OL} = 8mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4mA)	V_{OH}	2.4	—	V
Standby Current (V_{CC} = Min to Max, $\overline{E}$ = V_{IH}, I_{OUT} = 0mA)	I_{SB}	—	40	mA
Peak Power-On Current (V_{CC} = V_{SS} to V_{CC} Min, $\overline{E}$ = Lower of V_{CC} or V_{IH} Min)*	I_{PO}	—	50	mA

Note: *A pull-up resistor to V_{CC} or the $\overline{CS}$ input is required to keep the device deselected. Otherwise, power-on current approaches I_{CC} active.

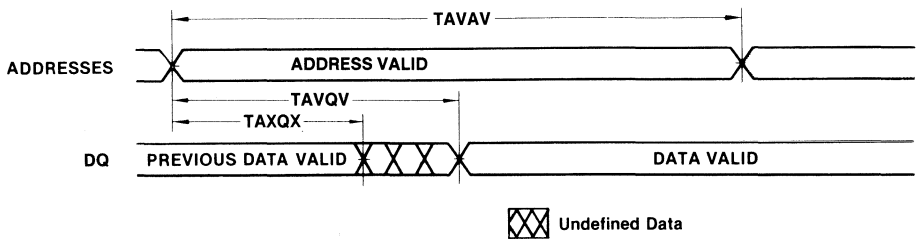
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

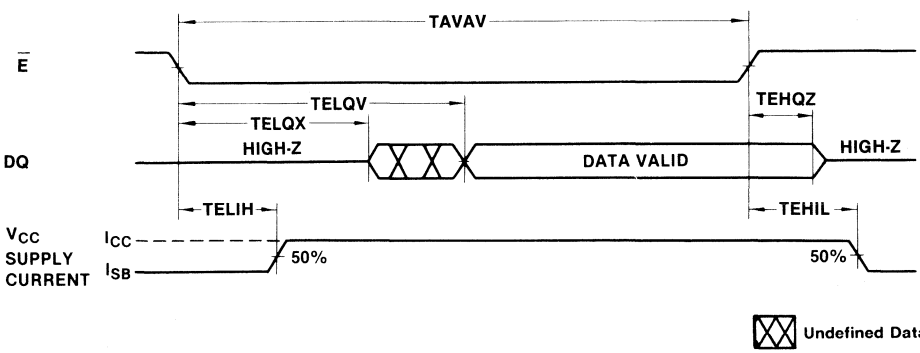
READ CYCLE

Parameter	NOTES	Symbol	MB8168-55			MB8168-70			Unit
			Min	Typ	Max	Min	Typ	Max	
Read Cycle Time		TAVAV	55	—	—	70	—	—	ns
Address Access Time		TAVQV	—	—	55	—	—	70	ns
Chip Enable Access Time		TELQV	—	—	55	—	—	70	ns
Output Hold from Address Change		TAXQX	5	—	—	5	—	—	ns
Chip Enable to Output Active	1 2	TELQX	10	—	—	10	—	—	ns
Chip Enable to Output in High Z	1 2	TEHQZ	—	—	30	—	—	40	ns
Chip Enable to Power Up Time	3	TELIH	0	—	—	0	—	—	ns
Chip Enable to Power Down Time	3	TEHIL	—	—	55	—	—	70	ns

READ CYCLE: ADDRESS CHANGING 4,5



READ CYCLE: $\overline{CS}$ CHANGING 4,6

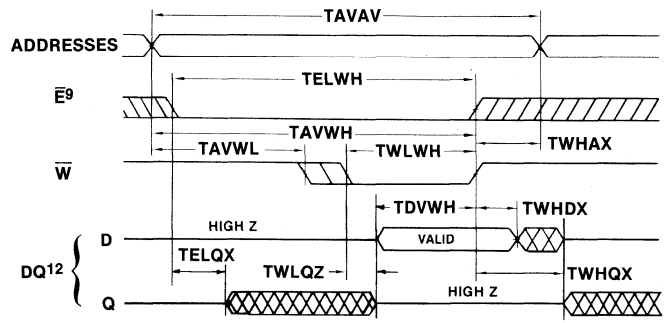


Notes: 1. Transition is measured at the point of ±500mV from steady state voltage.
2. This parameter is measured with specified loading in Fig. 2.
3. $I_H = I_{CC\,(Max)}$, $I_L = I_{SB\,(Max)}$
4. $\overline{W}$ is high for Read Cycle.
5. Device is continuously selected. $\overline{E} = V_{IL}$.
6. Addresses valid prior to or coincident with $\overline{E}$ transition low.

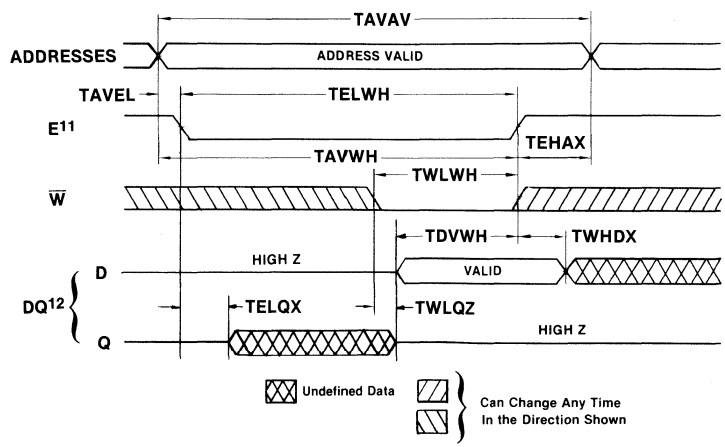
WRITE CYCLE

Parameter	NOTES	Symbol	MB8168-55 Min	MB8168-55 Typ	MB8168-55 Max	MB8168-70 Min	MB8168-70 Typ	MB8168-70 Max	Unit
Write Cycle Time		TAVAV	55	—	—	70	—	—	ns
Address Valid to End of Write		TAVWH	50	—	—	60	—	—	ns
Chip Enable to End of Write		TELWH	50	—	—	60	—	—	ns
Data Valid to End of Write		TDVWH	25	—	—	30	—	—	ns
Data Hold Time		TWHDX	0	—	—	0	—	—	ns
Write Pulse Width		TWLWH	50	—	—	60	—	—	ns
Write Recovery Time		TWHAX, TEHAX	0	—	—	0	—	—	ns
Address Setup Time		TAVWL, TAVEL	0	—	—	0	—	—	ns
Output Active From End of Write	7 8	TWHQX	0	—	—	0	—	—	ns
Write Enable to Output in High Z	7 8	TWLQZ	0	—	30	0	—	40	ns
Chip Enable to Output Active		TELQX	10	—	—	10	—	—	ns

WRITE CYCLE: $\overline{W}$ CONTROLLED[10]



WRITE CYCLE: $\overline{E}$ CONTROLLED[10]



Notes: 7. Transition is measureed at the point of ±500 mV from steady state voltage.
8. This parameter is measured with specified loading in Fig. 2.
9. If $\overline{E}$ goes high simultaneously with $\overline{W}$ high, the output remains in a high impedance state.
10. $\overline{E}$ or $\overline{W}$ must be high during address transitions.
11. If $\overline{W}$ is low for the entire cycle Data Out remains High Z throughout the cycle.
12. Q shows when the DQ pin is driven by the memory chip. D shows when the DQ pin is externally driven.

AC TEST CONDITIONS

Input Conditions:

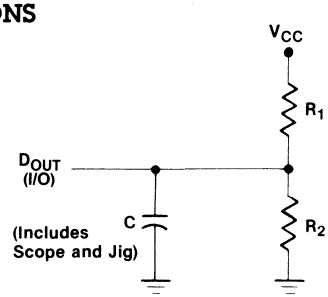
Input Pulse Levels:	**0V to 3.0V**
Input Pulse Rise/Fall Times:	**5 ns**
Input Timing Reference Level:	**1.5V**

Output Conditions:

Output Timing Reference Level:	**0.8V to 2.0V**

Output Load:

	R_1	R_2	C	Parameters Measured
Load I	480Ω	255Ω	30pF	except TELQX, TEHQZ, TWLQZ, and TWHQX
Load II	480Ω	255Ω	5pF	TELQX, TEHQZ, TWLQZ, and TWHQX



OUTPUT LOAD

DEVICE OPERATION

Controls

The MB8168 has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$). When $\overline{E} \geq V_{IH}$, the device is deselected and automatically controlled to the standby mode, reducing the power requirements to less than one-sixth of the selected state. When $\overline{E} \leq V_{IL}$, the device is selected (active) and read or write cycles may be performed. $\overline{E}$ should be controlled to track V_{CC} during the initial system power-on to prevent all of the MB8168's in a system from drawing active I_{CC} during power-up.

When $\overline{W} \geq V_{IH}$ and the chip is selected, a read cycle may be performed. When $\overline{W} \leq V_{IL}$ and the chip is selected a write cycle may be performed.

Read Cycle

A read cycle is selected when $\overline{E} \leq V_{IL}$ and $\overline{W} \geq V_{IH}$. Read access time is measured from either the $\overline{E}$ high to low transition or from valid address as shown in the read cycle timing diagrams.

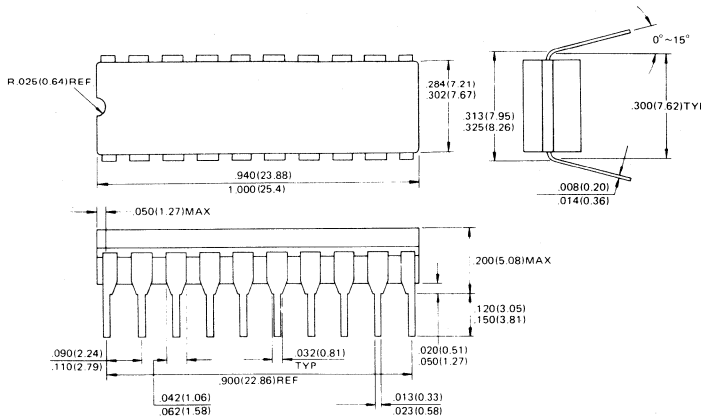
Write Cycle

A write cycle is seleted when $\overline{E} \leq V_{IL}$ and $\overline{W} \leq V_{IH}$. The actual beginning of the write cycle is initiated by the latter of $\overline{E}$ or $\overline{W}$ going low as shown in the write cycle timing diagrams. The address setup times shown in the timing diagrams must be met and the addresses must remain stable for the entire write cycle. The write cycle is terminated by either $\overline{E}$ or $\overline{W}$ going high. If the timing specifications are not met, data may be altered or lost.

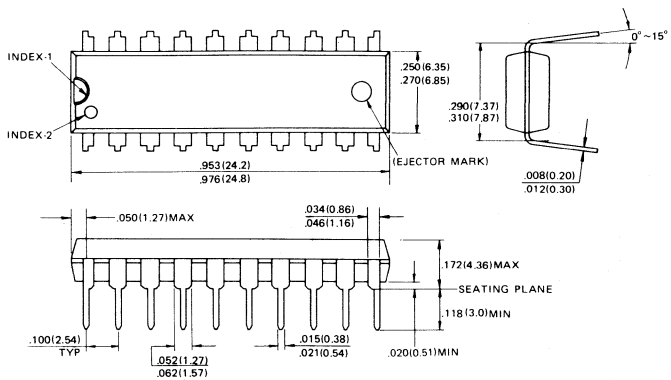
In summary, the write cycle may be initiated by the latter of $\overline{E}$ or $\overline{W}$ going low and may be terminated by $\overline{E}$ or $\overline{W}$ going high, whichever occurs first, and the setup and hold times must be referenced to the controlling signal transitions. Either $\overline{E}$ or $\overline{W}$ must be high (greater than V_{IH}), during an address transition.

PACKAGE DIMENSIONS Dimensions in inches (millimeters)

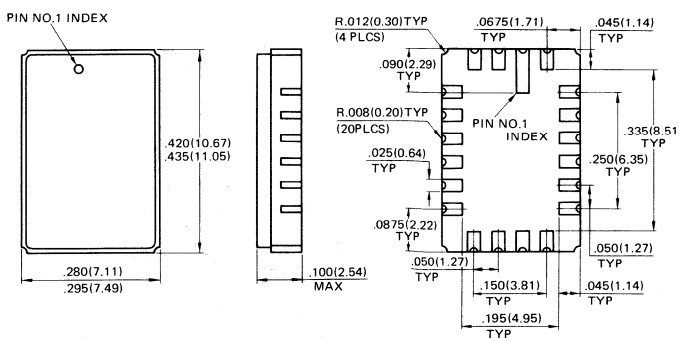
20-LEAD CERDIP DUAL IN-LINE PACKAGE
DIP-20C-C03



20-LEAD PLASTIC DUAL IN-LINE PACKAGE
DIP-20P-M01



20-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
LCC-20C-F01



MB8171-55, MB8171-70

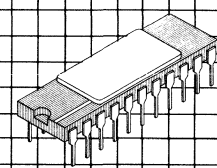
65,536-Bit Static Random Access Memory with Separate Data Input, Data Output and Automatic Power Down

Description

The Fujitsu MB8171 is a 65,536 word x 1-bit static random access memory fabricated with N-channel Silicon gate MOS technology. It uses fully static circuitry throughout and threrefore requires no clocks or refreshing to operate.

The MB8171 is designed for memory applications where high performance, low cost, large bit storage and simple interfacing are required.

All pins are TTL compatible and a single +5 volt power supply is required.



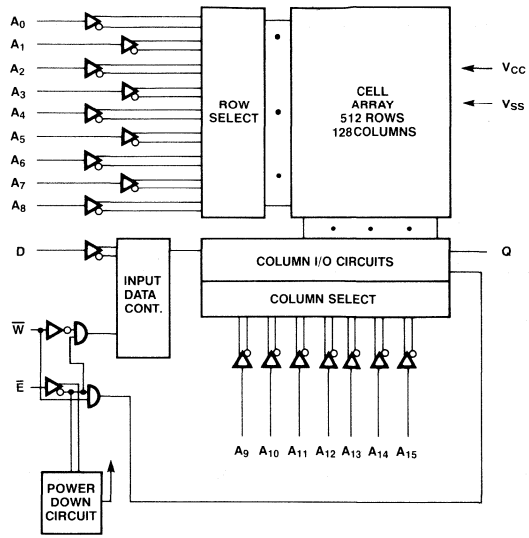
Ceramic Package DIP-22C-A01

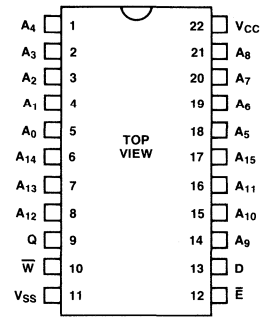
Features

- **Organization: 65,536 words x 1-bit**
- **Static operation: no clocks or refresh required**
- **Fast access time: TAVQV = TELQV = 55 ns max. (MB8171-55) TAVQV = TELQV = 70 ns max. (MB8171-70)**
- **Single +5V supply ±10% tolerance**
- **Separate data input and output**
- **TTL compatible inputs and output**
- **Chip enable for simplified memory expansion, automatic power down**
- **All inputs and output have protection against static charge**
- **Standard 22-pin Ceramic package (300 mil.)**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB8171 Block Diagram and Pin Assignments





TRUTH TABLE

$\overline{E}$	$\overline{W}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH-Z	STANDBY
L	L	WRITE	HIGH-Z	ACTIVE
L	H	READ	Q	ACTIVE

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Voltage on any pin with respect to V_{SS}	V_{IN}, V_{OUT}, V_{CC}	−3.5 to +7	V
Temperature under bias	T_{BIAS}	−10 to +85	°C
Storage temperature	T_{STG}	−65 to +150	°C
Power dissipation	P_D	1.2	W

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low voltage	V_{IL}	−3.0**		0.8	V
Input high voltage	V_{IH}	2.0		6.0	V
Ambient temperature*	T_A	0		70	°C

Note: * The operating ambient temperature range is guaranteed with transverse airflow exceeding 2m/s.
** −3.0 V Min. Pulse width less than 20 ns. (V_{IL} Min. = −0.5 V at DC level)

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input capacitance (V_{IN} = 0V)*	C_{IN}		5	pF
$\overline{E}$ capacitance (V_{IN} = 0V)*	$C_{\overline{E}}$		9	pF
Output capacitance (V_{OUT} = 0V)*	C_{OUT}		6	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Input leakage current	V_{IN} = 0V to V_{CC} V_{CC} = max.		I_{LI}	−10	0.01	10	μA
Output leakage current	$\overline{E}$ = V_{IH}, V_{OUT} = 0V to 4.5V V_{CC} = max.		I_{LO}	−50	0.1	50	μA
Power supply current	$\overline{E}$ = V_{IL} V_{CC} = max. I_{OUT} = 0 mA	T_A = 25°C	I_{CC}		90		mA
		T_A = 0°C				125	
Standby current	V_{CC} = min. to max. $\overline{E}$ = V_{IH}		I_{SB}		27	35	mA
Output low voltage	I_{OL} = 16 mA		V_{OL}			0.45	V
Output high voltage	I_{OH} = −4 mA		V_{OH}	2.4			V
Peak power on current	V_{CC} = 0V to V_{CC} min.* $\overline{E}$ = lower of V_{CC} or V_{IH} min.		I_{PO}			40	mA

Note: * A pull-up resistor to V_{CC} on the $\overline{E}$ input is required to keep the device deselected.
Otherwise, power-on current approaches I_{CC} active.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

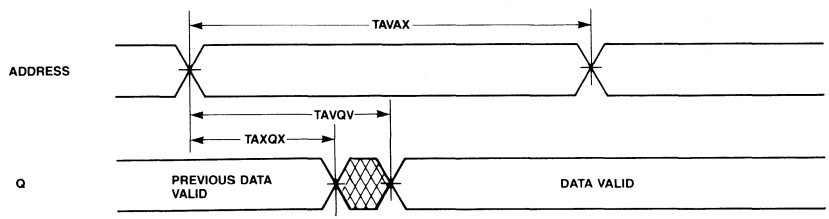
Read Cycle

Parameter	Symbol	MB8171-55 Min	MB8171-55 Max	MB8171-70 Min	MB8171-70 Max	Unit
Read cycle time	TAVAX	55		70		ns
Address access time	TAVQV		55		70	ns
Chip enable access time	TELQV		55		70	ns
Output hold from address change	TAXQX	5		5		ns
Chip enable to output in low-Z*1,2	TELQX	10		10		ns
Chip enable to output in high-Z*1,2	TEHQZ	0	30	0	40	ns
Chip enable to power up time	TELIH	0		0		ns
Chip enable to power down	TEHIL		30		35	ns

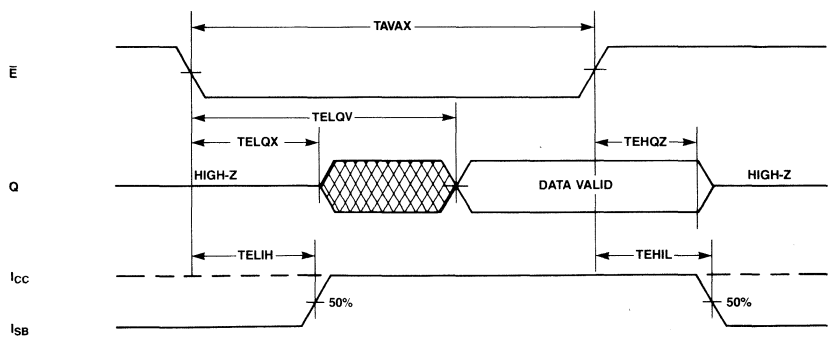
Notes: *1 Transition is measured at the point of ±500 mV from steady state voltage.

Read Cycle Timing Diagrams

Read Cycle: Address Controlled*1 *2



Read Cycle: $\overline{E}$ Controlled*2 *3



NOTES: *1 $\overline{E}$ IS LOW.
*2 $\overline{W}$ IS HIGH TO READ CYCLES.
*3 ADDRESS VALID PRIOR TO OR COINCIDENT WITH $\overline{E}$ TRANSITION LOW.

AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

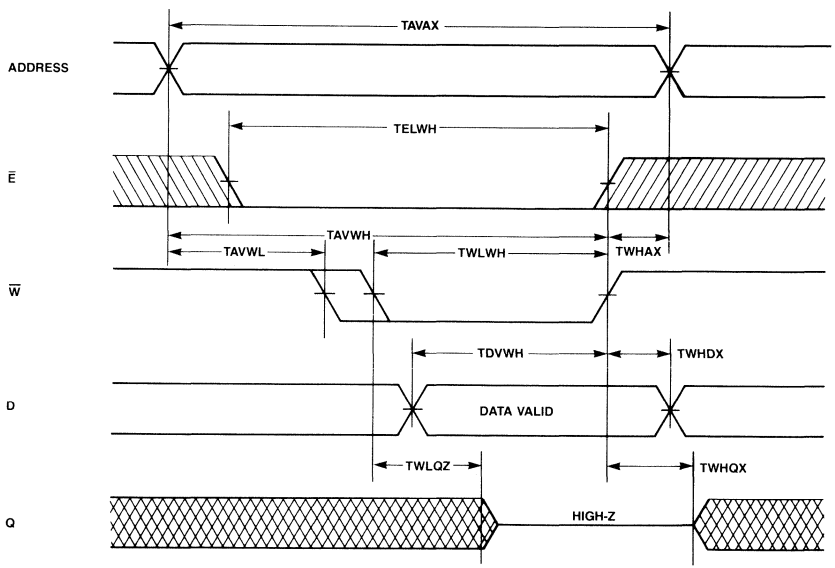
Write Cycle

Parameter	Symbol	MB8171-55 Min	MB8171-55 Max	MB8171-70 Min	MB8171-70 Max	Unit
Write cycle time	TAVAX	55		70		ns
Chip enable to end of write	TELWH	45		55		ns
Address valid to end of write	TAVWH	45		55		ns
Address setup time	TAVWL	5		10		ns
Address setup time	TAVEL	0		0		ns
Write pulse width	TWLWH	35		45		ns
Data valid to end of write	TDVWH	35		45		ns
Write recovery time	TWHAX	5		10		ns
Write recovery time	TEHAX	10		15		ns
Data hold time	TWHDX	0		0		ns
Data hold time	TEHDX	5		5		ns
Write enable to output in high-Z*1,2	TWLQZ	0	30	0	35	ns
Output active from end of write*1,2	TWHQX	0		0		ns

Notes: *1 Transition is measured at the point of ±500 mV from steady state voltage.

Write Cycle Timing Diagrams

Write Cycle: $\overline{W}$ Controlled*1 *2



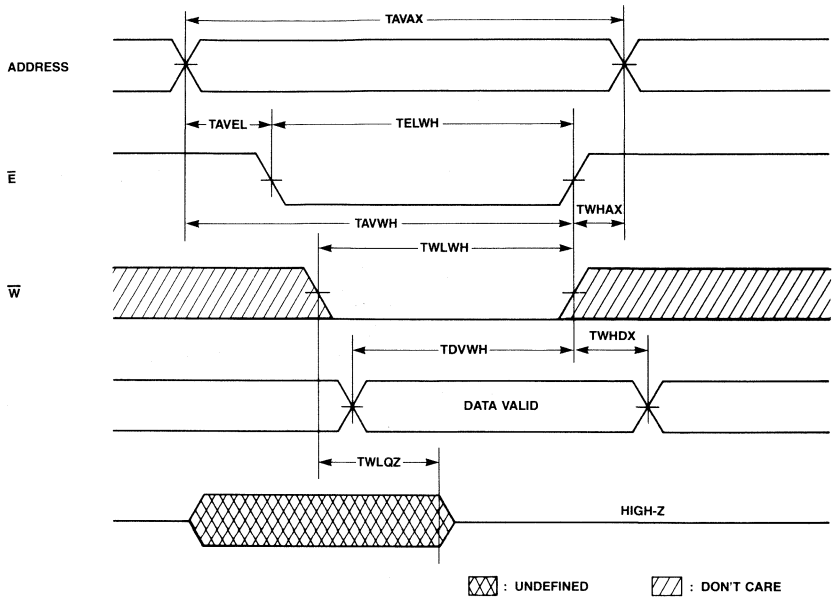
NOTES: *1 Ē OR W MUST BE HIGH DURING ADDRESS TRANSITIONS.
*2 IF Ē GOES HIGH SIMULTANEOUSLY WITH W̄ HIGH, THE OUTPUT REMAINS IN A HIGH IMPEDANCE STATE.

: UNDEFINED

AC Characteristics
(continued)
(Recommended operating conditions unless otherwise noted.)

Write Cycle Timing Diagram

Write Cycle: $\overline{E}$ Controlled[*1]

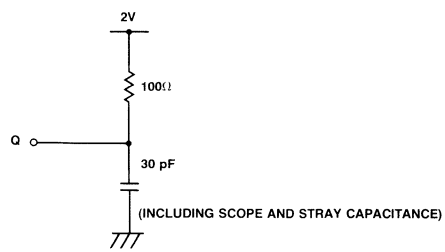


NOTES: *1 $\overline{E}$ OR $\overline{W}$ MUST BE HIGH DURING ADDRESS TRANSITIONS.

AC Test Conditions

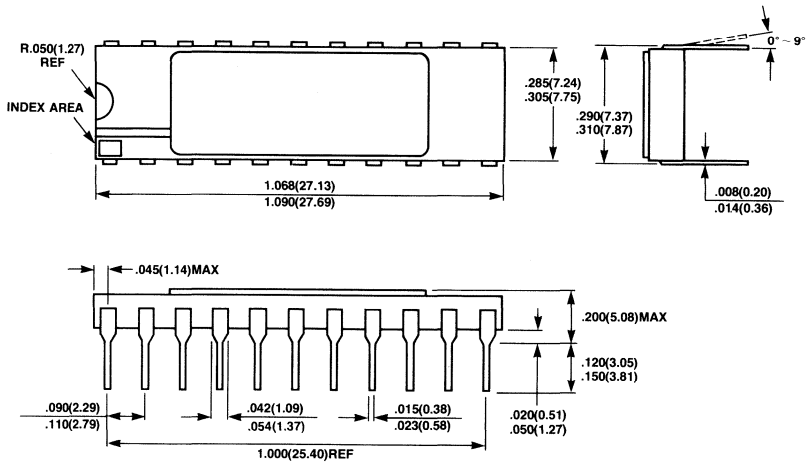
Input pulse levels:	0.8V to 2.2V
Input pulse rise and fall times:	5 ns
Timing measurement reference levels:	Input: 1.5V
	Output: 1.5V

Output Load:



Package Dimensions
Dimensions in inches
(millimeters)

22-Lead Ceramic (Metal Seal) Dual In-Line Package
(Case No.: DIP-22C-A01)



NMOS EPROMs

MBM2764/2764X 5-2
MBM27128 5-10
MBM27128X 5-17
MBM27256 5-27
MBM27256X/27256W 5-36

FUJITSU
MICROELECTRONICS, INC.

NMOS 65,536-BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

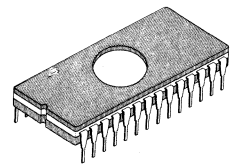
MBM2764-20
MBM2764-25
MBM2764-30
MBM2764-30-X

DESCRIPTION

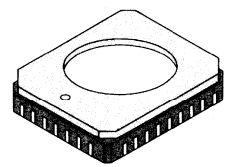
The Fujitsu MBM2764 is a high-speed 65,536-bit static N-channel MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially suited for applications where rapid turn-around and/or bit pattern experimentation are important.

A 28-pin dual in-line package with a transparent lid is used to package the MBM2764. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM2764 is fabricated using N-channel double polysilicon gate technology with single transistor stacked gate cells. It is organized as 8,192 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



CERDIP PACKAGE
DIP-28C-C01



LCC Package
LCC-32C-A01

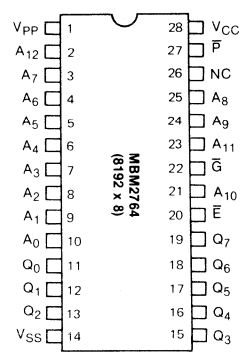
FEATURES

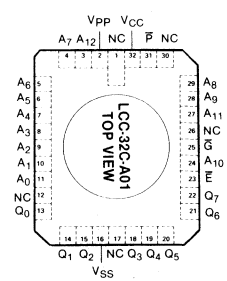
- **Organized as 8192 words by 8-bits, fully decoded**
- **Fast Access Time:**

MBM2764-20	**200 ns**
MBM2764-25	**250 ns**
MBM2764-30	**300 ns**
MBM2764-30-X	**300 ns**

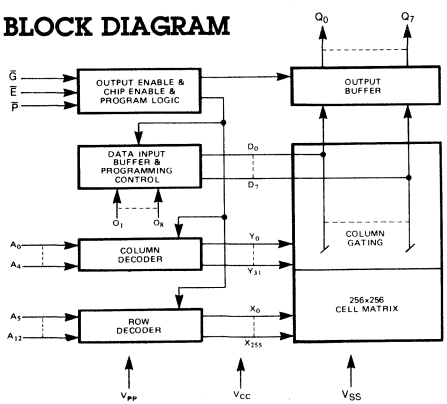
- **Simple programming requirements**
- **Single location programming**
- **Programs with Quick Pro™ (see page 4-7)**
- **Low power requirement:**
  550mW active
  193mW standby
- **Extended temperature range: MBM2764-30-X: −40°C to +85°C**
- **No clocks required, Fully static operation**
- **TTL compatible inputs/outputs**
- **Three-state output with OR-tie capability**
- **Output Enable $\overline{G}$ pin for simplified memory expansion**
- **Single +5V Operation**
- **Standard 28-pin DIP package**
- **Pin compatible with Intel 2764**

PIN ASSIGNMENT





MBM2764 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter		Symbol	Value	Unit
Temperature Under Bias	MBM2764-20/-25/30	T_A	−25 to +85	°C
	MBM2764-30-X		−50 to +95	
Storage Temperature		T_{stg}	−65 to +125	°C
Inputs/Outputs with Respect to V_{SS}		V_{IN}, V_{OUT}	−0.6 to +7	V
V_{CC} with Respect to V_{SS}		V_{CC}	−0.6 to +7	V
V_{PP} with Respect to V_{SS}		V_{PP}	−0.6 to +22	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

FUNCTIONS AND PIN CONNECTIONS V_{CC} (28) = +5, V_{SS} (14) = GND

Function (DIP Pin No.) / Mode	Address Input (2 ~ 10,21,23 ~ 25)	Data Q (11 ~ 13,15 ~ 19)	$\overline{E}$ (20)	$\overline{G}$ (22)	$\overline{P}$ (27)	I_{CC} Supply (28)	V_{PP} (1)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	I_{CC2}	V_{CC}
Output Disable	A_{IN}	High Z	V_{IL}	V_{IH}	Don't Care	I_{CC2}	V_{CC}
				Don't Care	V_{IL}		
Stand By	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	I_{CC1}	V_{CC}
Program	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{IL}	I_{CC2}	V_{PP}
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	I_{CC2}	V_{PP}
Program Inhibit	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	I_{CC1}	V_{PP}

Note: 1. $\overline{P}$ works as if G (output enable) during reading operation.

CAPACITANCE

(T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	4	6	pF
Ouput Capacitance (V_{OUT} = 0V)	C_{OUT}	8	12	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS} = GND)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature	
						MBM2764-20/-25/-30	MBM2764-30-X
Supply Voltage	V_{CC}	4.50	5.0	5.50	V	0 °C to +70 °C	−40 °C to +85 °C
Supply Voltage	V_{PP}	V_{CC} − 0.6	—	V_{CC} + 0.6	V		
Supply Voltage	V_{SS}	—	GND	—	V		
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 1	V		
Input Low Voltage	V_{IL}	−0.1	—	0.8	V		

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Conditions	Symbol	Min	Max	Unit
Input Load Current	$V_{IN} = 5.5V$	I_{LI}	—	10	μA
Output Leakage Current	$V_{OUT} = 5.5V$	I_{LO}	—	10	μA
V_{PP} Supply Current	$V_{PP} = V_{CC} \pm 0.6V$	I_{PP}	—	15	mA
V_{CC} Standby Current	$\overline{E} = V_{IH}$	I_{CC1}	—	35	mA
V_{CC} Supply Current (Active)	$\overline{E} = V_{IL}$	I_{CC2}	—	100	mA
Input Low Voltage	—	V_{IL}	−0.1	+0.8	V
Input High Voltage	—	V_{IH}	2.0	$V_{CC}+1$	V
Output Low Voltage	$I_{OL} = 2.1mA$	V_{OL}	—	0.45	V
Output High Voltage	$I_{OH} = -400\mu A$	V_{OH}	2.4	—	V

AC CHARACTERISTICS

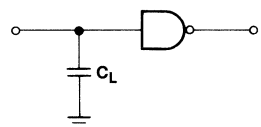
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MBM2764-20		MBM2764-25		MBM2764-30 MBM2764-30-X		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	TAVQV	—	200	—	250	—	300	ns	$\overline{E} = \overline{G} = V_{IL}$
$\overline{E}$ to Output Delay	TELQV	—	200	—	250	—	300	ns	$\overline{E} = V_{IL}$
$\overline{G}$ to Output Delay	TGLQV	10	70	10	100	10	120	ns	$\overline{E} = V_{IL}$
Output Enable High to Output Float	TGHQZ, TEHQZ	0	60	0	60	0	105	ns	$\overline{E} = V_{IL}$
Address to Output Hold	TAXQX	0	—	0	—	0	—	ns	$\overline{E} = \overline{G} = V_{IL}$

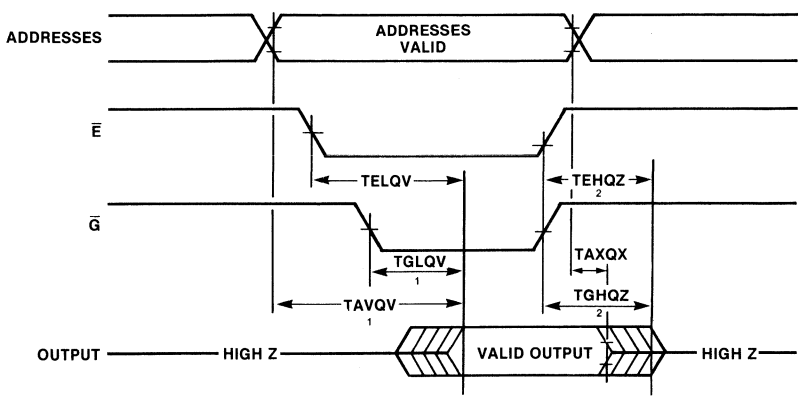
AC TEST CONDITIONS

Input Pulse levels: 0.8V to 2.2V
Input Rise and Fall Time: ≤20nsec
Timing Measurement Reference Levels: 1.0V and 2.0V for inputs
0.8V and 2.0V for outputs
1 TTL gate and C_L = 100 pF

Output Load:



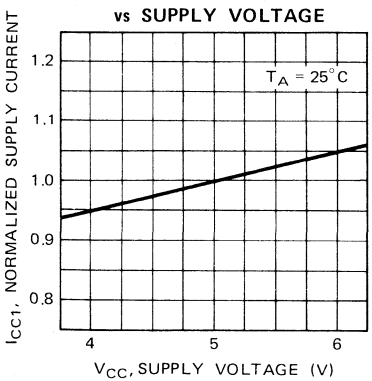
OPERATION TIMING DIAGRAM



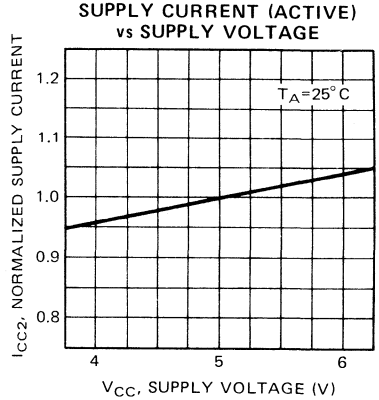
Notes: (1) $\overline{G}$ may be delay up to TAVQV—TGLQV after the falling edge of $\overline{E}$ without impact on TAVQV.
(2) TGHQZ or TEHQZ are specified from $\overline{G}$ or $\overline{E}$, whichever occurs first.

TYPICAL CHARACTERISTICS CURVES

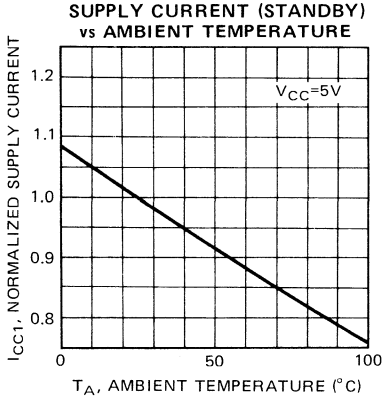
SUPPLY CURRENT (STANDBY)
vs SUPPLY VOLTAGE



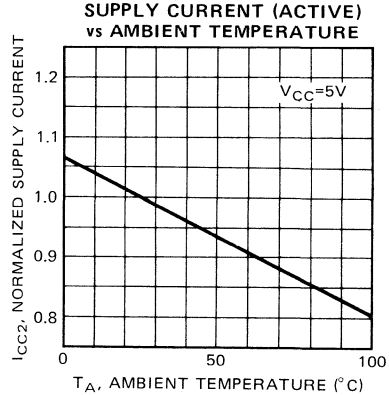
SUPPLY CURRENT (ACTIVE)
vs SUPPLY VOLTAGE



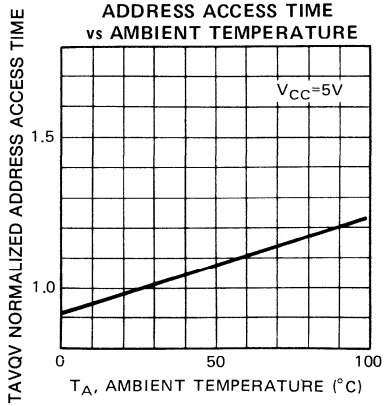
SUPPLY CURRENT (STANDBY)
vs AMBIENT TEMPERATURE



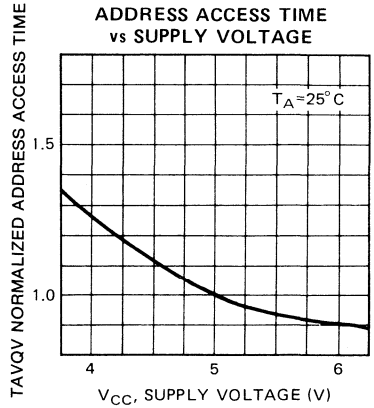
SUPPLY CURRENT (ACTIVE)
vs AMBIENT TEMPERATURE



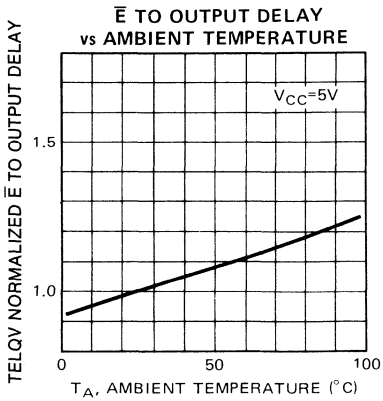
ADDRESS ACCESS TIME
vs AMBIENT TEMPERATURE

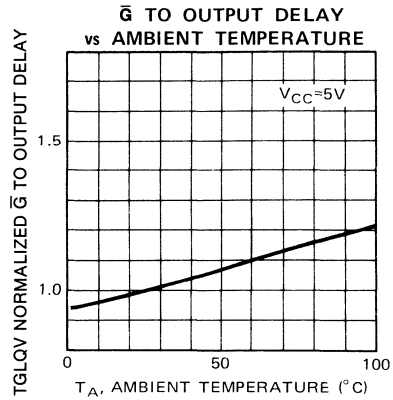


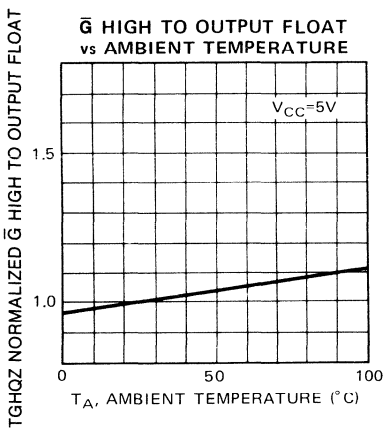
ADDRESS ACCESS TIME
vs SUPPLY VOLTAGE

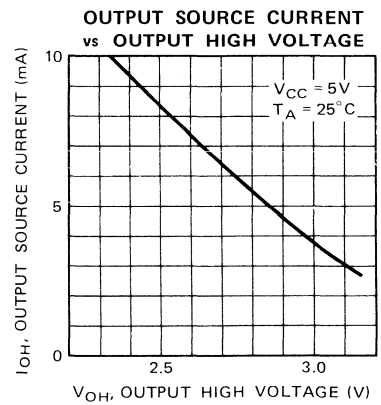


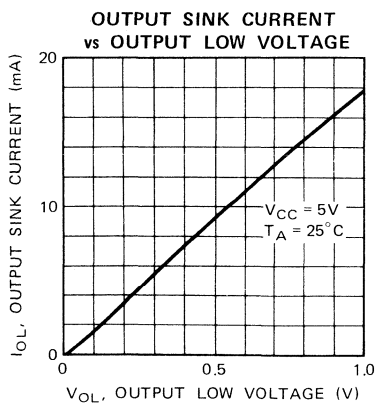
TYPICAL CHARACTERISTICS CURVES (Continued)

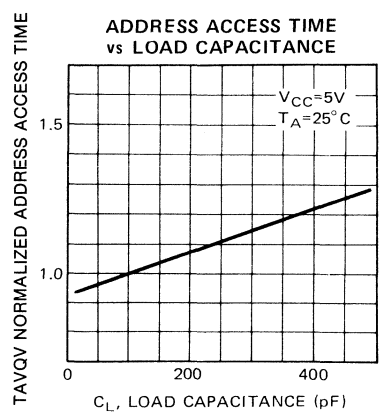












PROGRAMMING/ERASING INFORMATION

MEMORY CELL DESCRIPTION

The MBM2764 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 1). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 2). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 2.

Fig. 1 — MEMORY CELL

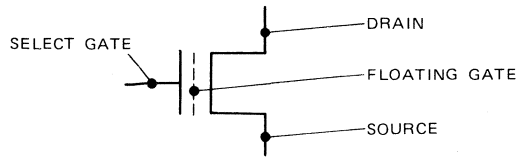
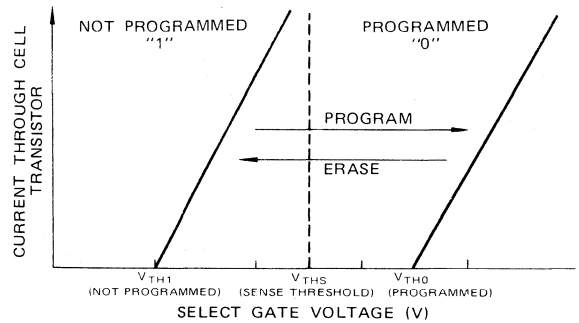


Fig. 2 — MEMORY CELL THRESHOLD SHIFT



CONVENTIONAL PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM2764 has all 65,536-bits in the "1" or high state. "0's" are loaded into the MBM2764 through the procedure of programming.

The programming mode is entered when +21V is applied to the V_{PP} pin and $\overline{E}$ and $\overline{P}$ are both at V_{IL}. During programming, $\overline{E}$ is kept at V_{IL}. A 0.1 μF capacitor between V_{PP} and V_{SS} is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. Eight bit patterns are placed on the respective output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, 50 msec, TTL low level pulse is applied to the $\overline{P}$ input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{P}$ input is prohibited when programming.

QUICK PRO™

In addition to the standard 50 millisecond pulse width programming procedure, the MBM2764 can be programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The algorithm (shown in figure 3) utilizes a sequence of 1 millisecond pulse to program each location. This algorithm will typically yield a savings of 86% in programming time per device when utilized in commercially available programmers. However, in custom programmer designs that require less overhead the savings can be even greater.

The programming mode is entered when +6V is applied to the VCC pin followed by applying +21V to VPP pin. A TTL low input must be applied to the E input. Conversely, a TTL high input must be applied to the G input. After the programming voltages and TTL levels have stabilized, a sequence of 1 millisecond pulses must be applied to the P pin for programming. After each pulse, a pulse counter must be incremented and the location should be checked for accuracy. Upon verification, an additional sequence of 1 millisecond pulses equal to the present value of the pulse counter must be applied to the location to ensure proper levels of stored charge. An alternate approach to the additional pulses would be to apply a single TTL low pulse with a width equivalent to the value of the pulse counter multiplied by 1 millisecond. When the pulse counter reaches a maximum of 20, the verification procedure is skipped and a flag is set to indicate a program failure. Upon completion of programming of the entire device, a final array verification (all locations) is required. All Fujitsu devices will typically require only two 1 millisecond pulses (one initial and one additional) to reach proper stored charge levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the MBM2764 to an ultraviolet light source. A dosage of 15W-seconds/cm^2 is required to completely erase an MBM2764. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å) with intensity of 12,000μW/cm^2 for 15 to 20 minutes.

The MBM2764 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM2764 and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the MBM2764 and such exposure should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMING / ERASING INFORMATION (Continued)

DC CHARACTERISTICS

(T_A = 25 ± 5 °C, V_{CC} = 5V ±5%, V_{PP} = 21V ±0.5V)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Leakage Current	I_{LI}	—	10	μA	V_{IN} = 0.45V–5.25V
Output Low Voltage	V_{OL}	—	0.45	V	I_{OL} = 2.1 mA
Output High Voltage	V_{OH}	2.4	—	V	I_{OH} = −400μA
V_{CC} Supply Current	I_{CC}	—	100	mA	—
Input Low Voltage	V_{IL}	−0.1	0.8	V	—
Input High Voltage	V_{IH}	2.0	V_{CC} +1	V	—
V_{PP} Supply Current	I_{PP}	—	30	mA	$\overline{CE} = \overline{PGM} = V_{IL}$

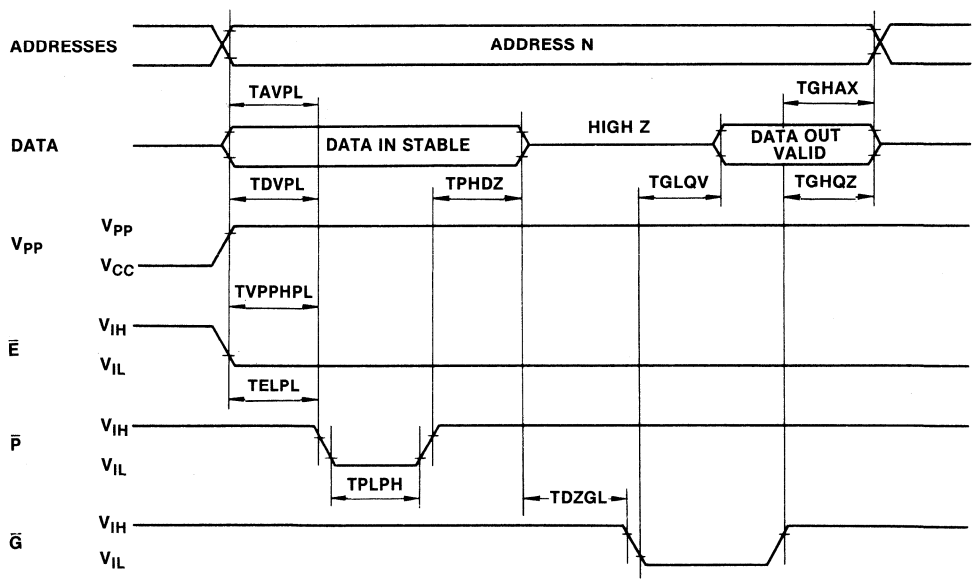
AC CHARACTERISTICS

(T_A = 25 ± 5 °C, V_{CC} = 5V ±5%, V_{PP} = 21V ± 0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	TAVPL	2	—	—	μs
$\overline{E}$ Setup Time	TELPL	2	—	—	μs
Data Setup Time	TDVPL	2	—	—	μs
Address Hold Time	TGHAX	0	—	—	μs
Data Hold Time [1]	TPHDZ	2	—	—	μs
Chip Enable to Output Float Delay	TGHQZ	—	—	130	ns
V_{PP} Setup Time	TVPPHL	2	—	—	μs
$\overline{P}$ Pulse Width-Conventional	TPLPH	45	50	55	ms
$\overline{P}$ Pulse Width-Quick-Pro™	TPLPH	0.95	1.00	1.05	ms
$\overline{G}$ Setup Time [1]	TDZGL	2	—	—	μs
Data Valid from $\overline{G}$	TGLQV	—	—	150	ns

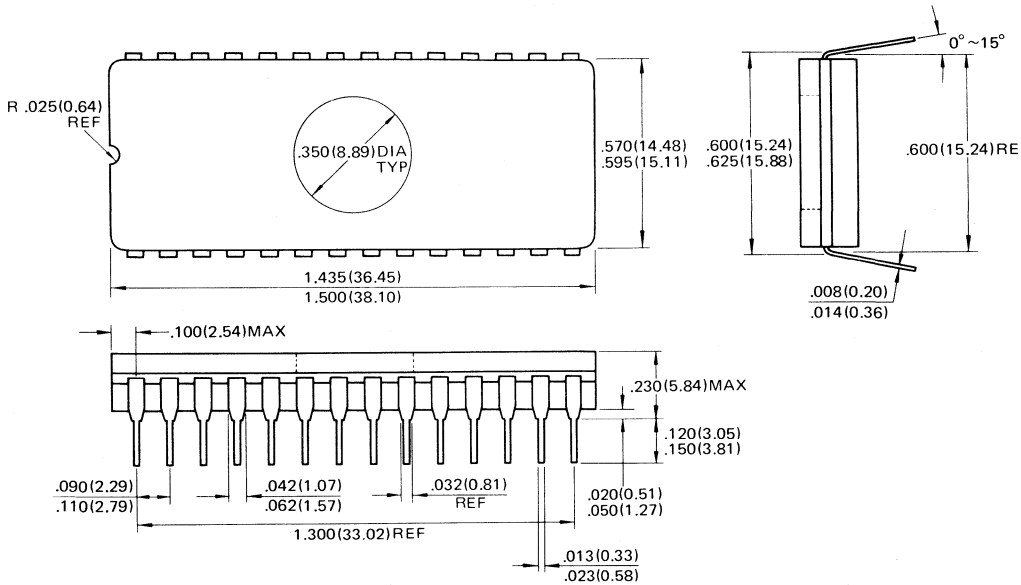
Notes:
[1] TPHDZ + TDZQL ≥ 50μs.

PROGRAMMING WAVEFORM



PACKAGE DIMENSIONS Dimensions in inches (millimeters)

28-LEAD CERAMIC (CERDIP WITH TRANSPARENT LID) DUAL IN-LINE PACKAGE DIP-28C-C01



MBM27128-20, MBM27128-25, MBM27128-30

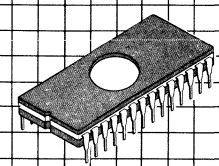
UV Erasable 131,072-Bit Read Only Memory

Description

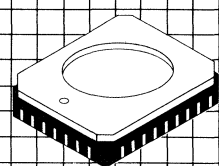
The Fujitsu MBM27128 is a high speed 131,072-bit static N-channel MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for applications where rapid turn-around and/or bit pattern experimentation are important.

A 28-pin dual in-line package or leadless chip carrier (32-pin) with a transparent lid is used to package the MBM27128. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM27128 is fabricated using N-channel double polysilicon gate technology with single transistor stacked gate cells. It is organized as 16,384 words by 8-bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in single supply systems.



Cerdip Package
DIP-28C-C01



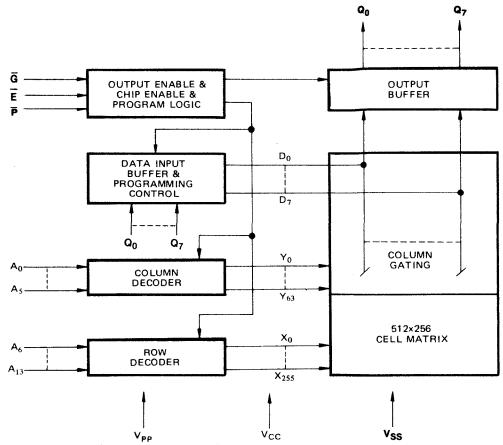
Ceramic Package
LCC-32C-A01

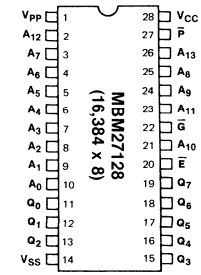
Features

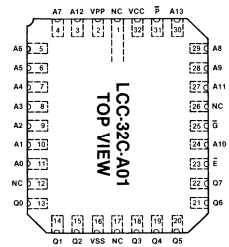
- **Organized as 16,384 x 8 fully decoded**
- **Low power requirement: [550 mW (act), 193 mW (standby)]**
- **No clocks required (fully static operation)**
- **Programmable utilizing the Quick Pro™ Algorithm**
- **Program compatible with the Intel int$_e$ligent Programming™ Algorithm**
- **Fast Access Time:**
  MBM27128-20 200 ns max.
  MBM27128-25 250 ns max.
  MBM27128-30 300 ns max.
- **TTL compatible inputs/outputs**
- **Three-state output with OR-tie capability**
- **Output Enable $\overline{G}$ pin provides precise control of the data bus**
- **Single +5V operation**
- **Standard 28-pin DIP package**
- **Pin compatible with Intel 27128**

Quick Pro™ is a trademark of Fujitsu Microelectronics Inc.
int$_e$ligent Programming™ is a trademark of Intel Corporation.

MBM27128 Block Diagram and Pin Assignments







Absolute Maximum Ratings
(See Note)

Parameter	Symbol		Unit
Temperature Under Bias	T_A	−25 to +85	°C
Storage Temperature	T_{stg}	−65 to +125	°C
Inputs/Outputs with Respect to V_{SS}	V_{IN}, V_{OUT}	−0.6 to +7	V
V_{PP} with Respect to V_{SS}	V_{PP}	−0.6 to +22	V
V_{CC} with Respect to V_{SS}	V_{CC}	−0.6 to +7	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Functions and Pin Connections

Mode	Function (DIP Pin No.) Address Input A_0-A_{13} (2-10,23-26,21)	Data Q_0-Q_7 (11-13,15-19)	$\overline{E}$ (20)	$\overline{G}$ (22)	$\overline{P}$ (27)	V_{CC} (28)	V_{PP} (1)	V_{SS} (14)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	V_{SS}
Output Disable	Don't Care	High Z	V_{IL}	V_{IH} / Don't Care	Don't Care / V_{IL}	V_{CC}	V_{CC}	V_{SS}
Stand by	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{CC}	V_{SS}
Program	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{IL}	V_{CC}	V_{PP}	V_{SS}
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{PP}	V_{SS}
Program Inhibit	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{PP}	V_{SS}

Capacitance
(T_A = 25°C, f = 1MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	—	4	6	pF
Ouput Capacitance (V_{OUT} = 0V)	C_{OUT}	—	8	12	pF

Recommended Operating Conditions
(Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
V_{CC} Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
V_{PP} Supply Voltage	V_{PP}	$V_{CC}-0.6$	—	$V_{CC}+0.6$	V	
Input High Voltage	V_{IH}	2.0	—	$V_{CC}+1$	V	
Input Low Voltage	V_{IL}	−0.1	—	0.8	V	

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

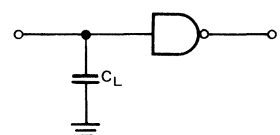
Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.5V)	I_{LI}	—	—	10	μA
Output Leakage Current (V_{OUT} = 5.5V)	I_{LO}	—	—	10	μA
V_{CC} Standby Current ($\overline{E} = V_{IH}$)	I_{CC1}	—	—	35	mA
V_{CC} Supply Current ($\overline{E} = V_{IL}$)	I_{CC2}	—	—	100	mA
V_{PP} Supply Current ($V_{PP} = V_{CC} \pm 0.6$V)	I_{PP}	—	—	5	mA
Output Low Voltage (V_{OL} = 2.1mA)	V_{OL}	—	—	0.45	V
Output High Voltage (I_{OH} = −400μA)	V_{OH}	2.4	—	—	V

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

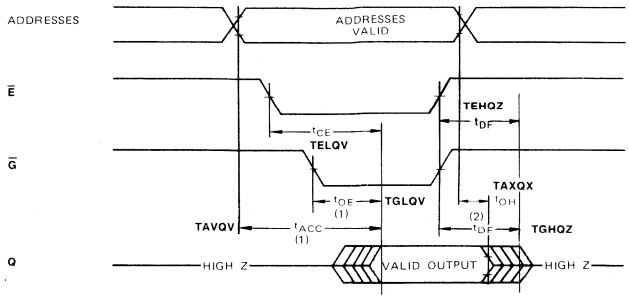
Parameter	Symbol Alternate	Symbol Standard*	MBM27128-20 Min	MBM27128-20 Max	MBM27128-25 Min	MBM27128-25 Max	MBM27128-30 Min	MBM27128-30 Max	Unit
Address Access Time	t_{ACC}	TAVQV		200		250		300	ns
$\overline{E}$ to Output Delay	t_{CE}	TELQV		200		250		300	ns
$\overline{G}$ to Output Delay	t_{OE}	TGLQV		70		100		120	ns
Address to Hold Time	t_{OH}	TAXQX	0		0		0		ns
$\overline{E}$ or $\overline{G}$ High to Output Float	t_{DF}	TGHQZ, TEHQZ	0	60	0	60	0	105	ns

AC Test Conditions
(Including programming)

Input Pulse levels:	**0.8V to 2.2V**
Input Rise and Fall Time:	**≤ 20nsec**
Timing Measurement Reference Levels:	**1.0V and 2.0V for inputs** **0.8V and 2.0V for outputs**
Output Load:	**1 TTL gate and C_L = 100 pF**



Operation Timing Diagram



Note 1. $\overline{G}$ may be delayed up to TAVQV-TGLQV after falling edge of $\overline{E}$ without impact on TAVQV.
Notes 2. TGHDZ or TEHQZ is specified from $\overline{G}$ or $\overline{E}$ respectively, which ever occurs first.

Programming/Erasing Information

Memory Cell Description

The MBM27128 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 1). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 2). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 2.

Conventional Programming

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27128 has all 131,072-bits in the "1" or high state. "0's" are loaded into the MBM27128 through the procedure of programming.

The programming mode is entered when +21V is applied to the V_{PP} pin and $\overline{E}$ and $\overline{P}$ are both at V_{IL}. During programming, $\overline{E}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and V_{SS} is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. Eight bit patterns are placed on the respective output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, 50 msec, TTL low level pulse is applied to the $\overline{P}$ input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{P}$ input is prohibited when programming.

Fig. 1 — Memory Cell

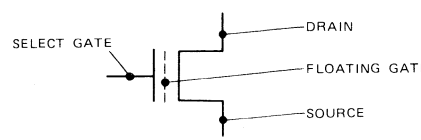
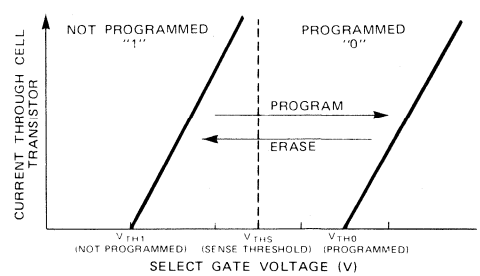


Fig. 2 — Memory Cell Threshold Shift



Programming/Erasure Information, continued

"Quick Pro™" Programming

In addition to the standard 50 millisecond pulse width programming procedure, the MBM27128 can be programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The algorithm (shown in figure 3) utilizes a sequence of 1 millisecond pulse to program each location. This algorithm will typically yield a savings of 86% in programming time per device when utilized in commercially available programmers. However, in custom programmer designs that require less overhead the savings can be even greater.

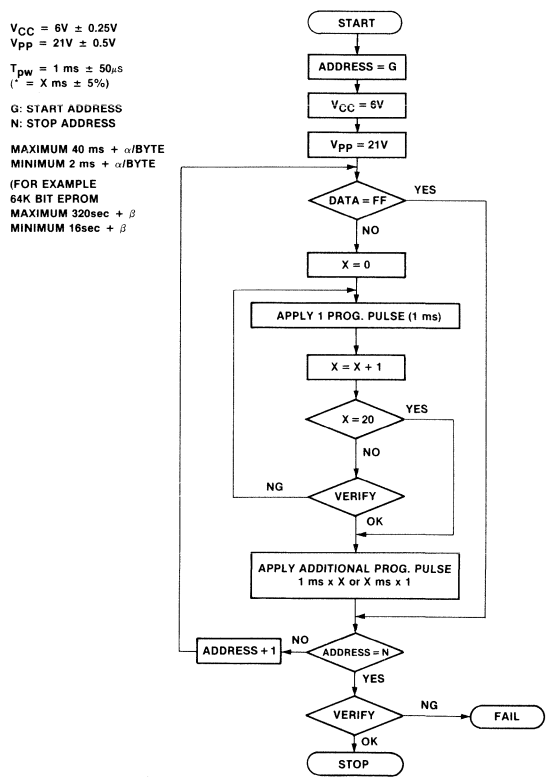
The programming mode is entered when +6V is applied to the VCC pin followed by applying +21V to VPP pin. A TTL low input must be applied to the $\overline{E}$ input and a TTL high input must be applied to the $\overline{G}$ input. After the programming voltages and TTL levels have stabilized, a sequence of 1 millisecond pulses must be applied to the $\overline{P}$ pin for programming. After each pulse, a pulse counter must be incremented and the location should be checked for accuracy. Upon verification, an additional sequence of 1 millisecond pulses equal to the present value of the pulse counter must be applied to the location to ensure proper levels of stored charge. An alternate approach to the additional pulses would be to apply a single TTL low pulse with a width equivalent to the value of the pulse counter multiplied by 1 millisecond. When the pulse counter reaches a maximum of 20, the verification procedure is skipped and a flag is set to indicate a program failure. Upon completion of programming of the entire device, a final array verification (all locations) is required. All Fujitsu devices will typically require only two 1 millisecond pulses (one initial and one additional) to reach sufficient stored charge levels.

Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the MBM27128 to an ultraviolet light source. A dosage of 15W-seconds/cm^2 is required to completely erase an MBM27128. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å) with intensity of 12,000μW/cm^2 for 15 to 20 minutes. The MBM27128 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM27128 and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the MBM27128 and such exposure should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

Figure 3. — Quick Pro™ Flow Chart



QUICK PRO™ IS A TRADEMARK OF FUJITSU LIMITED

Programming Characteristics

DC Characteristics

(T_A = 25 ±5°C,
V_{CC} = 5V ±5% (Conventional),
V_{CC} = 6V ± 0.25V (Quick Pro™)
V_{PP} = 21V ±0.5V)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input Leakage Current	I_{LI}	—	10	μA	V_{IN} = 5.25V/0.45V
V_{PP} Supply Current During Programming Pulse	I_{PP2}	—	30	mA	$\overline{E} = \overline{P} = V_{IL}$
V_{PP} Supply Current During Verify	I_{PP3}	—	5	mA	$\overline{E} = V_{IL}$ $\overline{P} = V_{IH}$
V_{PP} Supply Current Program Inhibit (Active)	I_{PP4}	—	5	mA	$\overline{E} = V_{IH}$
V_{CC} Supply Current Program Inhibit	I_{CC1}	—	35	mA	$\overline{E} = V_{IH}$
V_{CC} Supply Current Program & Verify	I_{CC2}	—	100	mA	—
Input Low Voltage	V_{IL}	−0.1	+0.8	V	—
Input High Voltage	V_{IH}	2.0	V_{CC} + 1	V	—
Output Low Voltage During Verify	V_{OL}	—	0.45	V	I_{OL} = 2.1 mA
Output High Voltage During Verify	V_{OH}	2.4	—	V	I_{OH} = −400μA

Note 1. V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.

Note 2. V_{PP} must not be greater than 21.5 volts including overshot. Permanent device change may occur if the device is taken out or put into socket remaining V_{PP} = 21 volts. Also, during $\overline{E} = \overline{P} = V_{IL}$, V_{PP} must not be switched from V_{CC} to 21 volts or vise-versa.

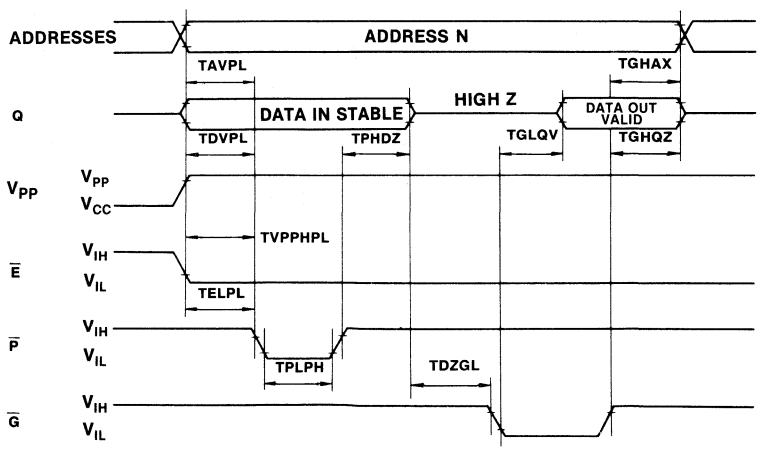
AC Characteristics

(T_A = 25 ±5°C,
V_{CC} = 5V ±5% (Conventional),
V_{CC} = 6V ± 0.25V (Quick Pro™)
V_{PP} = 21V ±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	TAVPL	2	—	—	μs
Chip Enable Setup Time	TELPL	2	—	—	μs
Output Enable Time [1]	TDZGL	2	—	—	μs
Data Setup Time	TDVPL	2	—	—	μs
Address Hold Time	TGHAX	0	—	—	μs
Data Hold Time [1]	TPHDZ	2	—	—	μs
Output Enable to Output Float Delay	TGHQZ	—	—	130	ns
Data Valid from Output Enable	TGLQV	—	—	150	ns
V_{PP} Setup Time	TVPPHPL	2	—	—	μs
$\overline{P}$ Pulse Width-Conventional	TPLPH	25	50	55	ms
$\overline{P}$ Pulse Width-Quick-Pro™	TPLPH	0.95	1.00	1.05	ms

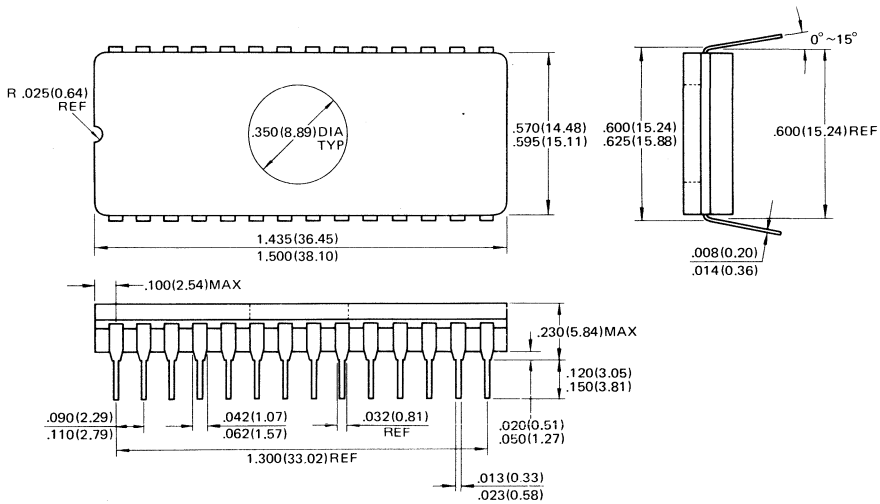
Note [1] TPHDZ + TDZGL ≥ 50μs.

Programming Waveform

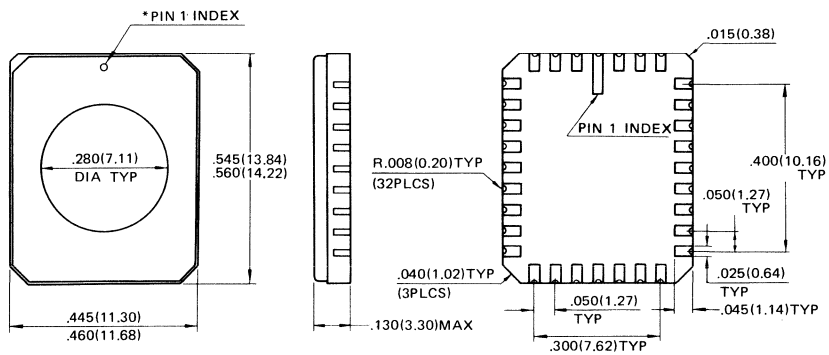


Package Dimensions
Dimensions in inches
(millimeters)

28-Lead Cerdip
(With Transparent Lid)
Dual In-Line Package
DIP-28C-C01



32-Pin Leadless Chip Carrier
LCC-32C-A01



*Shape of Pin 1 index: Subject to change without notice

FUJITSU

MBM27128-25-X, MBM27128-30-X

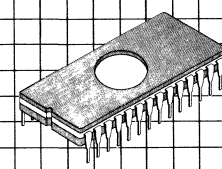
UV Erasable 131,072-Bit Read Only Memory

Description

The Fujitsu MBM27128-X is a high speed 131,072-bit static N-channel MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for applications where rapid turn-around and/or bit pattern experimentation are important.

A 28-pin Dual-In-Line package with a transparent lid is used to package the MBM27128-X. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM27128-X is fabricated using N-MOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 16,384 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.

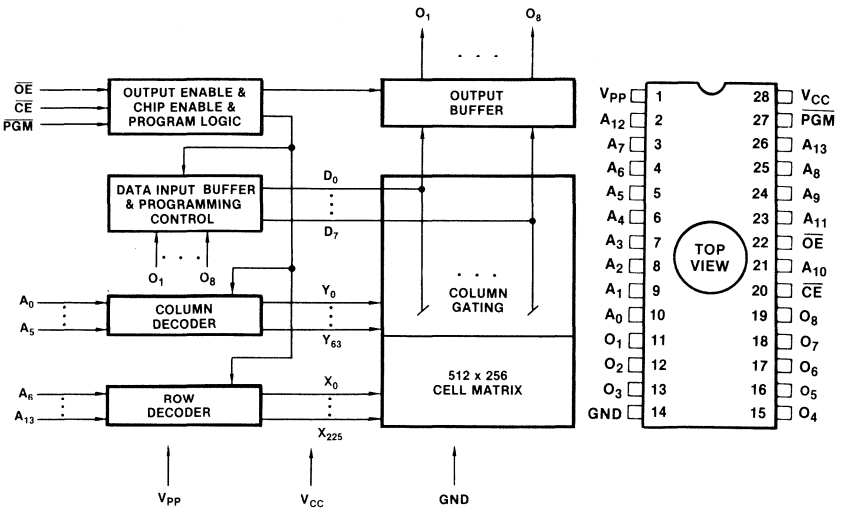


Cerdip Package
DIP-28C-C01

Features

- **Extended temperature range: −40°C to +85°C**
- **16,384 words x 8 bits organization, fully decoded**
- **Simple programming requirements**
- **Single location programming**
- **Programmable utilizing the Quick Pro™ Algorithm**
- **Programs with one 50ms or 1ms pulses**
- **Low power**
  Active: 660mW
  Standby: 220mW
- **No clocks required (fully static operation)**
- **Fast access time:**
  250ns max. (MBM27128-25-X)
  300ns max. (MBM27128-30-X)
- **TTL compatible inputs/outputs**
- **Three-state output with OR-tie capability**
- **Output Enable (OE) pin for simplified memory expansion**
- **Single +5V Supply, ±10% tolerance**
- **Standard 28-pin DIP package**
- **Interchangeable with Intel 27128-type device**

MBM27128-X Block Diagram and Pin Assignment



Absolute Maximum Ratings
(See Note)

Parameter	Symbol	Value	Unit
Temperature Under Bias	T_{BIAS}	−50 to +95	°C
Storage Temperature	T_{STG}	−65 to +125	°C
All Inputs/Outputs Voltage with Respect to GND	V_{IN}, V_{OUT}	−0.6 to +7	V
Voltage on A_9 with Respect to GND	V_{A9}	−0.6 to +13.5	V
V_{PP} Voltage with Respect to GND	V_{PP}	−0.6 to +22	V
Supply Voltage with Respect to GND	V_{CC}	−0.6 to +7	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operations sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Capacitance
(T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}	—	4	6	pF
Ouput Capacitance (V_{OUT} = 0V)	C_{OUT}	—	8	12	pF

Function and Pin Connections

Mode	Function (Pin No.) Address Input 2~10, 23~26, (21)	Data 11~13, (15~19)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{CC} (28)	V_{PP} (1)	GND (14)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	GND
Output Disable	A_{IN}	High Z	V_{IL}	V_{IH} Don't Care	Don't Care V_{IL}	V_{CC}	V_{CC}	GND
Stand by	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{CC}	GND
Program	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{IL}	V_{CC}	V_{PP}	GND
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{PP}	GND
Program Inhibit	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{PP}	GND

Recommended Operating Conditions
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
V_{PP} Supply Voltage	V_{PP}	$V_{CC}-0.6$	—	$V_{CC}+0.6$	V
Input High Voltage	V_{IH}	2.0	—	$V_{CC}+1$	V
Input Low Voltage	V_{IL}	−0.1	—	0.8	V
Operating Temperature	T_A	−40	—	85	°C

Note: *V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.5V)	I_{LI}	—	—	10	μA
Output Leakage Current (V_{OUT} = 5.5V)	I_{LO}	—	—	10	μA
V_{CC} Standby Current ($\overline{CE} = V_{IH}$)	I_{CC1}	—	—	40	mA
V_{CC} Supply Current ($\overline{CE} = V_{IL}$)	I_{CC2}	—	—	120	mA
V_{PP} Supply Current ($V_{PP} = V_{CC} \pm 0.6$V)	I_{PP1}	—	—	5	mA
Output Low Voltage (V_{OL} = 2.1mA)	V_{OL}	—	—	0.45	V
Output High Voltage (I_{OH} = −400μA)	V_{OH}	2.4	—	—	V

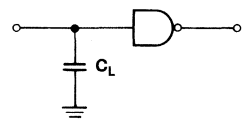
AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MBM27128-25-X Min	Typ	Max	MBM27128-30-X Min	Typ	Max	
Address Access Time*1	t_{ACC}	—	—	250	—	—	300	ns
$\overline{CE}$ to Output Delay	t_{CE}	—	—	250	—	—	300	ns
$\overline{OE}$ to Output Delay*1	t_{OE}	—	—	100	—	—	120	ns
Address to Output Hold Time	t_{OH}	0	—	—	0	—	—	ns
Output Enable High to Output Float*2	t_{DF}	0	—	60	0	—	105	ns

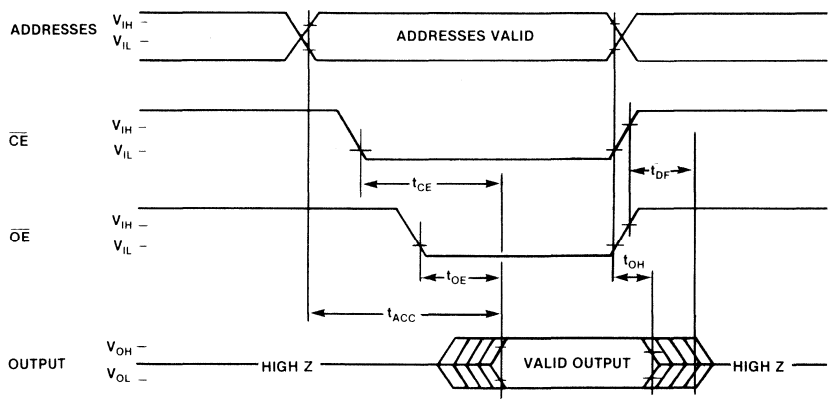
Note:
*1. OE may be delayed up to $t_{ACC}-t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
*2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first. Output Float is defined as the point where data is no longer driven.

Fig. 2 AC Test Conditions
(Including programming)

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Times:	≤20ns
Timing Measurement Reference Levels:	1.0V and 2.0V for inputs 0.8V and 2.0V for outputs
Output Load:	1 TTL gate and C_L = 100 pF



Operation Timing Diagram



Programming/Erasing Information

Memory Cell Description

The MBM27128-X is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 3). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 4). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 4.

Fig. 3 — Memory Cell

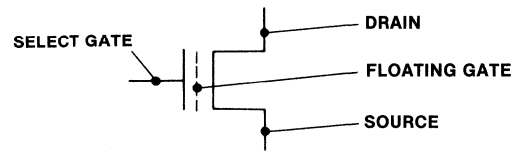
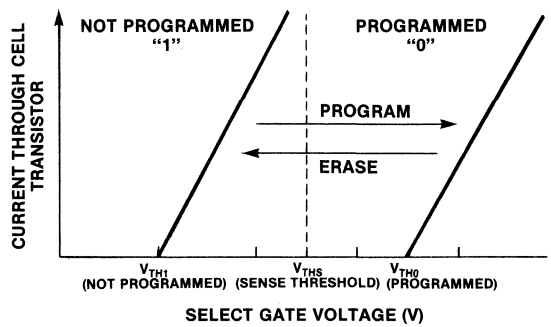


Fig. 4 — Memory Cell Threshold Shift



Programming

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27128-X has all 131,072 bits in the "1", or high, state. "0's" are loaded into the MBM27128-X through the procedure of programming.

Standard Programming

The programming mode is entered when +21V is applied to the V_{PP} pin and CE and $\overline{PGM}$ are both at V_{IL}. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8 bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, 50 msec, TTL low-level pulse is applied to the $\overline{PGM}$ input to accomplish the programming. The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{PGM}$ input is prohibited when programming.

Quick Programming

In addition to the standard 50 msec pulse width programming procedure, the MBM27128-X can be programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The algorithm (shown in Fig. 5) utilizes a sequence of 1 ms pulse to program each location.

The programming mode is entered when +21V and +6V are applied to the V_{PP} pin and V_{CC} pin respectively, and $\overline{PGM}$ and $\overline{OE}$ are V_{IH}. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. The 8 bit pattern are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a sequence of a 1 msec, TTL low-level pulse is applied to the $\overline{PGM}$ pin and after that additional pulse is applied to the $\overline{PGM}$ pin to accomplish the programming.

Programming/Erasure Information, continued

Procedure for Quick Pro™ (Refer to Fig. 5)

1) Input the start address (Address = G).

2) Set the $V_{CC} = 6V$ and $V_{PP} = 21V$.

3) Input data.

4) Compare the input data with FF. If data are FF, go to step 11). If not, proceed to the next step.

5) Clear the counter. (X←0).

6) Apply ONE programming pulse to PGM pin ($t_{PW} = 1$ ms Typ.)

7) Increment the counter (X←X + 1).

8) Compare the counter value with 20. If X = 20, go to step 10). If X < 20, proceed to the next step.

9) Verify the data. If programmed data are the same as input data, proceed to the next step. If not, go back to step 6).

10) Apply the additional programming pulse to the PGM pin (1 ms x X or X ms x 1).

11) Compare the address with the end address. If the programmed address is the end address, proceed to the next step.
If not, go back to step 3) for next address (G←G + 1).

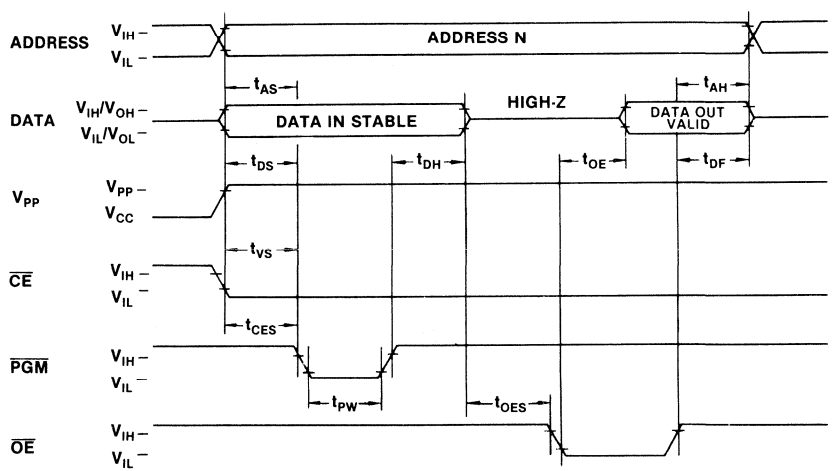
12) Verify the data. If the programmed data are not the same as the input data, the part failed. If the programmed data are the same as the input data, programming is completed.

Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the MBM27128-X to an ultraviolet light source. A dosage of 15W-seconds/cm^2 is required to completely erase an MBM27128-X. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12,000μW/cm^2 for 15 to 20 minutes. The MBM27128-X should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM27128-X and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV source at 2537Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the MBM27128-X and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

Programming Waveform

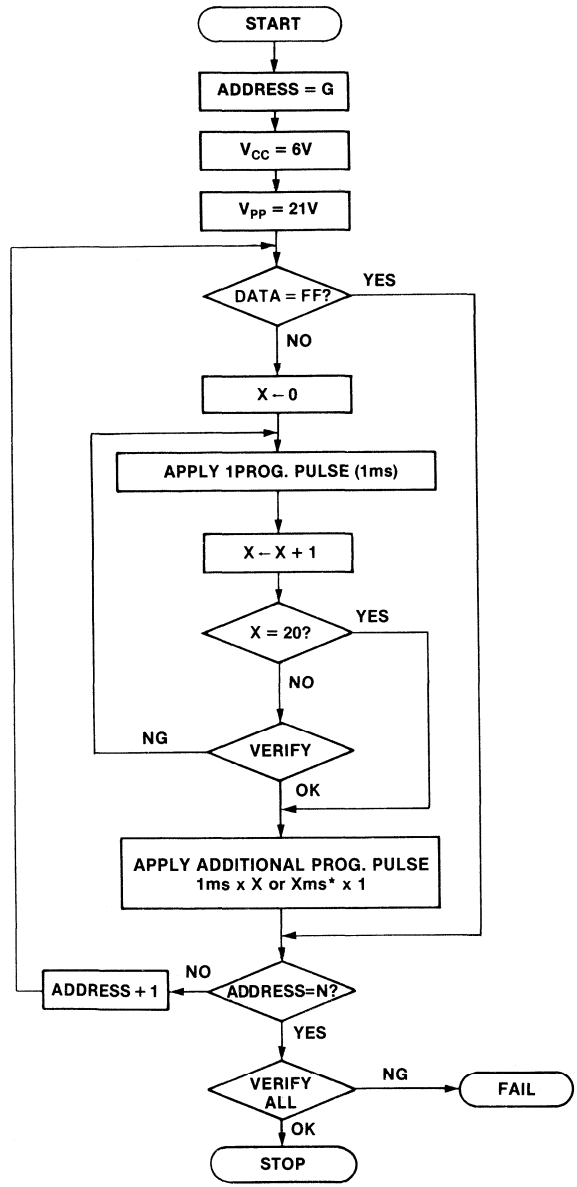


Programming/Erasure Information, continued

Fig. 5 — Programming Flow Chart For Quick Pro™

V_{CC} = 6V ± 0.25V
V_{PP} = 21V ± 0.5V
T_{PW} = 1ms ± 50ms
(* = Xms ± 5%)

G: START ADDRESS
N: STOP ADDRESS
X: COUNTER VALUE
MAXIMUM 42ms/BYTE
MINIMUM 1.9ms/BYTE



1. Standard Programming

DC Characteristics

(T_A = 25 ± 5 °C, V_{CC}*1 = 5V ± 5%, V_{PP}*2 = 21 ± 0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 5.25V/0.45V	I_{LI}	—	—	10	μA
V_{PP} Supply Current ($\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IL})	I_{PP2}	—	—	30	mA
V_{PP} Supply Current ($\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH})	I_{PP3}	—	—	5	mA
V_{PP} Supply Current ($\overline{CE}$ = V_{IH})	I_{PP4}	—	—	5	mA
V_{CC} Supply Current	I_{CC}	—	—	100	mA
Input Low Level	V_{IL}	−0.1	—	0.8	V
Input High Level	V_{IH}	2.0	—	V_{CC} + 1	V
Output Low Voltage During Verify (I_{OL} = 2.1mA)	V_{OL}	—	—	0.45	V
Output High Voltage During Verify (I_{OH} = −400 A)	V_{OH}	2.4	—	—	V

Note *1. V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.

Note *2. V_{PP} must not be greater than 22 volts including overshot. Permanent device damage may occur if the device is taken out of or placed into a socket with V_{PP} = 21 volts. Also, during $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 to 21 volts or vise-versa.

AC Characteristics

(T_A = 25 ± 5 °C, V_{CC} = V ± 5%, V_{PP} = 21 ± 0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{as}	2	—	—	μs
Chip Enable Setup Time	t_{CES}	2	—	—	μs
Output Enable Time	t_{OES}	2	—	—	μs
Data Setup Time	t_{DS}	2	—	—	μs
V_{PP} Setup Time	t_{VS}	2	—	—	μs
Address Hold Time	t_{AH}	0	—	—	μs
Data Hold Time	t_{DH}	2	—	—	μs
Output Enable to Output Float Delay	t_{DF}	0	—	130	ns
Data Valid from Output Enable	t_{OE}	—	—	150	ns
Programming Pulse Width	t_{PW}	45	50	55	ms

2. Quick Programming

DC Characteristics

(T_A = 25 ± 5 °C, V_{CC}*1 = 6V ± 0.25V, V_{PP}*2 = 21V ± 0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 6.25V/0.45V	I_{LI}	—	—	10	μA
V_{PP} Supply Current ($\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IL})	I_{PP2}	—	—	30	mA
V_{PP} Supply Current ($\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH})	I_{PP3}	—	—	5	mA
V_{PP} Supply Current ($\overline{CE}$ = V_{IH})	I_{PP4}	—	—	5	mA
V_{CC} Supply Current	I_{CC}	—	—	100	mA
Input Low Level	V_{IL}	−0.1	—	0.8	V
Input High Level	V_{IH}	2.0	—	V_{CC} + 1	V
Output Low Voltage During Verify (I_{OL} = 2.1mA)	V_{OL}	—	—	0.45	V
Output High Voltage During Verify (I_{OH} = −400A)	V_{OH}	2.4	—	—	V

Note *1. V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.

Note *2. V_{PP} must not be greater than 22 volts including overshot. Permanent device damage may occuring if the device is taken out of or placed into a socket with V_{PP} = 21 volts. Also, during $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 6 to 21 volts or vise-versa.

AC Characteristics

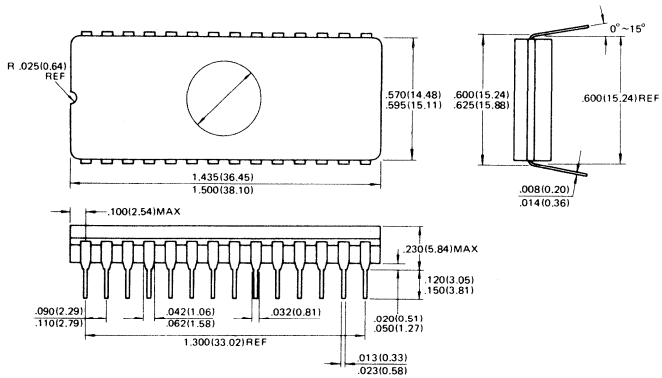
(T_A = 25 ± 5 °C, V_{CC} = 6V ± 0.25V, V_{PP} = 21 ± 0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{as}	2	—	—	μs
Chip Enable Setup Time	t_{CES}	2	—	—	μs
Output Enable Time	t_{OES}*	2	—	—	μs
Data Setup Time	t_{DS}	2	—	—	μs
V_{PP} Setup Time	t_{VS}	2	—	—	μs
Address Hold Time	t_{AH}	0	—	—	μs
Data Hold Time	t_{DH}*	2	—	—	μs
Output Enable to Output Float Delay	t_{DF}	0	—	130	ns
Data Valid from Output Enable	t_{OE}	—	—	150	ns
Programming Pulse Width	t_{PW}	0.95	—	1.05	ms

*t_{DH} + * t_{OES} ≥ 50μs

Package Dimensions
Dimensions in inches
(millimeters)

28-Lead Cerdip
(With Transparent Lid)
Dual In-Line Package
DIP-28C-C01



■ MBM27256-17, MBM27256-20, MBM27256-25

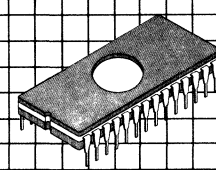
MOS 262,144-Bit UV Erasable and Electrically Programmable Read Only Memory

Description

The Fujitsu MBM27256 is a high speed 262,144-bit static NMOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for applications where rapid turn-around and/or bit pattern experimentation are important.

A 28-pin dual in-line package with a transparent lid is used to package the MBM27256. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM27256 is fabricated using NMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 32,768 words by 8-bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



Ceramic Package DIP-28C-C01

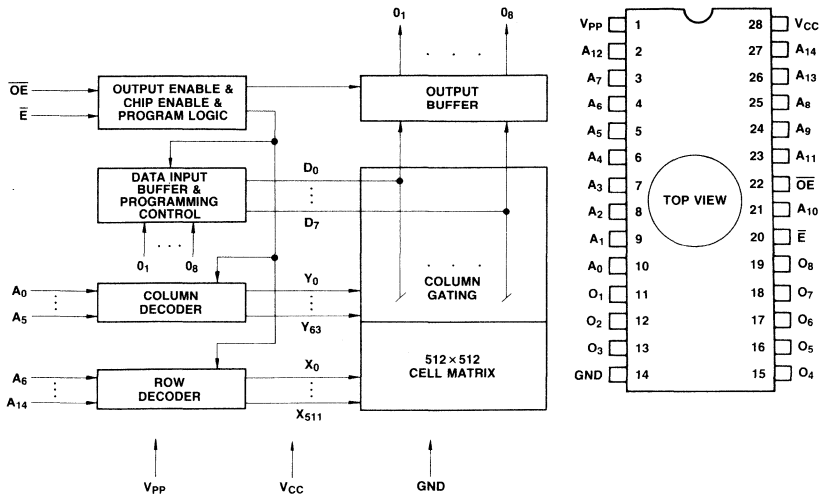
Features

- **32,768 words × 8-bit organization, fully decoded**
- **Single location programming**
- **Utilizes the faster programming algorithm QuickPro™**
- **Program voltage: 12.5V**
- **Low power requirement**
  Active: 525 mW
  Standby: 210 mW
- **No clocks required (fully static operation)**
- **Fast access time:**
  170 ns max. (MBM27256-17)
  200 ns max. (MBM27256-20)
  250 ns max. (MBM27256-25)
- **TTL compatible inputs/outputs**
- **Three-state output with OR-tie capability**
- **Output Enable (OE) pin for simplified memory expansion**
- **Single +5V supply, ±10% tolerance**
- **Standard 28-pin DP package**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

*QuickPro is a trademark of Fujitsu.

MBM27256 Block Diagram and Pin Assignment



Absolute Maximum Ratings
(see Note)

Rating	Symbol	Value	Unit
Temperature under Bias	T_{BIAS}	−25 to +85	°C
Storage Temperature	T_{STG}	−65 to +125	°C
All Inputs/Outputs Voltage with Respect to GND	V_{IN}, V_{OUT}	−0.6 to +7	V
Voltage on A_9 with Respect to GND	V_{A9}	−0.6 to +13.5	V
V_{PP} Voltage with Respect to GND	V_{PP}	−0.6 to +14	V
Supply Voltage with Respect to GND	V_{CC}	−0.6 to +7	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Functions and Pin Connections

	Function (Pin No.)						
Mode	**Address Input (2 ~ 10, 21, 23 ~ 27)**	**Data I/O (11 ~ 13, 15 ~ 19)**	**$\overline{E}$ (20)**	**$\overline{OE}$ (22)**	**V_{CC} (28)**	**V_{PP} (1)**	**GND (14)**
Read	A_{IN}	OUT	V_{IL}	V_{IL}	+5 V	+5 V	GND
Output Disable	A_{IN}	High-Z	V_{IL}	V_{IH}	+5 V	+5 V	GND
Standby	Don't Care	High-Z	V_{IH}	Don't Care	+5 V	+5 V	GND
Program	A_{IN}	IN	V_{IL}	V_{IH}	+6 V	+12.5 V	GND
Program Verify	A_{IN}	OUT	Don't Care	V_{IL}	+6 V	+12.5 V	GND
Program Inhibit	Don't Care	High-Z	V_{IH}	V_{IH}	+6 V	+12.5 V	GND

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}		4	6	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}		8	12	pF

Recommended Operating Conditions
(Reference to GND)

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
V_{PP} Supply Voltage	V_{PP}	V_{CC} −0.6		V_{CC} +0.6	V
Input High Voltage	V_{IH}	2.0		V_{CC} +1	V
Input Low Voltage	V_{IL}	−0.1		0.8	V
Operating Temperature	T_A	0		70	°C

Note: *V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

DC Characteristics
(Recommended operating conditions unless otherwise noted)

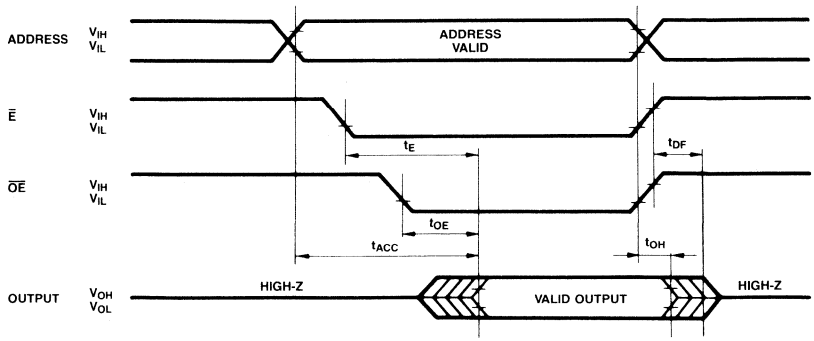
Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.5V)	I_{LI}			10	μA
Output Leakage Current (V_{OUT} = 5.5V)	I_{LO}			10	μA
V_{CC} Standby Current ($\overline{E}$ = V_{IH})	I_{CC1}			40	mA
V_{CC} Active Current ($\overline{E}$ = V_{IL})	I_{CC2}			100	mA
V_{PP} Supply Current (V_{PP} = V_{CC} ± 0.6V)	I_{PP1}			5	mA
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage (I_{OH} = −400μA)	V_{OH}	2.4			V

AC Characteristics
(Recommended operating conditions unless otherwise noted)

		MBM27256-17			MBM27256-20			MBM27256-25			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
Address Access Time*1 ($\overline{E}$ = $\overline{OE}$ = V_{IL})	t_{ACC}			170			200			250	ns
$\overline{E}$ to Output Delay ($\overline{OE}$ = V_{IL})	t_{CE}			170			200			250	ns
$\overline{OE}$ to Output Delay*1 ($\overline{E}$ = V_{IL})	t_{OE}			75			75			100	ns
Address to Output Hold	t_{OH}	0			0			0			ns
Output Enable High to Output Float*2	t_{DF}	0		60	0		60	0		60	ns

Notes: *1 $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{E}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{E}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

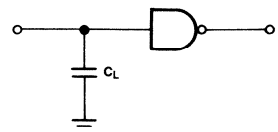
Operation Timing Diagram



AC Test Conditions

(including programming)

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Times:	≤20ns
Timing Measurement Reference Levels:	0.8V and 2.0V for inputs 0.8V and 2.0V for outputs
Output Load:	1 TTL gate and C_L = 100pF

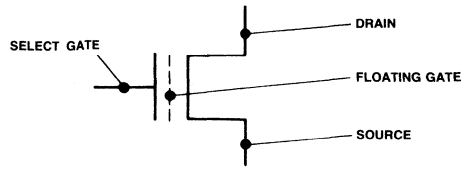


Programming/ Erasing Information

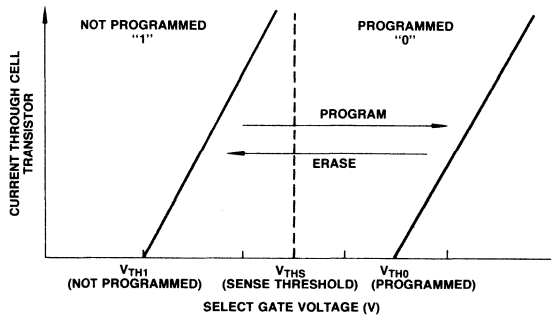
Memory Cell Description

The MBM27256 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Memory Cell diagram). The top gate is connected to the row decorder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Memory Cell Threshold Shift). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate. Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in the figure shown here.

Memory Cell



Memory Cell Threshold Shift



Programming

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27256 has all 262,144-bits in the "1", or high state. "0's" are loaded into the MBM27256 through the procedure of programming.

The MBM27256 is programmed with a fast programming algorithm called QuickPro™ designed by Fujitsu. The programming mode is entered when +12.5V and +6V are applied to V_{PP} and V_{CC} respectively, and $\overline{E}$ and $\overline{OE}$ are V_{IH}. A 0.1 μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. The 8-bit data pattern to be written is placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 1 ms programming pulse is applied to $\overline{E}$ and after that one additional pulse, which is 3 times as wide as previous pulse, is applied to $\overline{E}$ to accomplish the programming.

Procedure of QuickPro™ (Refer to the attached flowchart.)

1) Set the start address (=G) at the address pins.
2) Set V_{CC} = 6V, V_{PP} = 12.5V and $\overline{E}$ = V_{IH}.
3) Clear the programming pulse counter (X← 0).
4) Input data to respective pins.
5) Apply ONE programming pulse (t_{PW} = 1 ms Typ.) to $\overline{E}$.
6) Increment the counter (X←X + 1).
7) Compare the number (= X) of applied programming pulse with 25 and then verify the programmed data: If programmed data is verified, go to the next step regardless of X value. If X = 25 and programmed data is not verified, the device fails. If X = 25 and programmed data is not verified, go back to the step 5).
8) Apply one additional wide programming pulse to $\overline{E}$ (3X ms).
9) Compare the address with an end address (=N). If the programmed address is the end address, proceed to the next step. If not, increment the address (G←G+1) and then go to the step 3) for the next address.
10) Set V_{CC} = V_{PP} = 5V.
11) Verify all programmed data: If the verification succeeds, the programming is complete. If any programmed data is not the same as original data, the device fails.

A continuous TTL low level should not apply to $\overline{E}$ input pin during the program mode (V_{PP} = 12.5V, V_{CC} = 6V and $\overline{OE}$ = V_{IH}) because it is required that one programming pulse width does not exceed 78.75 ms at each address.

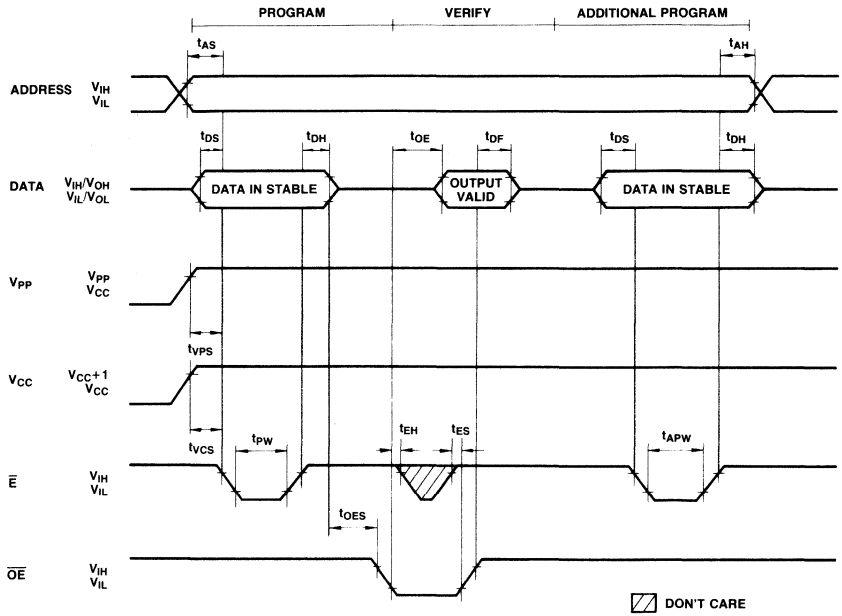
Programming/Erasing Information
(Continued)

Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the MBM27256 to an ultraviolet light source. A dosage of 15 W-seconds/cm^2 is required to completely erase an MBM27256. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000μW/cm^2 for 15 to 20 minutes. The MBM27256 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM27256 and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV source at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MBM27256, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

Programming Waveform



DC Characteristics
(T_A = 25±5°C,
V_{CC} *1 = 6V±0.25V,
V_{PP} *2 = 12.5V±0.3V)

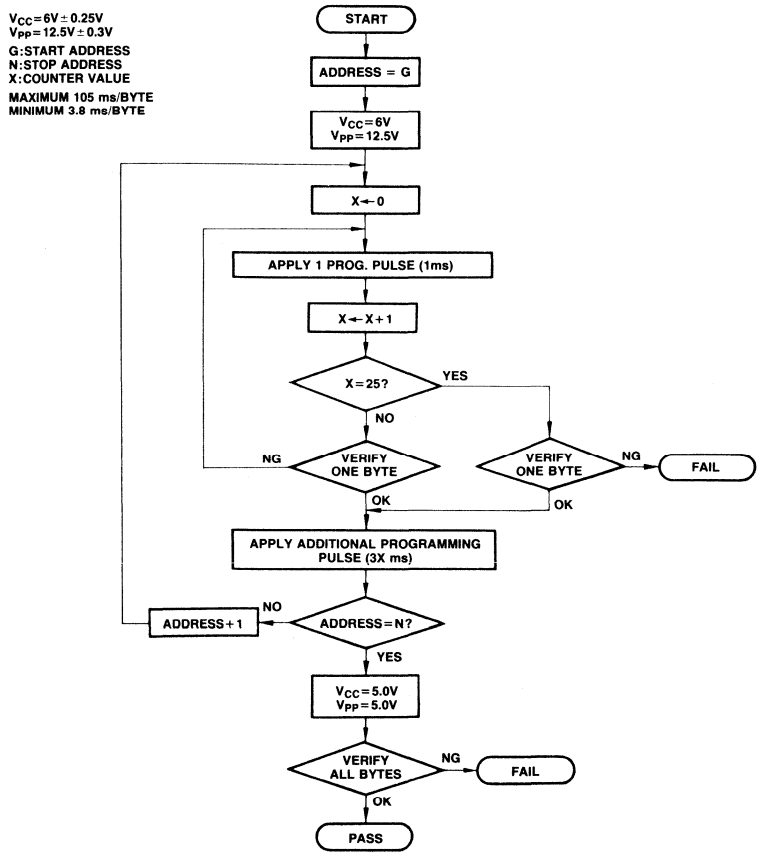
Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 6.25V/0.45V)	I_{IL}			10	μA
V_{PP} Supply Current ($\overline{E}$ = V_{IL}, $\overline{OE}$ = V_{IH})	I_{PP2}			50	mA
V_{PP} Supply Current ($\overline{OE}$ = V_{IL})	I_{PP3}			5	mA
V_{CC} Supply Current	I_{CC}			100	mA
Input Low Level	V_{IL}	−0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC}+1	V
Output Low Voltage During Verify (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OL} = −400μA)	V_{OH}	2.4			V

Notes: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
*2 V_{PP} must not be greater than 14 volts including overshoot. Permanent device damage may occur if the device is taken out of or put into a socket with V_{PP} = 12.5 volts. Also, during E = V_{IL}, V_{PP} must not be switched from 5 to 12.5 volts or vice-versa.

AC Characteristics
(T_A = 25±5°C,
V_{CC} = 6V±0.25V,
V_{PP} = 12.5V±0.3V)

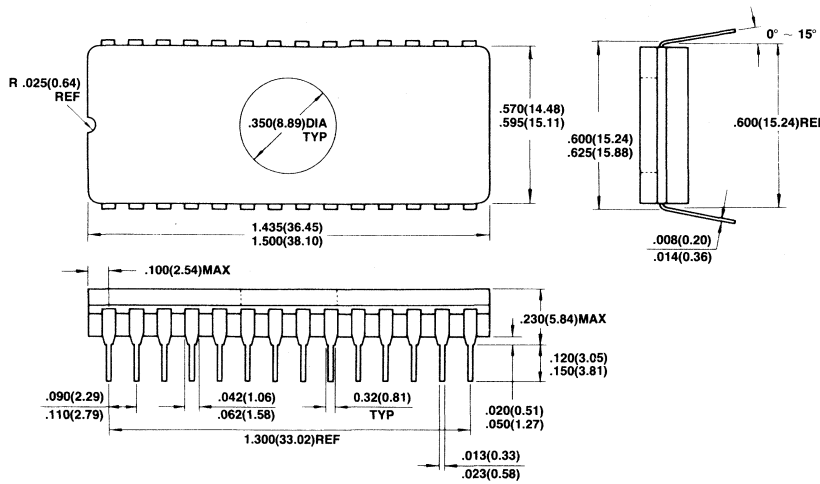
Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2			μs
Output Enable Setup Time	t_{OES}	2			μs
Chip Enable Setup Time	t_{ES}	2			μs
Data Setup Time	t_{DS}	2			μs
V_{PP} Setup Time	t_{VPS}	2			μs
V_{CC} Setup Time	t_{VS}	2			μs
Address Hold Time	t_{AH}	2			μs
Data Hold Time	t_{DH}	2			μs
Chip Enable Hold Time	t_{EH}	2			μs
Output Enable to Output Valid	t_{OE}			120	ns
Output Disable to Output Float Delay	t_{DF}			105	ns
Programming Pulse Width	t_{PW}	0.95	1	1.05	ms
Programming Pulse Number		1		25	times
Additional Programming Pulse Width	t_{APW}	2.85		63	ms

Programming Flow Chart



Package Dimensions
Dimensions in inches (millimeters)

28-Lead Ceramic (CERDIP with Transparent Lid) Dual In-Line Package (Case No.: DIP-28C-C01)



MBM27256-20-X, MBM27256-25-X, MBM27256-30-X, MBM27256-30-W

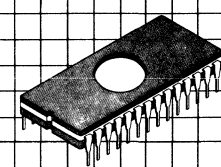
MOS 262,144-Bit UV Erasable and Electrically Programmable Read Only Memory

Description

The Fujitsu MBM27256-X and MBM27256-W are high speed 262,144-bit static NMOS erasable and electrically reprogrammable read only memories. It is especially well suited for applications where rapid turnaround and/or bit pattern experimentation are important.

A 28-pin Dual-In-Line package with a transparent lid is used to package the MBM27256-X and MBM27256-W. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM27256-X and MBM27256-W are fabricated using NMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 32,768 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



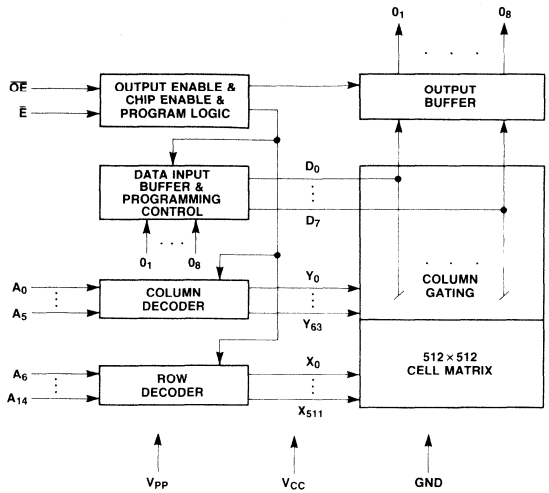
Ceramic Package DIP-28C-C01

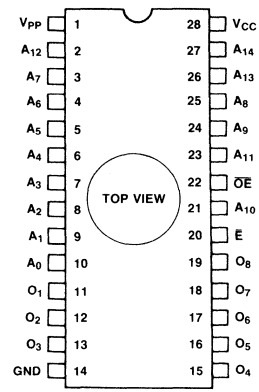
Features

- **32,768 words × 8-bit organization, fully decoded**
- **Single location programming**
- **Programmable utilizing the faster programming algorithm**
- **Program voltage: 12.5V**
- **Low power requirement**
  MBM27256-X active: 630 mW
  MBM27256-W active: 650 mW
  Standby: 237 mW
- **No clocks required (fully static operation)**
- **Fast access time:**
  200 ns max. (MBM27256-20-X)
  250 ns max. (MBM27256-25-X)
  300 ns max. (MBM27256-30-X)
  300 ns max. (MBM27256-30-W)
- **TTL compatible inputs/outputs**
- **Three-state output with OR-tie capability**
- **Output Enable ($\overline{OE}$) pin for simplified memory expansion**
- **Single +5V supply, ±5% tolerance**
- **Standard 28-pin DIP package**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MBM27256 Block Diagram and Pin Assignment





Absolute Maximum Ratings
(see Note)

Rating	Symbol	Value	Unit
Temperature under Bias	T_{BIAS}	−65 to +135* −50 to +95	°C
Storage Temperature	T_{STG}	−65 to +150* −65 to +125	°C
All Inputs/Outputs Voltage with Respect to GND	V_{IN}, V_{OUT}	−0.6 to +7	V
Voltage on A_9 with Respect to GND	V_{A9}	−0.6 to +13.5	V
V_{PP} Voltage with Respect to GND	V_{PP}	−0.6 to +14	V
Supply Voltage with Respect to GND	V_{CC}	−0.6 to +7	V

Note: *MBM27256-W
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Functions and Pin Connections

	Function (Pin No.)						
Mode	**Address Input (2 ~ 10, 21, 23 ~ 27)**	**Data I/O (11 ~ 13, 15 ~ 19)**	**$\overline{E}$ (20)**	**$\overline{OE}$ (22)**	**V_{CC} (28)**	**V_{PP} (1)**	**GND (14)**
Read	A_{IN}	OUT	V_{IL}	V_{IL}	+5 V	+5 V	GND
Output Disable	A_{IN}	High-Z	V_{IL}	V_{IH}	+5 V	+5 V	GND
Standby	Don't Care	High-Z	V_{IH}	Don't Care	+5 V	+5 V	GND
Program	A_{IN}	IN	V_{IL}	V_{IH}	+6 V	+12.5 V	GND
Program Verify	A_{IN}	OUT	Don't Care	V_{IL}	+6 V	+12.5 V	GND
Program Inhibit	Don't Care	High-Z	V_{IH}	V_{IH}	+6 V	+12.5 V	GND

Capacitance

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}		4	6	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}		8	12	pF

Recommended Operating Conditions

(Reference to GND)

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} Supply Voltage*1	V_{CC}	4.75	5.0	5.25	V
V_{PP} Supply Voltage	V_{PP}	V_{CC} −0.6		V_{CC} +0.6	V
Input High Voltage	V_{IH}	2.0		V_{CC} +1	V
Input Low Voltage	V_{IL}	−0.1		0.8	V
Operating Temperature	T_A	−40 −55*2		+85 +125*2	°C

Notes: *1 V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.
*2 MBM27256-30-W

DC Characteristics

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.25V)	I_{LI}			10	μA
Output Leakage Current (V_{OUT} = 5.25V)	I_{LO}			10	μA
V_{CC} Standby Current ($\overline{E}$ = V_{IH})	I_{CC1}			45	mA
V_{CC} Active Current ($\overline{E}$ = V_{IL})	I_{CC2}			120	mA
V_{PP} Supply Current (V_{PP} = V_{CC} ± 0.6V)	I_{PP1}			5	mA
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage (I_{OH} = −400μA)	V_{OH}	2.4			V

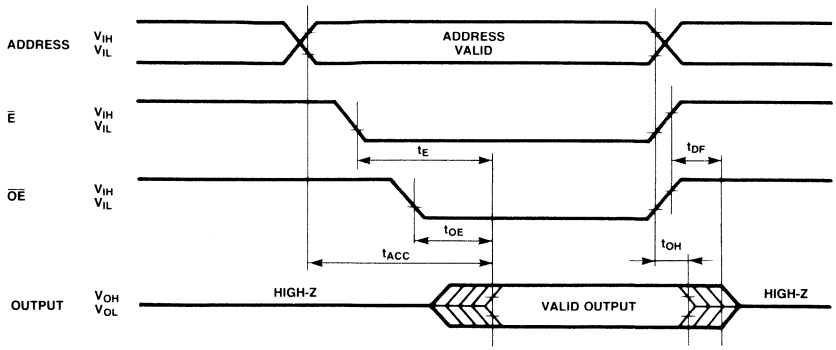
AC Characteristics

(Recommended operating conditions unless otherwise noted)

		MBM27256-20-X			MBM27256-25-X			MBM27256-30-X MBM27256-30-W			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
Address Access Time*1 ($\overline{E}$ = $\overline{OE}$ = V_{IL})	t_{ACC}			200			250			300	ns
$\overline{E}$ to Output Delay ($\overline{OE}$ = V_{IL})	t_E			200			250			300	ns
$\overline{OE}$ to Output Delay*1 ($\overline{E}$ = V_{IL})	t_{OE}			75			100			120	ns
Address to Output Hold	t_{OH}	0			0			0			ns
Output Enable High to Output Float*2	t_{DF}	0		60	0		60	0		105	ns

Notes: *1 $\overline{OE}$ may be delayed up to t_{ACC} − t_{OE} after the falling edge of $\overline{E}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{E}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

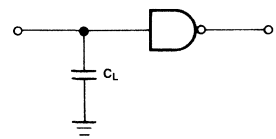
Operation Timing Diagram



AC Test Conditions

(including programming)

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Times:	≤20ns
Timing Measurement Reference Levels:	0.8V and 2.0V for inputs 0.8V and 2.0V for outputs
Output Load:	1 TTL gate and C_L = 100pF



Programming/ Erasing Information

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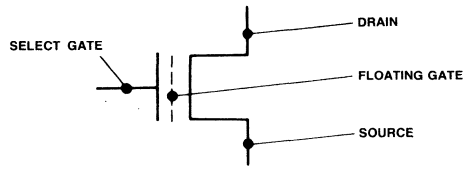
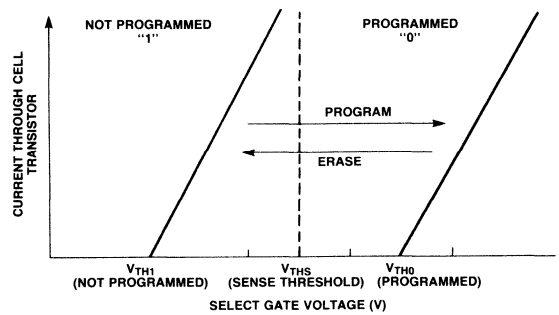
Memory Cell



Memory Cell Threshold Shift



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Procedure of QuickPro™ (Refer to the attached flowchart.)

1) Set the start address (=G) at the address pins.
2) Set V_{CC} = 6V, V_{PP} = 12.5V and $\overline{E}$ = V_{IH}.
3) Clear the programming pulse counter (X← 0).
4) Input data to respective pins.
5) Apply ONE programming pulse (t_{PW} = 1 ms Typ.) to $\overline{E}$.
6) Increment the counter (X←X + 1).
7) Compare the number (= X) of applied programming pulse with 25 and then verify the programmed data: If programmed data is verified, go to the next step regardless of X value. If X = 25 and programmed data is not verified, the device fails. If X = 25 and programmed data is not verified, go back to the step 5).
8) Apply one additional wide programming pulse to $\overline{E}$ (3X ms).
9) Compare the address with an end address (=N). If the programmed address is the end address, proceed to the next step. If not, increment the address (G←G+1) and then go to the step 3) for the next address.
10) Set V_{CC} = V_{PP} = 5V.
11) Verify all programmed data: If the verification succeeds, the programming completes. If any programmed data is not the same as input data, the device fails.

A continuous TTL low level should not apply to $\overline{E}$ input pin during the program mode (V_{PP} = 12.5V, V_{CC} = 6V and $\overline{OE}$ = V_{IH}) because it is required that one programming pulse width does not exceed 78.75 ms at each address.

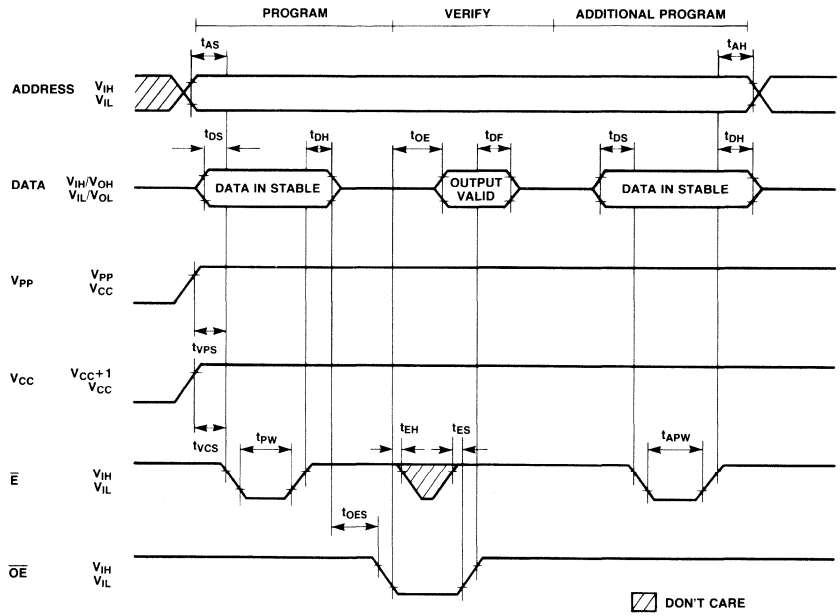
Programming/Erasing Information
(Continued)

Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the MBM27256 to an ultraviolet light source. A dosage of 15 W-seconds/cm^2 is required to completely erase an MBM27256. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000μW/cm^2 for 15 to 20 minutes. The MBM27256 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM27256 and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV source at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MBM27256, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

Programming Waveform



DC Characteristics

(T_A = 25±5°C, V_{CC} *1 = 6V±0.25V, V_{PP} *2 = 12.5V±0.3V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 6.25V/0.45V)	I_{IL}			10	μA
V_{PP} Supply Current ($\overline{E}$ = V_{IL}, $\overline{OE}$ = V_{IH})	I_{PP2}			50	mA
V_{PP} Supply Current ($\overline{OE}$ = V_{IL})	I_{PP3}			5	mA
V_{CC} Supply Current	I_{CC}			100	mA
Input Low Level	V_{IL}	−0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC}+1	V
Output Low Voltage During Verify (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OL} = −400μA)	V_{OH}	2.4			V

Notes: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
*2 V_{PP} must not be greater than 14 volts including overshoot. Permanent device damage may occur if the device is taken out of or put into a socket with V_{PP} = 12.5 volts. Also, during E = V_{IL}, V_{PP} must not be switched from 5 to 12.5 volts or vice-versa.

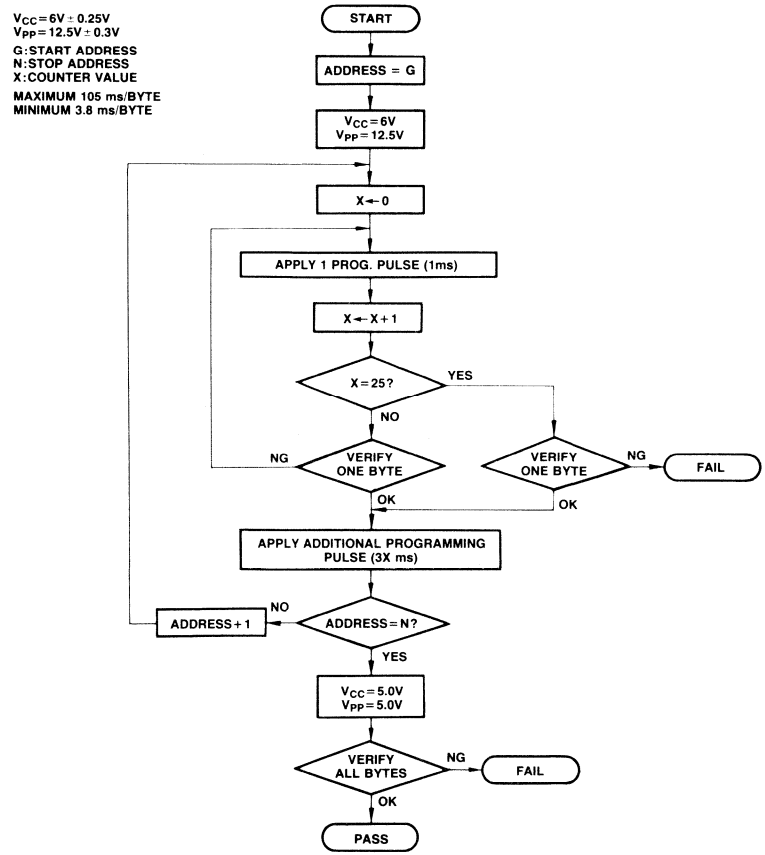
AC Characteristics

(T_A = 25±5°C, V_{CC} = 6V±0.25V, V_{PP} = 12.5V±0.3V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2			μs
Output Enable Setup Time	t_{OES}	2			μs
Chip Enable Setup Time	t_{ES}	2			μs
Data Setup Time	t_{DS}	2			μs
V_{PP} Setup Time	t_{VPS}	2			μs
V_{CC} Setup Time	t_{VS}	2			μs
Address Hold Time	t_{AH}	2			μs
Data Hold Time	t_{DH}	2			μs
Chip Enable Hold Time	t_{EH}	2			μs
Output Enable to Output Valid	t_{OE}			120	ns
Output Disable to Output Float Delay	t_{DF}			105	ns
Programming Pulse Width	t_{PW}	0.95	1	1.05	ms
Programming Pulse Number		1		20	times
Additional Programming Pulse Width	t_{APW}	2.85		63	ms

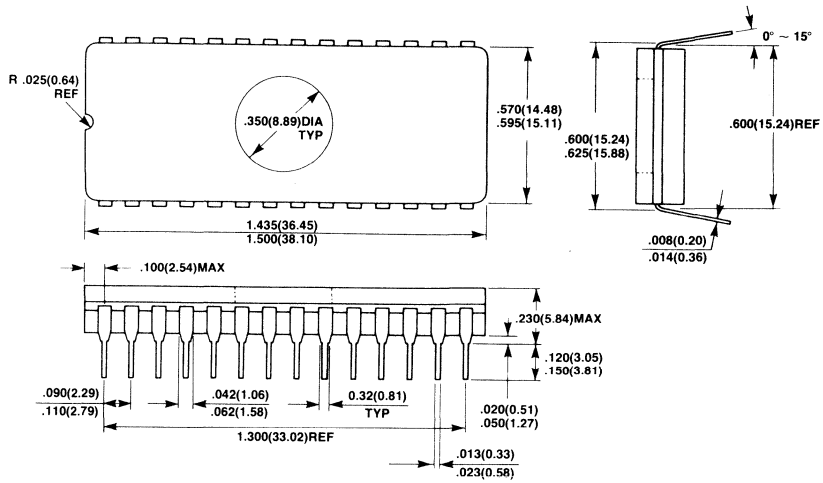
Programming/Erasing Information
(Continued)

Programming Flow Chart



Package Dimensions
Dimensions in inches (millimeters)

28-Lead Ceramic (CERDIP with Transparent Lid) Dual In-Line Package (Case No.: DIP-28C-C01)



CMOS EPROMs

MBM27C64 6-2
MBM27C64X/27C64W 6-13
MBM27C128 6-24
MBM27C256 6-35
MBM27C256A 6-47
MBM27C256AW 6-55
MBM27C512 6-64
MBM27C1001 6-72
MBM27C1024 6-74
MBM27C1028 6-76

MBM27C64-20, MBM27C64-25, MBM27C64-30

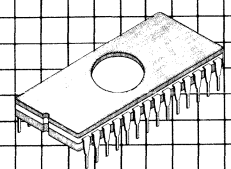
CMOS 65,536-BIT UV Erasable and Electrically Programmable Read Only Memory

Description

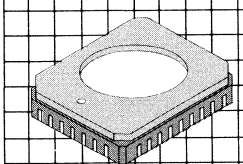
The Fujitsu MBM27C64 is a high speed 65,536-bit static Complementary MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially suited for applications where the extremely low power consumption of CMOS is essential. The device dissipates only 40 mW/MHz when active, typically 5μW when in standby, yet it provides the same high speed performance as the NMOS MBM2764-type devices.

This package is available in either a 28-pin dual-in-line package or a 32-pin LCC package both of which have a transparent lid. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can be programmed into the memory.

The MBM27C64 is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 8,192 words by 8-bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



Ceramic Package DIP-28C-C01

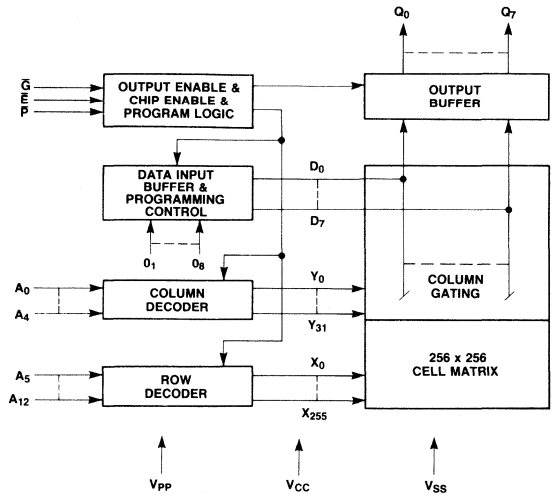


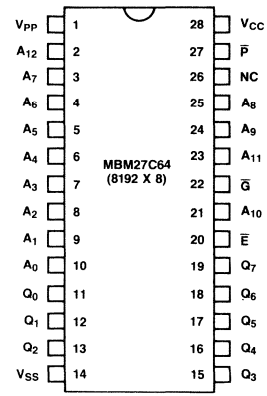
Leadless Chip Carrier LCC-32C-A01

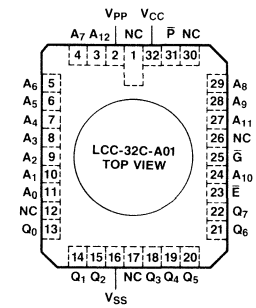
Features

- **CMOS Power Consumption:**
  500μW max. (Standby)
  5μW typ. (Standby)
  40mW/MHz (Active)
- **Fast access time:**
  MBM27C64-20 200 ns max.
  MBM27C64-25 250 ns max.
  MBM27C64-30 300 ns max.
- **Utilizes the same simple programming requirements as MBM2764**
- **Single +5V operation**
- **10% V_{CC} tolerance standard**
- **TTL compatible inputs/outputs**
- **Three-state output provides OR-tie capability**
- **Output Enable ($\overline{OE}$) pin provides precise data bus control**
- **Pin and function compatible with 2764-type devices**

MBM27C64 Block Diagram and Pin Assignments







Absolute Maximum Ratings
(See Note)

Parameter	Symbol	Value	Unit
Temperature under bias	T_A	−25 to +85	°C
Storage temperature	T_{STG}	−65 to +125	°C
Inputs/outputs with respect to V_{SS}	V_{IN}, V_{OUT}	−0.6 to +7	V
V_{CC} with respect to V_{SS}	V_{CC}	−0.6 to +7	V
V_{PP} with respect to V_{SS}	V_{PP}	−0.6 to +22	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Functions and Pin Connections
(V_{CC}(28) = +5, V_{SS}(14) = GND)

Mode	Address Input (2-N10, 21, 23-25)	Data I/O (11-13, 15-19)	$\overline{E}$ (20)	$\overline{G}$ (22)	$\overline{P}$ (27)	V_{CC} (28)	V_{PP} (1)
Read	A_{IN}	OUT	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}
Output disable	Don't care	High Z	V_{IL}	V_{IH} / Don't care	Don't care / V_{IL}	V_{CC}	V_{CC}
Stand by	Don't care	High Z	V_{IH}	Don't care	Don't care	V_{CC}	V_{CC}
Program	A_{IN}	IN	V_{IL}	V_{IH}	V_{IL}	V_{CC}	V_{PP}
Program verify	A_{IN}	OUT	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{PP}
Program inhibit	Don't care	High Z	V_{IH}	Don't care	Don't care	V_{CC}	V_{PP}

Recommended Operating Conditions
(Referenced to V_{SS} = GND)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply voltage*1	V_{CC}	4.50	5.0	5.50	V	0°C to +70°C*2
Supply voltage	V_{PP}	V_{CC} − 0.6		V_{CC} + 0.6	V	
Supply voltage	V_{SS}		GND		V	
Input high voltage	V_{IH}	2.0		V_{CC} + 0.3	V	
Input low voltage	V_{IL}	−0.1		0.8	V	

Notes: *1 V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.
*2 −40°C to +85°C available as MBM27C64-25X, MBM27C64-30X. −55°C to +125°C available as MBM27C64-30W.

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input capacitance (V_{IN} = 0V)	C_{IN}	4	6	pF
Output capacitance (V_{OUT} = 0V)	C_{OUT}	8	12	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ*1	Max	Unit
Input load current (V_{IN} = 5.50V)	I_{LI}			10	μA
Output leakage current (V_{OUT} = 5.50V)	I_{LO}			10	μA
V_{PP} supply current	I_{PP}		1	100	μA
V_{CC} standby current ($\overline{E}$ = V_{IH})	I_{SB1}			1	mA
V_{CC} standby current ($\overline{E}$ = V_{CC} − 0.3V to V_{CC} + 0.3V, I_{OUT} = 0 mA)	I_{SB2}		1	100	μA
V_{CC} active current ($\overline{E}$ = V_{IL})	I_{CC1}			30	mA
V_{CC} operation current (f = 4 MHz, I_{OUT} = 0 mA)	I_{CC2}			30	mA
Output low voltage (I_{OL} = 2.1 mA)	V_{OL}			0.45	V
Output high voltage (I_{OH} = −400 μA)	V_{OH}	2.4			V

Note: *1 V_{CC} = 5.0V and T_A = 25°C.

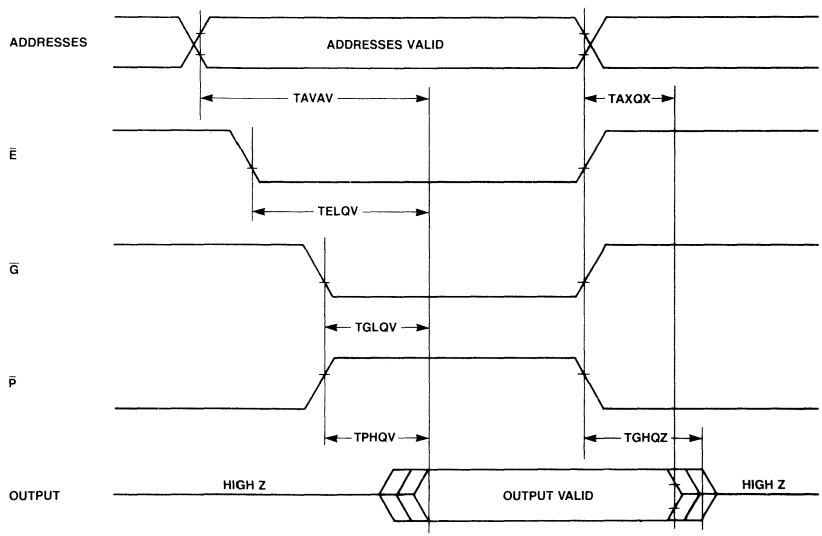
AC Characteristics

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MBM27C64-20 Min	MBM27C64-20 Max	MBM27C64-25 Min	MBM27C64-25 Max	MBM27C64-30 Min	MBM27C64-30 Max	Unit
Address to Output Delay ($\overline{E} = \overline{G} = V_{IL}$, $\overline{P} = V_{IH}$)	TAVAV		200		250		300	ns
$\overline{E}$ to Output Delay ($\overline{G} = V_{IL}$, $\overline{P} = V_{IH}$)	TELQV		200		250		300	ns
$\overline{G}$ to Output Delay ($\overline{E} = V_{IL}$, $\overline{P} = V_{IH}$)	TGLQV		70		100		120	ns
$\overline{P}$ to Output Delay ($\overline{E} = \overline{G} = V_{IL}$)	TPHQV		70		100		120	ns
Output Enable High to Output Float*2	TGHQZ	0	60	0	90	0	105	ns
Address to Output Hold	TAXQX	0		0		0		ns

Note: *2 TGHQZ is specified from $\overline{E}$, $\overline{G}$, or $\overline{P}$, whichever occurs first.

Operation Timing Diagram

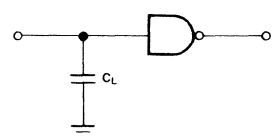


NOTE: $\overline{G}$ MAY BE DELAYED UP TO TAVAV—TGLQV AFTER THE FALLING EDGE OF $\overline{E}$ WITHOUT IMPACT ON TAVAV.

AC Test Conditions

Input Pulse Levels: 0.8 V to 2.2 V
Input Rise and Fall Time: ≤20 nsec
Timing Measurement Reference Levels: 1.0 and 2.0V for inputs
0.8 and 2.0V for outputs
1 TTL gate and C_L = 100 pF

OUTPUT LOAD:



Programming/Erasing Information

Memory Cell Description

The MBM27C64 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Memory Cell diagram). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Memory Cell Threshold Shift diagram). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in the Memory Cell Threshold Shift diagram.

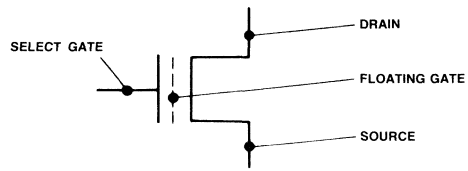
Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27C64 has all 65,536 bits in the "1" or high state. "0's" are loaded into the MBM27C64 through the procedure of programming.

Conventional Programming

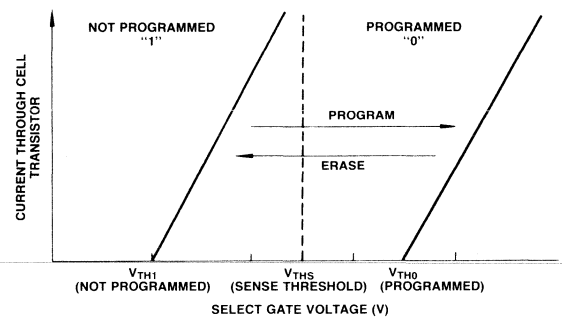
The programming mode is entered when +21V is applied to the V_{PP} pin and $\overline{E}$ and $\overline{P}$ are both at V_{IL}. During programming, $\overline{E}$ is kept at V_{IL}. A 0.1 μF capacitor between V_{PP} and V_{SS} is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. A pattern of eight bits are placed on the respective output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, 50 msec, TTL low level pulse is applied to the P input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automaticaly via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{P}$ input is prohibited when programming.

Memory Cell



Memory Cell Threshold Shift



Programming/Erasing Information
(Continued)

Quick Pro™ Programming

In addition to the standard 50 millisecond pulse width procedure, the MBM27C64 can be programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The algorithm (shown in the Quick Pro™ Program Flow Chart diagram) utilizes a sequence of 1 millisecond pulses to program each location. This algorithm will typically yield a savings of 86% in programming time per device when utilized in commercially available programmers. However, in custom programmer designs that require less overhead the savings can be even greater.

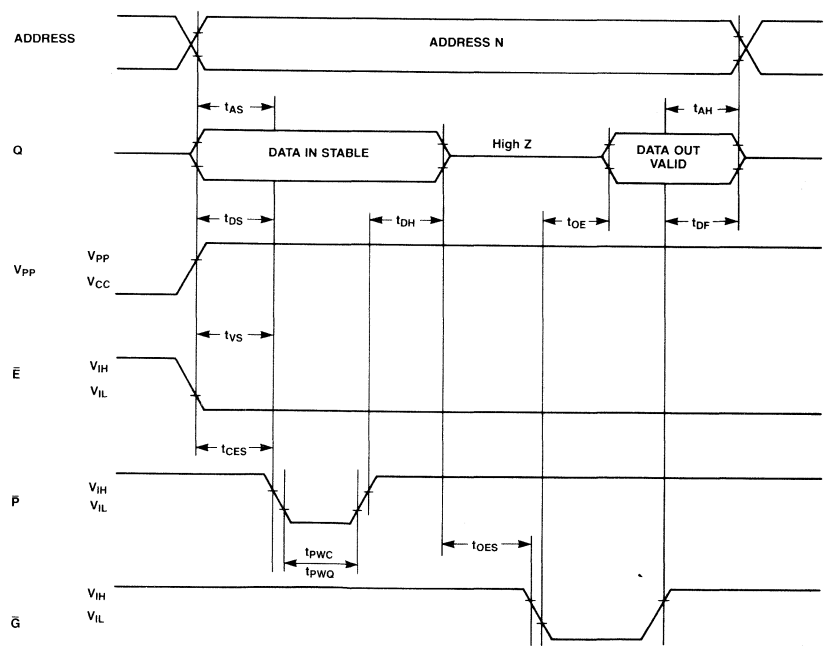
The programming mode is entered when +6V is applied to the V_{CC} pin followed by applying +21V to V_{PP} pin. A TTL low input must be applied to the $\overline{E}$ input and a TTL high input must be applied to the $\overline{G}$ input. After the programming voltages and TTL levels have stabilized, a sequence of 1 millisecond pulses must be applied to the $\overline{P}$ pin for programming. After each pulse, a pulse counter must be incremented and the location should be checked for accuracy. Upon verification, an additional sequence of 1 millisecond pulses equal to the present value of the pulse counter must be applied to the location to ensure proper levels of stored charge. An alternate approach to the additional pulses would be to apply a single TTL low pulse with a width equivalent to the value of the pulse counter multiplied by 1 millisecond. When the pulse counter reaches a maximum of 20, the verification procedure is skipped and a flag is set to indicate a program failure. Upon completion of programming of the entire device, a final array verification (all locations) is required. All Fujitsu devices will typically require only two 1 millisecond pulses (one initial and one additional) to reach proper stored charge levels.

Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the MBM27C64 to an ultraviolet light source. A dosage of 15W-seconds/cm^2 is required to completely erase an MBM27C64. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å) with intensity of 12,000 μW/cm^2) for 15 to 20 minutes. The MBM27C64 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM27C64 and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the MBM27C64 and such exposure should be prevented to realize maximum data retention. If used in such an environment, the package windows should be covered by an opaque label or substance.

Programming Waveform



DC Characteristics
(T_A = 25 ± 5°C,
V_{CC} = 5V ± 5%,
V_{PP} = 21V ± 0.5V)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input leakage current	I_{LI}		10	mA	V_{IN} = 0.45V–5.25V
Output low voltage during verify	V_{OL}		0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4		V	I_{OH} = 400 mA
V_{CC} supply current	I_{CC1}		30	mA	
Input low voltage	V_{IL}	−0.1	0.8	V	
Input high voltage	V_{IH}	2.0	V_{CC} + 0.3	V	
V_{PP} supply current during programming pulse	I_{PP2}		30	mA	E = P = V_{IL}

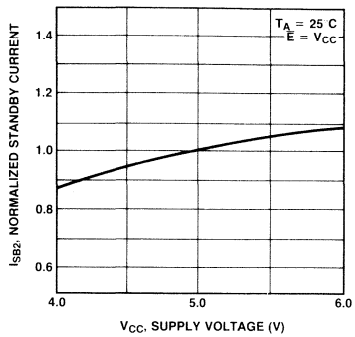
Notes: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
*2 V_{PP} must not be greater than 21.5 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 21 volts. Also, during $\overline{E}$ = $\overline{P}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 21 volts or vise-versa.

AC Characteristics
(T_A = 25 ± 5°C,
V_{CC} = 5V ± 5%,
V_{PP} = 21V ± 0.5V)

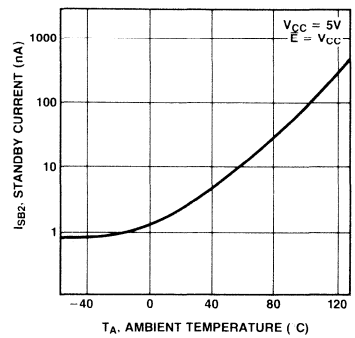
Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2			μs
$\overline{E}$ setup time	t_{CES}	2			μs
Data setup time	t_{DS}	2			μs
Address hold time	t_{AH}	0			μs
Data hold time	t_{DH}	2			μs
Chip enable to output float delay	t_{DF}	0		130	ns
V_{PP} setup time	t_{VS}	2			μs
$\overline{P}$ pulse width-conventional	t_{PWC}	25	50	55	ms
$\overline{P}$ pulse Width-Quick-Pro™	t_{PWQ}	0.95	1.00	1.05	ms
$\overline{G}$ setup time	t_{OES}	2			μs
Data valid from $\overline{G}$	t_{OE}			150	ns

Typical Characteristics Curves

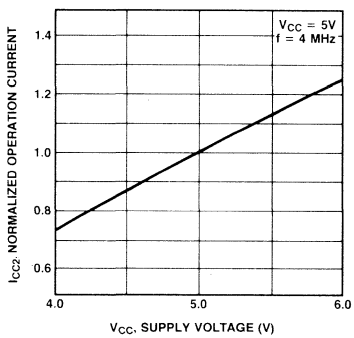
Standby Current vs. Supply Voltage



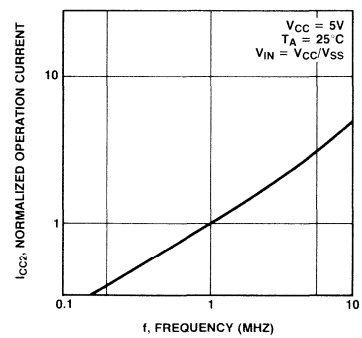
Standby Current vs. Ambient Temperature



Operation Current vs. Supply Voltage

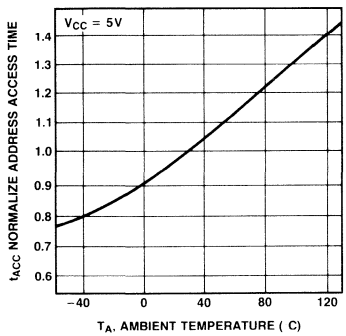


Operation Current vs. Frequency

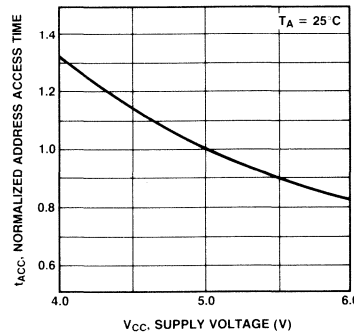


Typical Characteristics Curves
(Continued)

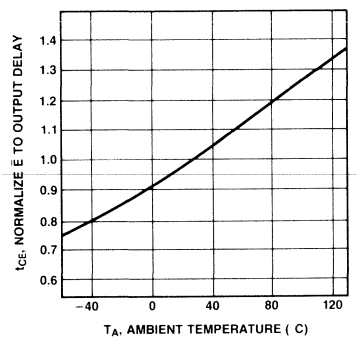
Address Access Time vs. Ambient Temperature



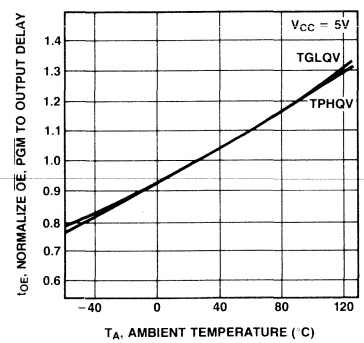
Address Access Time vs. Supply Voltage



$\overline{E}$ to Output Delay vs. Ambient Temperature

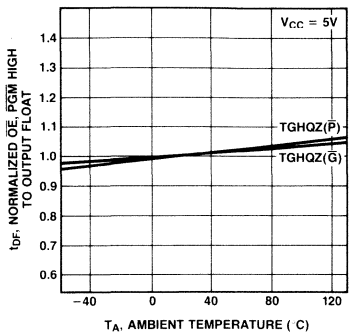


$\overline{G}$, $\overline{P}$ to Output Delay vs. Ambient Temperature

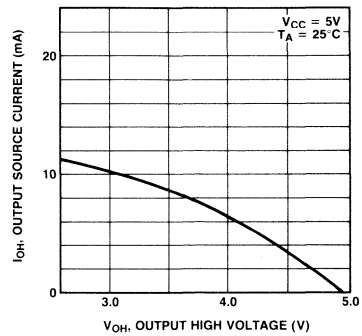


Typical Characteristics Curves
(Continued)

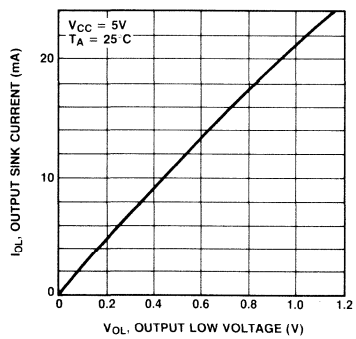
$\overline{G}$, $\overline{P}$ High to Output Float vs. Ambient Temperature



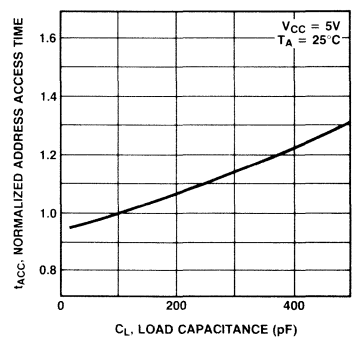
Output Source Current vs. Output High Voltage



Output Sink Current vs. Output Low Voltage

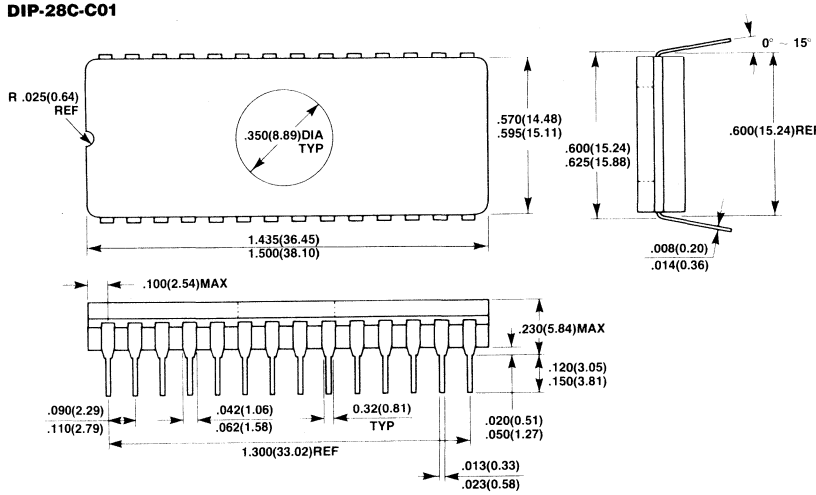


Address Access Time vs. Load Capacitance

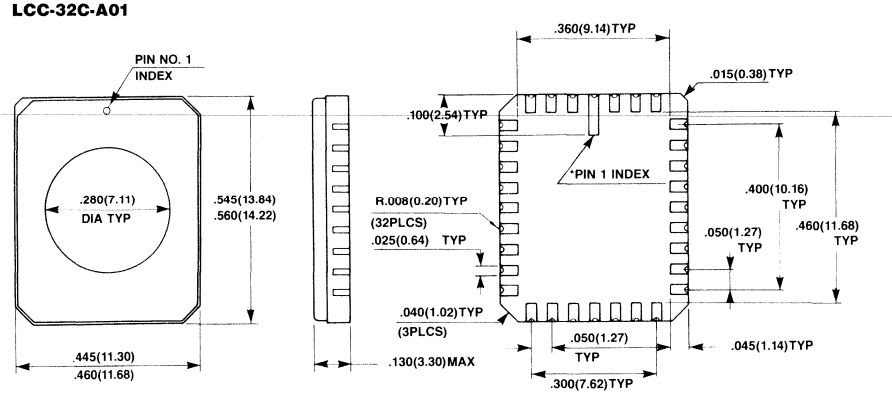


Package Dimensions
Dimensions in inches
(millimeters)

28-Lead Ceramic (Cerdip with Transparent Lid)
Dual In-Line Package
DIP-28C-C01



32-Pad Ceramic (Metal Seal) Leadless Chip Carrier
LCC-32C-A01



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE.

MBM27C64-25X, MBM27C64-30X, MBM27C64-30W

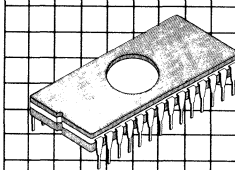
CMOS 65,536-BIT UV Erasable and Electrically Programmable Read Only Memory

Description

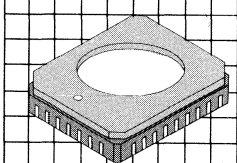
The Fujitsu MBM27C64 is a high speed 65,536-bit static Complementary MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially suited for applications where the extremely low power consumption of CMOS is essential. The device dissipates only 40 mW/MHz in the active mode and 5 μW in the standby mode. It provides the same high speed performance as the NMOS MBM2764-type devices.

This package is available in either a 28-pin dual-in-line package or a 32-pin LCC package both of which have a transparent lid. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can be programmed into the memory.

The MBM27C64 is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 8,192 words by 8-bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



Ceramic Package DIP-28C-C01

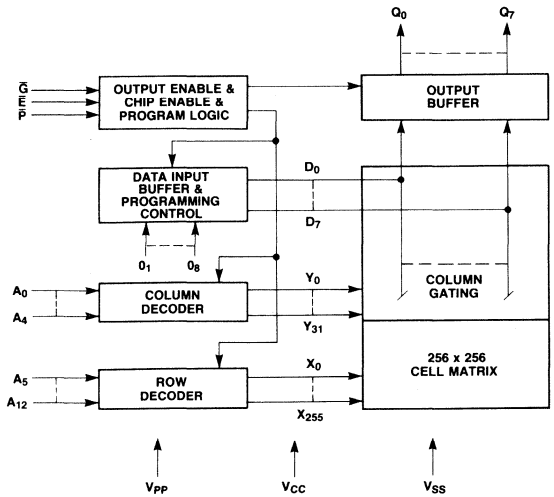


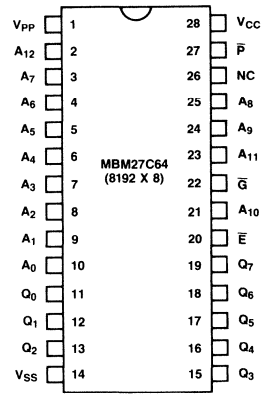
Leadless Chip Carrier LCC-32C-A01

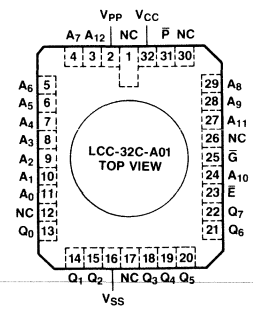
Features

- **Extended temp. range:**
  MBM27C64X −40°C to +85°C
  MBM27C64W −55°C to +125°C
- **CMOS power consumption:**
  550 μW max. (Standby)
  5μW typ. (Standby)
  42 mW/MHz (Active)
- **Fast access time:**
  MBM27C64-25X 250 ns max.
  MBM27C64-30X 300 ns max.
  MBM27C64-30W 300 ns max.
- **Utilizes the same simple programming requirements as MBM2764**
- **Single +5V operation**
- **10% V_{CC} tolerance standard**
- **TTL compatible inputs/outputs**
- **Three-state output provides OR-tie capability**
- **Output Enable ($\overline{OE}$) pin provides precise data bus control**
- **Pin and function compatible with 2764-type devices**

MBM27C64 Block Diagram and Pin Assignments







Absolute Maximum Ratings
(See Note)

Parameter	Symbol	MBM27C64X Value	MBM27C64W Value	Unit
Temperature under bias	T_A	−50 to +95	−65 to +135	°C
Storage temperature	T_{STG}	−65 to +125	−65 to +150	°C
Inputs/outputs with respect to V_{SS}	V_{IN}, V_{OUT}	−0.6 to +7	−0.6 to +7	V
V_{CC} with respect to V_{SS}	V_{CC}	−0.6 to +7	−0.6 to +7	V
V_{PP} with respect to V_{SS}	V_{PP}	−0.6 to +22	−0.6 to +22	V

Functions and Pin Connections
(V_{CC}(28) = +5, V_{SS}(14) = GND)

Mode	Function (Pin No.) Address Input (2-10, 21, 23-25)	Data I/O (11-13, 15-19)	$\overline{E}$ (20)	$\overline{G}$ (22)	$\overline{P}$ (27)	V_{CC} Supply (28)	V_{PP} (1)
Read	A_{IN}	OUT	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}
Output disable	Don't Care	High Z	V_{IL}	V_{IH} / Don't Care	Don't Care / V_{IL}	V_{CC}	V_{CC}
Stand by	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{CC}
Program	A_{IN}	IN	V_{IL}	V_{IH}	V_{IL}	V_{CC}	V_{PP}
Program verify	A_{IN}	OUT	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{PP}
Program inhibit	Don't Care	High Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{PP}

Recommended Operating Conditions
(Referenced to V_{SS} = GND)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Supply Voltage*1	V_{CC}	4.50	5.0	5.50	V	−40°C to +85°C MBM27C64X −55°C to +125°C MBM27C64W
Supply Voltage	V_{PP}	V_{CC} −0.6		V_{CC} +0.6	V	
Supply Voltage	V_{SS}		GND		V	
Input High Voltage	V_{IH}	2.0		V_{CC} +0.3	V	
Input Low Voltage	V_{IL}	−0.1		0.8	V	

Note: *1 V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input capacitance (V_{IN} = 0V)	C_{IN}	4	6	pF
Output capacitance (V_{OUT} = 0V)	C_{OUT}	8	12	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ*1	Max	Unit
Input load current (V_{IN} = 5.50V)	I_{LI}			10	μA
Output leakage current (V_{OUT} = 5.50V)	I_{LO}			10	μA
V_{PP} supply current	I_{PP}		1	100	μA
V_{CC} standby current ($\overline{E}$ = V_{IH})	I_{SB1}			1	mA
V_{CC} standby current ($\overline{E}$ = V_{CC} − 0.3V to V_{CC} + 0.3V, I_{OUT} = 0 mA)	I_{SB2}		1	100	μA
V_{CC} active current ($\overline{E}$ = V_{IL})	I_{CC1}			30	mA
V_{CC} operation current (f = 4 MHz, I_{OUT} = 0 mA)	I_{CC2}			30	mA
Output low voltage (I_{OL} = 2.1 mA)	V_{OL}			0.45	V
Output high voltage (I_{OH} = −400 μA)	V_{OH}	2.4			V

Note: *1 V_{CC} = 5.0V and T_A = 25°C.

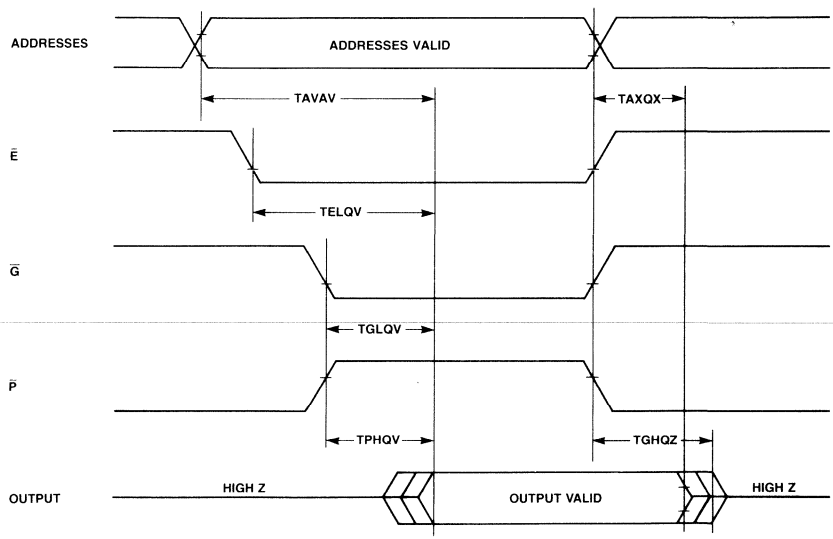
AC Characteristics

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MBM27C64-25X Min	MBM27C64-25X Max	MBM27C64-30X MBM27C64-30W Min	MBM27C64-30X MBM27C64-30W Max	Unit
Address to Output Delay ($\overline{E} = \overline{G} = V_{IL}$, $\overline{P} = V_{IH}$)	TAVAV		250		300	ns
$\overline{E}$ to Output Delay ($\overline{G} = V_{IL}$, $\overline{P} = V_{IH}$)	TELQV		250		300	ns
$\overline{G}$ to Output Delay ($\overline{E} = V_{IL}$, $\overline{P} = V_{IH}$)	TGLQV		100		120	ns
$\overline{P}$ to Output Delay ($\overline{E} = \overline{G} = V_{IL}$)	TPHQV		100		120	ns
Output Enable High to Output Float*2	TGHQZ	0	90	0	105	ns
Address to Output Hold	TAXQX	0		0		ns

Note: *2 TGHQZ is specified from $\overline{E}$, $\overline{G}$, or $\overline{P}$, whichever occurs first.

Operation Timing Diagram

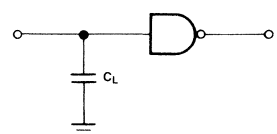


NOTE: $\overline{G}$ MAY BE DELAYED UP TO TAVAV—TGLQV AFTER THE FALLING EDGE OF $\overline{E}$ WITHOUT IMPACT ON TAVAV.

AC Test Conditions

Input Pulse Levels: 0.8 V to 2.2 V
Input Rise and Fall Time: ≤20 nsec
Timing Measurement Reference Levels: 1.0 and 2.0V for inputs
0.8 and 2.0V for outputs
1 TTL gate and C_L = 100 pF

OUTPUT LOAD:



Programming/Erasing Information

Memory Cell Description

The MBM27C64 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Memory Cell Diagram). The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Memory Cell Threshold Shift diagram). In the initial state, cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Memory Cell Threshold Shift diagram.

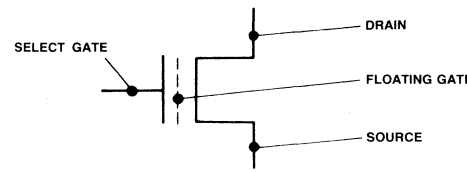
Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27C64 has all 65,536 bits in the "1" or high state. "0's" are loaded into the MBM27C64 through the procedure of programming.

Conventional Programming

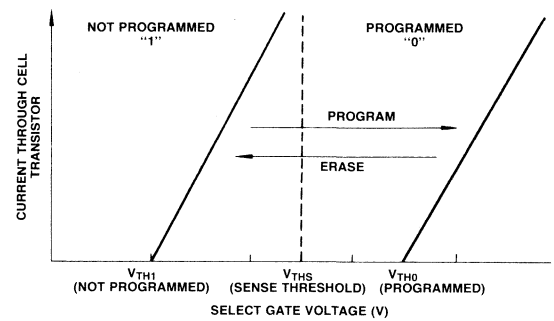
The programming mode is entered when +21V is applied to the V_{PP} pin and $\overline{E}$ and $\overline{P}$ are both at V_{IL}. During programming, $\overline{E}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and V_{SS} is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. A pattern of eight bits are placed on the respective output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, 50 msec, TTL low level pulse is applied to the $\overline{P}$ input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{P}$ input is prohibited when programming.

Memory Cell



Memory Cell Threshold Shift



Programming/Erasing Information
(Continued)

Quick Pro™ Programming

In addition to the standard 50 millisecond pulse width programming procedure, the MBM27C64 can be programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The algorithm (shown in figure 3) utilizes a sequence of 1 millisecond pulses to program each location. This algorithm will typically yield a savings of 86% in programming time per device when utilized in commercially available programmers. However, in custom programmer designs that require less overhead the savings can be even greater.

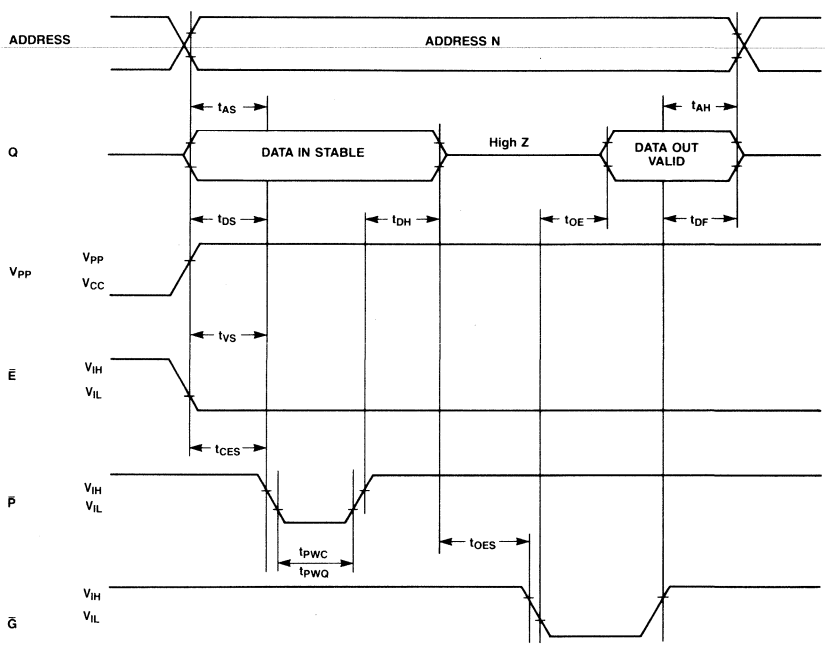
The programming mode is entered when +6V is applied to the V_{CC} pin followed by applying +21V to V_{PP} pin. A TTL low input must be applied to the $\overline{E}$ input and a TTL high input must be applied to the $\overline{G}$ input. After the programming voltages and TTL levels have stabilized, a sequence of 1 millisecond pulses must be applied to the $\overline{P}$ pin for programming. After each pulse, a pulse counter must be incremented and the location should be checked for accuracy. Upon verification, an additional sequence of 1 millisecond pulses equal to the present value of the pulse counter must be applied to the location to ensure proper levels of stored charge. An alternate approach to the additional pulses would be to apply a single TTL low pulse with a width equivalent to the value of the pulse counter multiplied by 1 millisecond. When the pulse counter reaches a maximum of 20, the verification procedure is skipped and a flag is set to indicate a program failure. Upon completion of programming of the entire device, a final array verification (all locations) is required. All Fujitsu devices will typically require only two 1 millisecond pulses (one initial and one additional) to reach proper stored charge levels.

Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the MBM27C64 to an ultraviolet light source. A dosage of 15W-seconds/cm^2 is required to completely erase an MBM27C64. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å) with intensity of 12,000 μW/cm^2) for 15 to 20 minutes. The MBM27C64 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM27C64 and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the MBM27C64 and such exposure should be prevented to realize maximum data retention. If used in such an environment, the package windows should be covered by an opaque label or substance.

Programming Waveform



DC Characteristics
(T_A = 25 ± 5°C,
V_{CC} = 5V ± 5%
V_{PP} = 21V ±0.5V)

Parameter	Symbol	Min	Max	Unit	Test Conditions
Input leakage current	I_{LI}		10	μA	V_{IN} = 0.45V–5.25V
Output low voltage during verify	V_{OL}		0.45	V	I_{OL} = 2.1 mA
Output high voltage during verify	V_{OH}	2.4		V	I_{OH} = −400 mA
V_{CC} supply current	I_{CC1}		30	mA	
Input low voltage	V_{IL}	−0.1	0.8	V	
Input high voltage	V_{IH}	2.0	V_{CC} + 0.3	V	
V_{PP} supply current during programming pulse	I_{PP2}		30	mA	E = P = V_{IL}

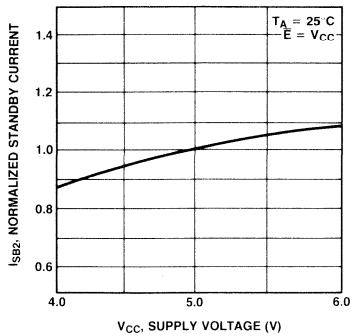
Notes: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
*2 V_{PP} must not be greater than 21.5 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 21 volts. Also, during $\overline{E}$ = $\overline{P}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 21 volts or vise-versa.

AC Characteristics
(T_A = 25 ± 5°C,
V_{CC} = 5V ± 5%
V_{PP} = 21V ±0.5V)

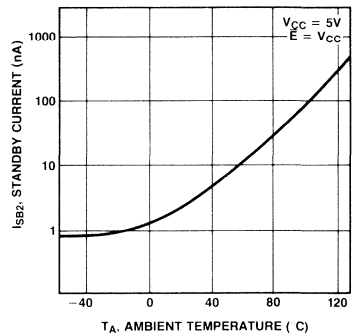
Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2			μs
$\overline{E}$ setup time	t_{CES}	2			μs
Data setup time	t_{DS}	2			μs
Address hold time	t_{AH}	0			μs
Data hold time	t_{DH}	2			μs
Chip enable to output float delay	t_{DF}	0		130	ns
V_{PP} setup time	t_{VS}	2			μs
$\overline{P}$ pulse width-conventional	t_{PWC}	25	50	55	ms
$\overline{P}$ pulse Width-Quick-Pro™	t_{PWQ}	0.95	1.00	1.05	ms
$\overline{G}$ setup time	t_{OES}	2			μs
Data valid from $\overline{G}$	t_{OE}			150	ns

Typical Characteristics Curves

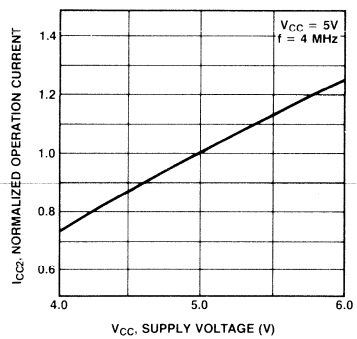
Standby Current vs. Supply Voltage



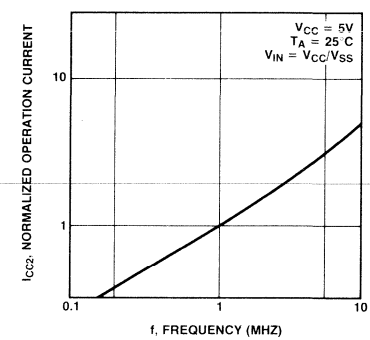
Standby Current vs. Ambient Temperature



Operation Current vs. Supply Voltage

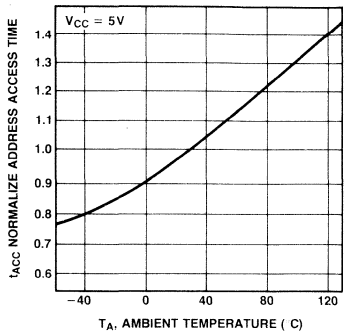


Operation Current vs. Frequency

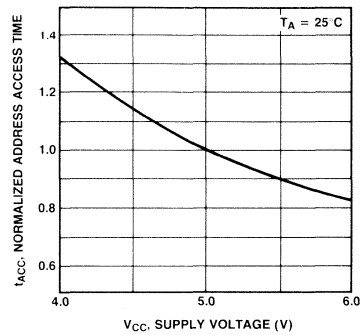


Typical Characteristics Curves

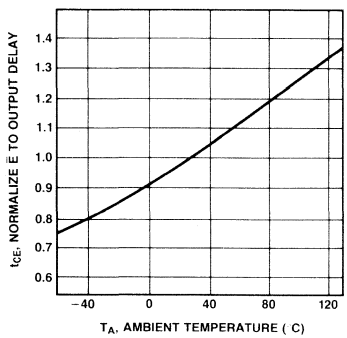
Address Access Time vs. Ambient Temperature



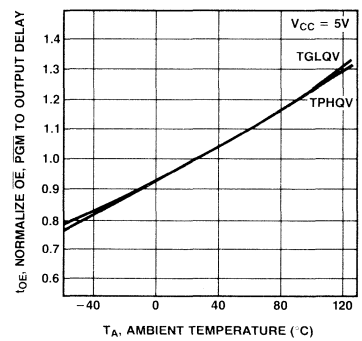
Address Access Time vs. Supply Voltage



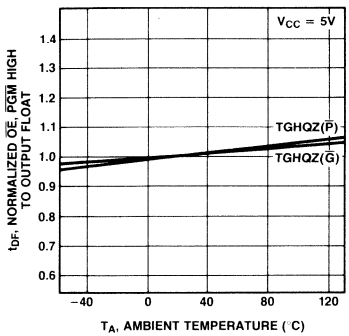
$\overline{E}$ to Output Delay vs. Ambient Temperature



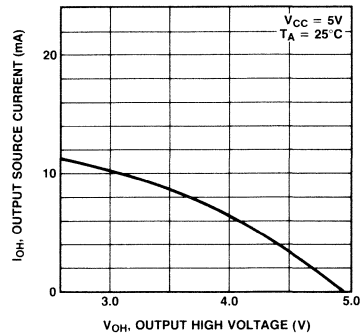
$\overline{G}$, $\overline{P}$ to Output Delay vs. Ambient Temperature



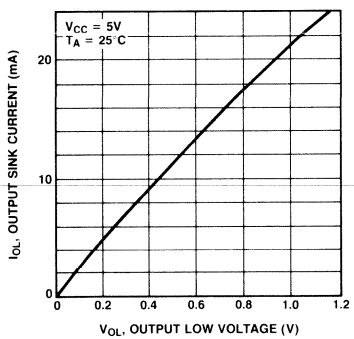
$\overline{G}$, $\overline{P}$ High to Output Float vs. Ambient Temp



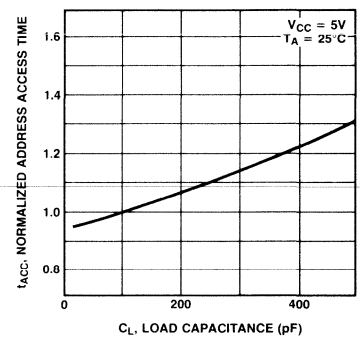
Output Source Current vs Output High Voltage



Output Sink Current vs Output Low Voltage



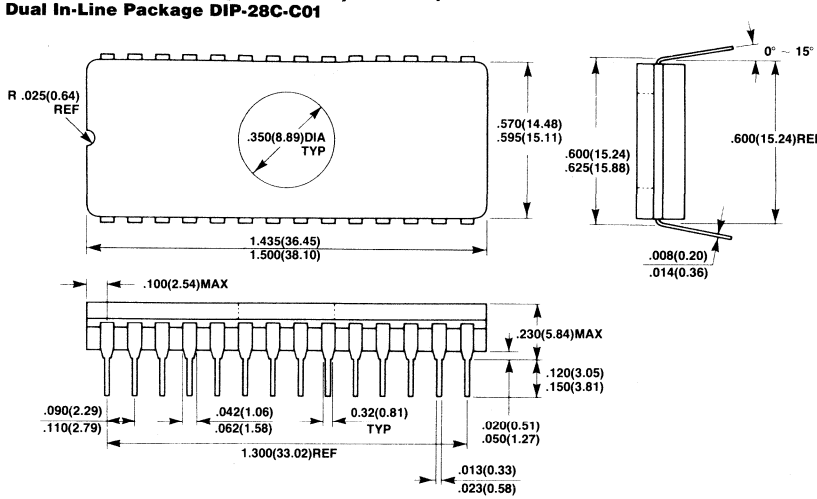
Address Access Time vs Load Capacitance



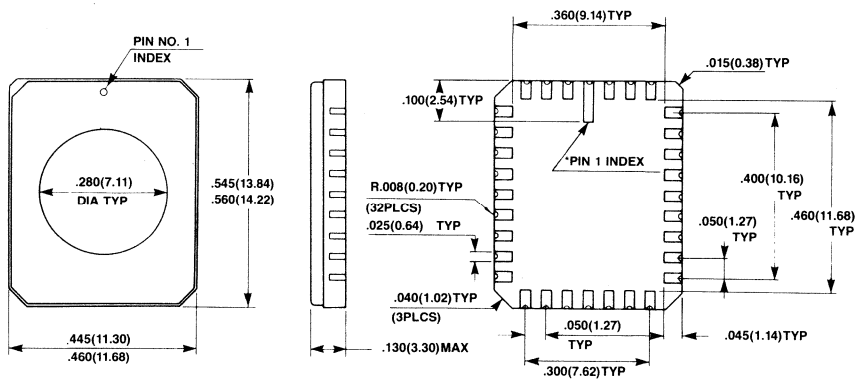
Package Dimensions

Dimensions in inches
(millimeters)

28-Lead Ceramic (Cerdip with Transparent Lid) Dual In-Line Package DIP-28C-C01



32-Pad Ceramic (Metal Seal) Leadless Chip Carrier LCC-32C-A01



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE.

FUJITSU

CMOS UV ERASABLE 131072-BIT READ ONLY MEMORY

MBM 27C128-20
MBM 27C128-25

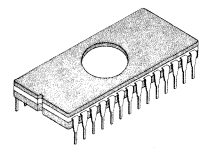
CMOS 131072 BIT UV ERASABLE AND ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY

The Fujitsu MBM 27C128 is a high speed 131,072 bit static complementary MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

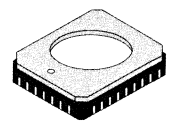
A 28-pin dual-in line package with a transparent lid and 32-Pad Leadless Chip Carrier (LCC) are used to package the MBM 27C128. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM 27C128 is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 16,384 words by 8 bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.

- CMOS power consumption
  Standby : 550μW max.
  Active : 41mW/MHz
- 16,384 words x 8 bits organization, fully decoded
- Single location programming
- Programmable utilizing the Quick Pro™ Algorithm
- Programs with one 50ms or 1ms pulses
- No clocks required (fully static operation)
- TTL compatible inputs/outputs
- Fast access time :
  200ns max. (MBM 27C128-20)
  250ns max. (MBM 27C128-25)
- Three-state output with OR-tie capability
- Output Enable ($\overline{OE}$) pin for simplified memory expansion
- Single +5V supply, ± 10% tolerance
- Standard 28-pin DIP package and 32-pad LCC
- Interchangeable with 27128-type device

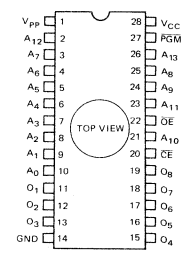


CERAMIC PACKAGE
DIP-28C-C01



CERAMIC PACKAGE
LCC-32C-A01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE)

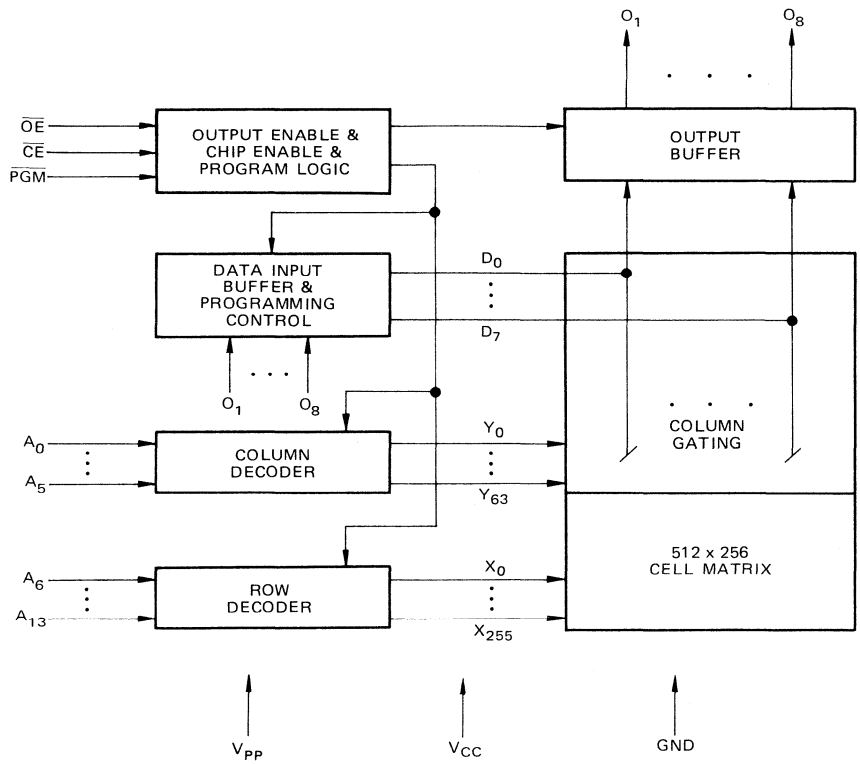
Rating	Symbol	Value	Unit
Temperature under Bias	T_{BIAS}	-25 to +85	°C
Strage Temperature	T_{STG}	-65 to +125	°C
All Inputs/Outputs Voltage with Respect to GND	V_{IN}, V_{OUT}	-0.6 to +7	V
Voltage on A_9 with Respect to GND	V_{A9}	-0.6 to +13.5	V
V_{PP} Voltage with Respect to GND	V_{PP}	-0.6 to +22	V
Supply Voltage with Respect to GND	V_{CC}	-0.6 to +7	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Quick Pro™ is a trademark of FUJITSU LIMITED

Fig. 1 – MBM 27C128 BLOCK DIAGRAM



CAPACITANCE (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V)	C_{IN}		4	6	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}		8	12	pF

FUNCTIONS AND PIN CONNECTIONS

Mode \ Function (Pin No.)	Address Input (2~10, 21, 23~26)	Data I/O (11~13, 15~19)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{CC} (28)	V_{PP} (1)	GND (14)
Read	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	GND
Output Disable	A_{IN}	High-Z	V_{IL}	V_{IH}	Don't Care	V_{CC}	V_{CC}	GND
				Don't Care	V_{IL}			
Standby	Don't Care	High-Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{CC}	GND
Program	A_{IN}	D_{IN}	V_{IL}	V_{IH}	V_{IL}	V_{CC}	V_{PP}	GND
Program Verify	A_{IN}	D_{OUT}	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{PP}	GND
Program Inhibit	Don't Care	High-Z	V_{IH}	Don't Care	Don't Care	V_{CC}	V_{PP}	GND

RECOMMENDED OPERATING CONDITIONS (Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} Supply Voltage*1	V_{CC}	4.5	5.0	5.5	V
V_{PP} Supply Voltage	V_{PP}	V_{CC} -0.6		V_{CC} +0.6	V
Input High Voltage	V_{IH}	2.0		V_{CC} +0.3	V
Input Low Voltage	V_{IL}	-0.1		0.8	V
Operating Temperature	T_A	0		70	°C

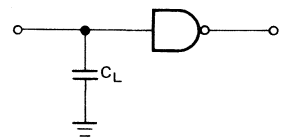
Note: *1 V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

DC CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.5V)	I_{LI}			10	μA
Output Leakage Current (V_{OUT} = 5.5V)	I_{LO}			10	μA
V_{PP} Supply Current	I_{PP}		1	100	μA
V_{CC} Standby Current ($\overline{CE}$ = V_{IH})	I_{SB1}			1	mA
V_{CC} Standby Current ($\overline{CE}$ = V_{CC} − 0.3V to V_{CC} + 0.3V, I_{OUT} = 0mA)	I_{SB2}		1	100	μA
V_{CC} Active Current ($\overline{CE}$ = V_{IL})	I_{CC1}			30	mA
V_{CC} Operation Current (f = 4MHZ, I_{OUT} = 0mA)	I_{CC2}			30	mA
Output Low Voltage (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage (I_{OH} = −400μA)	V_{OH1}	2.4			V
Output High Voltage (I_{OH} = −100μA)	V_{OH2}	V_{CC} - 0.7			V

Fig. 2 – AC TEST CONDITIONS (INCLUDING PROGRAMMING)

Input Pulse Levels:	0.8V to 2.2V
Input Rise and Fall Times:	≤ 20ns
Timing Measurement Reference Levels:	1.0V and 2.0V for inputs 0.8V and 2.0V for outputs
Output Load:	1 TTL gate and C_L = 100pF



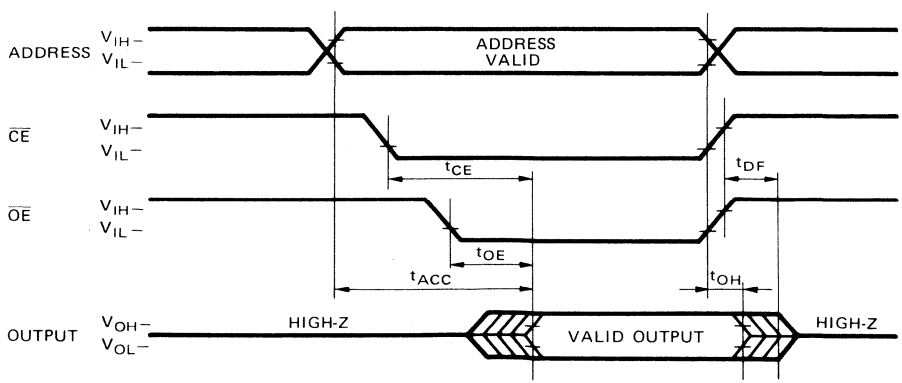
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM 27C128-20			MBM 27C128-25			Unit
		Min	Typ	Max	Min	Typ	Max	
Address Access Time*1	t_{ACC}			200			250	ns
$\overline{CE}$ to Output Delay	t_{CE}			200			250	ns
$\overline{OE}$ to Output Delay*1	t_{OE}			70			100	ns
Address to Output Hold	t_{OH}	0			0			ns
Output Enable High to Output Float*2	t_{DF}	0		60	0		60	ns

Notes: *1 $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

OPERATION TIMING DIAGRAM



PROGRAMMING/ERASING INFORMATION

MEMORY CELL DESCRIPTION

The MBM 27C128 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Fig. 3). The top gate is connected to the row decorder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Fig. 4). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Fig. 4.

Fig. 3 – MEMORY CELL

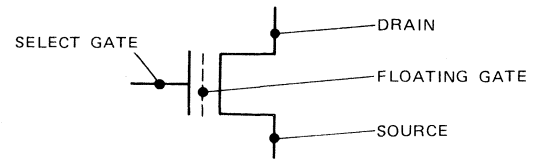
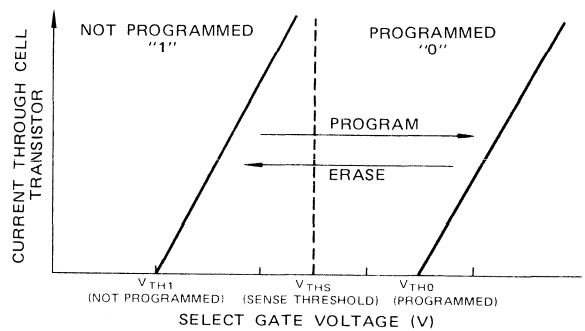


Fig. 4 – MEMORY CELL THRESHOLD SHIFT



PROGRAMMING

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM 27C128 has all 131,072 bits in the "1", or high, state. "0's" are loaded into the MBM 27C128 through the procedure of programming.

Standard Programming

The programming mode is entered when +21V is applied to the V_{PP} pin and $\overline{CE}$ and $\overline{PGM}$ are both at V_{IL}. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8 bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50 msec, TTL low-level pulse is applied to the $\overline{PGM}$ input to accomplish the programming. The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50 msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55 msec. Therefore, applying a DC level to the $\overline{PGM}$ input is prohibited when programming.

Quick Programming

In addition to the standard 50 msec pulse width programming procedure, the MBM 27C128 can be programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The algorithm utilizes a sequence of a 1ms pulse to program each location. The programming mode is entered when +21V and +6V are applied to the V_{PP} pin and V_{CC} pin respectively, and $\overline{PGM}$ and $\overline{OE}$ are V_{IH}. During programming, $\overline{CE}$ is kept at V_{IL}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. The 8 bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a sequence of a 1 msec, TTL low-level pulse is applied to the $\overline{PGM}$ pin and after that additional pulse is applied to the $\overline{PGM}$ pin to accomplish the programming.

Procedure of Quick Pro™ (Refer to the attached flow chart.)

1) Input the start address (Address=G)
2) Set the V_{CC}=6V and V_{PP}=21V
3) Input data.
4) Compare the input data with FF.

Quick Pro™ is a trademark of FUJITSU LIMITED

PROGRAMMING/ERASING INFORMATION (continued)

If data are FF, go to the step 11). If not, proceed the next step.

5) Clear the counter (X←0).
6) Apply ONE programming pulse to $\overline{PGM}$ pin (t_{PW} = 1ms Typ.).
7) Inclement the counter (X←X+1).
8) Compare the counter value with 20. If X=20, go to the step 10). If X<20, proceed the next step.
9) Verify the data. If the programmed data are the same as the input data, proceed the next step. If not, go back to the step 6).
10) Apply the additional programming pulse to the $\overline{PGM}$ pin (1ms x X or Xms x 1).
11) Compare the address with the end address. If the programmed address is the end address, proceed the next step. If not, go back to the step 3) for next address (G←G+1).
12) Verify the data. If the programmed data are not the same as the input data, the part is failed. If the programmed data the same as the input data, programming is at an end.

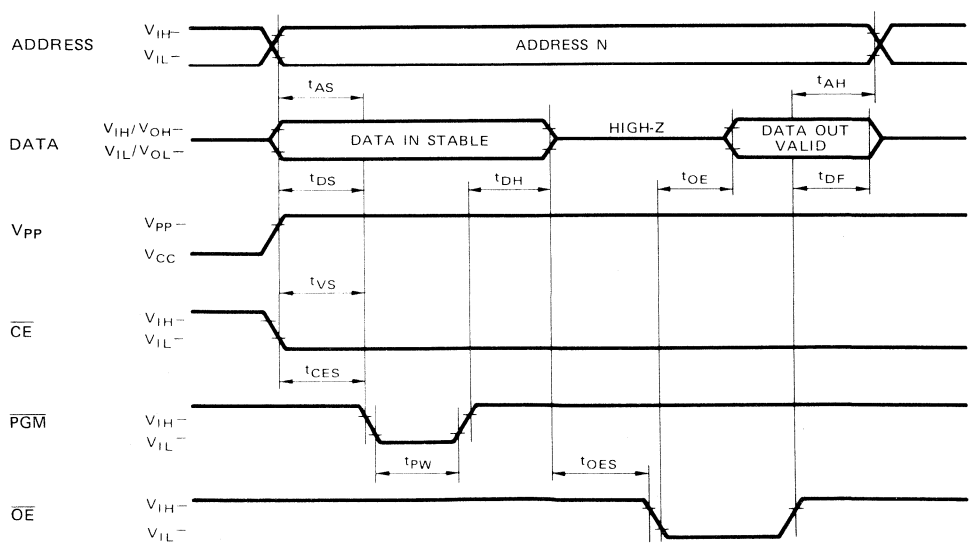
All that is required is that initial 1 msec program pulse and additional program pulse (21 msec Max.) be applied at each address to be programmed. It is necessary that one program pulse width does not exceed 21 msec. Therefore, applying a DC level to the $\overline{PGM}$ input is prohibited when programming.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the MBM 27C128 to an ultraviolet light source. A dosage of 15 W-seconds/cm^2 is required to completely erase an MBM 27C128. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000μW/cm^2 for 15 to 20 minutes. The MBM 27C128 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM 27C128 and similar devices, will erase with light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV source at 2537Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MBM 27C128, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMING WAVEFORM



1. Standard Programming

DC CHARACTERISTICS

(T_A = 25±5°C, V_{CC}^{*1} = 5V±5%, V_{PP}^{*2} = 21±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 5.25V/0.45V)	I_{LI}			10	μA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}			30	mA
V_{CC} Supply Current	I_{CC}			30	mA
Input Low Level	V_{IL}	-0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC}+ 0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OH} = -400μA)	V_{OH}	2.4			V

Note: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
*2 V_{PP} must not be greater than 22 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 21 volts. Also, during $\overline{CE}$=$\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 to 21 volts or vise-versa.

AC CHARACTERISTICS

(T_A = 25±5°C, V_{CC} = 5V±5%, V_{PP} = 21±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2			μs
Chip Enable Setup Time	t_{CES}	2			μs
Output Enable Setup Time	t_{OES}	2			μs
Data Setup Time	t_{DS}	2			μs
V_{PP} Setup Time.	t_{VS}	2			μs
Address Hold Time	t_{AH}	0			μs
Data Hold Time	t_{DH}	2			μs
Output Enable to Output Float Delay	t_{DF}	0		130	ns
Data Valid from Output Enable	t_{OE}			150	ns
$\overline{PGM}$ Pulse Width	t_{PW}	45	50	55	ms

PROGRAMMING/ERASING INFORMATION (continued)

2. Quick Programming

DC CHARACTERISTICS

(T_A = 25±5°C, V_{CC}*1 = 6V±0.25V, V_{PP}*2 = 21V±0.5V

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 6.25V/0.45V)	I_{LI}			10	μA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}			30	mA
V_{CC} Supply Current	I_{CC}			30	mA
Input Low Level	V_{IL}	-0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC}+0.3	V
Output Low Voltage During Verfify (I_{OL} = 2.1mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OH} = -400μA)	V_{OH}	2.4			V

Note: * 1 V_{CC} must be applied either coincidently or before V_{PP} and removed either concidently or after V_{PP}.
* 2 V_{PP} must not be greater than 22 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 21 volts. Also, during $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 6 to 21 volts or vise-versa.

AC CHARACTERISTICS

(T_A = 25±5°C, V_{CC} = 6V±0.25V, V_{PP} = 21V±0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2			μs
Chip Enable Setup Time	t_{CES}	2			μs
Output Enable Setup Time	t_{OES}*	2			μs
Data Setup Time	t_{DS}	2			μs
V_{PP} Setup Time	t_{VS}	2			μs
Address Hold Time	t_{AH}	0			μs
Data Hold Time	t_{DH}*	2			μs
Output Enable to Output Float Delay	t_{DF}	0		130	ns
Data Valid from Output Enable	t_{OE}			150	ns
$\overline{PGM}$ Pulse Width	t_{PW}	0.95	1	1.05	ms

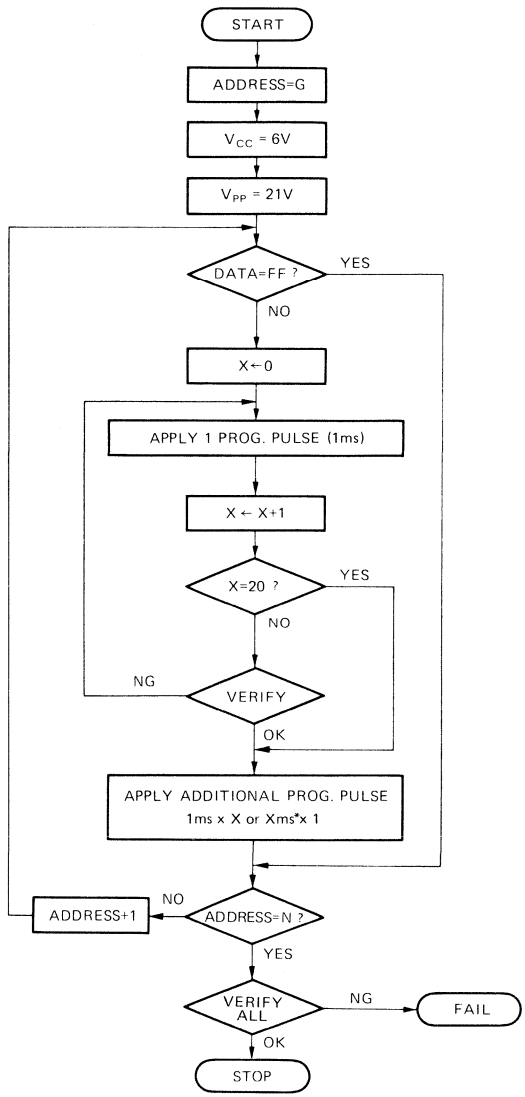
* $t_{DH} + t_{OES} \geq 50\mu s$

PROGRAMMING FLOW CHART FOR Quick Pro™

V_{CC} = 6V±0.25V
V_{PP} = 21V±0.5V

T_{PW} = 1ms±50μs
(* = Xms±5%)

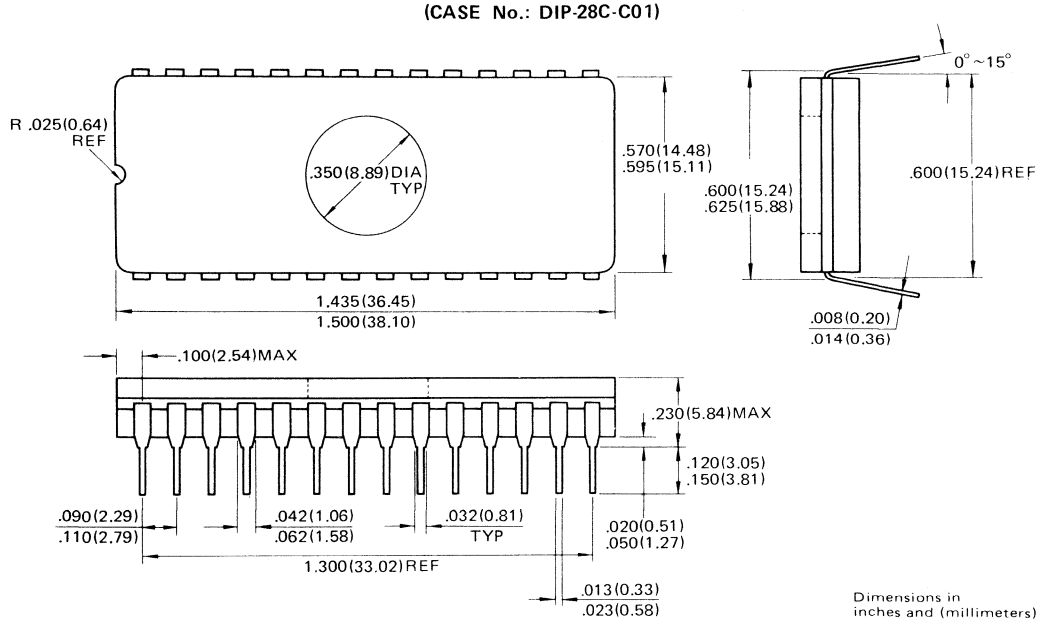
G : START ADDRESS
N : STOP ADDRESS
X : COUNTER VALUE
MAXIMUM 42ms/BYTE
MINIMUM 1.9ms/BYTE



Quick Pro™ is a trademark of FUJITSU LIMITED

PACKAGE DIMENSIONS

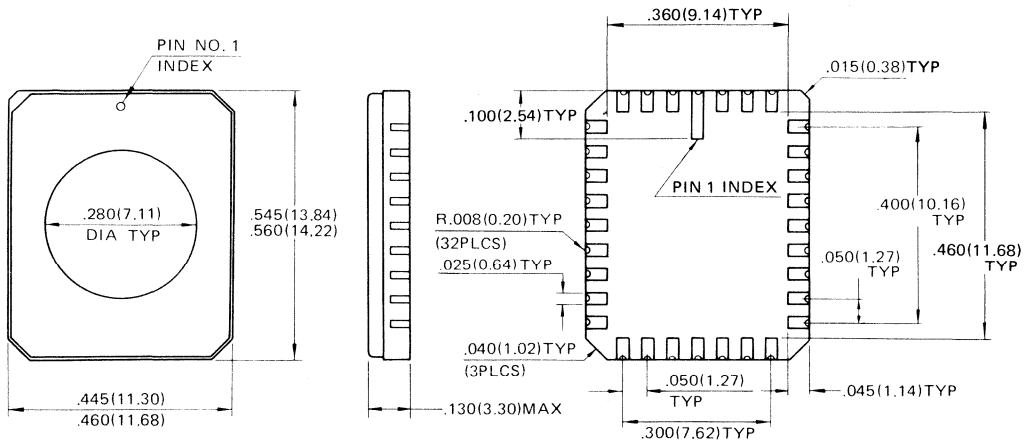
28-LEAD CERAMIC (CERDIP WITH TRANSPARENT LID) DUAL IN-LINE PACKAGE
(CASE No.: DIP-28C-C01)



Dimensions in
inches and (millimeters)

PACKAGE DIMENSIONS

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No. : LCC-32C-A01)



Dimensions in
inches (millimeters)

*Shape of Pin index: Subject to change without notice

MBM27C256-25, MBM27C256-30

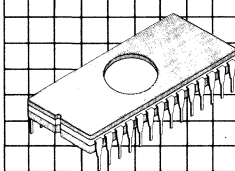
CMOS 32,768 x 8-Bit UV Erasable and Electrically Programmable Read Only Memory

Description

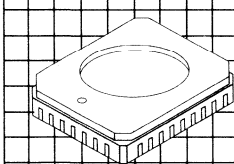
The Fujitsu MBM27C256 is a high speed 262,144-bits complementary MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

A 28-pin dual-in line package with a transparent lid and 32-pad Leadless Chip Carrier (LCC) are used to package the MBM27C256. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM27C256 is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 32,768 words by 8-bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



Ceramic Package
DIP-28C-C01

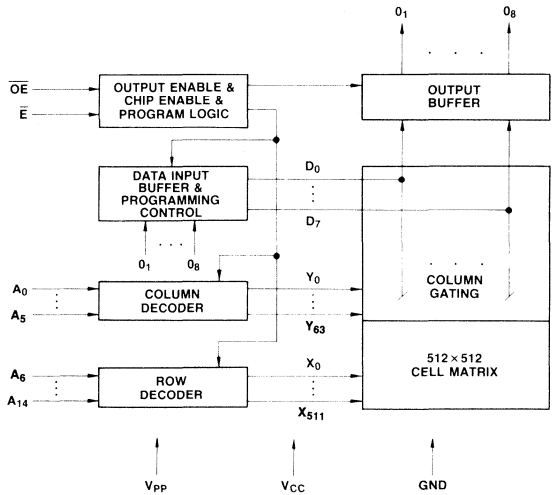


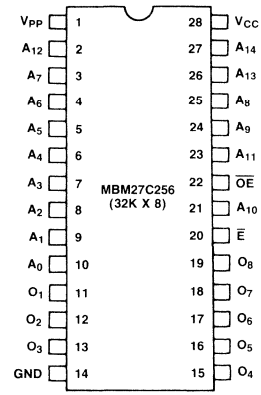
Leadless Chip Carrier
LCC-32C-A01

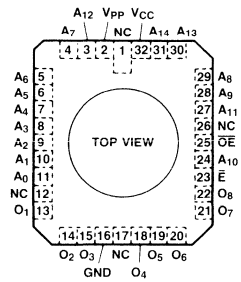
Features

- **CMOS Power Consumption: 550 μW max. (Standby) 40 mW/MHz (Active)**
- **32,768 words by 8-bits organization, fully decoded**
- **Simple programming requirements**
- **Single location programming**
- **High speed programming algorithm (typically two 1 ms pulses)**
- **No clock required (fully static operation)**
- **Single +5V supply, ±10%**
- **TTL compatible inputs and outputs**
- **3-state output with OR-tie capability**
- **Output Enable ($\overline{OE}$) pin for simplified memory expansion**
- **Fast Access Time: MBM27C256-25 250 ns max. MBM27C256-30 300 ns max.**
- **Single +5V operation**
- **Standard 28-pin DIP package/32-pad LCC**

MBM27C256 Block Diagram and Pin Assignments







Absolute Maximum Ratings
(See Note)

Parameter	Symbol	Value	Unit
Temperature under bias	T_{BIAS}	−25 to +85	°C
Storage temperature	T_{STG}	−65 to +125	°C
Inputs/outputs with respect to GND	V_{IN}, V_{OUT}	−0.6 to +7	V
Voltage on A_9 with respect to GND	V_{A9}	−0.6 to +13.5	V
V_{PP} with respect to GND	V_{PP}	−0.6 to +22	V
V_{CC} with respect to GND	V_{CC}	−0.6 to +7	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may effect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Functions and Pin Connections

Function (Pin No.) / Mode	Address Input (2~10, 21, 23~27)	Data I/O (11~13, 15~19)	$\overline{E}$ (20)	$\overline{OE}$ (22)	V_{CC} (28)	V_{PP} (1)	GND (14)
Read	A_{IN}	OUT	V_{IL}	V_{IL}	V_{CC}	V_{CC}	GND
Output disable	A_{IN}	High Z	V_{IL}	V_{IH}	V_{CC}	V_{CC}	GND
Stand by	Don't care	High Z	V_{IH}	Don't care	V_{CC}	V_{CC}	GND
Program	A_{IN}	IN	V_{IL}	V_{IH}	V_{CC}	V_{PP}	GND
Program verify	A_{IN}	OUT	V_{IL}	V_{IL}	V_{CC}	V_{PP}	GND
Program inhibit	Don't care	High Z	V_{IH}	Don't care	V_{CC}	V_{PP}	GND

Recommended Operating Conditions
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
V_{CC} supply voltage*1	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
V_{PP} supply voltage	V_{PP}	V_{CC} − 0.6		V_{CC} + 0.6	V	
Input high voltage	V_{IH}	2.0		V_{CC} +0.3	V	
Input low voltage	V_{IL}	−0.1		0.8	V	

Note: *1 V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance (V_{IN} = 0V)	C_{IN}		4	6	pF
Output capacitance (V_{OUT} = 0V)	C_{OUT}		8	12	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Input load current (V_{IN} = 5.5V)	I_{LI}			10	μA
Output leakage current (V_{OUT} = 5.5V)	I_{LO}			10	μA
V_{PP} supply current	I_{PP}		1	100	μA
V_{CC} standby current ($\overline{E}$ = V_{IH})	I_{SB1}			1	mA
V_{CC} standby current ($\overline{E}$ = V_{CC} −0.3V to V_{CC} +0.3V, I_{OUT} = 0 mA)	I_{SB2}		1	100	μA
V_{CC} active current ($\overline{E}$ = V_{IL})	I_{CC1}			30	mA
V_{CC} operation current (f = 4 MHz, I_{OUT} = 0 mA)	I_{CC2}			30	mA
Output low voltage (I_{OL} = 2.1 mA)	V_{OL}			0.45	V
Output high voltage (I_{OH} = −400 μA)	V_{OH1}	2.4			V
Output high voltage (I_{OH} = −100 μA)	V_{OH2}	V_{CC} − 0.7			V

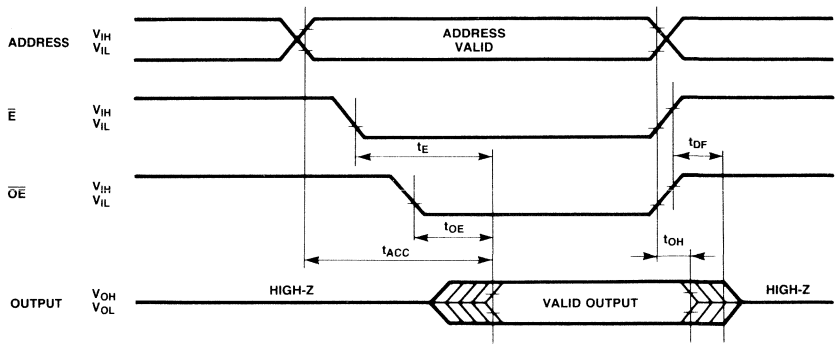
AC Characteristics

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MBM27C256-25 Min	MBM27C256-25 Max	MBM27C256-30 Min	MBM27C256-30 Max	Unit
Address access time *1 ($\overline{E} = \overline{OE} = V_{IL}$)	t_{ACC}		250		300	ns
$\overline{E}$ to output valid ($\overline{OE} = V_{IL}$)	t_E		250		300	ns
$\overline{OE}$ to output valid ($\overline{E} = V_{IL}$)*1	t_{OE}		100		120	ns
$\overline{OE}$, $\overline{E}$ high to output float*2	t_{DF}	0	60	0	105	ns
Address to output hold	t_{OH}	0		0		ns

Notes: *1 $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the following edge of $\overline{E}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$, $\overline{E}$, whichever occurs first. Output float is defined as the point where data is a no longer driven.

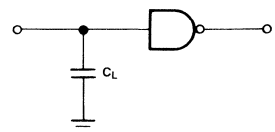
Operation Timing Diagram



AC Test Conditions

(Including programming)

Input Pulse Levels: ..... 0.8V to 2.2V
Input Rise and Fall Time: ..... ≤20 ns
Timing Measurement Reference Levels: .... 1.0V and 2.0V for inputs
0.8V and 2.0V for outputs
Output Load: ..... 1 TTL gate and C_L = 100 pF



Programming/Erasing Information

Memory Cell Description

The MBM27C256 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate as shown in Memory Cell diagram. The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold as shown in Memory Cell Threshold Shift diagram. In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line as shown in Memory Cell Threshold Shift diagram.

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27C256 has all 262,144-bits in the "1", or high, state. "0's" are loaded into the MBM27C256 through the procedure of programming.

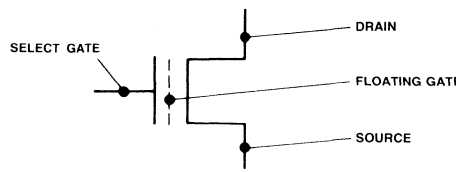
The MBM27C256 is programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The programming mode is entered when +21V and +6V are applied to the V_{PP} pin and V_{CC} pin respectively, and $\overline{E}$ and $\overline{OE}$ are at V_{IH}. A 0.1 μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. The 8-bit pattern are placed on the respective output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a sequence of single TTL low-level pulse is applied to the $\overline{E}$ pin followed by an additional pulse to the $\overline{E}$ pin to accomplish the programming.

Procedure of Quick Pro™ (Refer to the attached flow chart.)

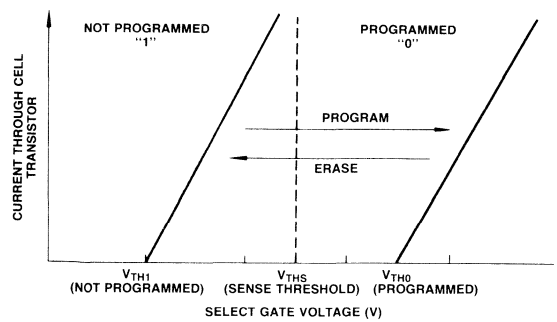
1. Input the start address (start address = G).
2. Set the V_{CC} = 6V and V_{PP} = 21V.
3. Input data.
4. Compare the input data with FF. If the data are FF, go to step 11. If not, proceed to the next step.
5. Clear the counter (X = 0).
6. Apply ONE programming pulse to the $\overline{E}$ pin (t_{PW} = 1 ms typ.).
7. Increment the counter (X = X + 1).
8. Compare the number of counter value with 20. If X = 20, go to step 10. If X < 20, proceed to the next step.
9. Verify the programmed data. If the programmed data are the same as the input data, proceed to the next step. If not, go back to step 6.
10. Apply the additional programming pulse to the $\overline{E}$ pin (1 ms x X or X ms x 1).
11. Compare the address with the end address. If the programed address is the end address, proceed to the next step. If not, proceed from step 3 for next address (GG + 1).
12. Verify all the data. If the programmed data is not the same as the input data, the part failed. If it is, the program is completed.

A continuous TTL low input should not be applied to the $\overline{E}$ pin during the program mode (V_{PP} = 21V, V_{CC} = 6V and $\overline{OE}$ = V_{IH}). Because it is required that one programming pulse width does not exceed 21 msec at each address.

Memory Cell



Memory Cell Threshold Shift



Programming/Erasing Information
(Continued)

Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the MBM27C256 to an ultraviolet light source. A dosage of 15W-seconds/cm^2 is required to completely erase an MBM27C256. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å) with intensity of 12,000 μW/cm^2) for 15 to 20 minutes. The MBM27C256 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM27C256 and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the MBM27C256, and such exposure should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

AC Characteristics

(T_A = 25 ± 5°C,
V_{CC} = 6V ± 0.25V,
V_{PP} = 21V ± 0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2			μs
Chip enable setup time	t_{CES}	2			μs
Output enable setup time	t_{OES}	2			μs
Data setup time	t_{DS}	2			μs
V_{PP} setup time	t_{VS}	2			μs
Address hold time	t_{AH}	2			μs
Output enable hold time	t_{OEH}	2			μs
Data hold time	t_{DH}	2			μs
Output enable recovery time	t_{OR}	2			μs
Chip enable to data valid	t_{DV}			1	μs
Output disable to output float delay	t_{DF}			105	ns
Programming pulse width	t_{PW}	0.95	1	1.05	ms
Additional programming pulse width	t_{APW}	0.95	1	21	ms

Programming/ Erasing Information
(Continued)

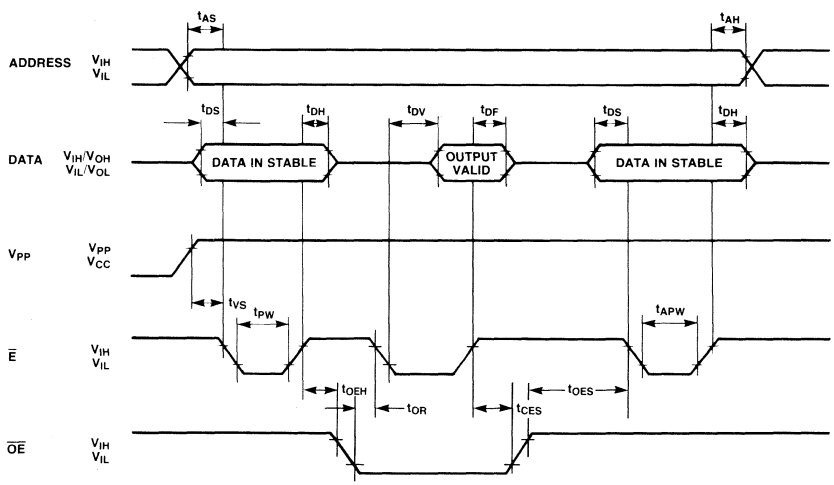
DC Characteristics

(T_A = 25 ± 5°C,
V_{CC} = 6V ±0.25V,
V_{PP} = 21V ± 0.5V)

Parameter	Symbol	Min	Typ	Max	Unit
Input leakage current (V_{IN} = 5.25V/0.45V)	I_{LI}			10	μA
V_{PP} supply current during programming pulse ($\overline{E}$ = V_{IL})	I_{PP}			40	mA
V_{CC} supply current	I_{CC}			30	mA
Input low level	V_{IL}	−0.1		0.8	V
Input high level	V_{IH}	2.0		V_{CC} + 0.3	V
Output low voltage during verify (I_{OL} = 2.1 mA)	V_{OL}			0.45	V
Output high voltage during verify (I_{OH} = −400 μA)	V_{OH}	2.4			V

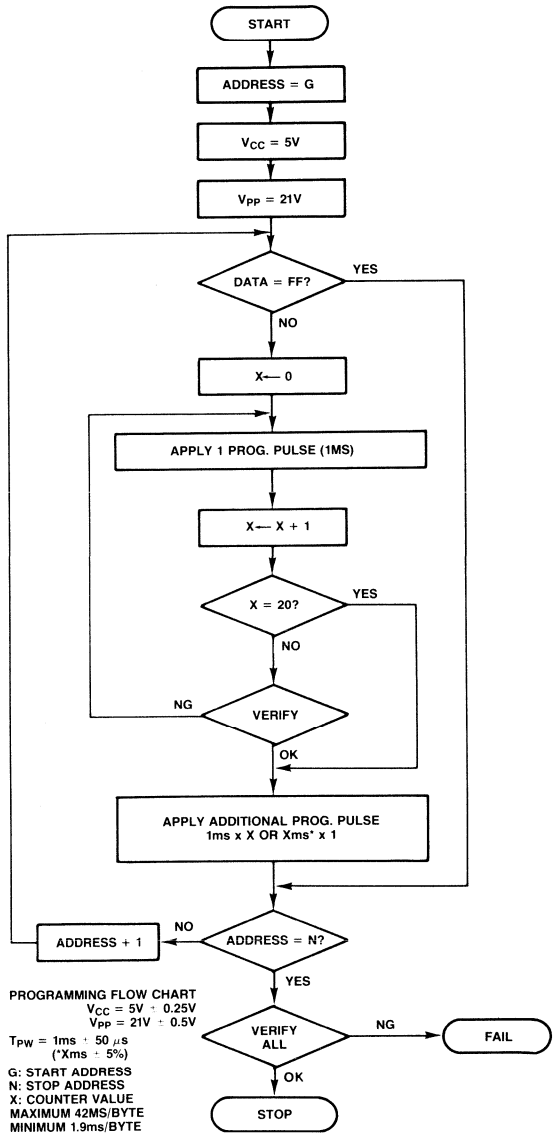
Notes: V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
V_{PP} must not be greater than 21.5V including overshoot. Permanent device damage may occur if the device is taken out or put into socket with V_{PP} = 21 volts. Also, during $\overline{E}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 21 volts or vise-versa.

Programming Waveform



Programming/Erasing Information
(Continued)

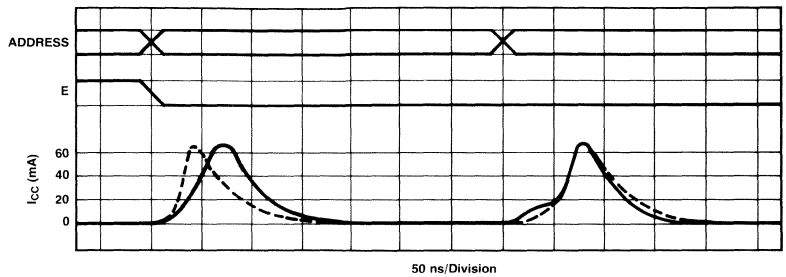
Quick Program Flow Chart



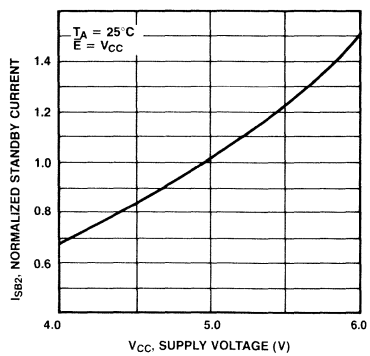
Characteristics Curves

(Dotted curves are for "HA" version.)

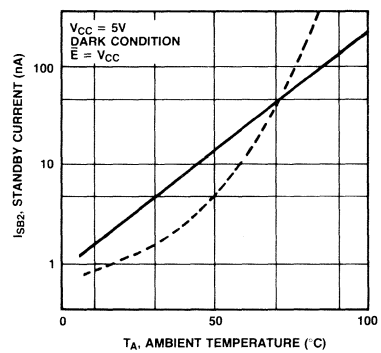
Current Waveform V_{CC} = 5.0V, T_A = 25°C



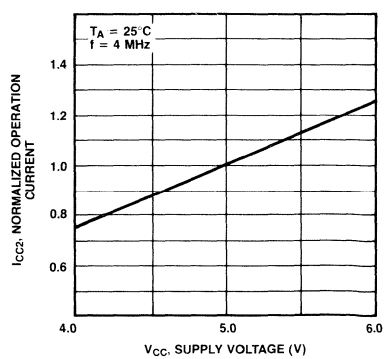
Standby Current vs. Supply Voltage



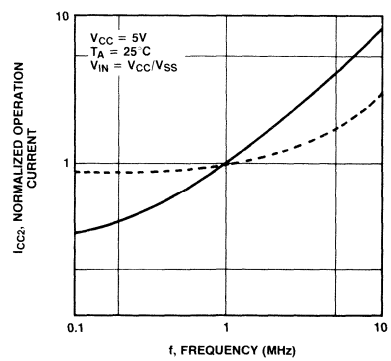
Standby Current vs. Ambient Temperature



Operating Current vs. Supply Voltage

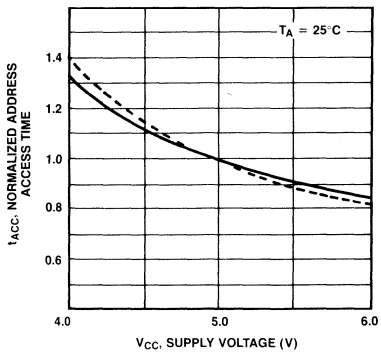


Operation Current vs. Frequency

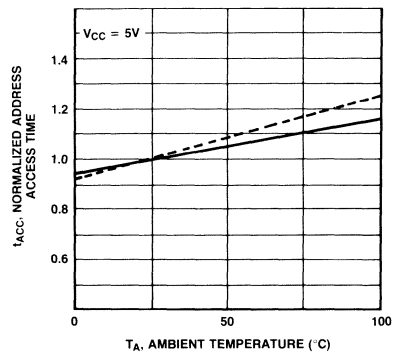


Characteristics Curves
(Continued)
(Dotted curves are for "HA" version.)

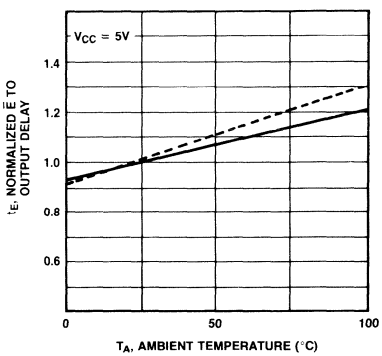
Address Access Time vs. Supply Voltage



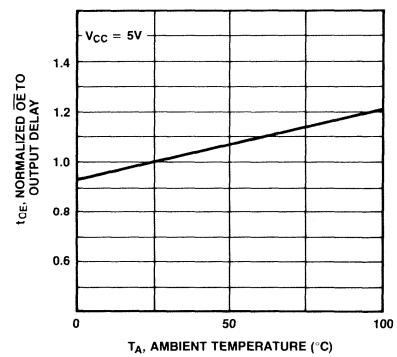
Address Access Time vs. Ambient Temperature



$\overline{E}$ to Output Delay vs. Ambient Temperature

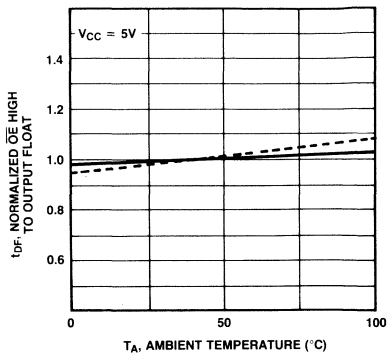


$\overline{OE}$ to Output Delay vs. Ambient Temperature

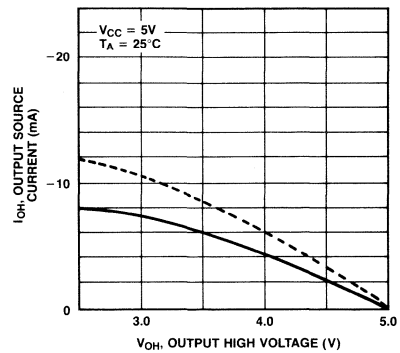


Characteristics Curves
(Continued
(Dotted curves are for "HA" version.)

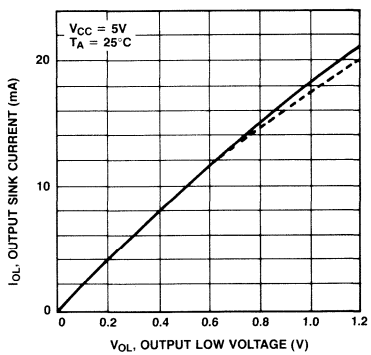
$\overline{OE}$ High to Output Float vs. Ambient Temperature



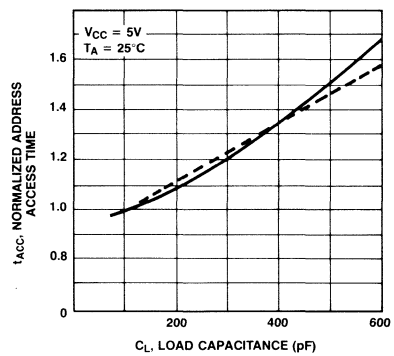
Output Source Current vs. Output High Voltage



Output Sink Current vs. Output Low Voltage



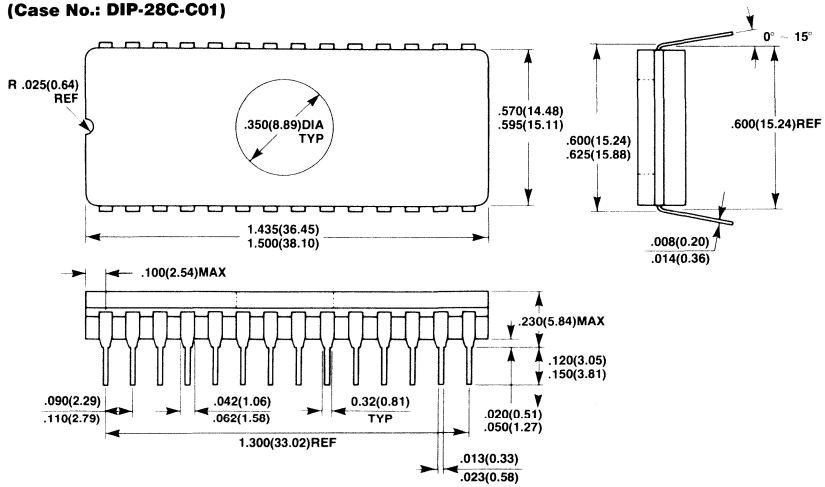
Address Access Time vs. Load Capacitance



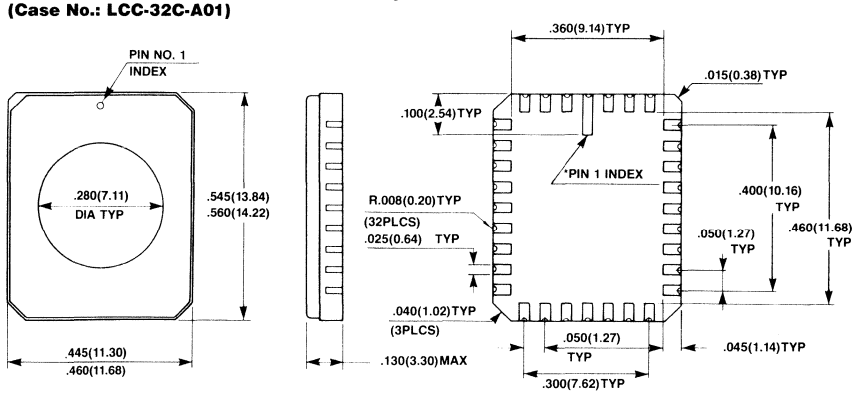
Package Dimensions

Dimensions in inches
(millimeters)

28-Lead Ceramic (CERDIP with Transparent Lid) Dual In-Line Package (Case No.: DIP-28C-C01)



32-Pad Ceramic (Metal Seal) Leadless Chip Carrier (Case No.: LCC-32C-A01)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE.

Advanced Information

FUJITSU

■ MBM27C256A-20, MBM27C256A-25

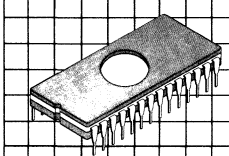
CMOS UV Erasable 262,144-Bit
Read Only Memory

Description

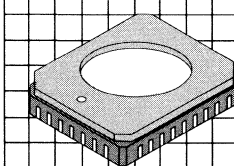
The Fujitsu MBM27C256A is a high speed 262,144-bit complementary MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

A 28-pin dual-in line package with a transparent lid and 32-pad Leadless Chip Carrier (LCC) are used to package the MBM27C256A. The transparent lid allows the user to expose the device to ultra-violet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM27C256A is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 32,768 words by 8-bits for use in microprocessor applications.



Ceramic Package DIP-28C-C01



Leadless Chip Carrier LCC-32C-A01

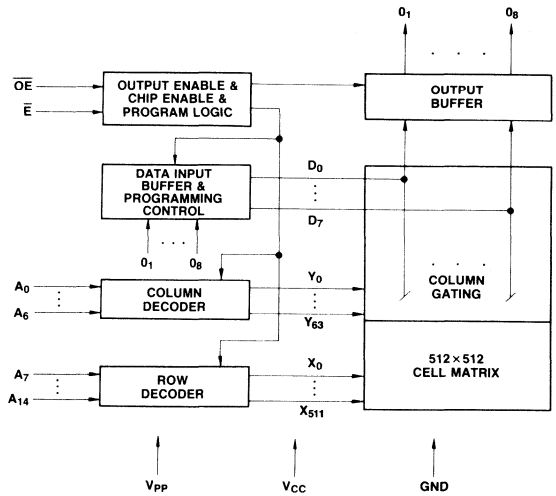
Features

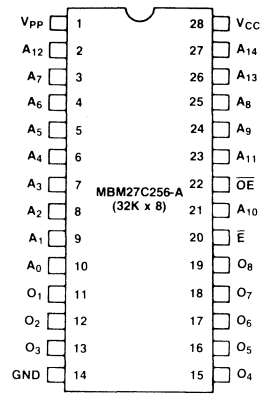
- **CMOS power consumption**
  Standby: 550 μW max.
  Active: 41 mW/MHz
- **32,768 words x 8-bits organization, fully decoded**
- **Program voltage: 12.5V**
- **Programmable utilizing the Quick Pro™ algorithm**
- **Programs with 1 ms pulses**
- **No clocks required (fully static operation)**
- **Fast access time:**
  200 ns max. (MBM27C256A-20)
  250 ns max. (MBM27C256A-25)
- **TTL compatible inputs/outputs**
- **Three-state output with OR-tie capability**
- **Output Enable ($\overline{OE}$) pin for simplified memory expansion**
- **Single +5V supply; +10% tolerance**
- **Standard 28-pin DIP package and 32-pad LCC**

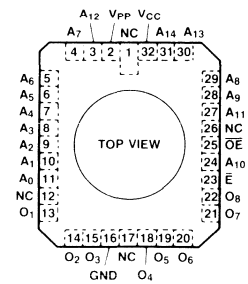
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Quick Pro™ is a trademark of FUJITSU LIMITED

MBM27C256A Block Diagram and Pin Assignments







Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Temperature under bias	T_{BIAS}	−25 to +85	°C
Storage temperature	T_{STG}	−65 to +125	°C
All inputs/outputs voltage with respect to GND	V_{IN}, V_{OUT}	−0.6 to +7	V
Voltage on A_9 with respect to GND	V_{A9}	−0.6 to +13.5	V
V_{PP} voltage with respect to GND	V_{PP}	−0.6 to +14	V
Supply voltage with respect to GND	V_{CC}	−0.6 to +7	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Functions and Pin Connections

	Address Input (2 ~ 10, 21, 23, 25 ~ 27)	Data I/O (11 ~ 13, 15 ~ 19)	CE (20)	OE (22)	V_{CC} (28)	V_{PP} (1)	GND (14)	A_9 (24)
Read	A_{IN}	OUT	V_{IL}	V_{IL}	+5V	+5V	GND	A_{IN}
Output disable	A_{IN}	High-Z	V_{IL}	V_{IH}	+5V	+5V	GND	A_{IN}
Standby	Don't care	High-Z	V_{IH}	Don't care	+5V	+5V	GND	Don't care
Program	A_{IN}	IN	V_{IL}	V_{IH}	+6V	+12.5V	GND	A_{IN}
Program verify	A_{IN}	OUT	Don't care	V_{IL}	+6V	+12.5V	GND	A_{IN}
Program inhibit	Don't care	High-Z	V_{IH}	V_{IH}	+6V	+12.5V	GND	Don't care
Electronic signature	A_{IN}	Code	V_{IL}	V_{IL}	+5V	+5V	GND	+12V

Recommended Operating Conditions
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} supply voltage*	V_{CC}	4.5	5.0	5.5	V
V_{PP} supply voltage	V_{PP}	V_{CC} − 0.6		V_{CC} + 0.6	V
Input high voltage	V_{IH}	2.0		V_{CC} + 0.3	V
Input low voltage	V_{IL}	−0.1		0.8	V
Operating temperature	T_A	0		70	°C

Note: *V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

DC Characteristics
(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Input load current (V_{IN} = 5.5V)	I_{LI}			10	μA
Output leakage current (V_{OUT} = 5.5V)	I_{LO}			10	μA
V_{PP} supply current (V_{PP} = V_{CC} ± 0.6V)	I_{PP}		1	100	μA
V_{CC} standby current ($\overline{E}$ = V_{IH})	I_{SB1}			1	mA
V_{CC} standby current ($\overline{E}$ = V_{CC} ± 0.3V, I_{OUT} = 0 mA)	I_{SB2}		1	100	μA
V_{CC} active current ($\overline{E}$ = V_{IL})	I_{CC1}			30	mA
V_{CC} operation current (f = 4 MHz, I_{OUT} = 0 mA)	I_{CC2}			30	mA
Output low voltage (I_{OL} = 2.1 mA)	V_{OL}			0.45	V
Output high voltage (I_{OH} = −400 μA)	V_{OH1}	2.4			V
Output high voltage (I_{OH} = −100 μA)	V_{OH2}	V_{CC} − 0.7			V

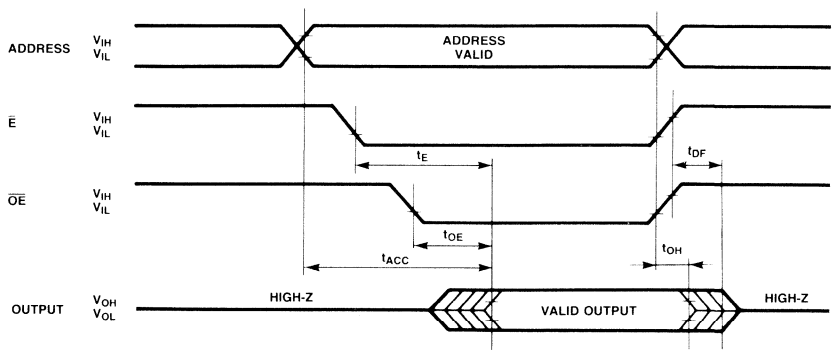
AC Characteristics

(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM27C256A-20 Min	MBM27C256A-20 Typ	MBM27C256A-20 Max	MBM27C256A-25 Min	MBM27C256A-25 Typ	MBM27C256A-25 Max	Units
Address access time*1 ($\overline{E} = \overline{OE} = V_{IL}$)	t_{ACC}			200			250	ns
$\overline{E}$ to output delay ($\overline{OE} = V_{IL}$)	t_E			200			250	ns
$\overline{OE}$ to output delay*1 ($\overline{E} = V_{IL}$)	t_{OE}			75			100	ns
Address to output hold	t_{OH}	0			0			ns
Output enable high to output*2 float*2	t_{DF}	0		60	0		60	ns

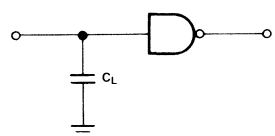
Notes: *1 $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{E}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{E}$, whichever occurs first. Output float is defined as the point where data is no longer driven.

Operation Timing Diagram



AC Test Conditions (Including Programming)

Input pulse levels:	0.45V to 2.4V
Input rise and fall times:	≤20 ns
Timing measurement reference levels:	1.0V and 2.0V for inputs 0.8V and 2.0V for outputs
Output load:	1 TTL gate and C_L = 100 pF



Programming/Erasing Information

Programming

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27C256A has all 262,144 bits in the "1", or high state. "0's" are loaded into the MBM27C256A through the procedure of programming.

The MBM27C256A is programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The programming mode is entered when +12.5V and +6V are applied to V_{PP} and V_{CC} respectively, and $\overline{E}$ and $\overline{OE}$ are V_{IH}. A 0.1μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. Eight bit data patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 1 ms programming pulse is applied to E and after that one additional pulse which is 3 times as wide as previous pulse is applied to E to accomplish the programming.

Procedure of Quick Pro™ (Refer to the attached flowchart.)

1) Set the start address (=G) at the address pins.
2) Set V_{CC} = 6V, V_{PP} = 12.5V and $\overline{E}$ = V_{IH}.
3) Clear the programming pulse counter (X ← 0).
4) Input data to respective pins.
5) Apply ONE programming pulse (t_{PW} = 1 ms Typ.) to $\overline{E}$.
6) Increment the counter (X ← X + 1).
7) Compare the number (=X) of applied programming pulse with 25 and then verify the programmed data. If programmed data is verified, go to the next step regardless of X value. If X = 25 and programmed data is not verified, the device fails. If X = 25 and programmed data is not verified, go back to the step 5).
8) Apply one additional wide programming pulse to $\overline{E}$ (3X ms).
9) Compare the address with an end address (=N). If the programmed address is the end address, proceed to the next step. If not, increment the address (G ← G + 1) and then go to the step 3) for the next address.
10) Set V_{CC} = V_{PP} = 5V.
11) Verify the all programmed data. If the verification succeeds, the programming completes. If any programmed data is not the same as original data, the device fails.

A continuous TTL low level should not apply to $\overline{E}$ input pin during the program mode (V_{PP} = 12.5V, V_{CC} = 6V and $\overline{OE}$ = V_{IH}) because it is required that one programming pulse width does not exceed 78.75 ms at each address.

Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the MBM27C256A to an ultraviolet light source. A dosage of 15 W-seconds/cm^2 is required to completely erase an MBM27C256A. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (A)) with intensity of 12000μW/cm^2 for 15 to 20 minutes.

The MBM27C256A should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM27C256A and similar devices, will erase with light sources having wavelengths shorter than 4000A. Although erasure time will be much longer than with UV source at 2537A, nevertheless the exposure to fluorescent light and sunlight will eventually erase the MBM27C256A, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

Electronic Signature

The MBM27C256A has electronic signature mode which is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.

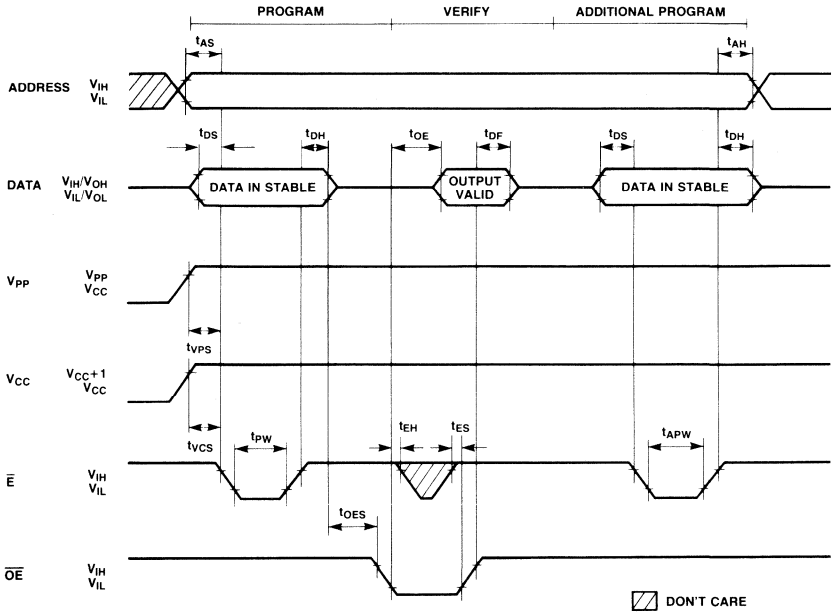
The electronic signature is activated when +12V is applied to address A_9 (pin 24) of the MBM27C256A. Two identifier bytes are read out from the outputs by toggling address line A_0 (pin 10) from V_{IL} to V_{IH}. The address lines from A_1 to A_{13} must be held at V_{IL} to keep the electronic signature mode.

A_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	Definition
V_{IL}	0	0	1	0	0	0	0	0	Manufacture
V_{IH}	0	1	0	0	0	1	1	0	Device

Note: A_9 = 12V ± 0.5V
$A_1 \sim A_8 = A_{10} \sim A_{13} = E = OE = V_{IL}$.

Programming/Erasing Information
(Continued)

Programming Waveform



DC Characteristics
(T_A = 25 ± 5°C, V_{CC}*1 = 6V ± 0.25V, V_{PP}*2 = 12.5V ± 0.3V)

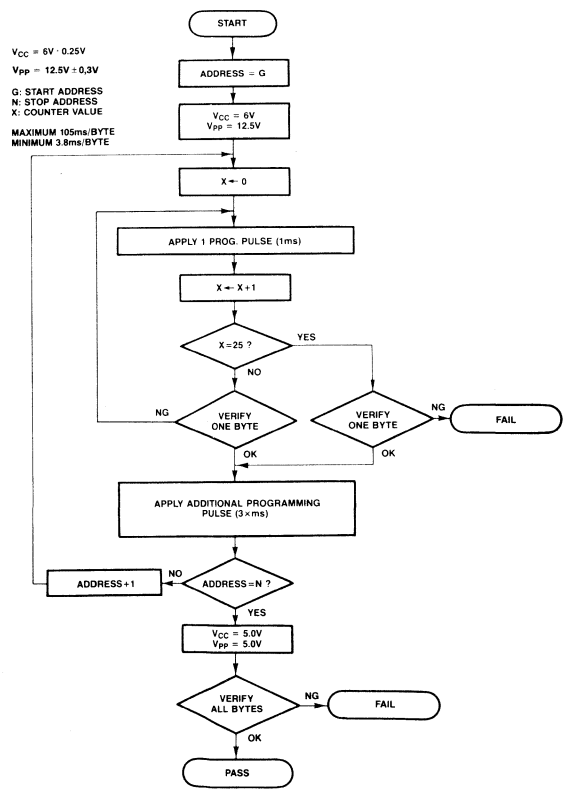
Parameter	Symbol	Min	Typ	Max	Unit
Input leakage current (V_{IN} = 6.25V/0.45V)	I_{IL}			10	μA
V_{PP} supply current ($\overline{E}$ = V_{IL}, $\overline{OE}$ = V_{IH})	I_{PP2}			50	mA
V_{PP} supply current ($\overline{OE}$ = V_{IL})	I_{PP3}			5	mA
V_{CC} supply current	I_{CC}			30	mA
Input low level	V_{IL}	−0.1		0.8	V
Input high level	V_{IH}	2.0		V_{CC} + 0.3	V
Output low voltage during verify (I_{OL} = 2.1 mA)	V_{OL}			0.45	V
Output high voltage during verify (I_{OH} = −400 μA)	V_{OH}	2.4			V

Notes: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
2 V_{PP} must not be greater than 14 volts including overshoot. Permanent device damage may occur if the device is taken out or put into socket remaining V_{PP} = 12.5 volts, Also, during E = V_{IL}, OE = V_{IH}, V_{PP} must not be switched from V_{CC} to V_{PP} volts or vice versa.

AC Characteristics
(T_A = 25 ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V

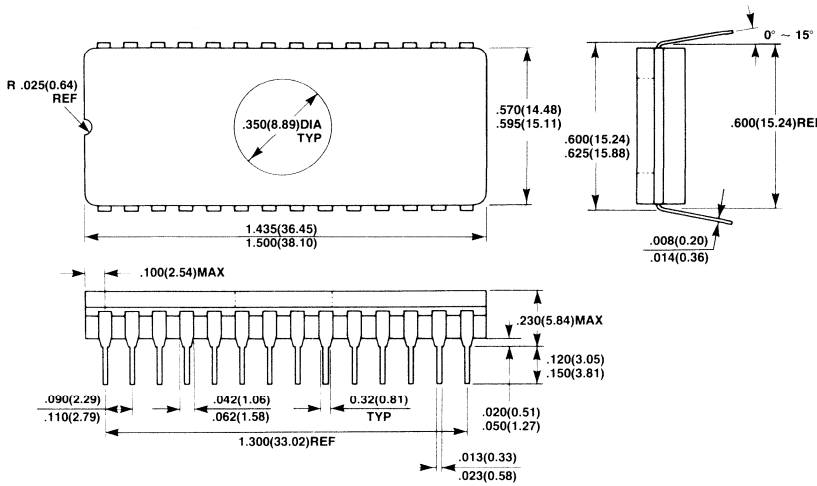
Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2			μs
Output enable setup time	t_{OES}	2			μs
Chip enable setup time	t_{ES}	2			μs
Data setup time	t_{DS}	2			μs
V_{PP} setup time	t_{VPS}	2			μs
V_{CC} setup time	t_{VCS}	2			μs
Address hold time	t_{AH}	2			μs
Data hold time	t_{DH}	2			μs
Chip enable hold time	t_{CEH}	2			μs
Output enables to output valid	t_{OE}			120	ns
Output disable to output float delay	t_{DF}			105	ns
Programming pulse width	t_{PW}	0.95	1	1.05	ms
Programming pulse number		1		25	times
Additional programming pulse width	t_{APW}	2.85		78.75	ms

Programming Flow Chart

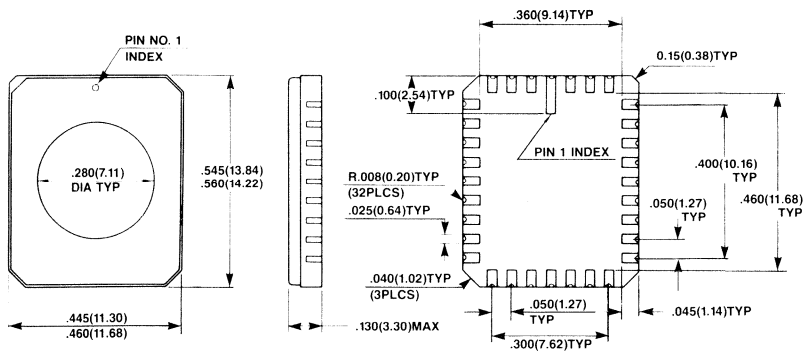


Package Dimensions
Dimensions in inches
(millimeters)

28-Lead Ceramic (Cerdip With Transparent Lid) Dual In-Line Package (Case No.: DIP-28C-C01)



32-Pad Ceramic (Metal Seal) Leadless Chip Carrier (Case No.: LCC-32C-A01)



Shape of Pin index: Subject to change without notice

MBM27C256A-20-W
MBM27C256A-25-W

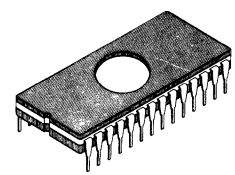
CMOS 32,768 x 8-Bit UV Erasable and Electrically Programmable Read Only Memory

Description

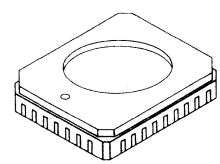
The Fujitsu MBM27C256A-W is a high speed 262,144-bits UV erasable and electrically reprogrammable read only memory (EPROM) with CMOS technology. It is especially well suited for applications where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

A 28-pin dual-in line package with a transparent lid and 32-pad Leadless Chip Carrier (LCC) are used to package the MBM27C256A-W. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM27C256A-W is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 32,768 words by 8-bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.



Ceramic Package DIP-28C-C01

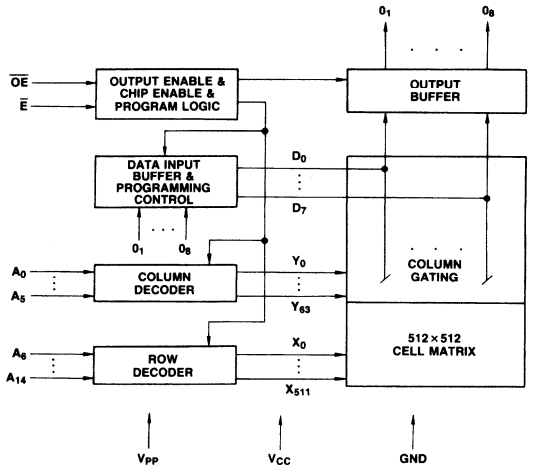


Leadless Chip Carrier LCC-32C-A01

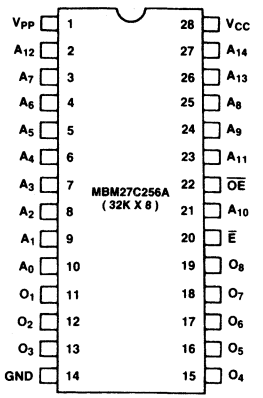
Features

- **Wide temperature range: −55°C to +125°C**
- **CMOS Power Consumption: 550 μW max. (Standby) 41 mW/MHz (Active)**
- **32,768 words by 8-bits organization, fully decoded**
- **Simple programming requirements**
- **Single location programming**
- **High speed programming algorithm (typically two 1 ms pulses)**
- **No clock required (fully static operation)**
- **Programming voltage: 12.5V**
- **Single +5V supply, ±10%**
- **TTL compatible inputs and outputs**
- **3-state output with OR-tie capability**
- **Output Enable ($\overline{OE}$) pin for simplified memory expansion**
- **Fast access time: MBM27C256A-20-W 200 ns max. MBM27C256A-25-W 250 ns max.**
- **Single +5V operation**
- **Standard 28-pin DIP package/32-pad LCC**

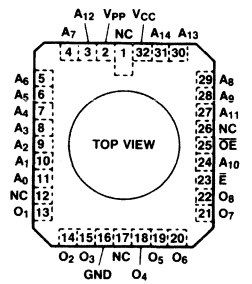
MBM27C256A Block Diagram and Pin Assignments



C256-3



C256-4



C256-5

Absolute Maximum Ratings
(See Note)

Parameter	Symbol	Value	Unit
Temperature under bias	T_{BIAS}	−65 to +125	°C
Storage temperature	T_{STG}	−65 to +150	°C
Inputs/outputs with respect to GND	V_{IN}, V_{OUT}	−0.6 to +7	V
Voltage on A_9 with respect to GND	V_{A9}	−0.6 to +13.5	V
V_{PP} with respect to GND	V_{PP}	−0.6 to +14	V
V_{CC} with respect to GND	V_{CC}	−0.6 to +7	V

Note:

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. It is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Functions and Pin Connections

Function (Pin No.) / Mode	Address Input (2~10, 21, 23~27)	A_9 (24)	Data I/O (11~13, 15~19)	$\overline{E}$ (20)	$\overline{OE}$ (22)	V_{CC} (28)	V_{PP} (1)	GND (14)
Read	A_{IN}	A_{IN}	OUT	V_{IL}	V_{IL}	+5V	+5V	GND
Output disable	A_{IN}	A_{IN}	High Z	V_{IL}	V_{IH}	+5V	+5V	GND
Stand by	Don't care	Don't care	High Z	V_{IH}	Don't care	+5V	+5V	GND
Program	A_{IN}	A_{IN}	IN	V_{IL}	V_{IH}	+6V	+12.5V	GND
Program verify	A_{IN}	A_{IN}	OUT	V_{IL}	V_{IL}	+6V	+12.5V	GND
Program inhibit	Don't care	Don't care	High Z	V_{IH}	Don't care	+6V	+12.5V	GND
Electronic signature	A_{IN}	+12V	Code	V_{IL}	V_{IL}	+5V	+5V	GND

Recommended Operating Conditions
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
V_{CC} supply voltage (1)	V_{CC}	4.5	5.0	5.5	V	−55°C to +125°C
V_{PP} supply voltage	V_{PP}	$V_{CC}-0.6$		$V_{CC}+0.6$	V	
Input high voltage	V_{IH}	2.0		$V_{CC}+0.3$	V	
Input low voltage	V_{IL}	−0.1		0.8	V	

Note:
1. V_{CC} must be applied either before or coincident with V_{PP} and removed either after or coincident with V_{PP}.

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance (V_{IN} = 0V)	C_{IN}		4	6	pF
Output capacitance (V_{OUT} = 0V)	C_{OUT}		8	12	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Input load current (V_{IN} = 5.5V)	I_{LI}			10	μA
Output leakage current (V_{OUT} = 5.5V)	I_{LO}			10	μA
V_{PP} supply current	I_{PP}		1	100	μA
V_{CC} standby current ($\overline{E}$ = V_{IH})	I_{SB1}			1	mA
V_{CC} standby current ($\overline{E}$ = $V_{CC}-0.3$V to $V_{CC}+0.3$V, I_{OUT} = 0 mA)	I_{SB2}		1	100	μA
V_{CC} active current ($\overline{E}$ = V_{IL})	I_{CC1}			30	mA
V_{CC} operation current (f = 4 MHz, I_{OUT} = 0 mA)	I_{CC2}			30	mA
Output low voltage (I_{OL} = 2.1 mA)	V_{OL}			0.45	V
Output high voltage (I_{OH} = −400 μA)	V_{OH1}	2.4			V
Output high voltage (I_{OH} = −100 μA)	V_{OH2}	$V_{CC}-0.7$			V

AC Characteristics

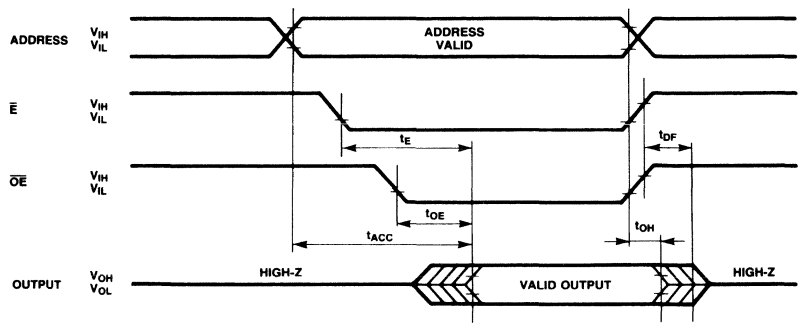
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MBM27C256A-20 Min	MBM27C256A-20 Max	MBM27C256A-25 Min	MBM27C256A-25 Max	Unit
Address access time (1) ($\overline{E} = \overline{OE} = V_{IL}$)	t_{ACC}		200		250	ns
$\overline{E}$ to output valid ($\overline{OE} = V_{IL}$)	t_E		200		250	ns
$\overline{OE}$ to output valid ($\overline{E} = V_{IL}$) (1)	t_{OE}		75		100	ns
$\overline{OE}$, $\overline{E}$ high to output float (2, 3)	t_{DF}	0	60	0	60	ns
Address to output hold (3)	t_{OH}	0		0		ns

Notes:

1. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the following edge of $\overline{E}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$, $\overline{E}$, whichever occurs first. Output float is defined as the point where data is no longer driven.
3. Sampling, not 100% tested.

Operation Timing Diagram

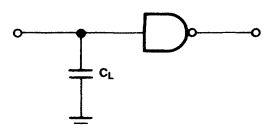


C256-6

AC Test Conditions

(Including programming)

Input Pulse Levels: .....0.45V to 2.4V
Input Rise and Fall Time: .....≤20 ns
Timing Measurement Reference Levels: 1.0V and 2.0V for inputs
0.8V and 2.0V for outputs
Output Load: .....1 TTL gate and C_L = 100 pF



C256-7

Programming/Erasing Information

Memory Cell Description

The MBM27C256A-W is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate as shown in Memory Cell diagram. The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold as shown in Memory Cell Threshold Shift diagram. In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line as shown in Memory Cell Threshold Shift diagram.

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27C256A-W has all 262,144-bits in the "1", or high, state. "0's" are loaded into the MBM27C256A-W through the procedure of programming.

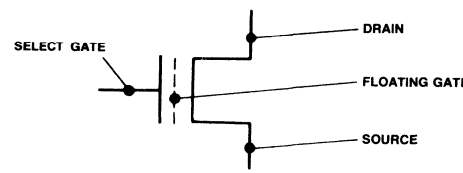
The MBM27C256A-W is programmed with a fast programming algorithm designed by Fujitsu called Quick Pro™. The programming mode is entered when +12.5V and +6V are applied to the V_{PP} pin and V_{CC} pin respectively, and $\overline{E}$ and $\overline{OE}$ are at V_{IH}. A 0.1 μF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. The 8-bit pattern is placed on the respective output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a sequence of single TTL low-level pulses are applied to the $\overline{E}$ pin followed by an additional pulse to the $\overline{E}$ pin to accomplish the programming.

Procedure of Quick Pro™ (Refer to the attached flow chart.)

1) Input the start address (start address = G).
2) Set V_{CC} = 6V, V_{PP} = 12.5V and $\overline{E}$ = V_{IH}.
3) Clear the programming pulse counter (X ← 0).
4) Input data to respective pins.
5) Apply ONE programming pulse (t_{PW} = 1 ms Typ.) to $\overline{E}$.
6) Increment the counter (X ← X + 1).
7) Compare the number (= X) of applied programming pulse with 25 and then verify the programmed data. If the programmed data is verified, go to the next step regardless of X value. If X = 25 and programmed data is not verified, the device fails.
8) Apply one additional wide programming pulse to $\overline{E}$ (3X ms).
9) Compare the address with an end address (= N). If the programmed address is the end address, proceed to the next step. If not, increment the address (G ← G + 1) and then go to the step 3) for the next address.
10) Set V_{CC} = V_{PP} = 5V.
11) Verify all the data. If the programmed data is not the same as the input data, the part failed. If it is the same, the program is completed.

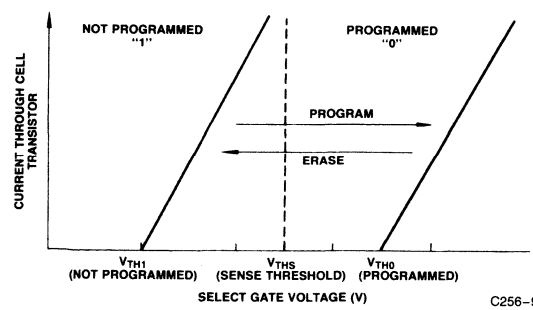
A continuous TTL low level should not apply to $\overline{CE}$ input pin during the program mode (V_{PP} = 12.5V, V_{CC} = 6V and $\overline{OE}$ = V_{IH}) because it is required that one programming pulse width does not exceed 78.75 ms at each address.

Memory Cell



C256-8

Memory Cell Threshold Shift



C256-9

Quick Pro™ is a trademark of Fujitsu Limited.

Programming/Erasing Information (Continued)

Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the MBM27C256A-W to an ultraviolet light source. A dosage of 15W-seconds/cm^2 is required to completely erase an MBM27C256A-W. This dosage can be obtained by exposure to an ultraviolet lamp (wavelength of 2537 Angstroms (Å) with intensity of 12,000 μW/cm^2) for 15 to 20 minutes. The MBM27C256A-W should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM27C256A-W and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless, the exposure to fluorescent light and sunlight will eventually erase the MBM27C256A-W and such exposure should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

AC Characteristics

(T_A = 25°C ± 5°C,
V_{CC} = 6V ± 0.25V,
V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	2			μs
Chip enable setup time	t_{CES}	2			μs
Output enable setup time	t_{OES}	2			μs
Data setup time	t_{DS}	2			μs
V_{PP} setup time	t_{VS}	2			μs
Address hold time	t_{AH}	2			μs
Output enable hold time (1)	t_{OEH}	2			μs
Data hold time	t_{DH}	2			μs
Output enable recovery time (1)	t_{OR}	2			μs
Chip enable to data valid	t_{DV}			1	μs
Output disable to output float delay	t_{DF}			105	ns
Programming pulse width	t_{PW}	0.95	1	1.05	ms
Additional programming pulse width	t_{APW}	2.85		78.75	ms
Programming pulse number	X	1		25	times

Note:

1. $t_{OEH} + t_{OR} \geq 50\ \mu s$.

Electronic Signature

The MBM27C256A-W has electronic signature mode which is intended to be used with programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm.

The electronic signature is activated when +12V is applied to address line A_9 (pin 24) of the MBM27C256A-W. Two identifier bytes are read out from the outputs by toggling address line A_0 (pin 10) from V_{IL} to V_{IH}. The address lines from A_1 and A_{13} must be held at V_{IL} to keep the electronic signature mode. See the table below.

A_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	Definition
V_{IL}	0	0	1	0	0	0	0	0	Manufacture
V_{IH}	0	1	0	0	0	1	1	0	Device

Notes:

A_9 = 12V ± 0.5V.
A_1 thru A_8 = A_{10} thru A_{13} = $\overline{CE}$ = $\overline{OE}$ = V_{IL}.
A_{14} = Either V_{IL} or V_{IH}.

Programming/Erasing Information (Continued)

DC Characteristics
(T_A = 25°C ± 5°C,
V_{CC} = 6V ± 0.25V,
V_{PP} = 21V ± 0.5V)

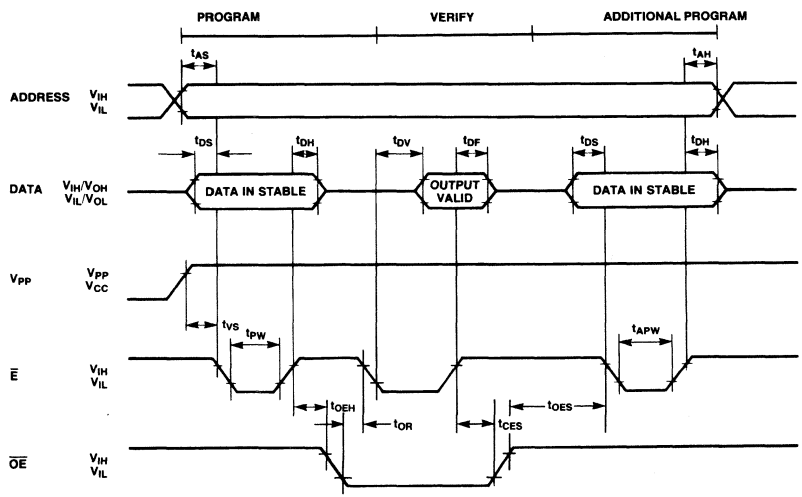
Parameter	Symbol	Min	Typ	Max	Unit
Input leakage current (V_{IN} = 5.25V/0.45V)	I_{LI}			10	μA
V_{PP} supply current during programming pulse ($\overline{E}$ = V_{IL})	I_{PP}			40	mA
V_{CC} supply current	I_{CC}			30	mA
Input low level	V_{IL}	−0.1		0.8	V
Input high level	V_{IH}	2.0		V_{CC} + 0.3	V
Output low voltage during verify (I_{OL} = 2.1 mA)	V_{OL}			0.45	V
Output high voltage during verify (I_{OH} = −400 μA)	V_{OH}	2.4			V

Notes:

V_{CC} must be applied either coincident with or before V_{PP} and removed either coincident with or after V_{PP}.

V_{PP} must not be greater than 21.5V including overshoot. Permanent device damage may occur if the device is taken out or put into socket with V_{PP} = 21V. Also, during $\overline{E}$ = V_{IL}, V_{PP} must not be switched from 5V to 21V or vice-versa.

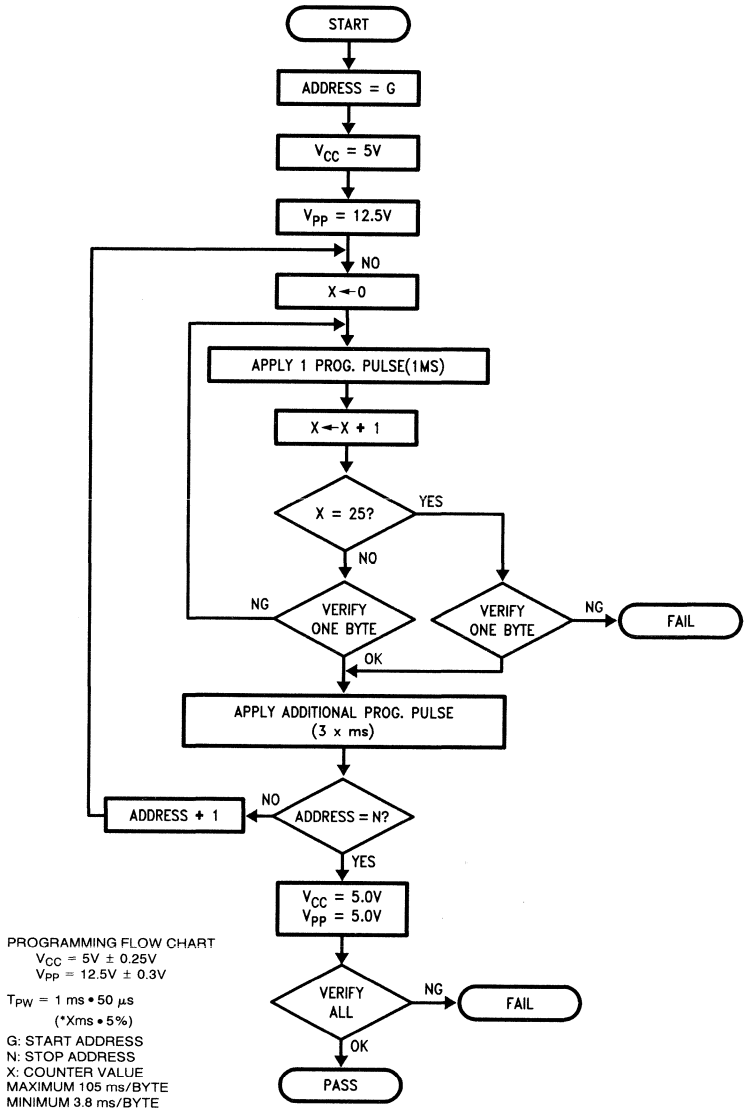
Programming Waveform



C256-10

Programming/Erasing Information (Continued)

Quick Program Flow Chart



PROGRAMMING FLOW CHART
V_{CC} = 5V ± 0.25V
V_{PP} = 12.5V ± 0.3V

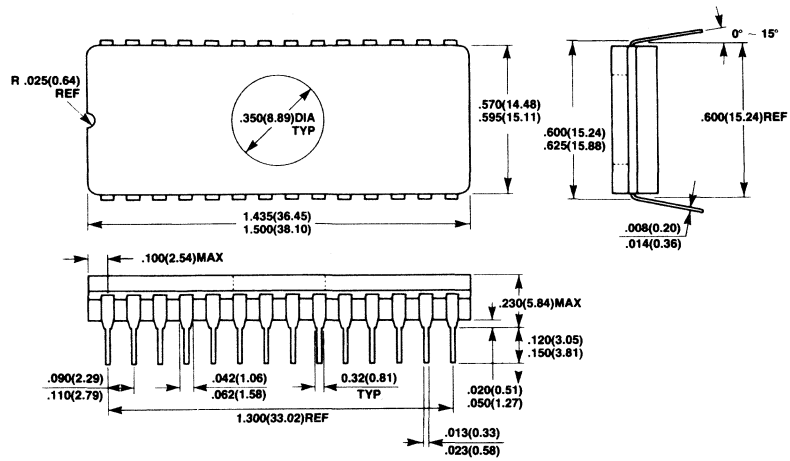
T_{PW} = 1 ms • 50 μs
(*Xms • 5%)

G: START ADDRESS
N: STOP ADDRESS
X: COUNTER VALUE
MAXIMUM 105 ms/BYTE
MINIMUM 3.8 ms/BYTE

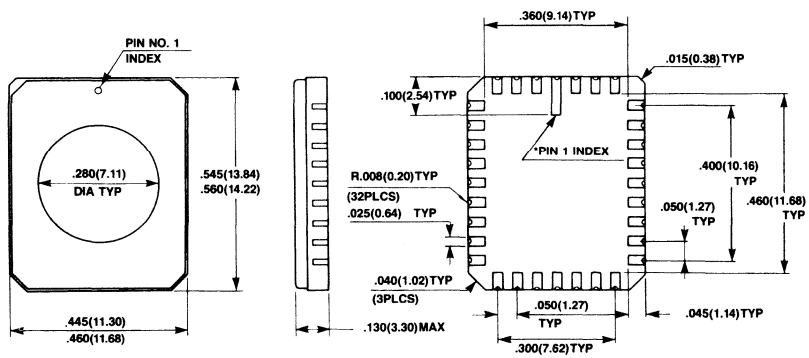
C256-11

Package Dimensions
Dimensions in inches
(millimeters)

28-Lead Ceramic (CERDIP with Transparent Lid)
Dual In-Line Package
(Case No.: DIP-28C-C01)



32-Pad Ceramic (Metal Seal) Leadless Chip Carrier
(Case No.: LCC-32C-A01)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE.

MBM27C512-25, MBM27C512-30

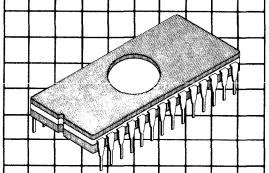
CMOS 524,288-Bit UV Erasable and Electrically Programmable Read Only Memory

Description

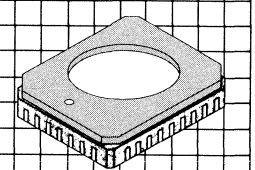
The Fujitsu MBM27C512 is a high speed 524,288-bit static complementary MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for application where rapid turn-around and/or-bit pattern experimentation, and low-power consumption are important.

A 28-pin dual-in line package with a transparent lid and 32-Pad Leadless Chip Carrier (LCC) are used to package the MBM27C512. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory-bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM27C512 is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 65,536 words by 8-bits for use in microprocessor application. Single +5V operation greatly facilitates its use in systems.



Ceramic Package
DIP-28C-C01



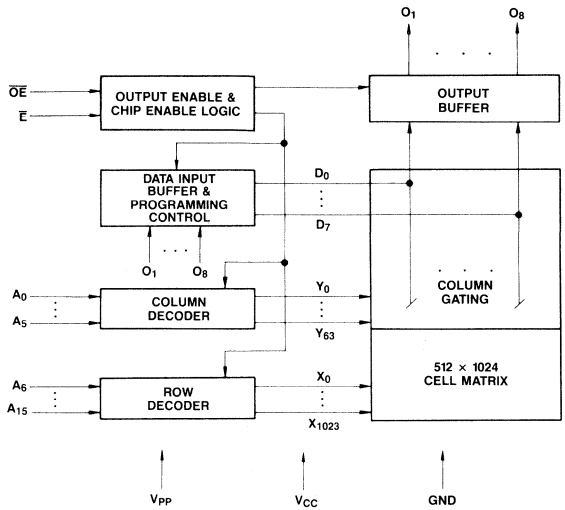
Ceramic Package
LCC-32C-A01

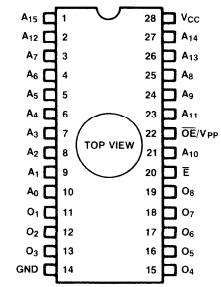
Features

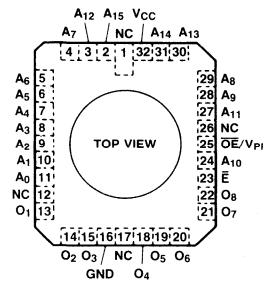
- **CMOS power consumption**
  Standby: 525 μW max.
  Active: 40 mW/MHz
- **65,536 words × 8-bits organization, fully decoded**
- **Single location programming**
- **Programmable utilizing the Quick Pro Algorithm**
- **VPP = 12.5V**
- **Programs with 1 ms pulses**
- **No clocks required (fully static operation)**
- **TTL compatible inputs/outputs**
- **Fast access time:**
  250 ns max. (MBM27C512-25)
  300 ns max. (MBM27C512-30)
- **Three-state output with OR-tie capability**
- **Output Enable ($\overline{OE}$) pin for simplified memory expansion**
- **Single +5V supply, ±5% tolerance**
- **Standard 28-pin DP package and 32-pad LCC**
- **Interchangeable with 27512-type device**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MBM27C512 Block Diagram and Pin Assignments







Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Temperature under Bias	T_{BIAS}	−25 to +85	°C
Storage Temperature	T_{STG}	−65 to +125	°C
All Inputs/Outputs Voltage with Respect to GND	V_{IN}, V_{OUT}	−0.6 to +7	V
Voltage on A_9 with Respect to GND	V_{A9}	−0.6 to 13.5	V
V_{PP} Voltage with Respect to GND	V_{PP}	−0.6 to +14	V
Supply Voltage with Respect to GND	V_{CC}	−0.6 to +7	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (V_{IN} = 0V, except $\overline{OE}/V_{PP}$)	C_{IN1}		4	6	pF
$\overline{OE}/V_{PP}$ Input Capacitance (V_{IN} = 0V)	C_{IN2}			20	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}		8	12	pF

Functions and Pin Connections

Mode	Function (Pin No.) Address Input (1 ~ 10, 21, 23 ~ 27)	Data I/O (11 ~ 13, 15 ~ 19)	$\overline{E}$ (20)	$\overline{OE}/V_{PP}$ (22)	V_{CC} (28)	GND (14)
Read	A_{IN}	OUT	V_{IL}	V_{IL}	5V	GND
Output Disable	A_{IN}	High-Z	V_{IL}	V_{IH}	5V	GND
Standby	Don't Care	High-Z	V_{IH}	Don't Care	5V	GND
Program	A_{IN}	IN	V_{IL}	12.5V	6V	GND
Program Verify	A_{IN}	OUT	V_{IL}	V_{IL}	6V	GND
Program Inhibit	Don't Care	High-Z	V_{IH}	12.5V	6V	GND

Recommended Operating Conditions
(Referenced to GND)

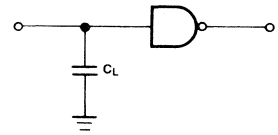
Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input High Voltage	V_{IH}	2.0		V_{CC} +0.3	V
Input Low Voltage	V_{IL}	−0.1		0.8	V
Operating Temperature	T_A	0		70	°C

DC Characteristics
(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Unit
Input Load Current (V_{IN} = 5.25V)	I_{LI}			10	μA
Output Leakage Current (V_{OUT} = 5.25V)	I_{LO}			10	μA
V_{CC} Standby Current ($\overline{E}$ = V_{IH})	I_{SB1}			1	mA
V_{CC} Standby Current ($\overline{E}$ = V_{CC} ±0.3V, I_{OUT} = 0 mA)	I_{SB2}		1	100	μA
V_{CC} Active Current ($\overline{E}$ = V_{IL})	I_{CC1}			30	mA
V_{CC} Operation Current (f = 4 MHz, I_{OUT} = 0 mA)	I_{CC2}			30	V
Output Low Voltage (I_{OL} = 2.1 mA)	V_{OL}			0.45	V
Output High Voltage (I_{OH} = −400 μA)	V_{OH1}	2.4			V
Output High Voltage (I_{OH} = −100 μA)	V_{OH2}	V_{CC} −0.7			V

AC Test Conditions
(including programming)

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Times:	≤20 ns
Timing Measurement Reference Levels:	0.8V and 2.0V for inputs 0.8V and 2.0V for outputs
Output Load:	1 TTL gate and C_L = 100 pF

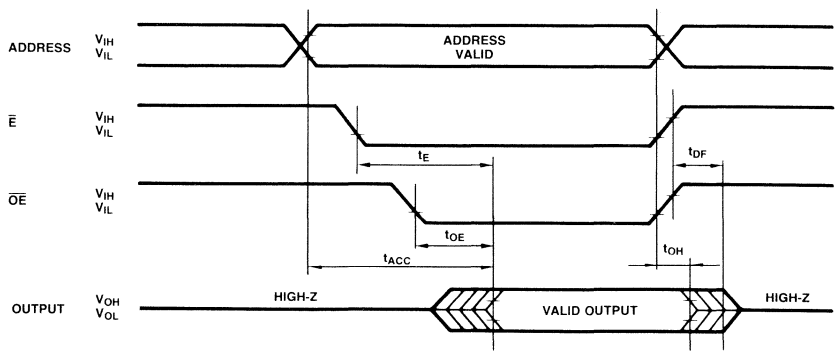


AC Characteristics
(Recommended operating conditions unless otherwise noted)

Parameter	Symbol	MBM27C512-25 Min	MBM27C512-25 Typ	MBM27C512-25 Max	MBM272C512-30 Min	MBM272C512-30 Typ	MBM272C512-30 Max
Address Access Time*1 (E = OE = V_{IL})	t_{ACC}			250			300
E to Output Delay (OE = V_{IL})	t_E			250			300
OE to Output Delay*1 (E = V_{IL})	t_{OE}			100			120
Address to Output Hold	t_{OH}	0			0		
OE, E High to Output Float*2	t_{DF}	0		60	0		105

Notes: *1 OE may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{E}$ without impact on t_{ACC}.
*2 t_{DF} is specified from OE or $\overline{E}$, whichever occurs first. Output Float is defined as the point where data is no longer driven.

Operation Timing Diagram
(including programming)

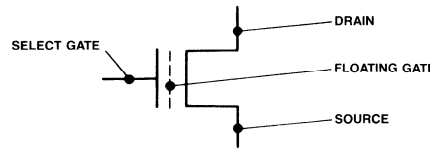


Programming/Erasing Information

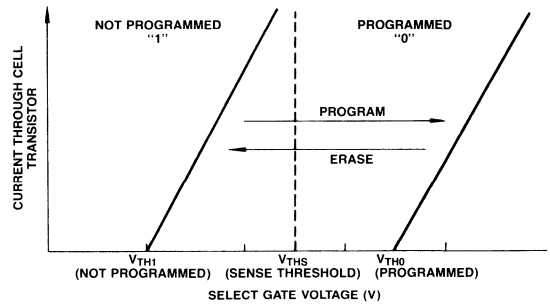
Memory Cell Description

The MBM27C512 is fabricated using a single-transistor stacked gate cell construction, implemented via double-layer polysilicon technology. The individual cells consist of a bottom floating gate and a top select gate (see Memory Cell diagram). The top gate is connected to the row decorder, while the floating gate is used for charge storage. The cell is programmed by the injection of high energy electrons through the oxide and onto the floating gate. The presence of the charge on the floating gate causes a shift in the cell threshold (refer to Memory Cell Threshold Shift). In the initial state, the cell has a low threshold (V_{TH1}) which will enable the transistor to be turned on when the cell is selected (via the top select gate). Programming shifts the threshold to a higher level (V_{TH0}), thus preventing the cell transistor from turning on when selected. The status of the cell (i.e., whether programmed or not) can be determined by examining its state at the sense threshold (V_{THS}), as indicated by the dotted line in Figure 4.

Memory Cell



Memory Cell Threshold Shift



Programming

Upon delivery from Fujitsu, or after each erasure (see Erasure section), the MBM27C512 has all 524,288-bits in the "1", or high, state. "0's" are loaded into the MBM27C512 through the procedure of programming.

The MBM27C512 is programmed with a fast programming algorithm designed by Fujitsu, called Quick Pro™. The programming mode is entered when +12.5V and +6V are applied to the $\overline{OE}/V_{PP}$ pin and V_{CC} pin respectively and $\overline{E}$ is V_{IH}. A 0.1 μF capacitor between $\overline{OE}/V_{PP}$ Pin and GND Pin is needed to prevent excessive voltage transients which could damage the device. The address to be programmed is applied to the proper address pins. The 8-bit pattern is placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and the data are stable, a sequence of 1 ms TTL low-level pulse is applied to the $\overline{E}$ pin and after that, an additional pulse is applied to the $\overline{E}$ pin to accomplish the programming. Refer to the attached flow chart.

Procedure of Quick Pro™ (Refer to the attached flowchart.)

1) Input the start address (=G).
2) Set V_{CC} = 6V, V_{PP} = 12.5V.
3) Clear the programming pulse counter (X← 0).
4) Apply ONE programming pulse (t_{PW} = 1 ms Typ.) to $\overline{E}$.
5) Increment the counter (X←X+1).
6) Compare the number (=X) of applied programming pulse with 20. If X = 25, go to step 8). If X < 25, proceed to next step.
7) Verify the data. If programmed data is the same as input data, proceed to next step. If not, go back to step 6).
8) Apply the additional programming pulse (3 x ms).
9) Compare the address with an end address (=N). If the programmed address is the end address, proceed to next step. If not, increment the address (G← G+1) and then go to step 3) for the next address.
10) Verify the all programmed data. If the programmed data are the same as original data, programming was successful.

A continuous TTL low level should not apply to $\overline{E}$ input pin during the program mode because it is required that one programming pulse width does not exceed 78.75 msec at each address.

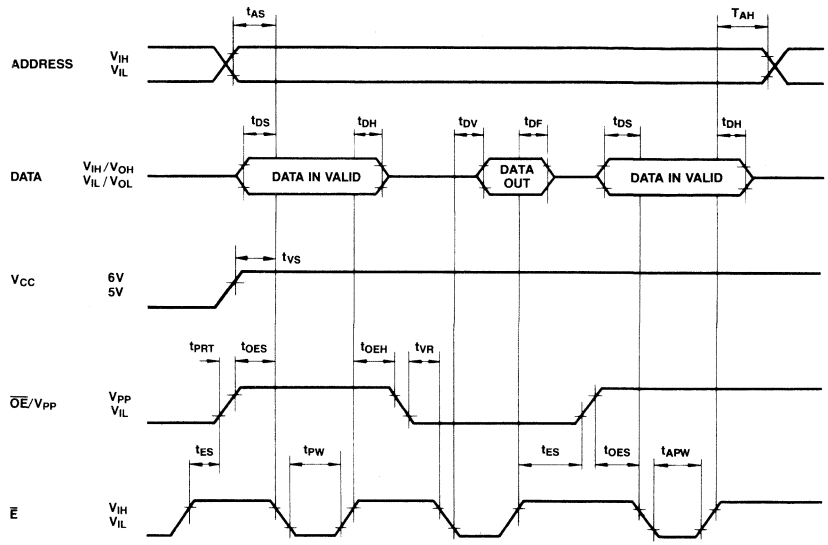
Programming/Erasing Information
(Continued)

Erasure

In order to clear all locations of their programmed contents, it is necessary to expose the MBM27C512 to an ultra-violet light source. A dosage of 15 W-seconds/cm^2 is required to completely erase an MBM27C512. This dosage can be obtained by exposure to an ultra-violet lamp (wavelength of 2537 Angstroms (Å)) with intensity of 12000 μW/m^2 for 15 to 20 minutes. The MBM27C512 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the MBM27C512 and similar devices will erase with light sources having wavelengths shorter than 4000Å. Although erasure time will be much longer than with UV source at 2537Å, nevertheless the exposure to fluorescent light or sunlight will eventually erase the MBM27C512, and such exposure should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

Programming Waveform



DC Characteristics
(T_A = 25±5°C, V_{CC}*1 = 5V±5%, V_{PP}*2 = 12.5±0.3 V)

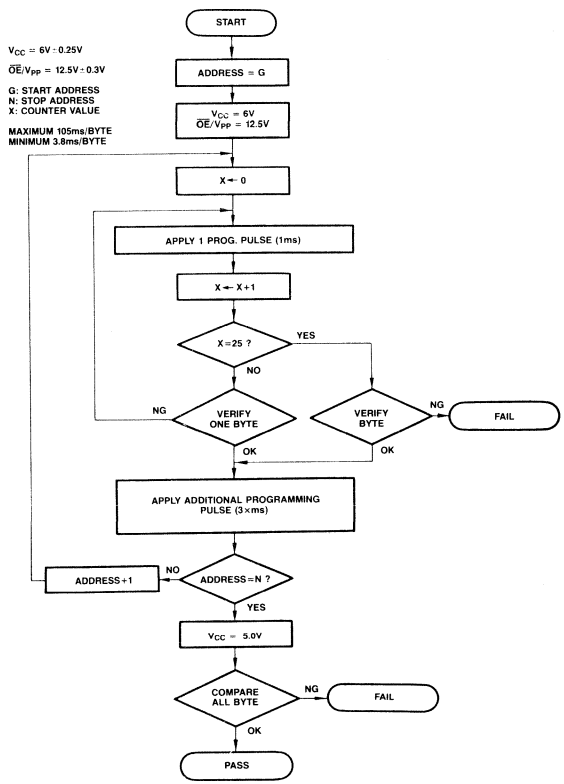
Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IN} = 5.25 V/0.45 V)	I_{LI}			10	μA
V_{PP} Supply Current During Programming Pulse ($\overline{E}$ = V_{IL})	I_{PP}			50	mA
V_{CC} Supply Current	I_{CC}			30	mA
Input Low Level	V_{IL}	−0.1		0.8	V
Input High Level	V_{IH}	2.0		V_{CC} + 0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1 mA)	V_{OL}			0.45	V
Output High Voltage During Verify (I_{OH} = −400 μA)	V_{OH}	2.4			V

Note: *1 V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.
*2 V_{PP} must not be greater than 14 volts including overshoot. Permanent device damage may occur if the device is taken out of or put into a socket with V_{PP} = 12.5 volts. Also, during $\overline{E}$ = V_{IL}, V_{PP} must not be switched from 5 to 12.5 volts or vice-versa.

AC Characteristics
(T_A = 25±5°C,
V_{CC} = 6V±0.25V,
V_{PP} = 12.5V±0.3V)

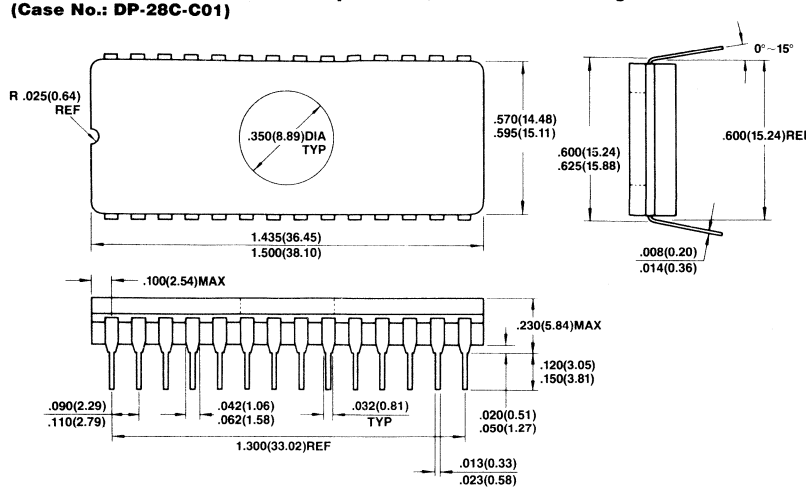
Parameter	Symbol	Min	Typ	Max	Unit
Address Setup Time	t_{AS}	2			μs
Chip Enable Setup Time	t_{ES}	2			μs
Output Enable Setup Time	t_{OES}	2			μs
Data Setup Time	t_{DS}	2			μs
V_{CC} Setup Time	t_{VS}	2			μs
Address Hold Time	t_{AH}	2			μs
Data Hold Time	t_{DH}	2			μs
Output Enable Hold Time	t_{OEH}	2			μs
V_{PP} Recovery Time	t_{VR}	2			μs
Chip Enable to Data Valid	t_{DV}			1	μs
Output Disable to Output Float Delay	t_{DF}	0		130	ns
V_{PP} Program Pulse Rise Time	t_{PRT}	50			ns
Programming Pulse Width	t_{PW}	0.95	1	1.05	ms
Additional Programming Pulse Width	t_{APW}	2.85	3	78.75	ms

Programming Flow Chart

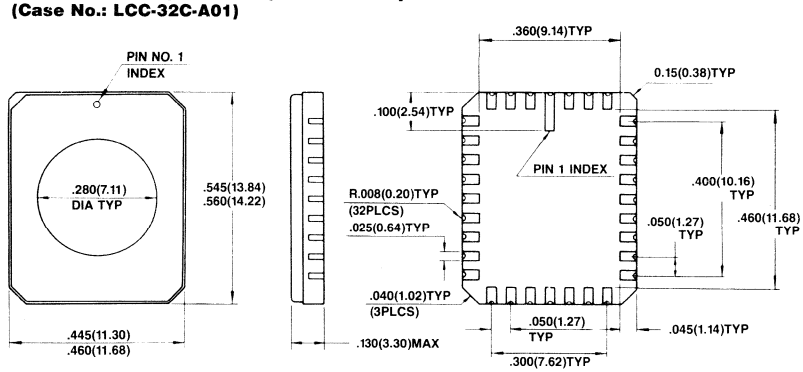


Package Dimensions
Dimensions in inches
(millimeters)

28-Lead Ceramic (ERDP with Transparent lid) Dual In-Line Package (Case No.: DP-28C-C01)



32-Pad Ceramic (Metal Seal) Leadless Chip Carrier (Case No.: LCC-32C-A01)



*Shape of Pin index: Subject to change without notice

Advanced Information

MOS Memories

FUJITSU

■ MBM27C1001-20, MBM27C1001-25

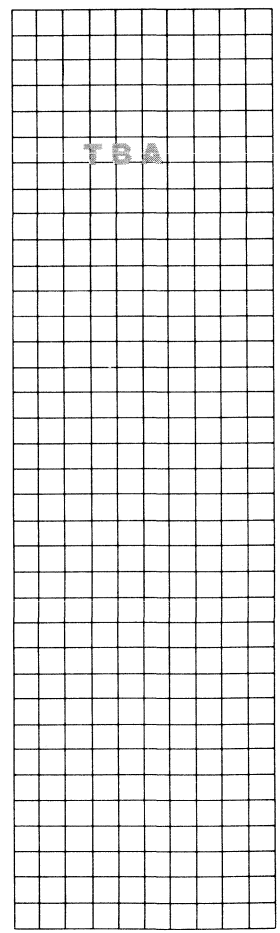
CMOS 1,048,576-Bit UV Erasable
Read Only Memory

Description

The Fujitsu MBM27C1001 is a high speed 1,048,576-bits complementary MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

A 32-pin dual-in line package with a transparent lid is used to package the MBM27C1001. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM27C1001 is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 131,072 words by 8-bits for use in microprocessor applications.

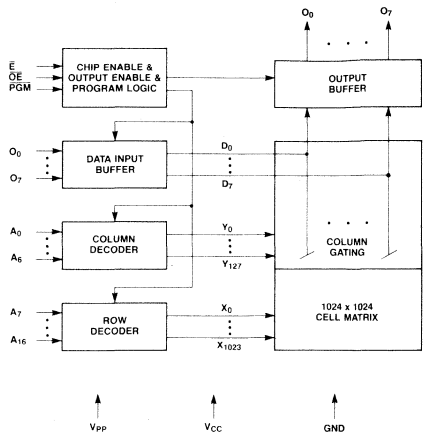


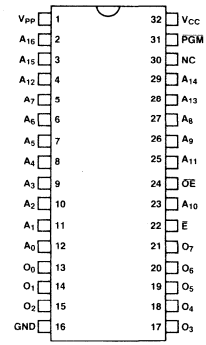
Features

- **131,072 words x 8-bit organization, fully decoded**
- **Four words programming**
- **Programmable utilizing the Quick Pro™ algorithm**
- **Programming voltage: 12.5V**
- **Low power consumption: 42 mW/MHz max. (Active) 550 μW max. (Standby)**
- **No clocks required (fully static operation)**
- **TTL compatible inputs/outputs**
- **Three-State output for wired-OR capability**
- **Output Enable pin for simplified memory expansion**
- **Single +5V supply, ±10%tolerance**
- **Fast access time: 200 ns max. (MBM27C1001-20) 250 ns max. (MBM27C1001-25)**
- **32-pin Ceramic (Cerdip) DIP package**

Mask Rom Comp

MBM27C1001 Block Diagram and Pin Assignment

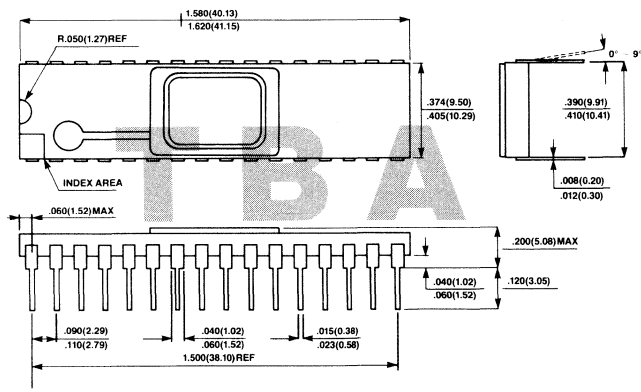




Package Dimensions

Dimensions in inches (millimeters)

32-Lead Ceramic (Cerdip with Transparent Lid) Dual In-Line Package



MBM27C1024-20, MBM27C1024-25

CMOS 1,048,576-Bit UV Erasable Read Only Memory

Description

The Fujitsu MBM27C1024 is a high speed 1,048,576-bits complementary MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

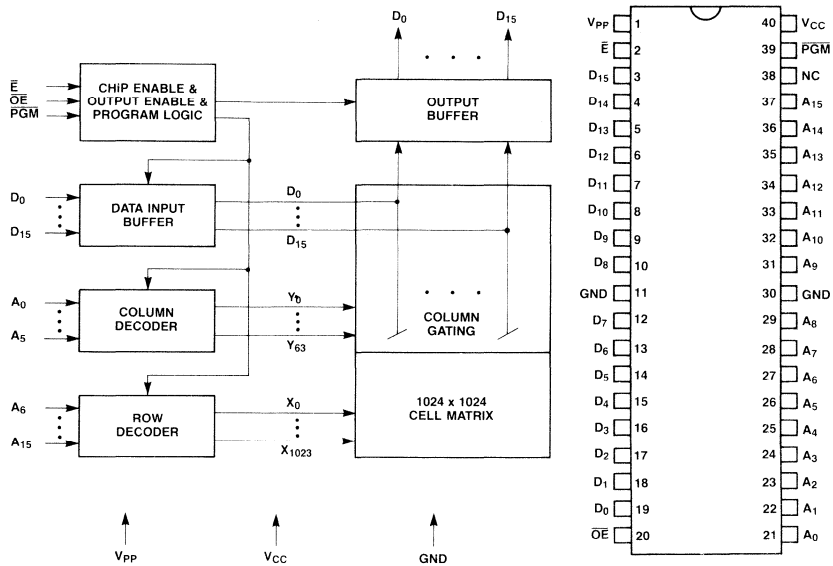
A 40-pin dual-in line package with a transparent lid and 44-pad leadless chip carrier (LCC) are used to package the MBM27C1024. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM27C1024 is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 65,536 words by 16-bits for use in microprocessor applications. Single +5V operation greatly facilitates its use in systems.

Features

- **65,536 words x 16-bit organization, fully decoded**
- **Single location programming**
- **Programmable utilizing the Quick Pro™ algorithm**
- **Programming voltage: 12.5V**
- **Low power consumption: 42 mW/MHz max. (Active) 550 μW max. (Standby)**
- **No clocks required (fully static operation)**
- **TTL compatible inputs/outputs**
- **Three-State output for wired-OR capability**
- **Output Enable pin for simplified memory expansion**
- **Single +5V supply, ±10% tolerance**
- **Fast access time: 200 ns max. (MBM27C1024-20) 250 ns max. (MBM27C1024-25)**
- **JEDEC approved pin assignment**
- **40-pin Ceramic (Cerdip) DIP package /44-pad Ceramic LCC**

MBM27C1024 Block Diagram and Pin Assignment



Advanced Information

FUJITSU

MBM27C1028-15, MBM27C1028-20, MBM27C1028-25

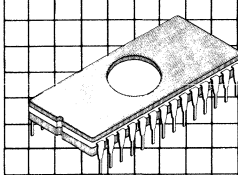
CMOS 1,048,576-Bit UV
Erasable Read Only Memory

Description

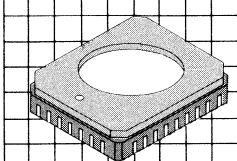
The Fujitsu MBM27C1028 is a high speed 1,048,576-bits complementary MOS erasable and electrically reprogrammable read only memory (EPROM). It is especially well suited for application where rapid turn-around and/or bit pattern experimentation, and low-power consumption are important.

Multiplexed address and data pin permit the MBM27C1028 to be housed in a 28-pin dual-in-line package and 32-pad LCC. The transparent lid allows the user to expose the device to ultraviolet light in order to erase the memory bit pattern previously programmed. At the completion of erasure, a new pattern can then be written into the memory.

The MBM27C1028 is fabricated using CMOS double polysilicon gate technology with single transistor stacked gate cells. It is organized as 65,536 words by 16-bits for use in the newer microprocessor applications.



Ceramic Package DIP-28C-C01

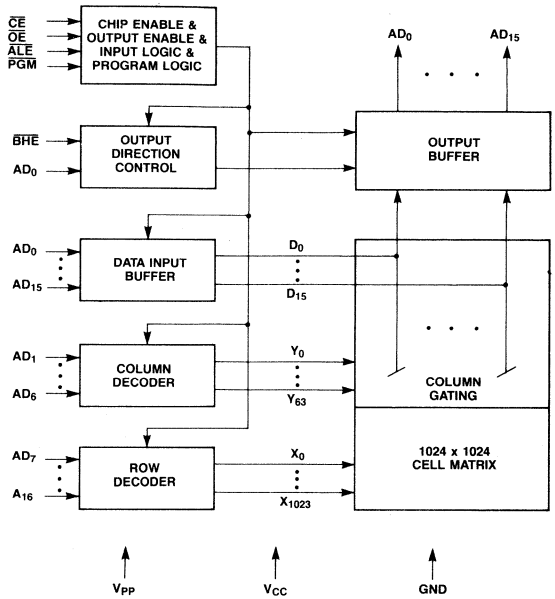


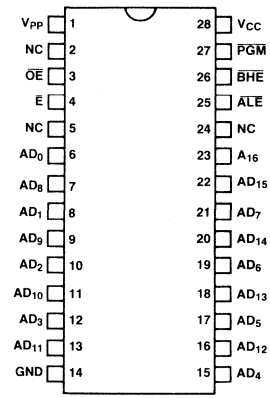
Ceramic Package LCC-32C-A01

Features

- **65,536 words x 16-bit organization, fully decoded**
- **Single location programming**
- **Programmable utilizing the Quick Pro™ algorithm**
- **Programming voltage: 12.5V**
- **Low power consumption**
  42 mW/MHz max. (Active)
  550 μW max. (Standby)
- **On-chip latches for addresses**
- **Output unlatched at read/programming cycle**
- **Provide electrical changeable control signal $\overline{BHE}$ and ADD pin (for word transfer or byte transfer upper half or lower half)**
- **TTL compatible inputs/outputs**
- **No interface is required to the MBL8086/MBL80186**
- **Single +5V supply, ±10% tolerance**
- **Fast access time:**
  200 ns max. (MBM27C1028-20)
  250 ns max. (MBM27C1028-25)
- **JEDEC approved pin assignment**
- **28-pin Ceramic (Cerdip) DIP package/32-pad Ceramic LCC**

MBM27C1028 Block Diagram and Pin Assignment





FUNCTIONAL TRUTH TABLE

	AD_0	A_1–A_{15}	A_{16}	$\overline{ALE}$	$\overline{BHE}$	$\overline{E}$	$\overline{OE}$	$\overline{PGM}$	V_{CC}	V_{PP}
STANDBY	HIGH-Z	HIGH-Z	X	X	X	V_{IH}	X	X	5V	5V
READ ADDRESS LATCH	*	A_{IN}	A_{IN}	↓	*	V_{IL}	V_{IH}	V_{IH}	5V	5V
READ	OUT*	OUT*	X	V_{IL}	X	V_{IL}	V_{IL}	V_{IH}	5V	5V
OUTPUT DISABLE	HIGH-Z	HIGH-Z	X	V_{IL}	X	V_{IL}	V_{IH} / X	X / V_{IL}	5V	5V
PROGRAM ADDRESS LATCH	V_{IL}	A_{IN}	A_{IN}	↓	V_{IL}	V_{IL}	V_{IH}	V_{IH}	6V	12.5V
PROGRAM	IN	IN	X	V_{IL}	X	V_{IL}	V_{IH}	V_{IL}	6V	12.5V
PROGRAM VERIFY	OUT	OUT	X	V_{IL}	X	V_{IL}	V_{IL}	V_{IH}	6V	12.5V
PROGRAM INHIBIT	HIGH-Z	HIGH-Z	X	X	X	V_{IH}	X	X	6V	12.5V

X: Either V_{IL} or V_{IH}
A_{IN}: Address Input
IN: Data Input
OUT: Data Output

*OUTPUT TRUTH TABLE

AD_0	$\overline{BHE}$	AD_0–AD_7	AD_8–AD_{15}
V_{IL}	V_{IL}	D_0–D_7	D_8–D_{15}
V_{IL}	V_{IH}	D_0–D_7	HIGH-Z
V_{IH}	V_{IL}	HIGH-Z	D_8–D_{15}
V_{IH}	V_{IH}	HIGH-Z	HIGH-Z

Recommended Operating Conditions
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
input high level	V_{IH}	2.0		V_{CC} + 0.3	V
Input low level	V_{IL}	−0.1		0.8	V
Operating temperature	T_A	0		70	°C

DC Characteristics
(Recommended operating conditions unless otherwise noted)

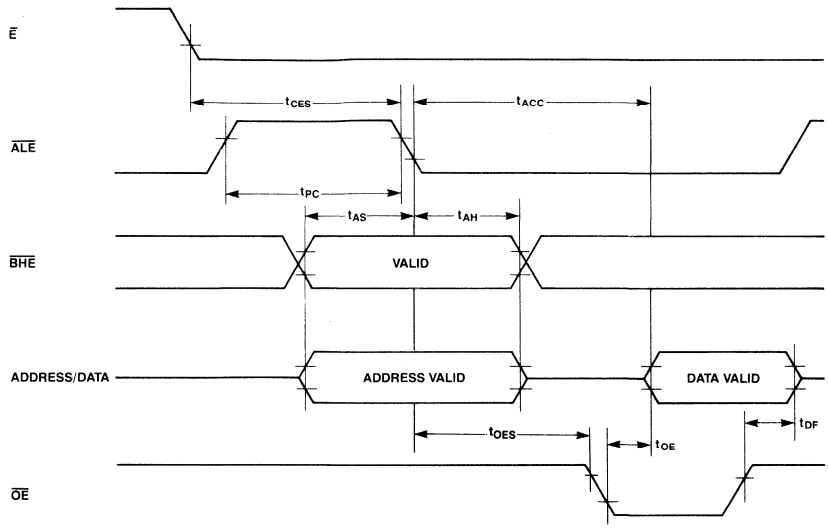
Parameter	Symbol	Min	Typ	Max	Unit
Input high level leakage current	I_{LI}	−10		10	μA
Output leakage current	I_{LO}	−10		10	μA
V_{CC} standby current ($\overline{E}$ = TTL V_{IH})	I_{SB1}			1	mA
V_{CC} standby current ($\overline{E}$ = CMOS V_{IH})	I_{SB2}		1	100	μA
V_{CC} active current ($\overline{E}$ = V_{IL})	I_{CC1}			50	mA
V_{CC} operation current ($\overline{E}$ = V_{IL})	I_{CC2}			50	mA
V_{PP} supply current	I_{PP}		1	100	μA
Output low level (I_{OL} = 2.1 mA)	V_{OL}			0.45	V
Output high level (I_{OH} = −400 μA)	V_{OH1}	2.4			V
Output high level (I_{OH} = −100 μA)	V_{OH2}	V_{CC} − 0.7			V

AC Characteristics
(Recommended operating conditions unless otherwise noted)

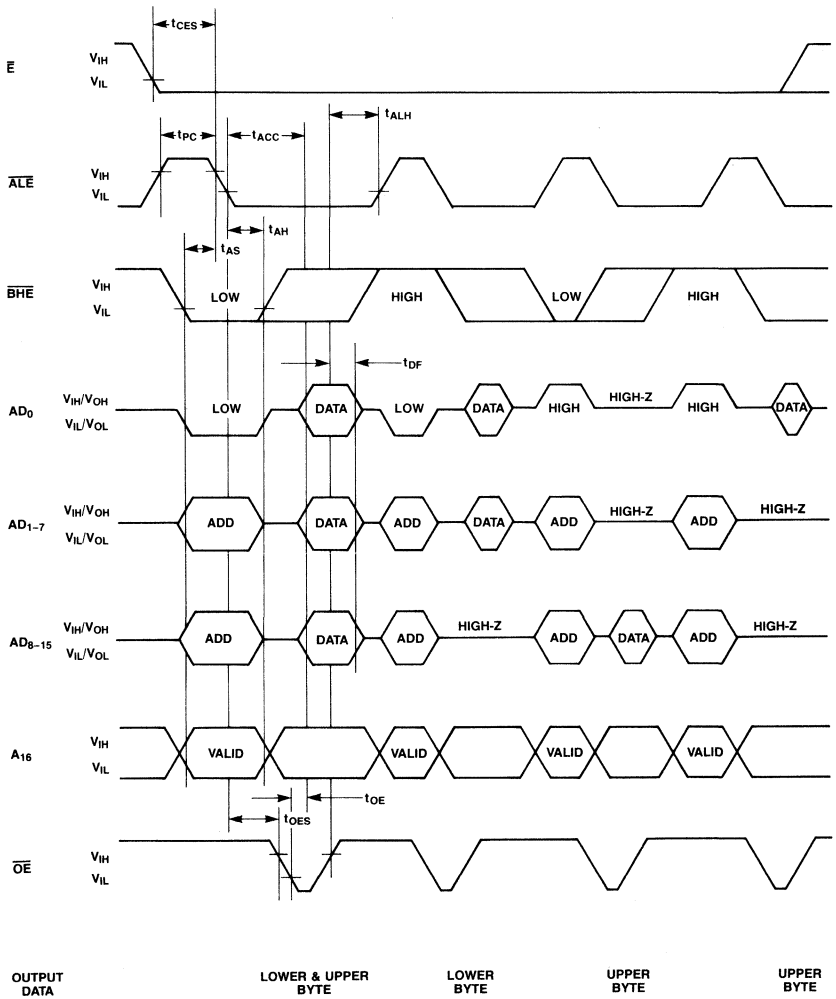
		MBM27C1028						
		-15		-20		-25		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
$\overline{ALE}$ active to output valid	t_{ACC}		150		200		250	ns
$\overline{ALE}$ precharge time	t_{PC}	60		75		100		ns
$\overline{ALE}$ setup time	t_{ALS}	0		0		0		ns
Address setup time	t_{AS}	20		25		30		ns
Address hold time	t_{AH}	20		25		30		ns
$\overline{E}$ setup time	t_{CES}	60		75		100		ns
$\overline{OE}$ to output valid*1	t_{OE}		60		70		100	ns
$\overline{OE}$ high to output float*2	t_{DF}		60		60		60	ns
$\overline{OE}$ setup time	t_{OES}	20		25		30		

Note: *2 Output float is defined as the point where data is no longer driven.

Read Waveform



Read Waveform



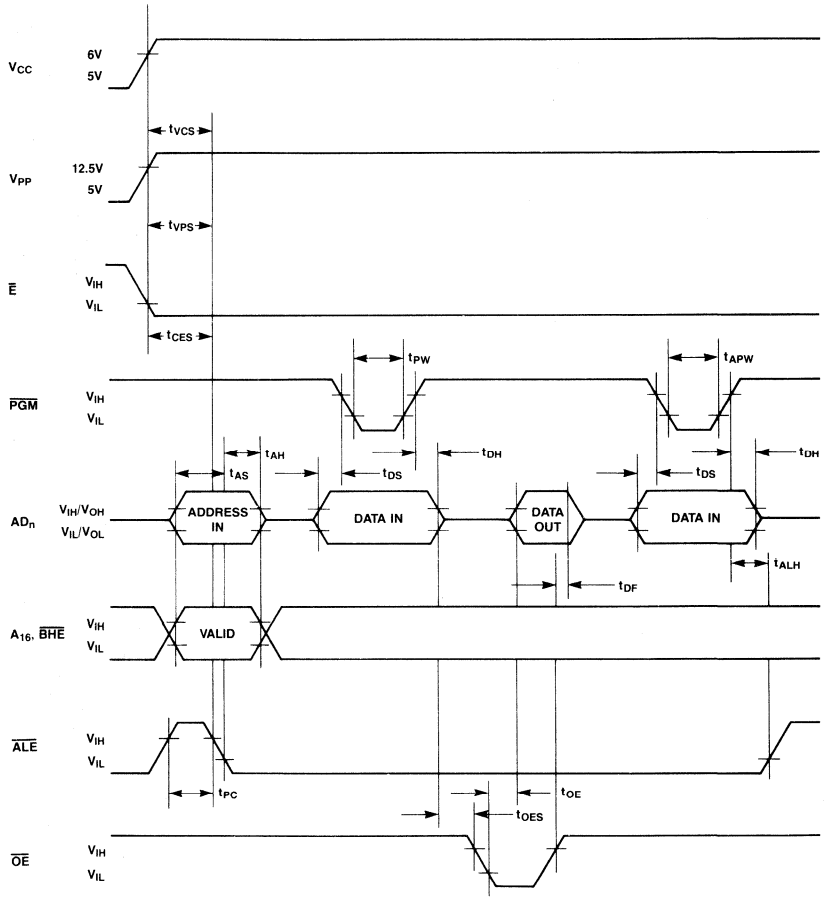
DC Characteristics During Programming
(T_A = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Min	Typ	Max	Unit
Input high level	V_{IH}	2.0		V_{CC} + 0.3	V
Input low level	V_{IL}	−0.1		0.8	V
Input load current	I_{LI}	−10		10	μA
V_{CC} supply current	I_{CC3}			50	mA
V_{PP} supply current	I_{PP2}			50	mA
Output low level (I_{OL} = 2.1 mA)	V_{OL}			0.45	V
Output high level (I_{OH} = −400 μA)	V_{OH}	2.4			V

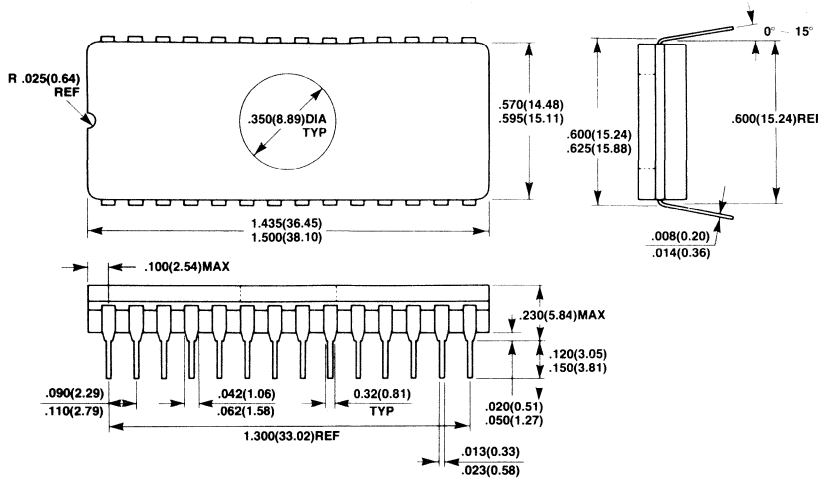
AC Characteristics During Programming

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} setup time	t_{VCS}	4			μs
V_{PP} setup time	t_{VPS}	4			μs
$\overline{E}$ setup time	t_{CES}	4			μs
Address setup time	t_{AS}	1			μs
Address hold time	t_{AH}	1			μs
$\overline{ALE}$ precharge time	t_{PC}	2			μs
$\overline{ALE}$ low hold time	t_{ALH}	2			μs
Data setup time	t_{DS}	2			μs
Data hold time	t_{DH}	2			μs
$\overline{OE}$ setup time	t_{OES}	2			μs
$\overline{OE}$ to output valid	t_{OE}			120	ns
$\overline{OE}$ to output float	t_{DF}			105	ns
Programming pulse width	t_{PW}	0.95	1.00	1.05	ms
Additional programming pulse number	n	1		25	times

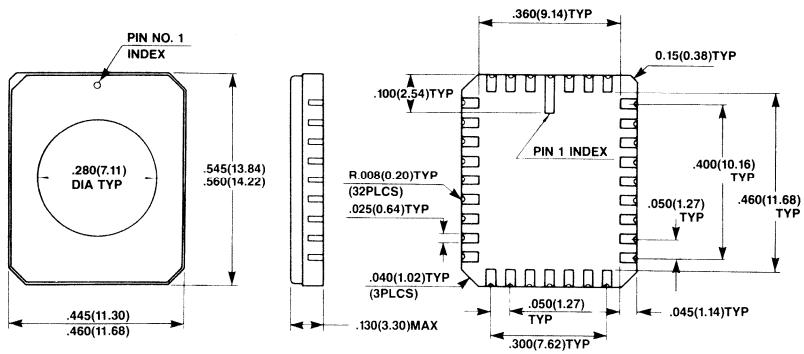
Programming Waveform



28-Lead Ceramic (Cerdip with Transparent Lid) Dual In-Line Package (Case No.: DIP-28C-C01)



32-Pad Ceramic (Metal Seal) Leadless Chip Carrier (Case No.: LCC-32C-A01)



*Shape of Pin index: Subject to change without notice

CMOS EEPROMs

MBM28C64 7-2
MBM28C65 7-10
MBM2212 7-18

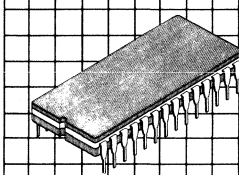
MBM28C64-25, MBM28C64-35

CMOS 65,536-Bit Electrically Erasable Read Only Memory

Description

The Fujitsu MBM28C64 is a 65,536-bit CMOS electrically erasable read-only memory (EE PROM). The MBM28C64 uses internally latched address, and data protection circuitry to protect against short write pulses and noise on $\overline{W}$. The device dissipates only 110 mW in the active mode and 550 μW in standby.

The MBM28C64 is ideal for a wide variety of applications which require non-volatility and in system data modification. The MBM28C64 is available in a 28-pin ceramic dual in-line package.

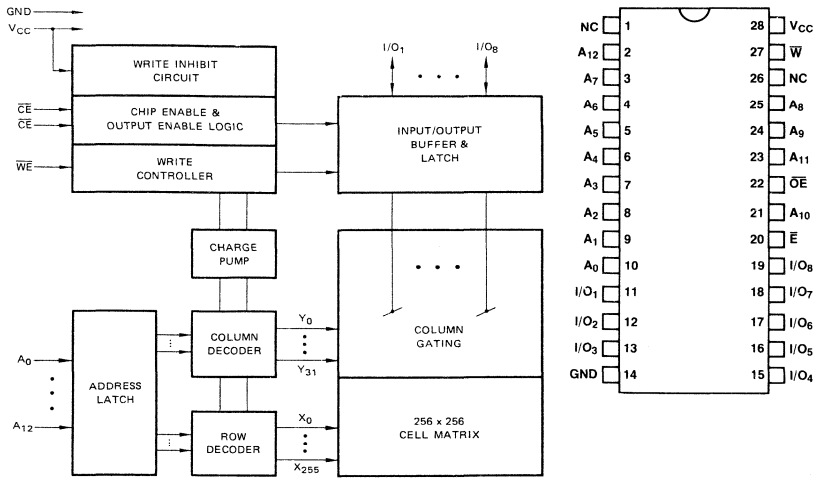


DIP-28C-C02

Features

- **8,192 words x 8-bit, fully decoded**
- **Internally latched address/data in writing**
- **Automatic Byte-Erase before Write**
- **Self-timed Byte Write**
- **Data protection against short write pulse and noise on W**
- **On chip data verification**
- **DATA POLLING**
- **Low power**
  Active: 165 mW
  Standby: 550 μW
- **Access time**
  250 ns max. (MBM28C64-25)
  350 ns max. (MBM28C64-35)
- **Chip erase capability**
- **TTL compatible input/output for fully MPU interface**
- **Three-state output for wired-OR capability**
- **Output enable (OE) for simplified memory expansion**
- **Single +5V supply, ±10%tolerance**
- **Minimum Endurance of 10000 Erase/Write cycle per Byte**
- **JEDEC approved pin out and package**

MBM28C64 Block Diagram and Pin Assignment



Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Supply voltage with respect to GND	V_{CC}	−0.3 to +7.0	V
All input/output voltage with respect to GND	V_{IN}, V_{OUT}	−0.3 to V_{CC} + 0.3	V
Voltage on A_9 with respect to GND	V_{A9}	−0.3 to +13.5	V
Voltage on $\overline{OE}$ with respect to GND	V_{OE}	−0.3 to + 15.5	V
Temperature under bias	T_{BIAS}	−25 to +85	°C
Storage temperature	T_{STG}	−65 to +125	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Function and Pin Connections

Function (Pin No.) / Mode	Address Input (2 to 10, 21, 23 to 25)	$\overline{E}$ (20)	$\overline{OE}$ (22)	$\overline{W}$ (27)	Data I/O (12 to 14, 16 to 20)	Power
Read	A_{IN}	V_{IL}	V_{IL}	V_{IH}	OUT	Active
Standby and write inhibit	Don't care	V_{IH}	Don't care	Don't care	High-Z	Standby
Write	A_{IN}	V_{IL}	V_{IH}	V_{IL}	IN	Write
$\overline{DATA}$ polling*	A_{IN}	V_{IL}	V_{IL}	V_{IH}	$I/O_8 = \overline{I8}$ I/O_1 to I/O_7 = High-Z	Write
					OUT	Active
Write inhibit	A_{IN}	Don't care	V_{IL} Don't care	Don't care V_{IH}	High-Z	Active
Chip erase	Don't care	V_{IL}	V_{OE}	V_{IL}	V_{IH}	Chip Erase

Note: * The address must be applied to the address. From then on all output data becomes input data from the point where the write mode is completed.
V_{OE}: 13.5V ±1.5V

Recommended Operating Conditions
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.0		V_{CC} +0.3	V
Input low voltage	V_{IL}	−0.1		0.8	V
Operating temperature	T_A	0		70	°C

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance (V_{IN} = 0V)	C_{IN}			10	pF
Output capacitance (V_{OUT} = 0V)	C_{OUT}			10	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol	Min	Max	Unit
Input leakage current	V_{IN} = 5.5V	I_{LI}	−10	10	μA
Output leakage current	V_{OUT} = 5.5V	I_{LO}	−10	10	μA
V_{CC} standby current	$\overline{CE} = V_{IH}$	I_{SB1}		1	mA
V_{CC} standby current	$\overline{CE} = V_{CC} \pm 0.3V$	I_{SB2}		100	μA
V_{CC} active current	$\overline{CE} = V_{IL}$	I_{CC1}		30	mA
V_{CC} active current	f = 4 MHz, I_{OUT} = 0 mA	I_{CC2}		30	mA
V_{CC} write current	$\overline{CE} = V_{IL}$, $\overline{WE} = V_{IL}$	I_{CCW}		30	mA
V_{CC} chip erase current	$\overline{CE} = \overline{WE} = V_{IL}$, $\overline{OE} = V_{OE}$	I_{CCE}		60	mA
Output low level	I_{OL} = 2.1 mA	V_{OL}		0.45	V
Output high level	I_{OH} = 400 μA	V_{OH}	2.4		V
Operation inhibit level		V_{INH}		3	V
Chip erase voltage		V_{OE}	12	15	V

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

		MBM28C64-25		MBM28C64-35		
Parameter	Symbol	Min	Max	Min	Max	Unit
Address access time	t_{ACC}		250		350	ns
$\overline{E}$ to output delay	t_E		250		350	ns
$\overline{OE}$ to output delay*1	t_{OE}		100		120	ns
$\overline{E}$, $\overline{OE}$ high to output float*2	t_{DF}		60		80	ns
$\overline{OE}$ high to output	t_{OH}	0		0		ns

Notes: *1 t_{OE} is specified the point where both t_{CE} and t_{ACC} settled.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{E}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

AC Characteristics (Byte Write)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	20			ns
Chip enable setup time	t_{CS}	20			ns
Output enable setup time	t_{OES}	20			ns
Write pulse width	t_{WP}	100			ns
Address hold time	t_{AH}	50			ns
Data setup time	t_{DS}	50			ns
Data hold time	t_{DH}	20			ns
Chip enable hold time	t_{CH}	0			ns
Output enable hold time	t_{OEH}	20			ns
Write enable hold time	t_{WEH}	10			ns
Byte write cycle time	t_{WR}		10	40	ms
Write recovery time	t_{RE}	50			ns
Number of write per byte	N	10			x1000

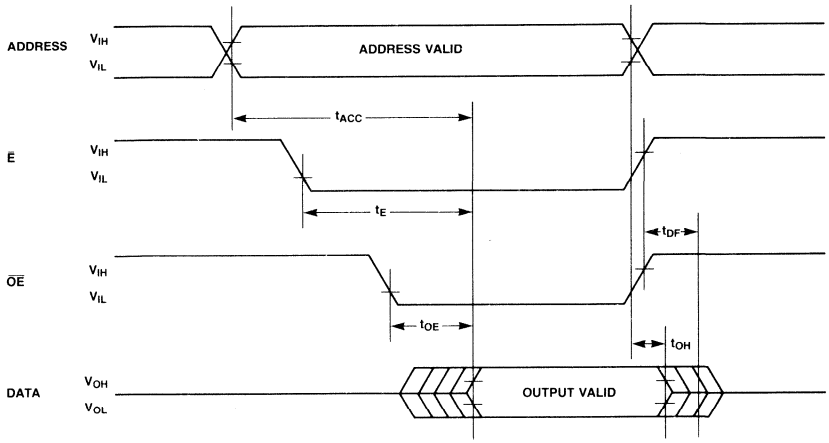
AC Characteristics (Chip Erase*1)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Chip enable setup time	t_{CS}	150			ns
Ouput enable setup time	t_{OES}	150			ns
Write pulse width	t_{WP}	5		20	ms
Data setup time	t_{DS}	150			ns
Data hold time	t_{DH}	100			ns
Chip enable hold time	t_{CH}	100			ns
Output enable hold time	t_{OEH}	100			ns

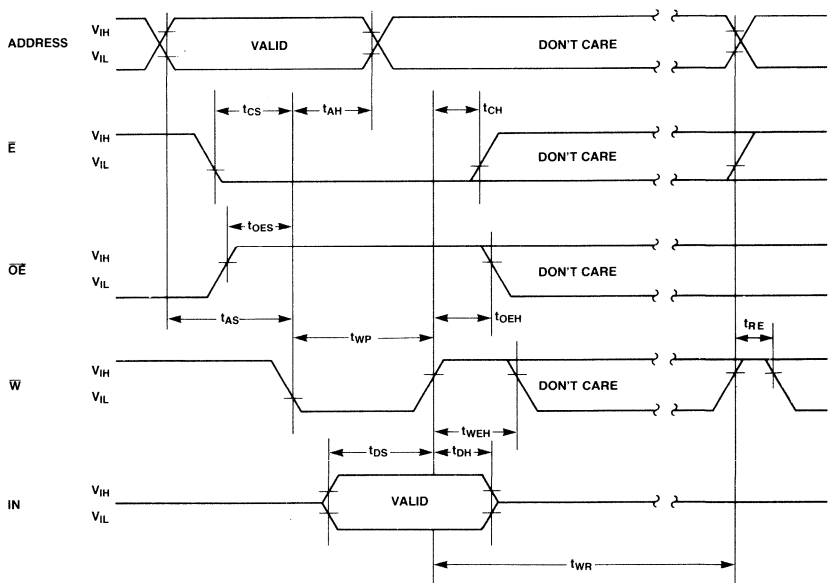
Note: *1 $\overline{OE}$ = 13.5V ± 1.5V.

Timing Diagrams

Read Waveform

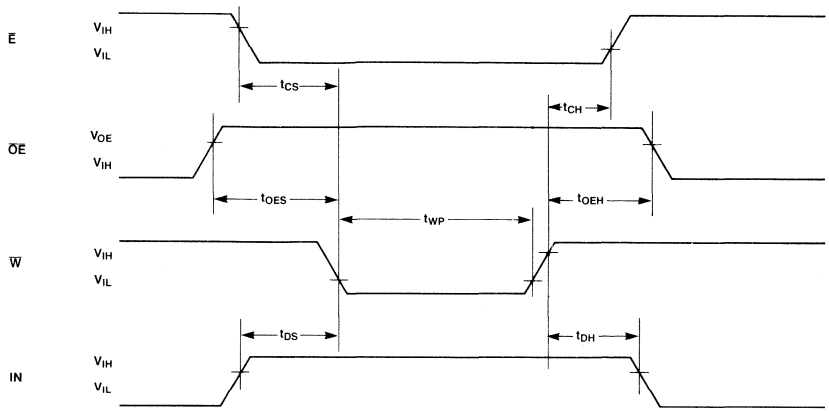


Byte Write Waveform



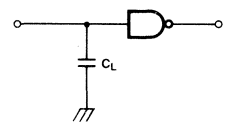
Timing Diagrams
(Continued)

Chip Erase Waveform



AC Test Conditions

Input Pulse Levels:	0.45V to 2.4V
Input Rise/Fall Times:	≤20 ns
Input Reference Levels:	0.8V to 2.0V
Output Reference Levels:	0.8V, to 2.0V
Output Load:	1 TTL Gate and C_L = 100 pF



Write Information

Byte Write

The MBM28C64's write mode is similar to that of Static RAM. The write cycle is completely self-timed, and initiated by a low going TTL pulse on the $\overline{W}$ pin. On the falling edge of $\overline{W}$, the address data is latched. On the rising edge of $\overline{W}$, the input data are latched. During the write cycle, the MBM28C64 automatically erases the memory data previously written, write new data into the memory and verify to ensure successfully the byte write.

Chip Erase

The MBM28C64 has a chip erase mode using external power supply which all data can be written to high state (=the erased state). The erase mode is initiated by setting $\overline{OE}$ to 13.5V and applying low TTL level to $\overline{W}$ while holding all data inputs on high TTL level.

$\overline{DATA}$ Polling

The MBM28C64 features $\overline{DATA}$ Polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of that byte at I/O_8. After completion of the write cycle, true data is available.

$\overline{DATA}$ Polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

DATA Protection

The MBM28C64 has three features to prevent an erroneous initiation of write mode.

V_{CC} Detector: When the V_{CC} is less than +3V during V_{CC} power-on and power-off, all functions are inhibited.

Noise Filter: When initiating write cycle, the write pulse of less than 20 ns is locked.

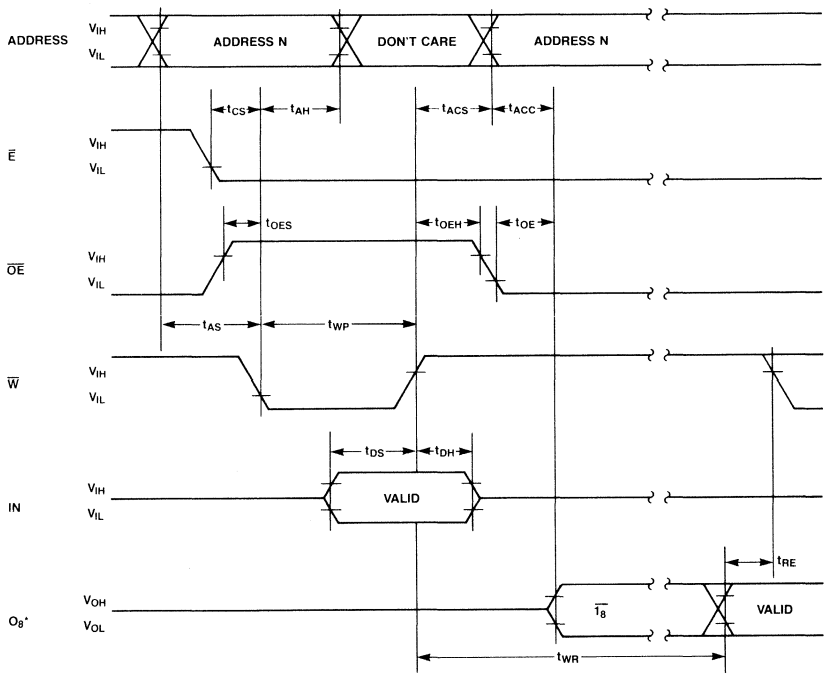
Write Inhibit: When $\overline{OE}$ is low TTL or $\overline{E}$ is high TTL, the initiation of write cycle is inhibited.

AC Characteristics (DATA Polling)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Address setup time to $\overline{W}$	t_{ACS}	20			ns
Address access time	t_{ACC}			350	ns
Output enable access time	t_{OE}			120	ns

Note: *1 t_{OE} delays up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{E}$ without impact on t_{ACC}.

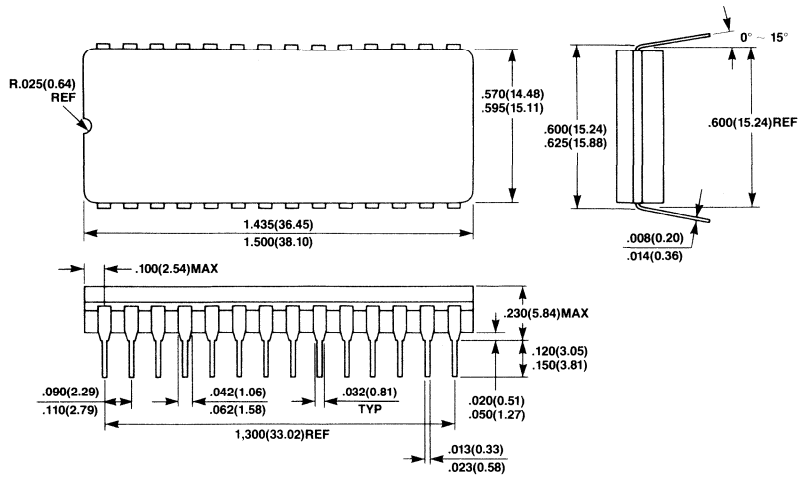
Data Polling Waveform



NOTE: *O_1 THROUGH O_7 ARE IN HIGH-Z STATE TILL END OF WRITE.

Package Dimensions
Dimensions in inches
(millimeters)

28-Lead Ceramic Dual In-Line Package
(Case No.: DIP-28C-C02)



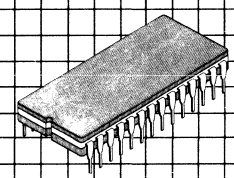
MBM28C65-25, MBM28C65-35

CMOS 65,536-Bit Electrically Erasable Read Only Memory

Description

The Fujitsu MBM28C65 is a 65,536-bit CMOS electrically erasable read-only memory (EE PROM). The MBM28C65 uses internally latched address, and data protection circuitry to protect against short write pulses and noise on $\overline{W}$. The device dissipates only 110 mW in the active mode and 550 μW in standby.

The MBM28C65 is ideal for a wide variety of applications which require non-volatility and in system data modification. The MBM28C65 is available in a 28-pin ceramic dual in-line package, and 32-pin LCC.

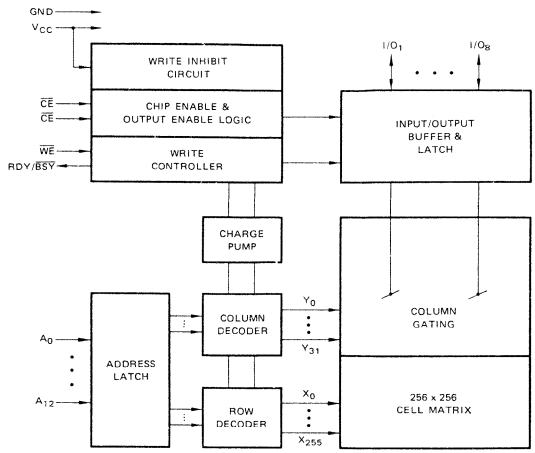


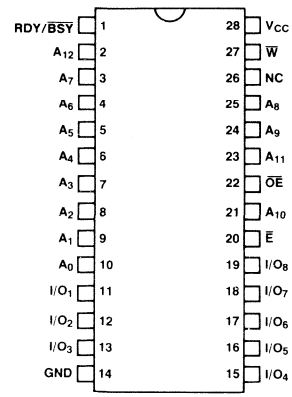
DIP-28C-C02

Features

- 8,192 words x 8-bit, fully decoded
- Internally latched address/data in writing
- Automatic Byte-Erase before Write
- Self-timed Byte Write
- Data protection against short write pulse and noise on $\overline{W}$
- On chip data verification
- Two write status identifiers READY/BUSY (open drain) and DATA POLLING
- Low power
  Active: 165 mW
  Standby: 550 μW
- Access time
  250 ns max. (MBM28C65-25)
  350 ns max. (MBM28C65-35)
- Chip erase capability
- TTL compatible input/output for fully MPU interface
- Three-state output for wired-OR capability
- Output enable (OE) for simplified memory expansion
- Single +5V supply, ±10%tolerance
- Minimum Endurance of 10000 Erase/Write cycle per Byte
- JEDEC approved pin out and package

MBM28C65 Block Diagram and Pin Assignment





Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Supply voltage with respect to GND	V_{CC}	−0.3 to +7.0	V
All input/output voltage with respect to GND	V_{IN}, V_{OUT}	−0.3 to V_{CC} + 0.3	V
Voltage on A_9 with respect to GND	V_{A9}	−0.3 to +13.5	V
Voltage on $\overline{OE}$ with respect to GND	V_{OE}	−0.3 to +13.5	V
Temperature under bias	T_{BIAS}	−25 to +85	°C
Storage temperature	T_{STG}	−65 to +125	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Function and Pin Connections

Function (Pin No.) / Mode	Address Input (2 to 10, 21, 23 to 25)	$\overline{E}$ (20)	$\overline{OE}$ (22)	$\overline{W}$ (27)	RDY/BSY (Open Drain) (1)	Data I/O (12 to 14, 16 to 20)	Power
Read	A_{IN}	V_{IL}	V_{IL}	V_{IH}	High-Z	OUT	Active
Standby and write inhibit	Don't care	V_{IH}	Don't care	Don't care	High-Z	High-Z	Standby
Write	A_{IN}	V_{IL}	V_{IH}	V_{IL}	V_{OL}	IN	Write
$\overline{DATA}$ polling*	A_{IN}	V_{IL}	V_{IL}	V_{IH}	V_{OL}	$I/O_8 = \overline{I8}$ I/O_1 to I/O_7 = High-Z	Write
						OUT	Active
Write inhibit	A_{IN}	Don't care	V_{IL} Don't care	Don't care V_{IH}	High-Z	High-Z	Active
Chip erase	Don't care	V_{IL}	V_{OE}	V_{IL}	V_{OL}	V_{IH}	Write

Note: * The address must be applied to the address. From then on all output data becomes input data from the point where the write mode is completed.
V_{OE}: 13.5V ±1.5V

Recommended Operating Conditions
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.0		V_{CC} +0.3	V
Input low voltage	V_{IL}	−0.1		0.8	V
Operating temperature	T_A	0		70	°C

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance (V_{IN} = 0V)	C_{IN}			10	pF
Output capacitance (V_{OUT} = 0V)	C_{OUT}			10	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol	Min	Max	Unit
Input leakage current	V_{IN} = 5.5V	I_{LI}	−10	10	μA
Output leakage current	V_{OUT} = 5.5V	I_{LO}	−10	10	μA
V_{CC} standby current	$\overline{E} = V_{IH}$	I_{SB1}		1	mA
V_{CC} standby current	$\overline{E} = V_{CC} \pm 0.3V$	I_{SB2}		100	μA
V_{CC} active current	$\overline{E} = V_{IL}$, f = 0 MHz	I_{CC1}		20	mA
V_{CC} active current	f = 4 MHz, I_{OUT} = 0 mA	I_{CC2}		20	mA
V_{CC} write current	$\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$	I_{CCW}		40	mA
Output low level	I_{OL} = 2.1 mA	V_{OL}		0.45	V
Output high level	I_{OH} = 400 μA	V_{OH}	2.4		V
Operation inhibit level		V_{INH}		3	V
Chip erase voltage		V_{OE}	12	15	V
V_{CC} Chip Erase Current	$\overline{E} = \overline{W} = V_{IL}$ $\overline{OE} = V_{OE}$	I_{CCE}		100	mA

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MBM28C64-25		MBM28C64-35		Unit
		Min	Max	Min	Max	
Address access time	t_{ACC}		250		350	ns
$\overline{E}$ to output delay	t_E		250		350	ns
$\overline{OE}$ to output delay*1	t_{OE}		100		120	ns
$\overline{E}$, $\overline{OE}$ high to output float*2	t_{DF}		60		80	ns
$\overline{OE}$ high to output	t_{OH}	0		0		ns

Notes: *1 t_{OE} is specified the point where both t_{CE} and t_{ACC} settled.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{E}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

AC Characteristics (Byte Write)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Address setup time	t_{AS}	20			ns
Chip enable setup time	t_{CS}	20			ns
Output enable setup time	t_{OES}	20			ns
Write pulse width	t_{WP}	100			ns
Address hold time	t_{AH}	50			ns
Data setup time	t_{DS}	50			ns
Data hold time	t_{DH}	20			ns
Chip enable hold time	t_{CH}	0			ns
Output enable hold time	t_{OEH}	20			ns
Write enable hold time	t_{WEH}	10			ns
Time to device busy	t_{DB}			120	ns
Byte write cycle time	t_{WR}		10	40	ms
Write recovery time	t_{RE}	50			ns
Number of write per byte	N	10			x1000
RDY/$\overline{BSY}$ to output time*	t_{RBO}			100	ns

Note: *If $\overline{E}$ = $\overline{OE}$ = V_{IL} and RDY/$\overline{BSY}$ is going to OFF, the read data is valid after t_{RBO}

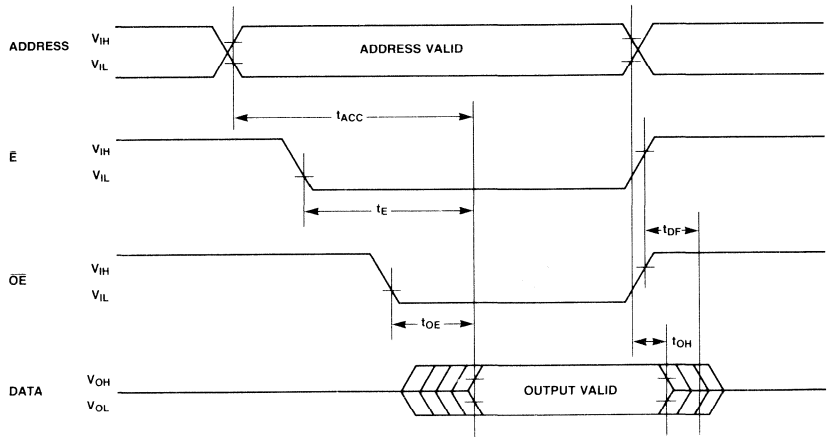
AC Characteristics (Chip Erase*1)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Chip enable setup time	t_{CS}	150			ns
Ouput enable setup time	t_{OES}	150			ns
Write pulse width	t_{WP}	5		20	ms
Data setup time	t_{DS}	150			ns
Data hold time	t_{DH}	100			ns
Chip enable hold time	t_{CH}	100			ns
Output enable hold time	t_{OEH}	100			ns
Time to Device Busy	t_{DB}			120	ns
Time to Device Ready	t_{DR}			120	ns

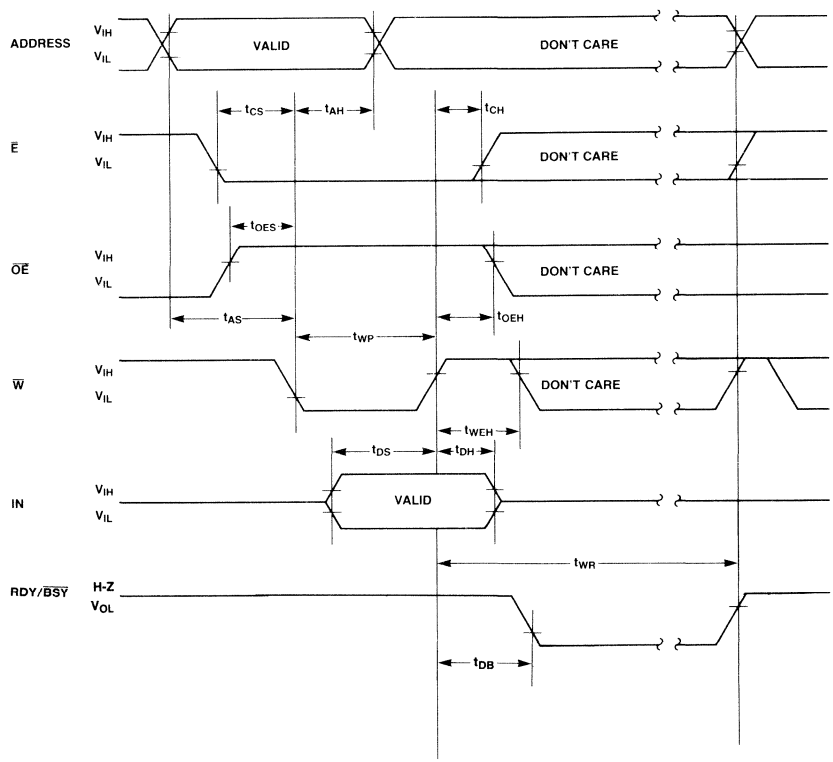
Note: *1 $\overline{OE}$ = 13.5V ± 1.5V.

Timing Diagrams

Read Waveform

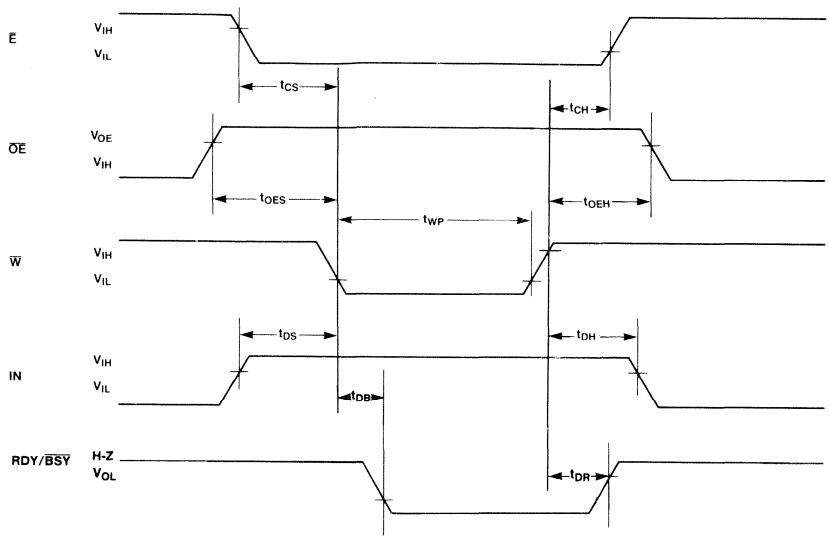


Byte Write Waveform



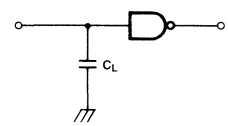
Timing Diagrams
(Continued)

Chip Erase Waveform



AC Test Conditions

Input Pulse Levels:	0.45V to 2.4V
Input Rise/Fall Times:	≤20 ns
Input Reference Levels:	0.8V to 2.0V
Output Reference Levels:	0.8V, to 2.0V
Output Load:	1 TTL Gate and C_L = 100 pF



Write Information

Byte Write

The MBM28C65's write mode is similar to that of Static RAM. The write cycle is completely self-timed, and initiated by a low going TTL pulse on the $\overline{W}$ pin. On the falling edge of $\overline{W}$, the address data is latched. On the rising edge of $\overline{W}$, the input data are latched. During the write cycle, the MBM28C65 automatically erases the memory data previously written, write new data into the memory and verify to ensure successfully the byte write.

Chip Erase

The MBM28C65 has a chip erase mode using external power supply which all data can be written to high state (=the erased state). The erase mode is initiated by setting $\overline{OE}$ to 13.5V and applying low TTL level to $\overline{W}$ while holding all data inputs on high TTL level.

$\overline{DATA}$ Polling

The MBM28C65 features $\overline{DATA}$ Polling to signal the completion of a byte write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of that byte at I/O_8. After completion of the write cycle, true data is available.

$\overline{DATA}$ Polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

DATA Protection

The MBM28C65 has three features to prevent an erroneous initiation of write mode.

V_{CC} Detector: When the V_{CC} is less than +3V during V_{CC} power-on and power-off, all functions are inhibited.

Noise Filter: When initiating write cycle, the write pulse of less than 20 ns is locked.

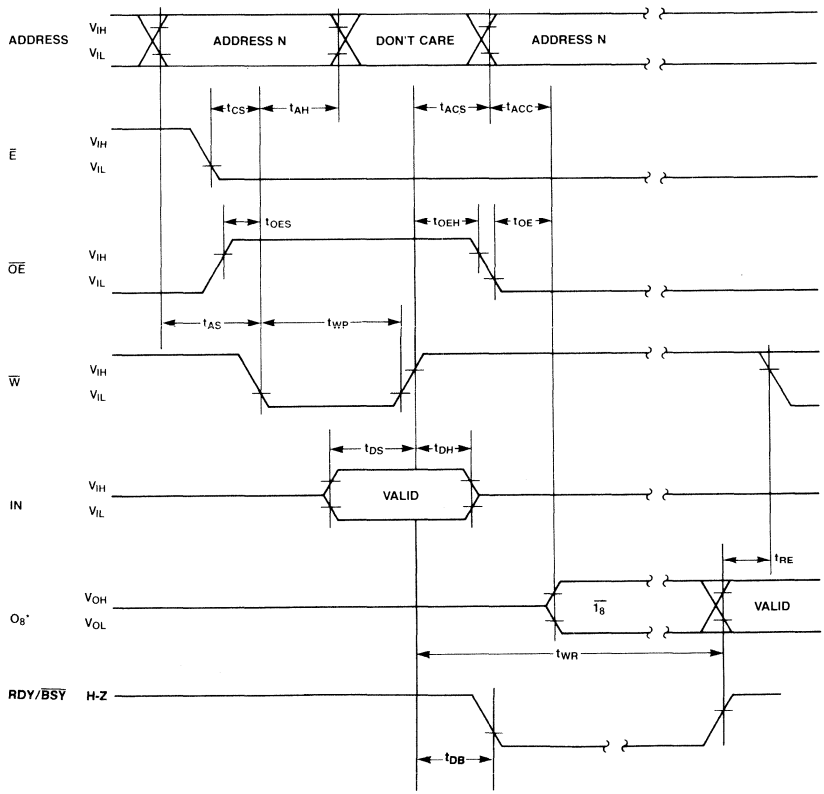
Write Inhibit: When $\overline{OE}$ is low TTL or $\overline{E}$ is high TTL, the initiation of write cycle is inhibited.

AC Characteristics ($\overline{DATA}$ Polling)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Address setup time to $\overline{W}$	t_{ACS}	20			ns
Address access time	t_{ACC}			350	ns
Output enable access time	t_{OE}			120	ns

Note: *1 t_{OE} delays up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{E}$ without impact on t_{ACC}.

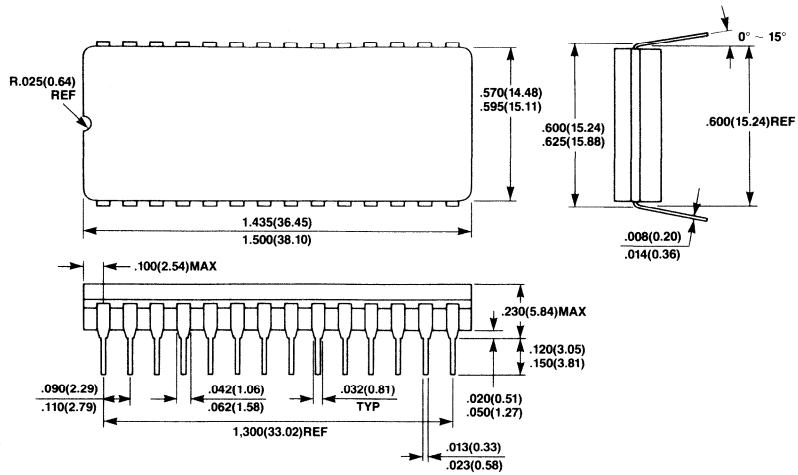
$\overline{Data}$ Polling Waveform



NOTE: *O_1 THROUGH O_7 ARE IN HIGH-Z STATE TILL END OF WRITE.

Package Dimensions
Dimensions in inches
(millimeters)

28-Lead Ceramic Dual In-Line Package
(Case No.: DIP-28C-C02)



MBM2212-20, MBM2212-25

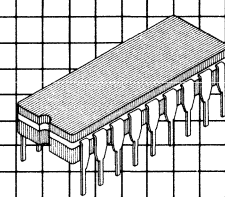
1,024-Bit Non-Volatile Random Access Memory

Description

The Fujitsu MBM2212 is a 1,024-bit non-volatile static random access memory (NVRAM) combined 1,024-bit static random access memory (SRAM) and electrically erasable and reprogrammable read only memory (EEPROM) on one-chip. It is designed for applications such as system potentiometer or electrical switch to memorize the system condition etc.

The MBM2212 is organized as 256 words by 4-bit. Each one bit is constituted with a combination of SRAM and EEPROM cell. The read and write operations are performed on the SRAM cell. The data transfer between SRAM and EEPROM is performed using two control pins. The store mode (transferring SRAM data to EEPROM) is executed with a single pulse applied to the $\overline{ST}$ pin. The recall mode (transferring EEPROM data to SRAM) is executed in 1.2 μs with one short pulse applied to the $\overline{RC}$ pin. Both store and recall operations are completed for all bits at one time.

The MBM2212 is fabricated using N-MOS silicon gate technology with stacked gate cells. Single +5V supply and TTL input/output level operations greatly facilitate microprocessor applications.

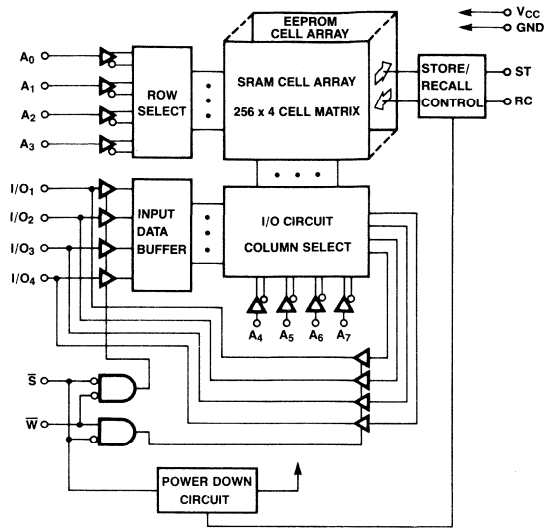


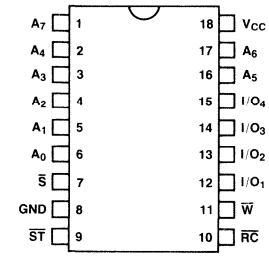
Cerdip DIP Package
DIP-18C-C01

Features

- **256 words x 4-bit organization, fully decoded**
- **10 ms self-timed auto store**
- **10 years data retention for each store**
- **Unlimited endurance for recall**
- **TTL compatible inputs/outputs**
- **Tri-state output**
- **Write protection on power-on/off and surge pulse**
- **Low power consumption; Active: 330 mW max. Standby: 165 mW max.**
- **Fast access time; 200 ns max. (MBM2212-20) 250 ns max. (MBM2212-25)**
- **Standard 18-pin DIP package**

MBM2212 Block Diagram and Pin Assignment





FUNCTIONAL TRUTH TABLE

MODE	$\overline{S}$	$\overline{W}$	$\overline{RC}$	$\overline{ST}$	I/O	V_{CC}	GND	POWER
Standby	V_{IH}	X	V_{IH}	V_{IH}	High-Z	5V	GND	Standby
Read	V_{IL}	V_{IH}	V_{IH}	V_{IH}	OUT	5V	GND	Active
Write	V_{IL}	V_{IL}	V_{IH}	V_{IH}	IN	5V	GND	Active
Recall	X	V_{IH}	V_{IL}	V_{IH}	High-Z	5V	GND	Standby
	V_{IH}	X						
Store	X	V_{IH}	V_{IH}	V_{IL}	High-Z	5V	GND	Active
	V_{IH}	X						

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Supply voltage with respect to GND	V_{CC}	−1.0 to +7.0	V
All input/output voltage with respect to GND	V_{IN}, V_{OUT}	−1.0 to +7.0	V
Output current with respect to GND	I_{OUT}	+5.0	mA
Temperature under bias	T_{BIAS}	−10 to +85	°C
Storage temperature	T_{STG}	−65 to +125	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high level	V_{IH}	2.0		V_{CC} + 0.5V	V
Input low level	V_{IL}	−1.0*		0.8	V
Operating Temperature	T_A	0		70	°C

Note: * For less than 50 ns undershoot, but −0.5V for DC.

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance (V_{IN} = 0V)	C_{IN}			6	pF
I/O capacitance ($V_{I/O}$ = 0V)	$C_{I/O}$			8	pF

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol	Min	Max	Unit
Input leakage current	V_{IN} = GND to 5.5V	$\|I_{LI}\|$		10	μA
I/O leakage current	$\overline{S}$ = V_{IH}, $V_{I/O}$ = GND to 5.5V	$\|I_{LO}\|$		10	μA
V_{CC} standby current	$\overline{S}$ = V_{IH} *1	I_{SB}		30	mA
V_{CC} active current	$\overline{S}$ = V_{IL} *2	I_{CC}		60	mA
Output low level	I_{OL} = 4.2 mA	V_{OL}		0.4	V
Output high level	I_{OH} = −2.0 mA	V_{OH}	2.4		V
Store inhibit voltage		V_{IHBT}		3	V

Note: *1 Supply current increases to I_{CC} while store mode regardless of $\overline{S}$ level
*2 Supply current reduces to I_{SB} while recall mode regardless of $\overline{S}$ level

SRAM Mode AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Read Mode
($\overline{W}$ = $\overline{ST}$ = $\overline{RC}$ = V_{IH})

		MBM2212-20		MBM2212-25		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	200		250		ns
Address access time	t_{AA}		200		250	ns
Chip select access time	t_{ACS}		200		250	ns
Output hold after address change	t_{OH}	50		50		ns
Chip select to output active*	t_{LZ}	10		10		ns
Chip select to output disable*	t_{HZ}		100		100	ns

Note: * Transition is measured at point of ± 500 mV from steady state voltage.

SRAM Mode AC Characteristics
(Continued)
(Recommended operating conditions unless otherwise noted.)

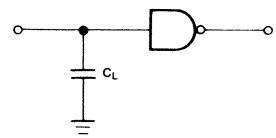
Write mode
($\overline{ST}$ = $\overline{RC}$ = V_{IH})

Parameter	Symbol	MBM2212-20/25 Min	Max	Unit
Write cycle time	t_{WC}	300		ns
Chip select to end of write ($\overline{W}$ = V_{IL})	t_{CW}	150		ns
Address setup time	t_{AS}	50		ns
Write pulse width ($\overline{S}$ = V_{IL})	t_{WP}	150		ns
Write recovery time*1	t_{WR}	25		ns
Data valid to end of write	t_{DW}	100		ns
Data hold time	t_{DH}	0		ns
Write enable to output high-Z*2	t_{WZ}		100	ns
Output active from end of write*3	t_{OW}	10		ns

Notes: *1 t_{WR} is defined from the end point of write.
*2 Transition is measured at point of ±500 mV from steady state voltage.
*3 If $\overline{S}$ goes high coincident with $\overline{W}$ high transition, DATA OUT remains in a high impedance state.

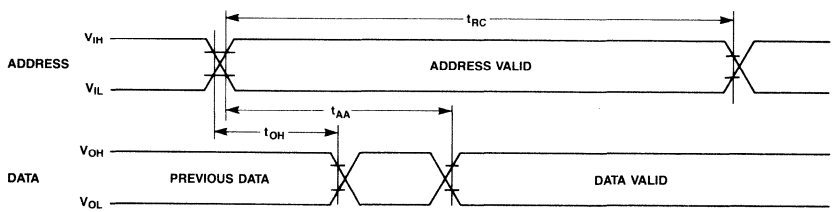
AC Test Conditions
(including EEPROM mode)

Input pulse levels:	0.6V to 2.4V
Input rise/fall times:	≤10 ns
Input reference levels:	0.8V, 2.2V
Output reference levels:	0.8V, 2,2V
Output Load:	1 TTL gate and C_L = 100 pF



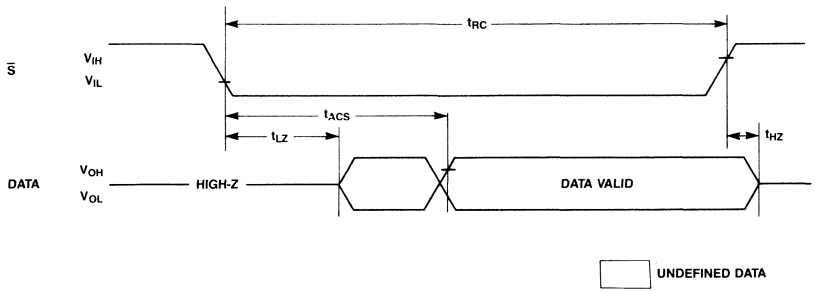
Read Cycle Timing Diagrams

Address Control Mode
($\overline{S}$ = V_{IL}, $\overline{W}$ = V_{IH})



Read Cycle Timing Diagrams
(Continued)

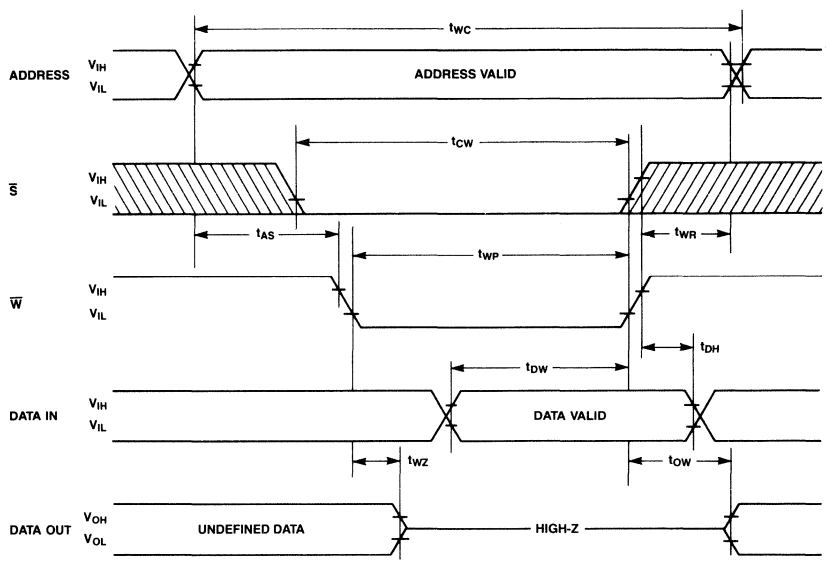
$\overline{S}$ Control Mode*
($\overline{W}$ = V_{IH})



NOTE: * ADDRESS BECOMES VALID PRIOR TO OR COINCIDENT WITH $\overline{S}$ LOW TRANSITION.

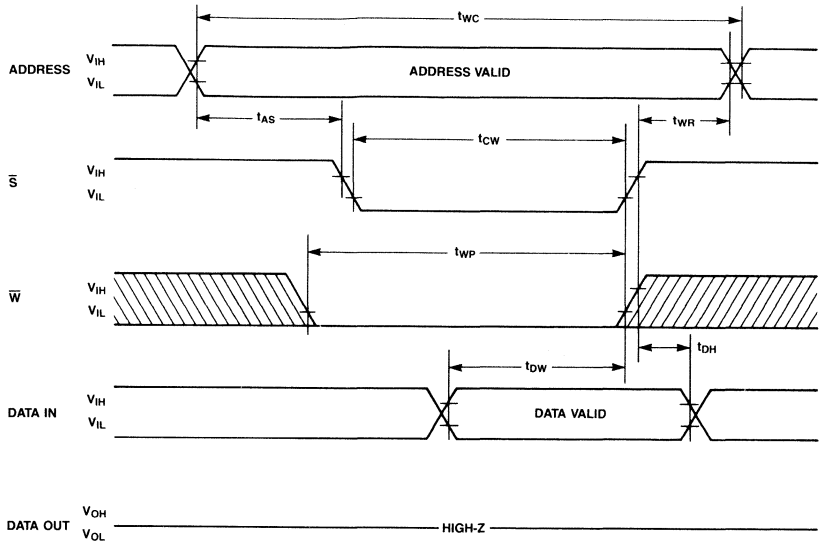
Write Cycle Timing Diagrams

$\overline{W}$ Control Mode



Write Cycle Timing Diagrams
(Continued)

$\overline{S}$ Control Mode



EEPROM Read/Write Information

The MBM2212 can not read or write EEPROM data externally and it must be transferred from/to SRAM cell array corresponding to each EEPROM bit. $\overline{RC}$ and $\overline{ST}$ pins are assigned to execute these operations easily.

Recall Mode

The recall mode is initiated when negative pulse (⊔) is applied to $\overline{RC}$ pin while either $\overline{S} = V_{IH}$ or $\overline{W} = V_{IH}$ and is completed within 1.2 μs. The supply current is reduced to standby current automatically. Please notice that the SRAM data is replaced by the EEPROM data after the execution of this operation.

Store Mode

The store mode is initiated when negative pulse (⊔) is applied to $\overline{ST}$ pin while either $\overline{S} = V_{IH}$ or $\overline{W} = V_{IH}$ and is completed within 10ms automatically by the on-chip timer. During this operation mode, all input and output pins are inhibited. The original SRAM data remains after the store mode.

The MBM2212 has two security circuits to prevent an erroneous store mode. Noise filter circuit for duration of less than 20 ns negative pulse on $\overline{ST}$ pin is on the chip. Auto-standby circuit prevents the stored data on the EEPROM cell array from destruction when V_{CC} is less than +3V.

When V_{CC} power is ON or OFF, the V_{IH} input level must be applied to $\overline{ST}$ pin before or while V_{CC} is greater than +3V.

These operation modes, store mode, recall mode and SRAM write mode have the same logical priority. Normally the first set logical condition determines the ensuing operation mode among $\overline{ST}$, $\overline{RC}$ and $\overline{W}$ pins.

AC Characteristics

(Recommended operating conditions unless otherwise noted.)

Recall Mode

($\overline{W} = \overline{ST} = V_{IH}$)

Parameter	Symbol	MBM2212-20/25 Min	MBM2212-20/25 Max	Unit
Recall cycle time	t_{RCC}	1200		ns
Recall pulse width	t_{RCP}	450		ns
$\overline{RC}$ to output disable*	t_{RCZ}		150	ns
$\overline{RC}$ to output active*	t_{ORC}	10		ns
$\overline{RC}$ to output valid	t_{ARC}		750	ns

Note: * Transition is measured at point of ±500 mV from steady state voltage.

Store Mode

($\overline{W} = \overline{RC} = V_{IH}$)

Parameter	Symbol	MBM2212-20 Min	MBM2212-20 Max	MBM2212-25 Min	MBM2212-25 Max	Unit
Store cycle time	t_{ST}		10		20	ns
Store pulse width*1	t_{STP}	100		100		ns
Store to output disable*2	t_{STZ}		500		500	ns
Output Valid from End of Store	t_{OST}		200		250	ns

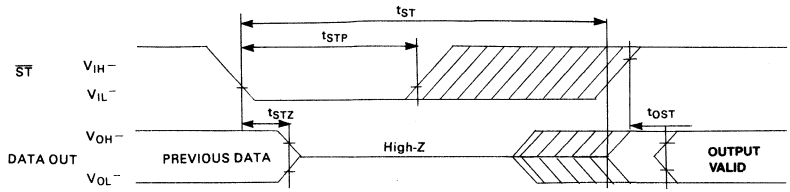
Note: *1 It is protected from entry into the store mode by less than 20 ns pulse width.
*2 Transition is measured at point of ±500 mV from steady state voltage.

Endurance

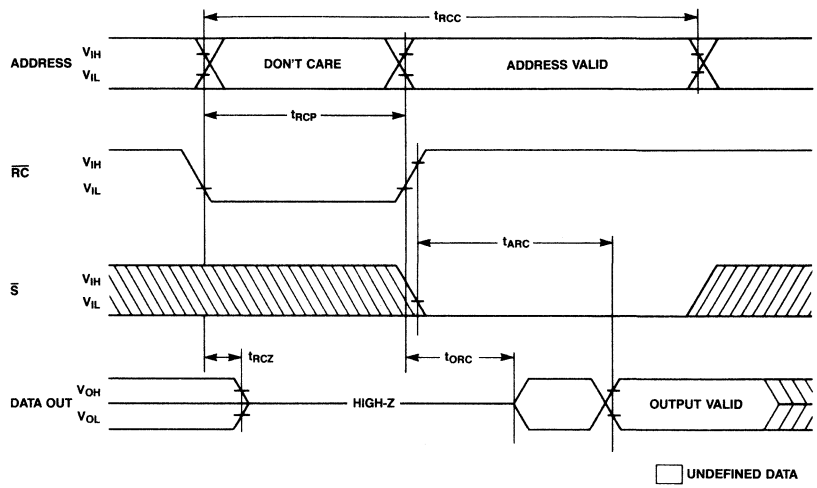
Number of store cycles	Number of data changes per bit	Unit
100,000	10,000	Times

EEPROM Read/Write Information
(Continued)

Store Cycle Timing Waveform

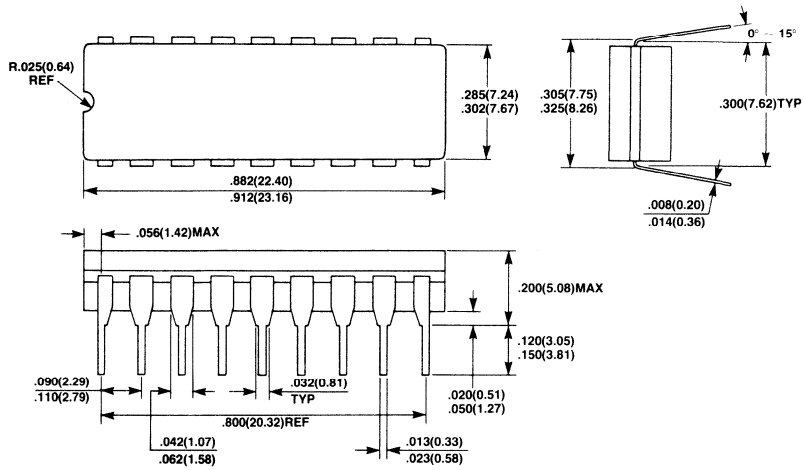


Recall Cycle Timing Waveform



Package Dimensions
Dimensions in inches
(millimeters) (Suffix: −Z)

18-Lead Ceramic (CERDIP) Dual-in-Line Package
(Case No.: DIP-18C-C01)



ROMs

MB83256 8-2
MB83512 8-8
MB831000 8-12
MB831124 8-18

MB83256-25

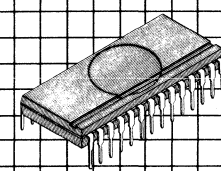
CMOS 262,144-Bit Mask-Programmable Read Only Memory

Description

The Fujitsu MB83256 is a CMOS Si-gate mask-programmable static read only memory organized as 32,768 words by 8-bits.

The MB83256 has TTL-compatible I/O and TRI-state output level with fully-static operation (i.e. no need of clock signal) and single +5V power supply. The device is designed for applications such as character generator or program storage which require large memory capacity and high-speed/low-power operation.

The MB83256 is packaged in a 28-pin dual-in-line package and its pin-out is compatible with standard 28-pin EPROM.



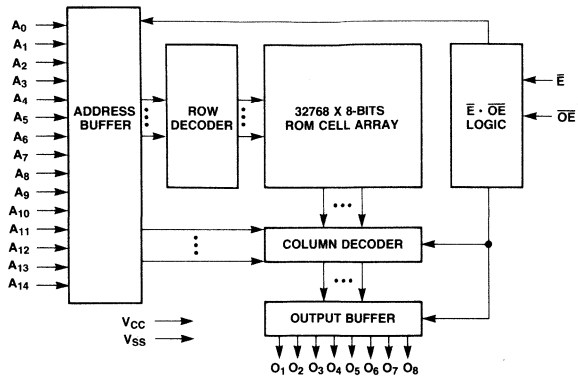
Plastic Package
DIP-28P-M02

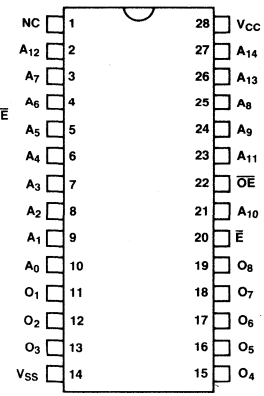
Features

- **32,768 words x 8-bits organization**
- **Fast access time: 250 ns. max.**
- **Complete static operation: No clock required**
- **ALL inputs and outputs are TTL compatible**
- **Three-state outputs**
- **+5V supply voltage**
- **Low power consumption: 83 mW (Operation) 8.3 mW (Standby, TTL input level) 165 μW (Standby, CMOS input level)**
- **Standard 28-pin DIP**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB83256 Block Diagram and Pin Assignment





TRUTH TABLE

$\overline{E}$	$\overline{OE}$	Mode	Output	Power Consumption Mode
H	X	Non-selected	High-Z	Standby
L	H	Non-selected	High-Z	Active
L	L	Selected	Output	Active

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Storage temperature range	T_{stg}	−40 to +125	°C
Operating temperature	T_A	−10 to +85	°C
Supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	−0.3 to V_{CC} + 0.3	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance (V_{OUT} = 0V)	C_{OUT}			10	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			7	pF

Recommended Operating Conditions
(Reference to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low voltage	V_{IL}	−0.3		0.8	V
Input high voltage	V_{IH}	2.2		V_{CC} + 0.3	V
Ambient temperature	T_A	0		70	°C

DC Characteristics

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Conditions	Symbol	MB83256-25 Min	MB83256-25 Max	Unit
Standby supply current	$\overline{E} = V_{IH}$	I_{SB1}		1.5	mA
	$\overline{E} = V_{CC}$, V_{IN} = GND or V_{CC}	I_{SB2}		30	μA
Active supply current	$\overline{E} - V_{IL}$, minimum cycle	I_{CC}		15	mA
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	−10	10	μA
Output leakage current	$\overline{E} = V_{IH}$, or $\overline{OE} = V_{IH}$	I_{LIO}	−10	10	μA
Output high voltage	I_{OH} = −400 μA	V_{OH}	2.4		V
Output low voltage	I_{OL} = 2.1 mA	V_{OL}		0.4	V

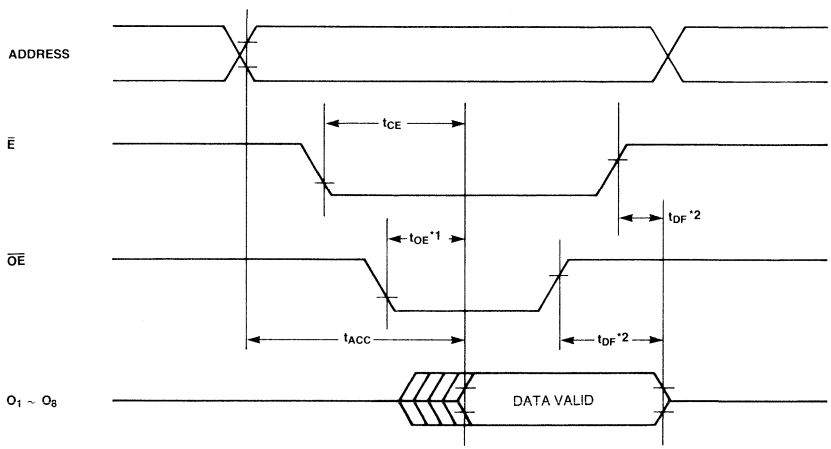
AC Characteristics

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB83256-25 Min	MB83256-25 Typ	MB83256-25 Max	Unit
Address access time ($\overline{E} = \overline{OE} = V_{IL}$)	t_{ACC}			250	ns
Chip enable access time ($\overline{OE} = V_{IL}$)	t_E			250	ns
Output enable access time*1	t_{OE}			100	ns
Output disable time*2	T_{DF}			80	ns
Output hold time	t_{OH}	0			ns

Note: *1 $\overline{OE}$ may be delayed up to ($t_{ACC} - t_{OE}$) after the falling edge of $\overline{E}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{E}$, whichever occurs earlier.

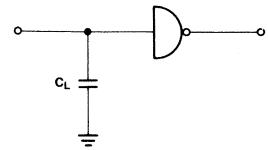
Timing Diagram



NOTES: *1 $\overline{OE}$ MAY BE DELAYED UP TO ($t_{ACC} - t_{OE}$) AFTER THE FALLING EDGE OF $\overline{E}$ WITHOUT IMPACT ON t_{ACC}.
*2 t_{DF} IS SPECIFIED FROM $\overline{OE}$ OR $\overline{E}$, WHICHEVER OCCURS EARLIER.

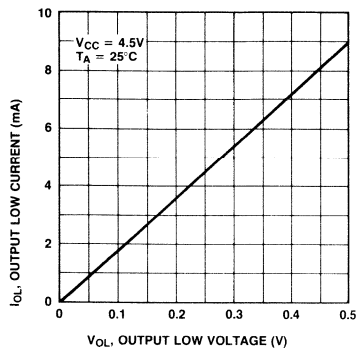
AC Test Conditions

Input Pulse Levels:	0.6V to 2.4V
Input Pulse Rise and Fall Time:	t_T = 10 ns
Timing Reference Levels:	Input: V_{IL} = 0.8V, V_{IH} = 2.2V Output: V_{OL} = 0.8V, V_{OH} = 2.2V
Output Load:	1 TTL Gate and C_L = 100 pF

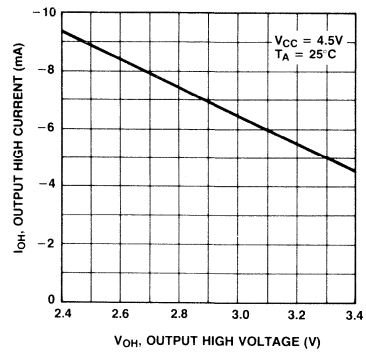


Typical Characteristics Curves
(Continued)

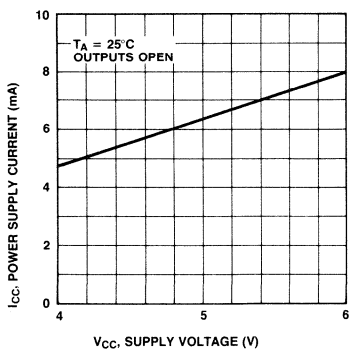
Output Low Current vs. Output Low Voltage



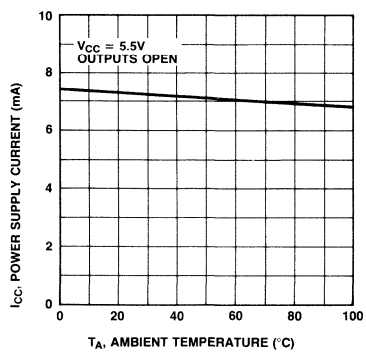
Output High Current vs. Output High Voltage



Power Supply Current vs. V_{CC} Supply Voltage

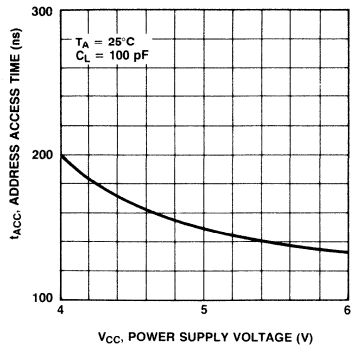


Power Supply Current vs. Ambient Temperature

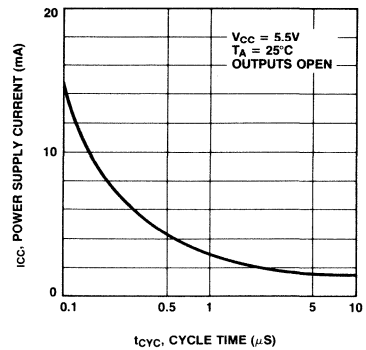


Typical Characteristics Curves
(Continued)

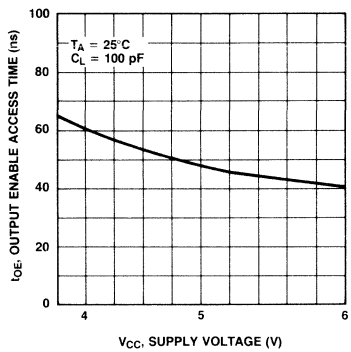
Address Access Time vs. V_{CC} Power Supply Voltage



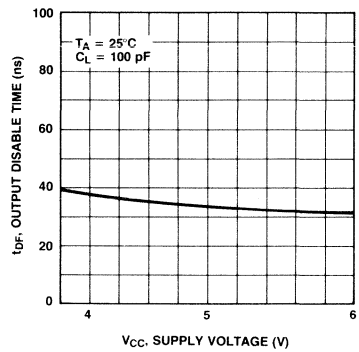
Power Supply Current vs. Cycle Time



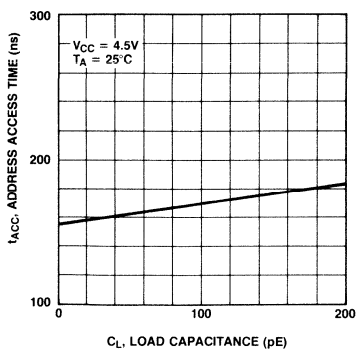
Output Enable Access Time vs. V_{CC} Supply Voltage



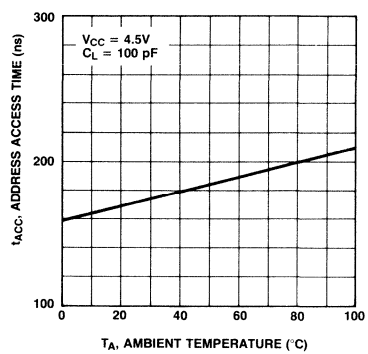
Output Disable Time vs. Ambient Temperature



Address Access Time vs. Load Capacitance

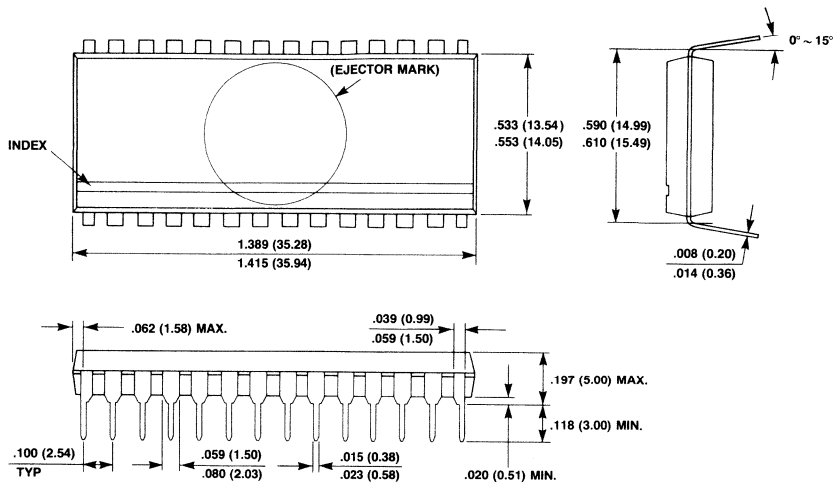


Address Access Time vs. Ambient Temperature



Package Dimensions
Dimensions in inches
(millimeters)

28-Lead Plastic Dual In-Line Package
(Case No.: DIP-28P-M02)



Preliminary

MOS Memories

FUJITSU

MB83512-15

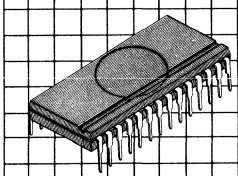
CMOS 524,288-Bit
Mask-Programmable
Read Only Memory

Description

The Fujitsu MB83512 is a CMOS Si-gate mask-programmable static read only memory organized as 65,536 words by 8-bits.

The MB83512 has TTL-compatible I/O and TRI-state output level with fully-static operation (i.e. no need of clock signal) and single +5V power supply. The device is designed for applications such as character generator or program storage which require large memory capacity and high-speed/low-power operation.

The MB83512 is packaged in a 28-pin dual-in-line package and its pin-out is compatible with standard 28-pin EPROM.



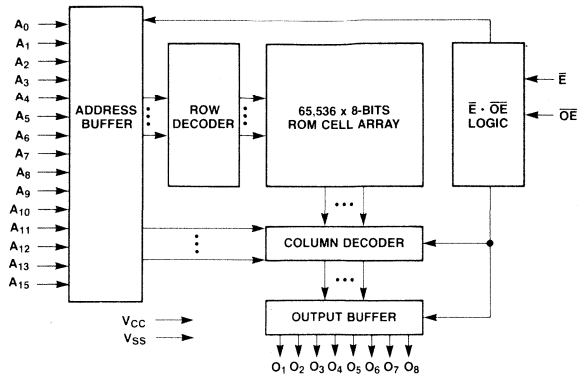
Plastic Package
DIP-28P-M02

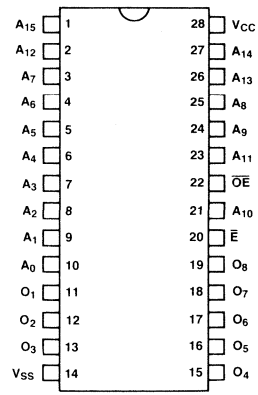
Features

- **65,536 words x 8-bits organization**
- **Fast access time: 150 ns max.**
- **Complete static operation: No clock required**
- **ALL inputs and outputs are TTL compatible**
- **Three-state outputs**
- **+5V supply voltage**
- **Low power consumption: 220 mW (Operation) 16.5 mW (Standby, TTL input level)**
- **275 μW (Standby, CMOS input level)**
- **Standard 28-pin DIP**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this impedance circuit.

MB83512-15 Block Diagram and Pin Assignment





TRUTH TABLE

$\overline{E}$	$\overline{OE}$	MODE	OUTPUT	POWER CONSUMPTION MODE
H	X	NON-SELECTED	HIGH-Z	STANDBY
L	H	NON-SELECTED	HIGH-Z	ACTIVE
L	L	SELECTED	OUTPUT	ACTIVE

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Storage temperature range	T_{STG}	−45 to +125	°C
Temperature under bias	T_{BIAS}	−10 to +85	°C
Supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
Output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output Capacitance (V_{OUT} = 0V)	C_{OUT}			10	pF
Input Capacitance (V_{IN} = 0V)	C_{IN}			7	pF

Recommended Operating Conditions
(Reference to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low voltage	V_{IL}	−0.3		0.8	V
Input high voltage	V_{IH}	2.2		V_{CC} + 0.3	V
Ambient temperature	T_A	0		70	°C

DC Characteristics
(Recommended operating conditions unless otherwise noted.)

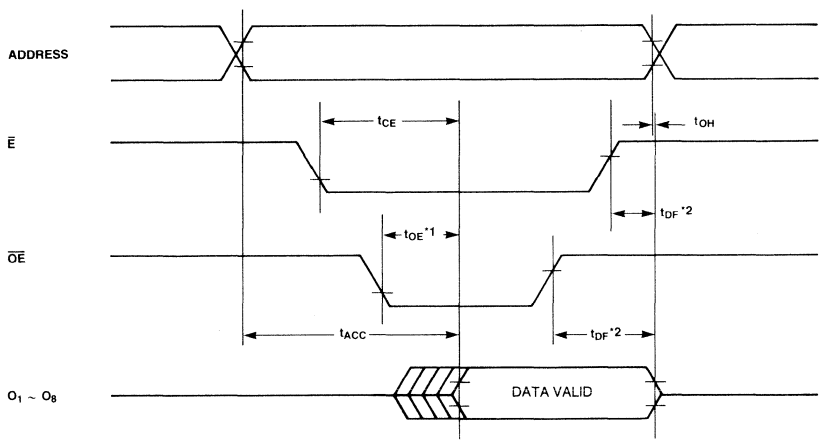
Parameter	Test Conditions	Symbol	MB83512-15 Min	Max	Unit
Standby supply current	$\overline{E} = V_{IH}$	I_{SB1}		3	mA
	$\overline{E} = V_{CC}$, V_{IN} = GND or V_{CC}	I_{SB2}		50	μA
Active supply current	$\overline{E} = V_{IL}$, minimum cycle	I_{CC}		40	mA
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	−10	10	μA
Output leakage current	$\overline{E} = V_{IH}$, or $\overline{OE} = V_{IH}$	I_{LO}	−10	10	μA
Output high voltage	I_{OH} = −400 μA	V_{OH}	2.4		V
Output low voltage	I_{OL} = 2.1 mA	V_{OL}		0.4	V

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB83512-15 Min	Typ	Max	Unit
Address access time ($\overline{E} = \overline{OE} = V_{IL}$)	t_{ACC}			150	ns
Chip enable access time ($\overline{OE} = V_{IL}$)	t_E			150	ns
Output enable access time*1	t_{OE}			80	ns
Output disable time*2	T_{DF}			60	ns
Output hold time	t_{OH}	0			ns

Notes: *1 $\overline{OE}$ may be delayed up to ($t_{ACC} - t_{OE}$) after the falling edge of $\overline{E}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{E}$, whichever occurs earlier.

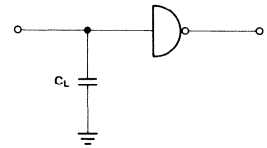
Timing Diagram



NOTES: *1 $\overline{OE}$ MAY BE DELAYED UP TO ($t_{ACC} - t_{OE}$) AFTER THE FALLING EDGE OF $\overline{E}$ WITHOUT IMPACT ON t_{ACC}.
*2 t_{DF} IS SPECIFIED FROM $\overline{OE}$ OR $\overline{E}$, WHICHEVER OCCURS EARLIER.

AC Test Conditions

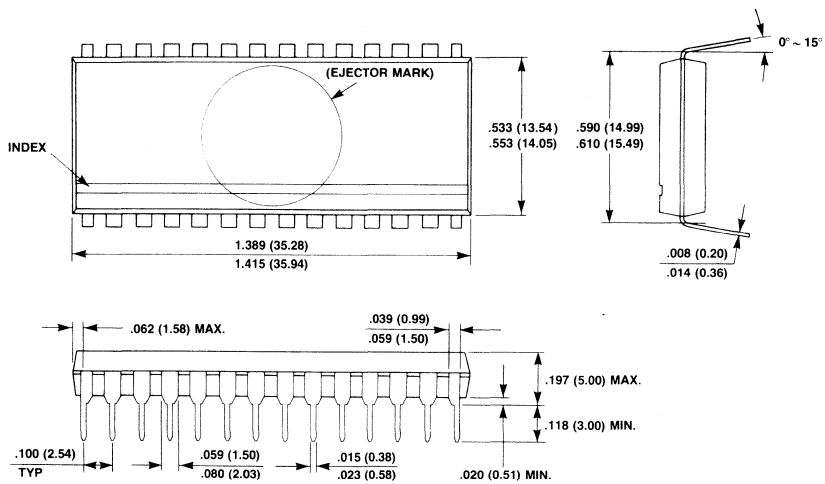
Input Pulse Levels:	0.6V to 2.4V
Input Pulse Rise and Fall Time:	t_T = 5 ns
Timing Reference Levels:	Input: V_{IL} = 0.8V, V_{IH} = 2.2V Output: V_{OL} = 0.8V, V_{OH} = 2.2V
Output Load:	1 TTL Gate and C_L = 100 pF



Package Dimensions

Dimensions in inches
(millimeters)

28-Lead Plastic Dual In-Line Package
(Case No.: DIP-28P-M02)



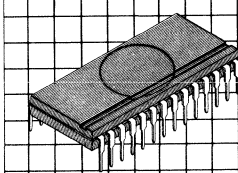
MB831000-15, MB831000-20

CMOS 1M-Bit Mask-Programmable Read Only Memory

Description

The Fujitsu MBM MB831000 is a CMOS Silicon gate Mask-programmable static read only memory organized as 131,072 by 8- bits.

The MB831000 has TTL-compatible I/O and TRI-STATE output level with fully-static operation (i.e., no need of clock signal) and single +5V power supply. The device is designed for applications such as character generator or program storage which require large memory capacity, high-speed and low-power operation.



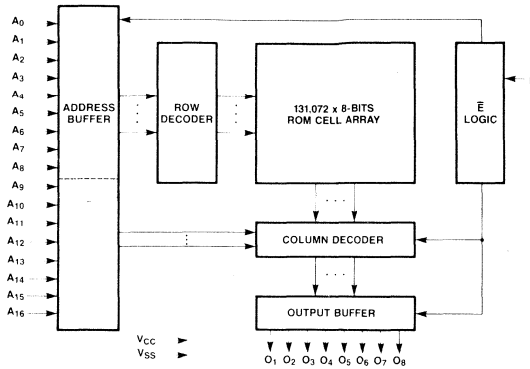
Plastic Package
DIP-28P-M02

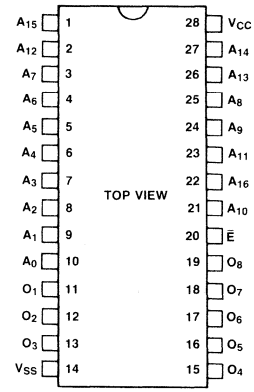
Features

- **131,072 words x 8-bits organization**
- **Access time:**
  150 ns (MB831000-15)
  200 ns (MB831000-20)
- **Completely static operation: No clock required**
- **All inputs and outputs are TTL compatible**
- **TRI-state output**
- **Single +5V supply, ±10% tolerance**
- **Low Power:**
  220 mW max. (Active)
  16.5 mW max. (Standby, TTL input level)
  275 μW max. (Standby, CMOS input level)
- **Standard 28-pin DIP**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB831000 Block Diagram and Pin Assignment





TRUTH TABLE

Ē	Mode	Output	Power Dissipation Mode
H	Not selected	High-Z	Standby
L	Selected	Output	Active

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
Output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Operating temperature	T_{BIAS}	−10 to +85	°C
Storage temperature range Referenced to GND	T_{STG}	−45 to +125	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low voltage	V_{IL}	−0.3		0.8	V
Input high voltage	V_{IH}	2.2		V_{CC} + 0.3	V
Ambient temperature	T_A	0		70	°C

Capacitance
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Output capacitance (V_{OUT} = 0V)	C_{OUT}			10	pF
Input capacitance (V_{IN} = 0V)	C_{IN}			7	pF

DC Characteristics

(Recommended operating conditions unless otherwise noted.)

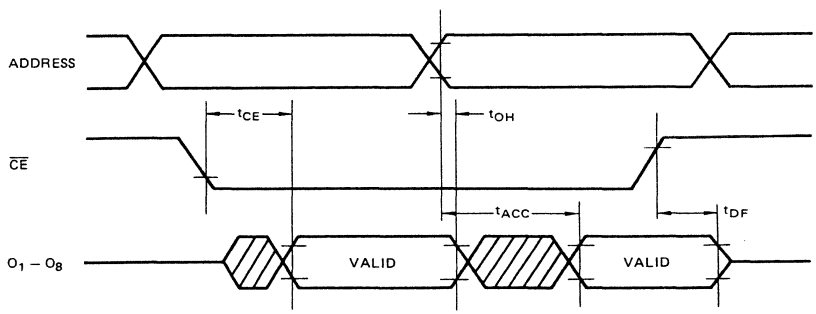
Parameter	Symbol	Min	Max	Unit	Test Condition
Active supply current	I_{CC}		40	mA	$\overline{E} = V_{IL}$, minimum cycle
Standby supply current	I_{SB1}		3	mA	$\overline{E} = V_{IH}$
	I_{SB2}		50	μA	$\overline{E} = V_{CC}$, V_{IN} = GND or V_{CC}
Input leakage current	I_{LI}	−10	10	μA	V_{IN} = 0 to V_{CC}
Output leakage current	$I_{LI/O}$	−10	10	μA	$\overline{E} = V_{IH}$
Output high voltage	V_{OH}	2.4		V	I_{OH} = −400 μA
Output low voltage	V_{OL}		0.4	V	I_{OL} = 2.1 mA

AC Characteristics

(Recommended operating conditions unless otherwise noted.)

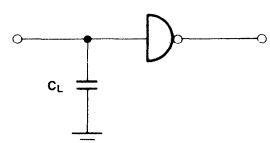
		MB831000-15		MB831000-20		
Parameter	Symbol	Min	Max	Min	Max	Unit
Address access time ($\overline{E} = V_{IL}$)	t_{ACC}		150		200	ns
Chip enable access time	t_E		150		200	ns
Output disable time	t_{DF}		60		60	ns
Output hold time	t_{OH}	0		0		ns

Timing Diagram



AC Test Condition

Input pulse level: 0.6 to 2.4V
Input pulse rise and fall time: t_T = 10 ns
Timing reference levels: Input: V_{IL} = 0.8 V, V_{IH} = 2.2 V
Output: V_{OL} = 0.8 V, V_{OH} = 2.2 V
Output load: 1 TTL Gate and 100 pF



MB831000 ROM Code Data Input Formats:

Fujitsu requires customers to provide ROM Code Data in the form of programmed EPROMs or Magnetic Tapes using Fujitsu's computer system. Fujitsu then will fabricate the MASKs utilizing the DATA provided from the customer.

Mask ROM Code Data Release by EPROMs:

- 128K EPROM:
When the customer releases his Mask ROM Data in the form of EPROMs, he should use 8 pcs of MBM27128 or equivalent and program data of 8 address blocks (Address 0 to 16K, 16K to 32K, 32K to 48K, 48K to 64K, 64K to 80K, 80K to 96K, 96K to 112K and 112K to 128K) of MB831000 to each MBM27128 EPROM. Fujitsu requires 3 sets, total 24 pcs, of such programmed EPROMs. (Two sets, total 16 pcs, are acceptable.)

In addition to the programmed sets, Fujitsu requires an additional set of blank EPROMs (8 pcs) for supplying customer ROM Data Code verification.

- 256K EPROM:
When the customer releases his Mask ROM Data in the form of EPROMs, he should use 4 pcs of MBM27C256 or equivalent and program data of 4 address blocks (Address 0 to 32K, 32K to 64K, 64K to 96K and 96K to 128K) of MB831000 to each MBM27C256 EPROM.

Fujitsu requires 3 sets, total 12 pcs, of such programmed EPROMs. (Two sets, total 8 pcs, are acceptable.)

In addition to the programmed sets, Fujitsu requires an additional set of blank EPROMs (4 pcs) for supplying customer ROM Data Code verification.

MSB LSB

A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	MBM27128 (No. 1: 0 to 16 K)													
0	0	1	MBM27128 (No. 2: 16 K to 32 K)													
0	1	0	MBM27128 (No. 3: 32 K to 48 K)													
0	1	1	MBM27128 (No. 4: 48 K to 64 K)													
1	0	0	MBM27128 (No. 5: 64 K to 80 K)													
1	0	1	MBM27128 (No. 6: 80 K to 96 K)													
1	1	0	MBM27128 (No. 7: 96 K to 112 K)													
1	1	1	MBM27128 (No. 8: 112 K to 128 K)													

MSB LSB

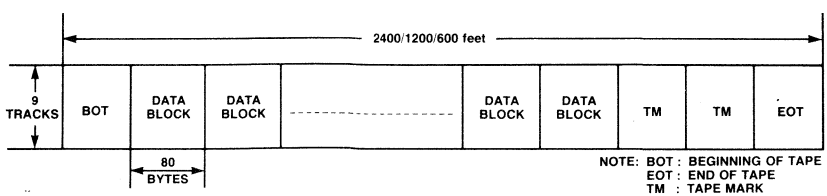
A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	MBM27C256 (No. 1: 0 to 32 K)														
0	1	MBM27C256 (No. 2: 32 K to 64 K)														
1	0	MBM27C256 (No. 3: 64 K to 96 K)														
1	1	MBM27C256 (No. 4: 96 K to 128 K)														

Mask ROM Code Data Release by Magnetic Tapes

When the customer releases his Mask ROM Code Data in the form of Magnetic Tapes (MT), he should use tapes that can be used on IBM compatible equipment and meet the following requirements.

- Physical Requirements:
  1 Length: 2400 feet, 1200 feet, or 600 feet
  2 Width: ½ inch
  3 Track: 9 tracks
  4 Density: 800 BPI or 1600 BPI

- MT Format:
  1 Label: No tape mark on the header of tape
  2 Record Size: 80 bytes/record
  3 Block Size: Single record/block
  4 File: Single file/volume
  5 Code Used: EBCDIC code



MB831000 ROM Code Data Input Formats:
(Continued)

- Data Block Format:

ROW NUMBER	1 9	10 15	16 19	20 67	68 72	73 80
	UNDEFINED FIELD	ADDRESS FIELD (1 HEAD ADDRESS)	UNDEFINED FIELD	DATA FIELD (16 WORDS)	UNDEFINED FIELD	SEQUENCE
NUMBER OF BYTE	9 BYTES	6 BYTES	4 BYTES	48 BYTES	5 BYTES	8 BYTES

NOTE: 1 BYTE/ROW

Undefined Field (Row 1 ~ 9/Row 16 ~ 19/Row 68 ~ 72):

In this field, blanks (ƀ) should be recorded.

Address Field (Row 10 ~ 15):

In the address field, the header address of the 16-word data that follow the address field should be recorded in the form of a five-digit hexadecimal number following a symbol "#". The correspondence of actual binary address to this hex address is shown in the following example.

	MSB																LSB
ADDRESS BIT	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
BINARY ADDRESS	0	0	0	1	1	1	0	1	1	1	0	0	1	0	0	1	0
HEX ADDRESS	0	3				B				9				2			
RECORDED FORM	#03B92																

Data Field (Row 20 ~ 67):

In this field, 16-word data with 16 successive addresses should be recorded in the form of two-digit hexadecimal numbers followed by a blank (ƀ). (The header data is for the address recorded in the address field.) The correspondence of actual binary data to this hex data is shown in the following example.

DATA BIT	08	07	06	05	04	03	02	01
BINARY DATA	1	1	1	1	0	0	1	0
HEX DATA	F				2			
RECORDED DATA	F2ƀ							

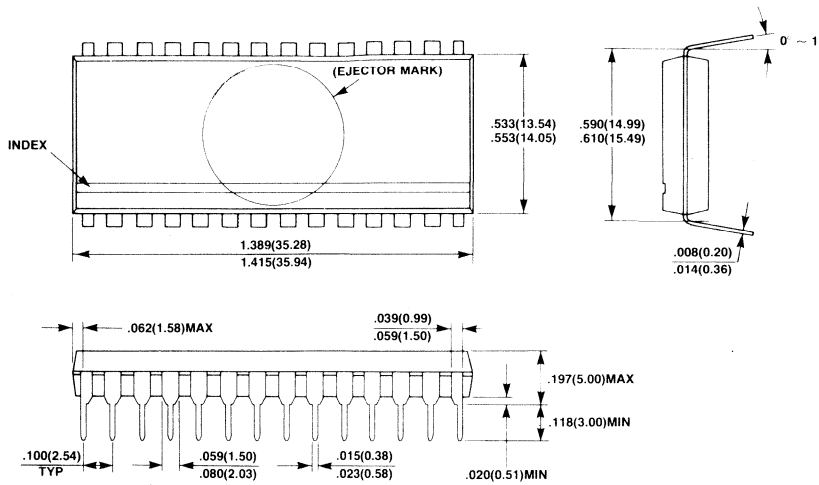
Sequence Number Field (Row 73 ~ 80)

In this field, the sequence number of each record (data block) should be recorded in the form of an eight-digit decimal number, which must be counted up by tens. All digits to the left of the most significant digit should be zeros, not blanks. Refer to the following example.

ADDRESS	DATA				SEQUENCE NO.
10 15	20 22	23 25		65 67	73 80
#03B92	F2ƀ	A0ƀ	----------	07ƀ	00000010

Package Dimensions
Dimensions in inches (millimeters)

28-Lead Plastic Dual In-Line Package (Case No.: DIP-28P-M02)



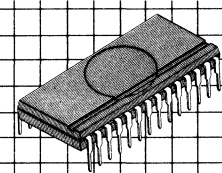
MB831124-35
1M-BIT (131,072×8) CMOS Read Only Memory

Description

The Fujitsu MB831124 is a CMOS Si-gate mask-programmable static read only memory organized as 131,072 words by 8 bits.

The MB831124 has TTL-compatible I/O and 3-state output level with $\overline{CE}$ clocked operation and single +5V power supply. The MB831124 is designed for applications such as character generator or program storage which require large memory capacity, high-speed and low power operation.

The package for the MB831124 is a standard 28-pin dual-in-line package.



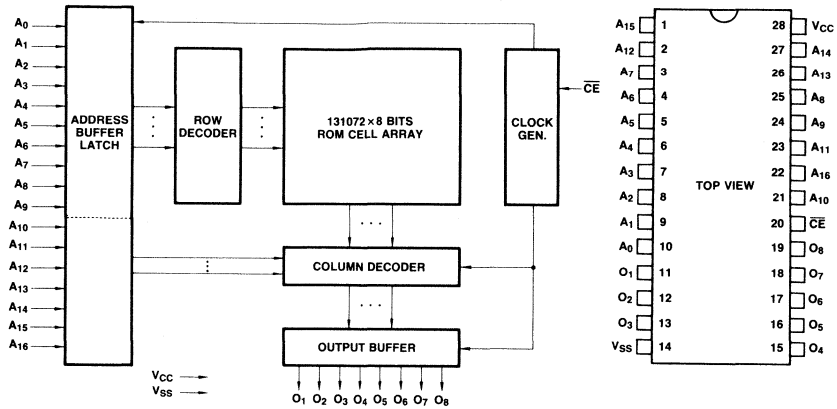
Plastic Package DIP-28P-M02

Features

- **Organization: 131,072 words × 8 bits**
- **Fast access time: 350 ns max. (MB831124-35)**
- **Fast cycle time: 460 ns max. (MB831124-35)**
- **Clocked control ($\overline{CE}$) periphery**
- **TTL compatible inputs/outputs**
- **Three-state outputs**
- **Single +5V supply, ±10% tolerance**
- **Power consumption: 138 mW (Operation) 5.5 mW (Standby, TTL input level) 0.165 mW (Standby, CMOS input level)**
- **Standard 28-pin DIP**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB831124 Block Diagram and Pin Assignment



Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +0.7	V
Input Voltage on Any Pin with respect to GND	V_{IN}	−0.5 to V_{CC} + 0.5	V
Output Voltage on Any Pin with respect to GND	V_{OUT}	−0.5 to V_{CC}+0.5	V
Temperature under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature	T_{STG}	−45 to + 125	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions
(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	−0.3		0.8	V
Input High Voltage	V_{IH}	2.2		V_{CC}+0.3	V
Ambient Temperature	T_A	0		70	°C

Capacitance
(T_A = 25°C, f = MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (V_{IN} = 0 V)	C_{IN}		10	pF
Output Capacitance (V_{OUT} = 0 V)	C_{OUT}		15	pF

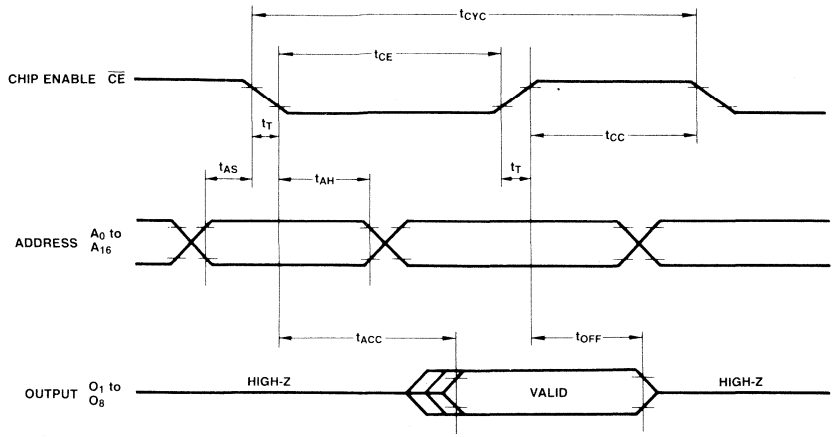
DC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Max	Unit
Input Leakage Current	V_{IN} = 0 V to V_{CC}	I_{LI}	−10	10	μA
Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0 V to V_{CC}	I_{LO}	−10	10	μA
Active Supply Current	t_{CYC} = 460 ns, t_{CE} = 350 ns	I_{CC1}		25	mA
Standby Supply Current	$\overline{CE}$ = V_{IH}	I_{SB1}		1	mA
Standby Supply Current	$V_{CC} - 0.2 \leq CE \leq V_{CC} + 0.2$	I_{SB2}		30	μA
Output Low Voltage	I_{OL} = 2.1 mA	V_{OL}		0.4	V
Output High Voltage	I_{OH} = −400 μA	V_{OH}	2.4		V

AC Characteristics
(Recommended operating conditions unless otherwise noted.)

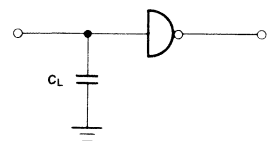
Parameters	Symbol	MB831124-35 Min	MB831124-35 Max	Unit	Conditions
Cycle Time	t_{CYC}	460		ns	$t_{CYC} = t_{CE} + t_{CC} + 2t_T$ t_T = 5 ns
Chip Enable Pulse Width	t_{CE}	350		ns	
Address Access Time	t_{ACC}		350	ns	
Output Disable Time	t_{OFF}		80	ns	
Address Setup Time	t_{AS}	0		ns	
Address Hold Time	t_{AH}	80		ns	
Chip Enable Off Time	t_{CC}	100		ns	

Timing Diagram



AC Test Conditions

Input Pulse Levels:	0.6 to 2.4 V
Input Pulse Rise and Fall Times:	5 ns
Timing Reference Levels:	Input: V_{IL} = 0.8 V, V_{IH} = 2.2 V Output: V_{OL} = 0.8 V, V_{OH} = 2.2 V
Output Load:	1 TTL Gate and C_L = 100 pF



MB831124 ROM Code Data Input Method

Mask ROM Code Data Release by EPROMs:

128K EPROM:

When the customer releases his Mask ROM Data in the form of EPROMs, he should use eight MBM27128 or equivalent and program data of 8 address blocks (Address 0 to 16 K, 16 K to 32 K, 32 K to 48 K, 48 K to 64 K, 64 K to 80 K, 80 K to 96 K, 96 K to 112 K and 112 K to 128 K) of the MB831124 to each MBM27128 EPROM. Fujitsu requires 3 sets, total 24 pcs, of such programmed EPROMs. (Two sets, total 16 pcs, are acceptable.)

In addition to the programmed sets, Fujitsu requires an additional set of blank EPROMs (8 pcs) for supplying customer ROM Data Code verification.

MSB LSB

A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	MBM27128 (No. 1: 0 to 16 K)													
0	0	1	MBM27128 (No. 2: 16 K to 32 K)													
0	1	0	MBM27128 (No. 3: 32 K to 48 K)													
0	1	1	MBM27128 (No. 4: 48 K to 64 K)													
1	0	0	MBM27128 (No. 5: 64 K to 80 K)													
1	0	1	MBM27128 (No. 6: 80 K to 96 K)													
1	1	0	MBM27128 (No. 7: 96 K to 112 K)													
1	1	1	MBM27128 (No. 8: 112 K to 128 K)													

256K EPROM:

When the customer releases his Mask ROM Data in the form of EPROMs, he should use four MBM27C256 or equivalent and program data of 4 address blocks (Address 0 to 32 K, 32 K to 64 K, 64 K to 96 K and 96 K to 128 K) of the MB831124 to each MBM27C256 EPROM.

Fujitsu requires 3 sets, total 12 pcs, of such programmed EPROMs. (Two sets, total 8 pcs, are acceptable.)

In addition to the programmed sets, Fujitsu requires an additional set of blank EPROMs (4 pcs) for supplying customer ROM Data Code verification.

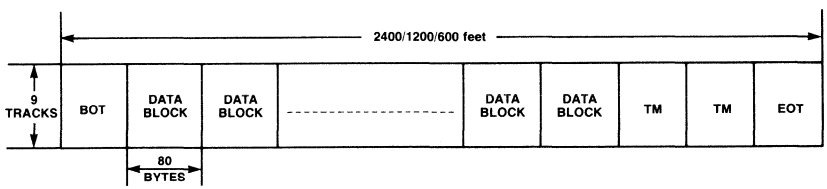
MSB LSB

A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	MBM27C256 (No. 1: 0 to 32 K)														
0	1	MBM27C256 (No. 2: 32 K to 64 K)														
1	0	MBM27C256 (No. 3: 64 K to 96 K)														
1	1	MBM27C256 (No. 4: 96 K to 128 K)														

Mask ROM Code Data Release by Magnetic Tapes:

When the customer releases his Mask ROM Code Data in the form of Magnetic Tapes (MT), he should use tapes that can be used on IBM compatible equipment and meet the following requirements.

- Physical Requirements:
  1. Length: 2400 feet, 1200 feet, or 600 feet
  2. Width: ½ inch
  3. Track: 9 tracks
  4. Density: 800 BPI or 1600 BPI
- MT Format:
  1. Label: No tape mark on the header of tape
  2. Record Size: 80 bytes/ record
  3. Block Size: Single record/ block
  4. File: Single file/volume
  5. Code Used: EBCDIC code



NOTE: BOT : BEGINNING OF TAPE
EOT : END OF TAPE
TM : TAPE MARK

■ Data Block Format:

ROW NUMBER	1 9	10 15	16 19	20 67	68 72	73 80
	UNDEFINED FIELD	ADDRESS FIELD (1 HEAD ADDRESS)	UNDEFINED FIELD	DATA FIELD (16 WORDS)	UNDEFINED FIELD	SEQUENCE
NUMBER OF BYTE	9 BYTES	6 BYTES	4 BYTES	48 BYTES	5 BYTES	8 BYTES

NOTE: 1 BYTE/ROW

Undefined Field (Row 1~9/ Row 16~19/Row 68~72):

In this field, blanks (ø) should be recorded.

Address Field (Row 10~15):

In the address field, the header address of the 16-word data that follows the address field should be recorded in the form of a five-digit hexadecimal number following a symbol "#". The corresponding binary address to this hex address is shown in the following example.

	MSB																LSB
ADDRESS BIT	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
BINARY ADDRESS	0	0	0	1	1	1	0	1	1	1	0	0	1	0	0	1	0
HEX ADDRESS	0	3				B				9				2			
RECORDED FORM	#03B92																

Data Field (Row 20~67):

In this field, 16-word data with 16 successive addresses should be recorded in the form of two-digit hexadecimal numbers followed by a blank (ø). (The header data is for the address recorded in the address field.) The corresponding binary data to this hex data is shown in the following example.

DATA BIT	08	07	06	05	04	03	02	01
BINARY DATA	1	1	1	1	0	0	1	0
HEX DATA	F				2			
RECORDED DATA	F2ø							

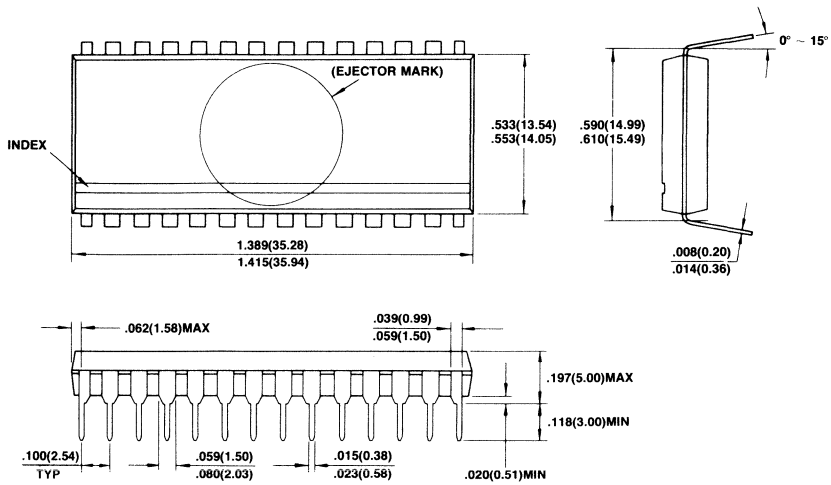
Sequence Number Field (Row 73~80):

In this field, the sequence number of each record (data block) should be recorded in the form of an eight-digit decimal number, which must be counted up by tens. All digits to the left of the most significant digit should be zeros, not blanks. Refer to the following example.

ADDRESS	DATA				SEQUENCE NO.
10 15	20 22	23 25		65 67	73 80
#03B92	F2ø	A0ø	----------	07ø	00000010

Package Dimensions
Dimensions in inches (millimeters)

28-Lead Plastic Dual In-Line Package (Case No.: DIP-28P-M02)



ECL RAMs

MBM10415AH 9-2
MBM10422A 9-8
MBM100422A 9-14
MBM10470A 9-20
MBM100470A 9-26
MBM10474A 9-31
MBM100474A 9-37
MBM10480 9-43
MBM100480 9-49
MBM10484 9-55
MBM100484 9-61
MBM10490 9-67
MBM100490 9-73
MB70801 9-79
MB70802 9-85
MB7700H Series 9-92
MBM93419 9-101

Advanced Information
MBM10422A 9-105
MBM100422A 9-106
MBM10474A 9-107
MBM100474A 9-108
MBM10480A 9-109
MBM100480A 9-110
MBM10484A/100484A 9-111
MBM10494/100494 9-112

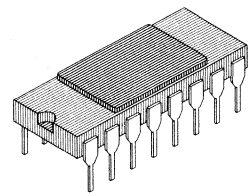
ECL 1024-BIT BIPOLAR RANDOM ACCESS MEMORY

DESCRIPTION

The Fujitsu MBM10415AH is a fully decoded 1024-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. It is organized as 1024 words by one bit, and features on-chip voltage compensation for improved noise margin.

The MBM10415AH offers extremely small cell and chip sizes, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MBM10415AH is specified over a temperature range of from 0°C to 75°C (ambient). It also features frit-sealed 16-pin dual in-line packaging, and is fully compatible with industry-standard 10K-series ECL families.

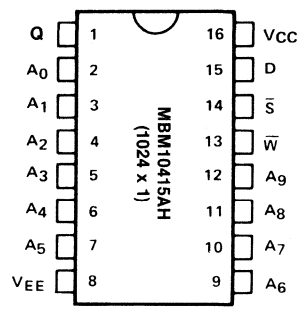


CERAMIC PACKAGE
DIP-16C-F01

FEATURES

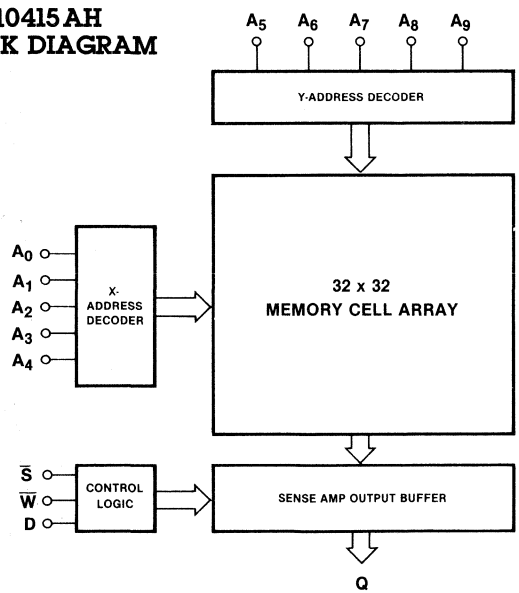
- **1024 words x 1-bit organization**
- **On-chip voltage compensation for improved noise margin**
- **Fully compatible with industry-standard 10K-series ECL families**
- **Address access time:**
  MBM10415AH: 20 ns Max.
- **Chip select access time:**
  MBM10415AH: 8 ns Max.
- **Open emitter output for ease of memory expansion**
- **Low power dissipation of 0.5mW/bit**
- **DOPOS and IOP processing**
- **Pin compatible with F10415 and MCM10146**

PIN ASSIGNMENT



*V_{CC} grounded

MBM10415AH BLOCK DIAGRAM



TRUTH TABLE

INPUT			OUTPUT	MODE
$\bar{S}$	$\bar{W}$	D_{IN}		
H	X	X	L	DISABLED
L	L	L	L	WRITE"L"
L	L	H	L	WRITE"H"
L	H	X	D_{OUT}	READ

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin (V_{CC})	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature Under Bias	T_A	−55 to +125	°C
Storage Temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature
Supply Voltage	V_{EE}	−5.46	−5.2	−4.94	V	0°C to +75°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	—	4	5	pF
Output Pin Capacitance	C_{OUT}	—	7	8	pF

DC CHARACTERISTICS

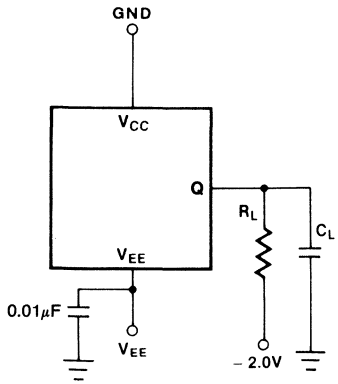
(V_{CC} = 0V, V_{EE} = −5.2V, Output load = 50Ω to −2.0V and Airflow ≥ 2.5 m/s unless otherwise noted.)

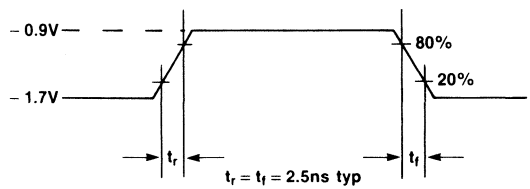
Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage ($V_{IN} = V_{IH\ max.}$ or $V_{IL\ min.}$)	V_{OH}	−1000 −960 −900	—	−840 −810 −720	mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IH\ max.}$ or $V_{IL\ min.}$)	V_{OL}	−1870 −1850 −1830	—	−1665 −1650 −1625	mV	0°C 25°C 75°C
Output High Voltage ($V_{IN} = V_{IH\ min.}$ or $V_{IL\ max.}$)	V_{OHC}	−1020 −980 −920	—	—	mV	0°C 25°C 75°C
Output Low Voltage ($V_{IN} = V_{IH\ min.}$ or $V_{IL\ max.}$)	V_{OLC}	—	—	−1645 −1630 −1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1145 −1105 −1045	—	−840 −810 −720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1870 −1850 −1830	—	−1490 −1475 −1450	mV	0°C 25°C 75°C
Input High Current ($V_{IN} = V_{IH\ max.}$)	I_{IH}	—	—	220	μA	0° to 75°C
Input Low Current ($V_{IN} = V_{IL\ min.}$)	I_{IL}	−50	—	—	μA	0° to 75°C
$\overline{S}$ Input Low Current ($V_{IN} = V_{IL\ min.}$)	I_{IL}	0.5	—	170	μA	0° to 75°C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	−125 −150	—	—	mA	75°C 0°C

AC CHARACTERISTICS

(Full Guaranteed Operating Ranges, Output Load = 50Ω to −2.0V and 30pf to GND and Airflow ≥ 2.5 m/s unless otherwise noted.)

AC TEST CONDITIONS





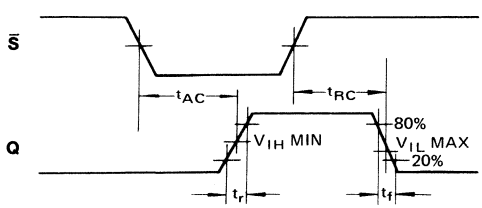
Output Load: RL = 50Ω
C_L = 30pF
(including jig and stray capacitance)

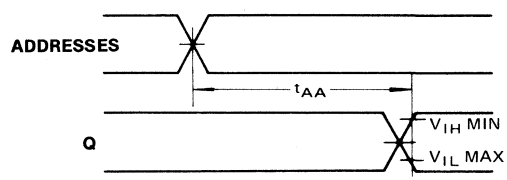
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	MBM10415AH Typ	MBM10415AH Max	Unit
Address Access Time	t_{AA}	13	20	ns
Chip Select Access Time	t_{AC}	5	8	ns
Chip Select Recovery Time	t_{RB}	5	8	ns

READ CYCLE

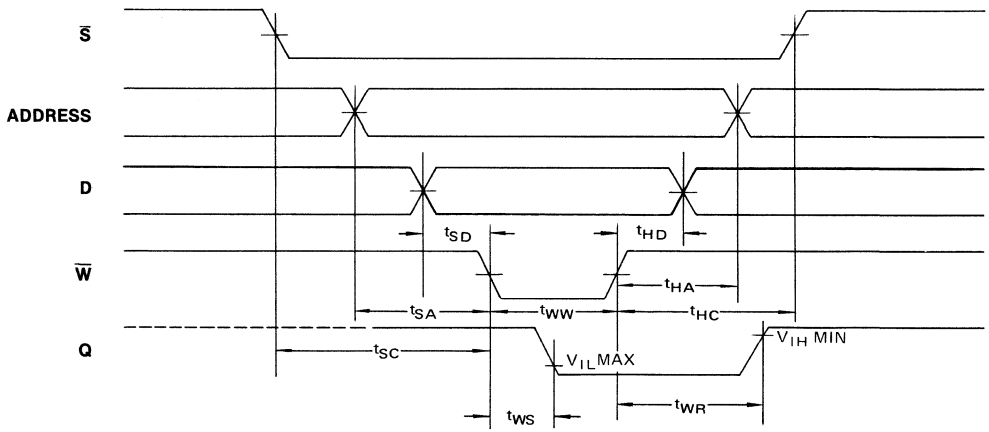




WRITE CYCLE

Parameter	Symbol	MBM10415AH			Unit
		Min	Typ	Max	
Write Pulse Width	t_{WW}	14	9	—	ns
Write Disable Time	t_{WS}	—	5	10	ns
Write Recovery Time	t_{WR}	—	5	10	ns
Address Set Up Time	t_{SA}	5	3	—	ns
Chip Select Set Up Time	t_{SC}	4	0	—	ns
Data Set Up Time	t_{SD}	4	0	—	ns
Address Hold Time	t_{HA}	3	0	—	ns
Chip Select Hold Time	t_{HC}	4	0	—	ns
Data Hold Time	t_{HD}	4	0	—	ns

WRITE CYCLE

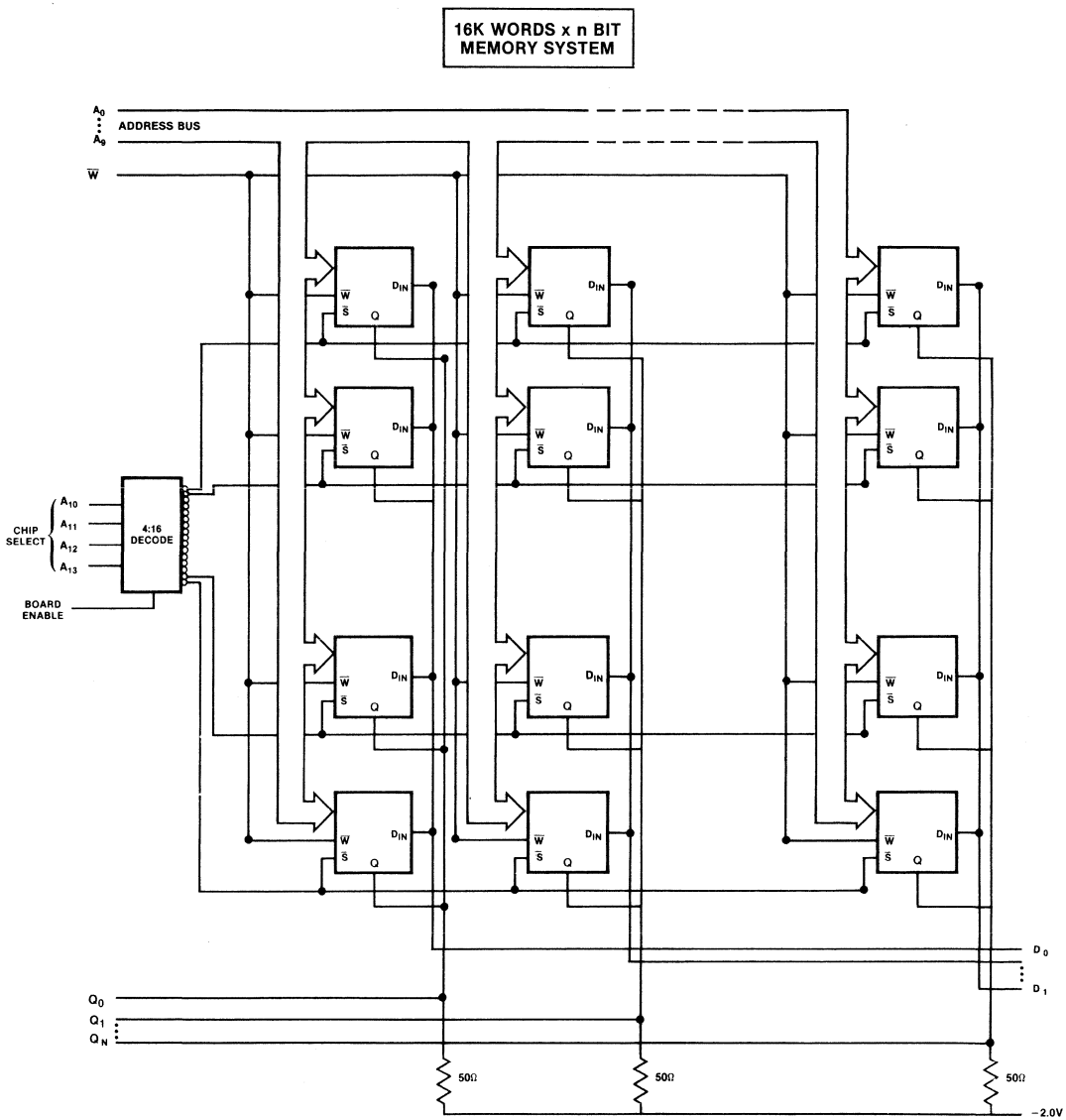


RISE TIME AND FALL TIME

Parameter	Symbol	MBM10415AH			Unit
		Min	Typ	Max	
Output Rise Time	t_r	—	5	—	ns
Output Fall Time	t_f	—	5	—	ns

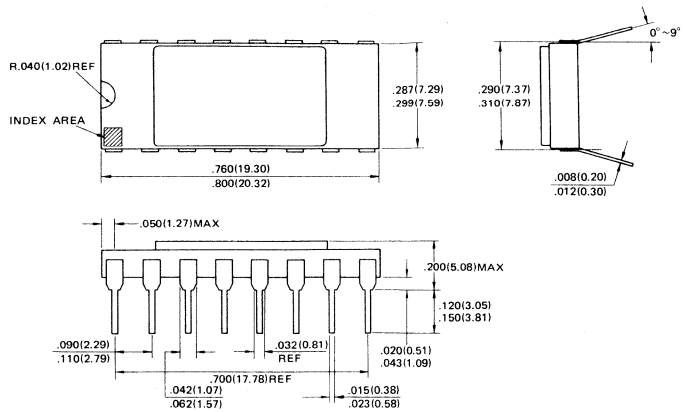
APPLICATIONS INFORMATION

LARGE SYSTEM APPLICATION



PACKAGE DIMENSIONS Dimensions in inches (millimeters)

16-LEAD CERAMIC (FRIT SEAL) DUAL IN-LINE PACKAGE
DIP-16C-F01



FUJITSU
MICROELECTRONICS, INC.

MBM10422A-7

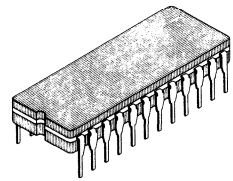
ECL 1024-BIT BIPOLAR RANDOM ACCESS MEMORY

DESCRIPTION

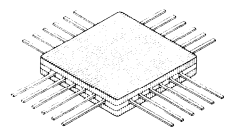
The Fujitsu MBM10422A is a fully decoded 1024-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 256 words by 4-bits and features on-chip voltage compensation for improved noise margin.

The MBM10422A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon), processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for MBM10422A is specified over a temperature range of 0°C to 75°C (T_A for DIP, T_C for flat package). It features cerdip 24-pin dual in-line and flat packaging, and is fully compatible with industry standard 10K-series ECL families.



CERDIP PACKAGE
DIP-24C-C05

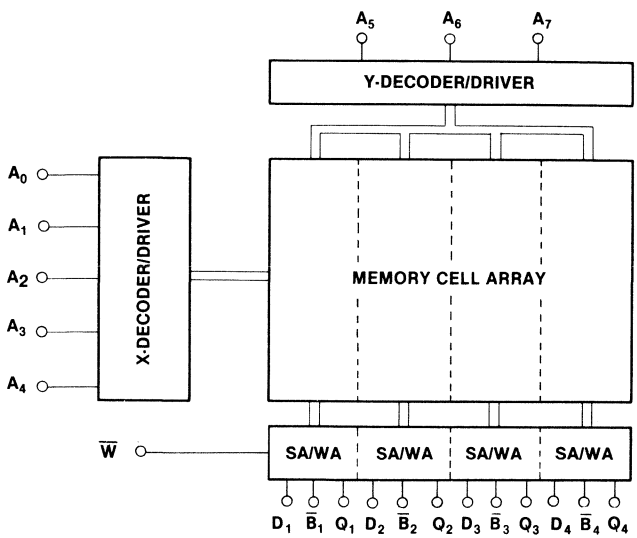


FLAT PACKAGE
FPT-24C-C02

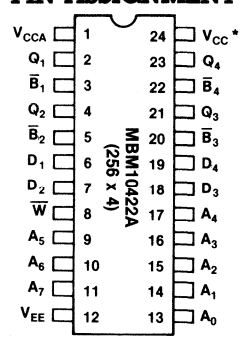
FEATURES

- **256 words x 4-bits organization**
- **On-chip voltage compensation for improved noise margin**
- **Fully compatible with industry-standard 10K-series ECL families**
- **Address access time: 7ns max.**
- **Block select access time: 5ns max.**
- **Open emitter output for easy memory expansion**
- **Power dissipation of 0.7 mW/bit**
- **DOPOS and IOP-II processing**
- **Pin compatible with F10422**

MBM10422 BLOCK DIAGRAM



PIN ASSIGNMENT



***V_{CC} Grounded**

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric field. It is therefore advised that normal precautions be taken to avoid appliction of any voltage higher than maximum rated voltages to this device.

TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{B}$	$\overline{W}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE"H"
L	L	L	L	WRITE"L"
L	H	X	DOUT	READ

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin (V_{CC})	V_{EE}	+0.5 to −7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	−30	mA
Temperature Under Bias	T_A	−55 to +125	°C
Storage Temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

GUARANTEED OPERATING CONDITIONS

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Temperature*
Supply Voltage	V_{EE}	−5.46	−5.2	−4.94	V	0 °C to +75 °C

* Ambient Temperature for DIP, case temperature for flat package

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}	—	4	5	pF
Output Pin Capacitance	C_{OUT}	—	6	8	pF

DC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −5.2V, Output load = 50Ω to −2.0V, T_A = 0 °C to 75 °C for DIP, T_C = 0 °C to 75 °C for flat package, and Airflow = ≥ 25 m/s, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output High Voltage ($V_{IN} = V_{IH\ max.}$ or $V_{IL\ min.}$)	V_{OH}	−1000 −960 −900	—	−840 −810 −720	mV	0 °C 25 °C 75 °C
Output Low Voltage ($V_{IN} = V_{IH\ max.}$ or $V_{IL\ min.}$)	V_{OL}	−1870 −1850 −1830	—	−1665 −1650 −1625	mV	0 °C 25 °C 75 °C
Output High Voltage ($V_{IN} = V_{IH\ min.}$ or $V_{IL\ max.}$)	V_{OHC}	−1020 −980 −920	—	—	mV	0 °C 25 °C 75 °C
Output Low Voltage ($V_{IN} = V_{IH\ min.}$ or $V_{IL\ max.}$)	V_{OLC}	—	—	−1645 −1630 −1605	mV	0 °C 25 °C 75 °C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	−1145 −1105 −1045	—	−840 −810 −720	mV	0 °C 25 °C 75 °C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	−1870 −1850 −1830	—	−1490 −1475 −1450	mV	0 °C 25 °C 75 °C
Input High Current ($V_{IN} = V_{IH\ max.}$)	I_{IH}	—	—	220	μA	0° to 75 °C
Input Low Current ($V_{IN} = V_{IL\ min.}$)	I_{IL}	−50	—	—	μA	0° to 75 °C
$\overline{B}$ Input Low Current ($V_{IN} = V_{IL\ min.}$)	I_{IL}	0.5	—	170	μA	0° to 75 °C
Power Supply Current (All Inputs and Outputs Open)	I_{EE}	−200	—	—	mA	0° to 75 °C

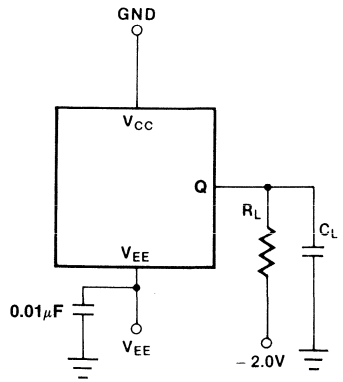
FUNCTIONAL DESCRIPTION

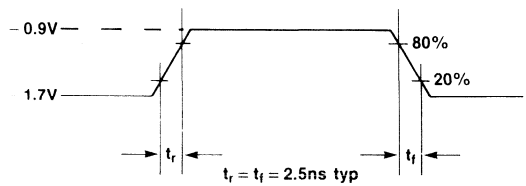
The Fujitsu MBM10422A-7 is fully decoded 1024-bit read/write random access memory organized as 256 words by 4-bits. Memory cell selection is achieved by means of a 8-bit address designated $A_0 \sim A_7$. The active low Block Select $\overline{B}$ input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable $\overline{W}$ input. With $\overline{W}$ and $\overline{B}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{W}$ is held high, while $\overline{B}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

AC CHARACTERISTICS

Output Load = 50Ω to −2.0V and 30pF to GND, T_A = 0°C to 75°C for DIP, T_C = 0°C to 75°C for flat package, and Airflow = ≥2.5 m/s, unless otherwise noted.

AC TEST CONDITIONS





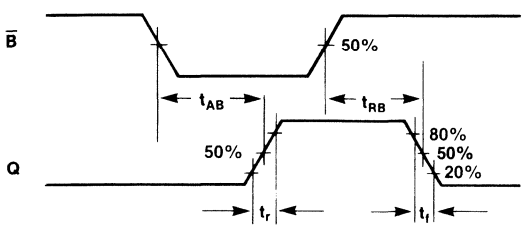
Output Load: RL = 50Ω
C_L = 30pF
(including jig and stray capacitance)

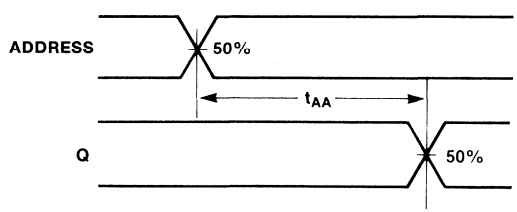
NOTE: All timing measurements referenced to 50% input levels.

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	—	5	7	ns
Block Select Access Time	t_{AB}	—	2.5	4	ns
Block Select Recovery Time	t_{RB}	—	2.5	4	ns

READ CYCLE TIMING DIAGRAMS

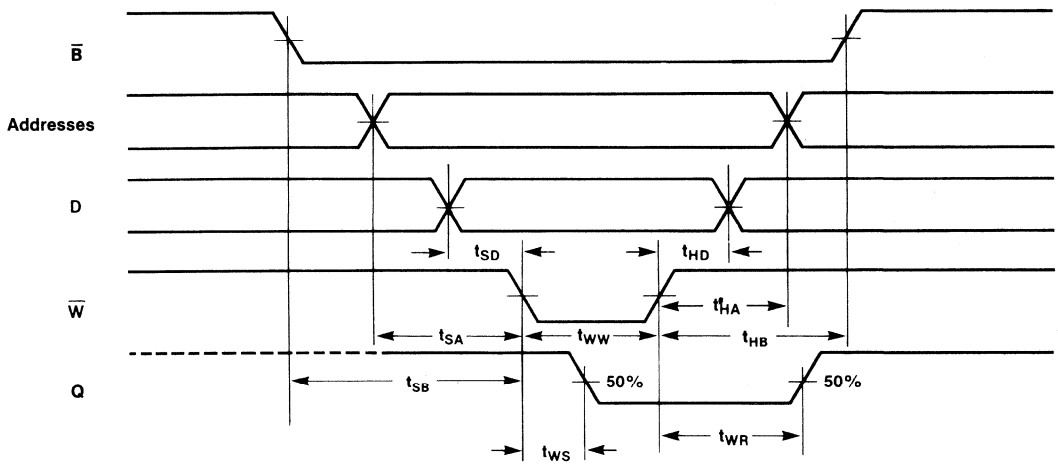




WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	5	—	—	ns
Write Disable Time	t_{WS}	—	—	4	ns
Write Recovery Time	t_{WR}	—	—	8	ns
Address Set Up Time	t_{SA}	1	—	—	ns
Block Select Set Up Time	t_{SB}	1	—	—	ns
Data Set Up Time	t_{SD}	1	—	—	ns
Address Hold Time	t_{HA}	1	—	—	ns
Block Select Hold Time	t_{HB}	1	—	—	ns
Data Hold Time	t_{HD}	1	—	—	ns

WRITE CYCLE

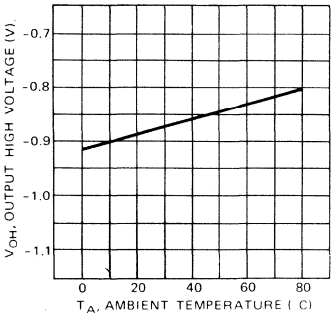


RISE TIME AND FALL TIME

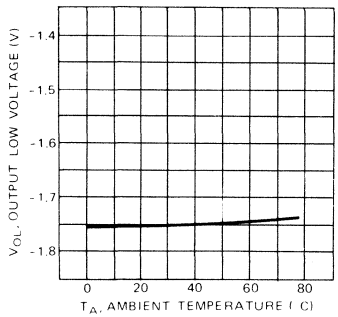
Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r	—	1.5	—	ns
Output Fall Time	t_f	—	1.5	—	ns

TYPICAL CHARACTERISTICS CURVES

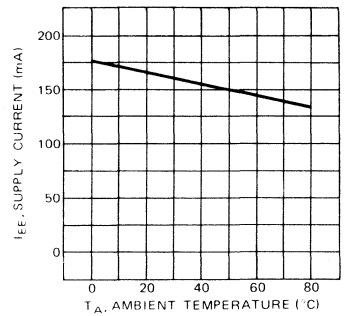
OUTPUT HIGH VOLTAGE
vs AMBIENT TEMPERATURE



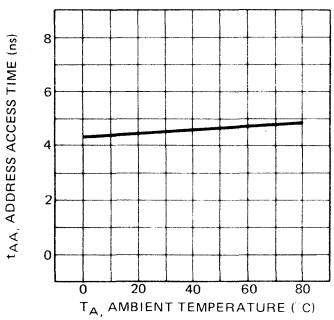
OUTPUT LOW VOLTAGE
vs AMBIENT TEMPERATURE



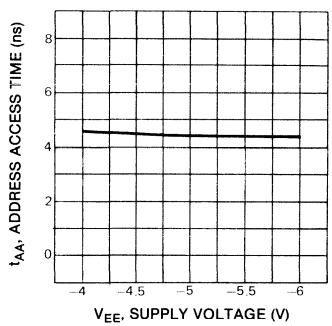
SUPPLY CURRENT
vs AMBIENT TEMPERATURE



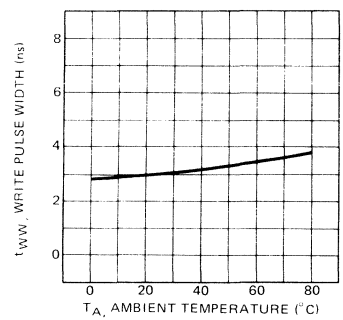
ADDRESS ACCESS TIME
vs AMBIENT TEMPERATURE



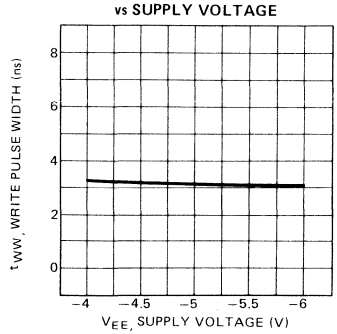
ADDRESS ACCESS TIME
vs SUPPLY VOLTAGE



WRITE PULSE WIDTH
vs AMBIENT TEMPERATURE

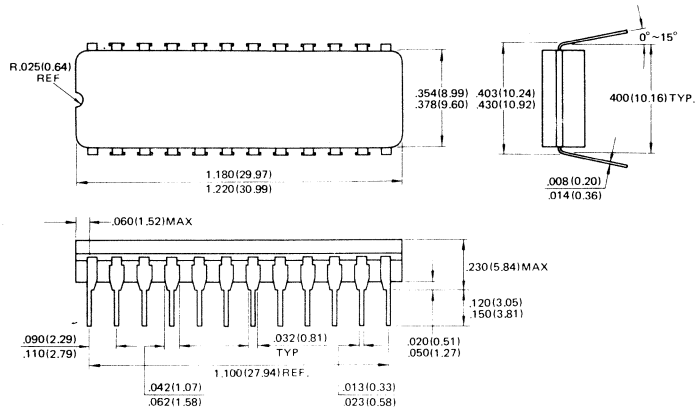


WRITE PULSE WIDTH
vs SUPPLY VOLTAGE

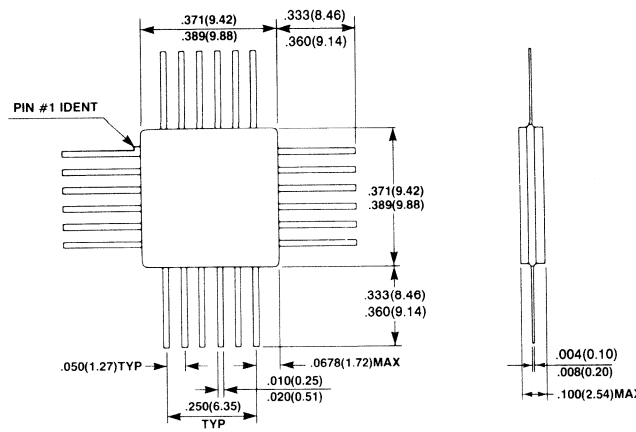


PACKAGE DIMENSIONS Dimensions in inches (millimeters)

24-LEAD CERDIP DUAL IN-LINE PACKAGE
DIP-24C-C05



24-LEAD CERDIP (FRIT SEAL) FLAT PACKAGE
FPT-24C-C02



MBM100422A-7

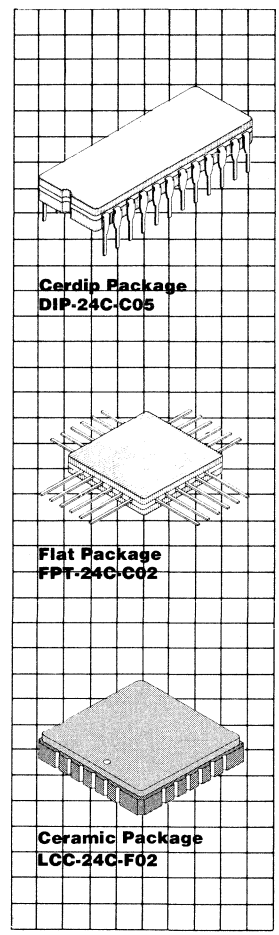
1024-Bit Bipolar ECL Random Access Memory

Description

The Fujitsu MBM100422A is a fully decoded 1024-bit ECL read/write random access memory designed for high speed scratch pad, control and buffer storage applications. This device is organized as 256 words by 4-bits, and it features on-chip voltage/temperature compensation for improved noise margin.

The MBM100422A offers extremely small cell and chip sizes, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

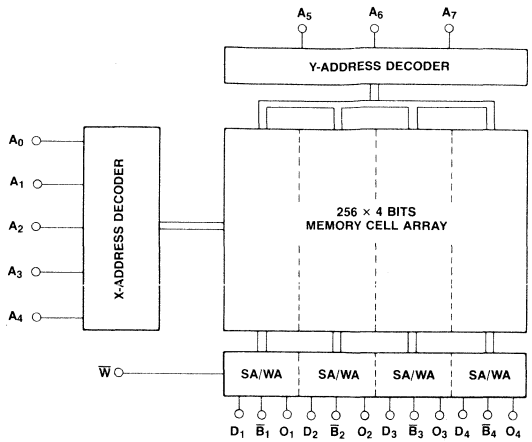
Operation for the MBM100422A is specified over a temperature range of 0°C to 85°C (ambient). It features cerdip 24-pin dual in-line or flat packaging, and is fully compatible with industry-standard 100K-series ECL families.

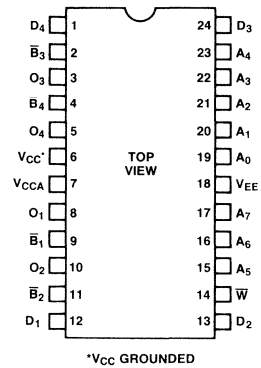


Features

- 256 words x 4-bits organization
- On-chip voltage/temperature compensation for improved noise margin
- Fully compatible with industry-standard 100K-series ECL families
- Address Access Time: 7ns max.
- Block Select Access Time: 4ns max.
- Open emitter output for easy memory expansion
- Low power dissipation of 0.7mW/bit
- DOPOS and IOP-II processing
- Pin compatible with the F100422

MBM100422A Block Diagram and Pin Assignment





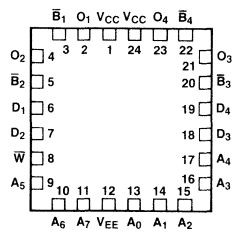
Dual In-Line Package

NOTE: DIP AND FLAT PACKAGE STYLES CONFORM TO THE SAME PIN ASSIGNMENT.

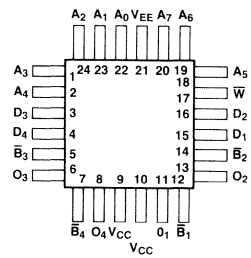
TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{B}$	$\overline{W}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	OUT	READ

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE



Leadless Chip Carrier



Flatpack

Functional Description

The Fujitsu MBM100422A is a fully decoded 1024-bit read/write random access memory organized as 256 words by 4 bits. Memory cell selection is achieved by means of a 8-bit address designated $A_0 \sim A_7$. The active low Block Select ($\overline{B}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{W}$) input. With $\overline{W}$ and $\overline{B}$ held low, the $\overline{B}$ data at D_{1-4} is written into the addressed location. To read, $\overline{W}$ is held high, while $\overline{B}$ is held low. Data at the addressed location is then transferred to OUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
V_{EE} pin potential to ground pin (V_{CC})	V_{EE}	+0.5 to −7.0	V
Input voltage	V_{IN}	+0.5 to V_{EE}	V
Output current (DC, output high)	I_{OUT}	−30	mA
Temperature under bias	T_A	−55 to +125	°C
Storage Temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

Guaranteed Operating Conditions
(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature
Supply voltage	V_{EE}	−5.7	−4.5	−4.2	V	0°C to +85°C

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input pin capacitance	C_{IN}		4		pF
Output pin capacitance	C_{OUT}		6		pF

DC Characteristics
(V_{CC} = 0V, V_{EE} = −4.5V, Output Load = 50Ω to −2.0V, T_A = 0°C to 85°C and Airflow ≥ 2.5 m/s, unless otherwise noted.)

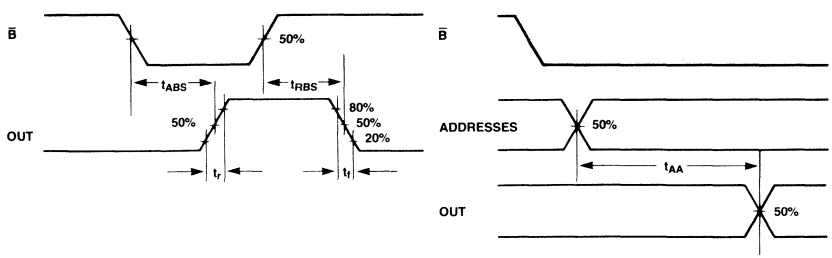
Parameter	Symbol	Min	Typ	Max	Unit
Output high voltage (V_{IN} = V_{IH} max. or V_{IL} min.)	V_{OH}	−1025		−880	mV
Output low voltage (V_{IN} = V_{IH} max. or V_{IL} min.)	V_{OL}	−1810		−1620	mV
Output high voltage (V_{IN} = V_{IH} min. or V_{IL} max.)	V_{OHC}	−1035			mV
Output low voltage (V_{IN} = V_{IH} min. or V_{IL} max.)	V_{OLC}			−1610	mV
Input high voltage (Guaranteed input voltage high for all inputs)	V_{IH}	−1165		−880	mV
Input low voltage (Guaranteed input voltage low for all inputs)	V_{IL}	−1810		−1475	mV
Input high current (V_{IN} = V_{IH} max.)	I_{IH}			220	μA
Input low current (V_{IN} = V_{IL} min.)	I_{IL}	−50			μA
$\overline{B}$ input low current (V_{IN} = V_{IL} min.)	I_{IL}	0.5		170	μA
Power supply current (All inputs and outputs open)	I_{EE}	−200			mA

AC Characteristics
(V_{CC} = 0V, V_{EE} = −4.5V ±5%, T_A = 0°C to 85°C, Output Load = 50Ω to −2.0V and 30 pF to GND, and Airflow ≥ 2.5 m/s; unless otherwise noted.)

Read Cycle

Parameter	Symbol	Min	Typ	Max	Unit
Address access time	t_{AA}		5	7	ns
Block select access time	t_{ABS}		2.5	4	ns
Block select recovery time	t_{RBS}		2.5	4	ns

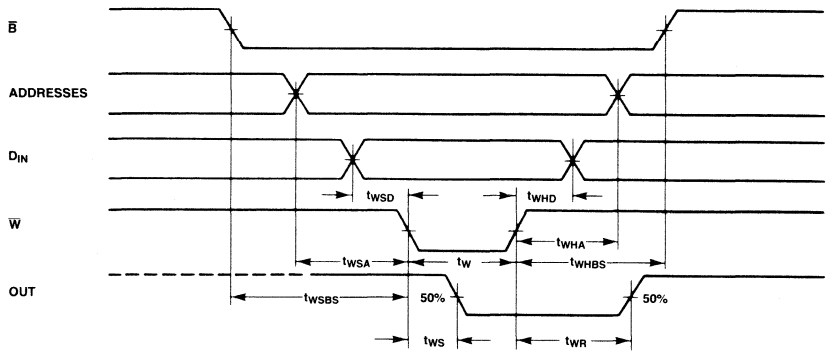
Read Cycle



Write Cycle

Parameter	Symbol	Min	Typ	Max	Unit
Write pulse width	t_W	5			ns
Write disable time	t_{WS}			4	ns
Write recovery time	t_{WR}			8	ns
Address set up time	t_{WSA}	1			ns
Block select set up time	t_{WSBS}	1			ns
Data set up time	t_{WSD}	1			ns
Address hold time	t_{WHA}	1			ns
Block select hold time	t_{WHBS}	1			ns
Data hold time	t_{WHD}	1			ns

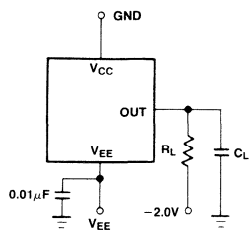
Write Cycle

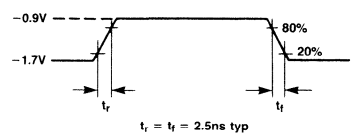


Rise Time and Fall Time

Parameter	Symbol	Min	Typ	Max	Unit
Output rise time	t_r		2		ns
Output fall time	t_f		2		ns

AC Test Conditions



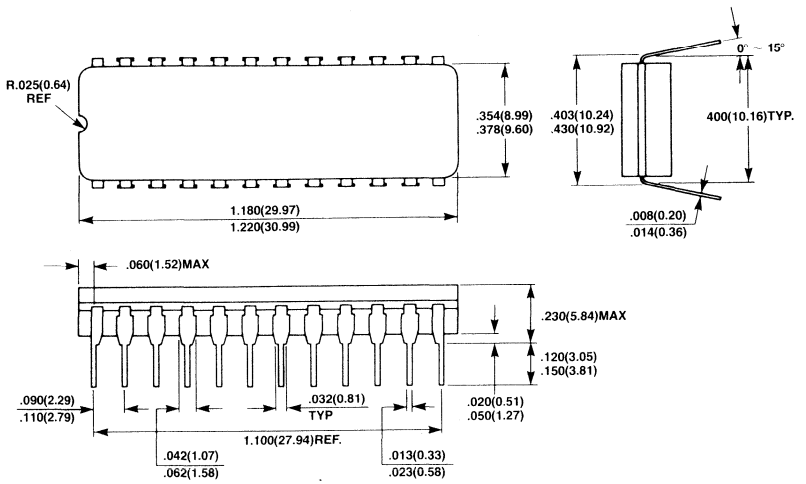


OUTPUT LOAD: $R_L = 50\Omega$
$C_L = 30pF$
(INCLUDING PROBE AND STRAY CAPACITANCE)

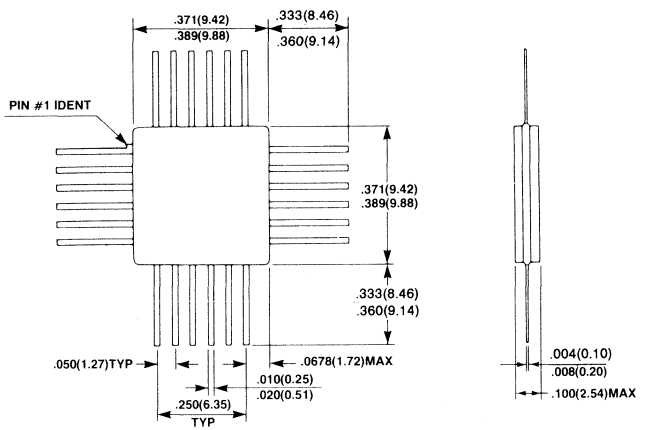
NOTE: ALL TIMING MEASUREMENTS REFERENCED TO 50% INPUT LEVELS.

Package Dimensions
Dimensions in inches
(millimeters)

24-Lead Cerdip Dual In-Line Package
DIP-24C-C05

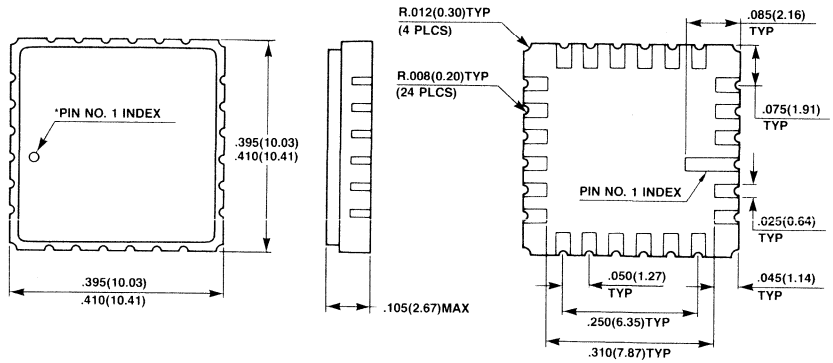


24-Lead Cerdip (Frit Seal) Flat Package
FPT-24C-C02



Package Dimensions
Dimensions in Inches
(millimeters)

24-Pad Ceramic (Frit Seal) Leadless Chip Carrier
(Case No.: LCC-24C-F02)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

MBM10470A-10, MBM10470A-15, MBM10470A-20

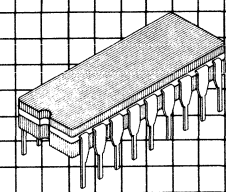
4096-Bit Bipolar ECL Random Access Memory

Description

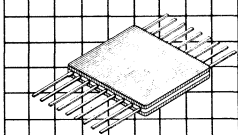
The Fujitsu MBM10470A is a fully decoded 4096-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by one bit, and it features on-chip voltage compensation for improved noise margin.

The MBM10470A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon), processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

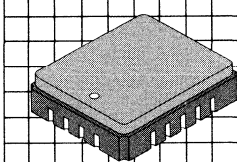
Operation for the MBM10470A is specified over a temperature range of from 0° to 75°C (ambient). It also feature 18-pin dual-in-line ceramic packaging, and is fully compatible with industry-standard 10K-series ECL families.



Ceramic Package
DIP-18C-C01



Ceramic Package
FPT-18C-C01



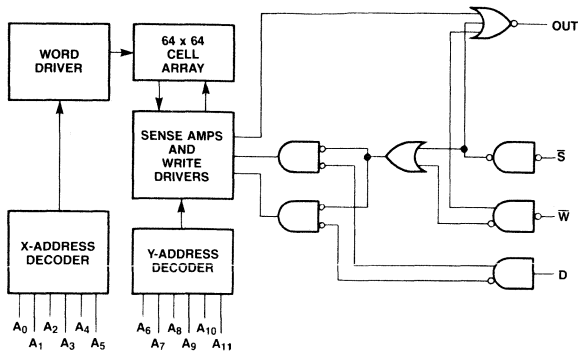
Ceramic Package
LCC-18C-F01

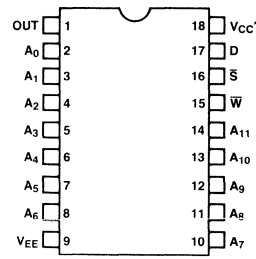
Features

- **4096 words x 1 bit organization**
- **On-chip voltage compensation for improved noise margin**
- **Fully compatible with industry-standard 10K-series ECL families**
- **Address access time:**
  10 nsec. max. (MBM10470A-10)
  15 nsec. max. (MBM10470A-15)
  20 nsec. max. (MBM10470A-20)
- **Chip select access time:**
  6 nsec. max. (MBM10470A-10)
  8 nsec. max. (MBM10470A-15)
  15 nsec. max. (MBM10470A-20)
- **Open emitter output for ease of memory expansion**
- **Low power dissipation for 0.22mW/bit**
- **DOPOS and IOP-II processing**
- **Pin compatible with the F10470**

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

MBM10470A Block Diagram and Pin Assignment





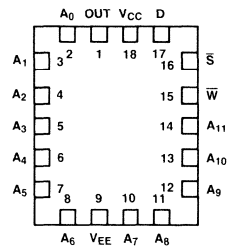
Dual In-Line Package

TRUTH TABLE

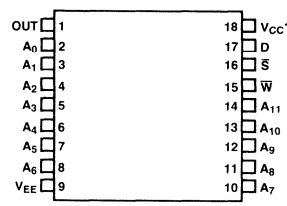
INPUT			OUTPUT	MODE
$\overline{S}$	$\overline{W}$	$\overline{D}$		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	OUT	READ

X = HIGH VOLTAGE LEVEL X = DON'T CARE

L = LOW VOLTAGE LEVEL



Leadless Chip Carrier



*VCC GROUNDED

Flat Package

Functional Description

The Fujitsu MBM10470A is a fully decoded 4096-bit read/write random access memory organized as 4096 words by one bit. Memory cell selection is achieved by means of a 12-bit address designated $A_0 \sim A_{11}$. The active low Chip Select ($\overline{S}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{W}$) input. With $\overline{W}$ and $\overline{S}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{W}$ is held high, while $\overline{S}$ is held low. Data at the addressed location is then transferred to OUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

Absolute Maximum Ratings
(See Note)

Parameter	Symbol	Value	Unit
V_{EE} pin potential to ground pin	V_{EE}	+0.5 to −7.0	V
Input voltage	V_{IN}	+0.5 to V_{EE}	V
Output current (DC, output high)	I_{OUT}	−30	mA
Temperature under bias	T_A	−55 to +125	°C
Storage temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Guaranteed Operating Conditions
(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature
Supply voltage	V_{EE}	−5.46	−5.2	−4.94	V	0°C to 75°C

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input pin capacitance	C_{IN}		4		pF
Output pin capacitance	C_{OUT}		6		pF

DC Characteristics

(V_{CC} = 0V, V_{EE} = −5.2V, Output Load = 50Ω to −2.0V, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output high voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	−1000 −960 −900		−840 −810 −720	mV	0°C 25°C 75°C
Output low voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	−1870 −1850 −1830		−1665 −1650 −1625	mV	0°C 25°C 75°C
Output high voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	−1020 −980 −920			mV	0°C 25°C 75°C
Output low voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			−1645 −1630 −1605	mV	0°C 25°C 75°C
Input high voltage (guaranteed input voltage high for all inputs)	V_{IH}	−1145 −1105 −1045		−840 −810 −720	mV	0°C 25°C 75°C
Input low voltage (guaranteed input voltage low for all inputs)	V_{IL}	−1870 −1850 −1830		−1490 −1475 −1450	mV	0°C 25°C 75°C
Input high current ($V_{IN} = V_{IH\ max}$)	I_{IH}			−220	μA	0°C to 75°C
Input low current ($V_{IN} = V_{IL\ min}$)	I_{IL}	−50			μA	0°C to 75°C
$\overline{S}$ input low current ($V_{IN} = V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power supply current (all inputs and output open)	I_{EE}	−200			mA	0°C to 75°C

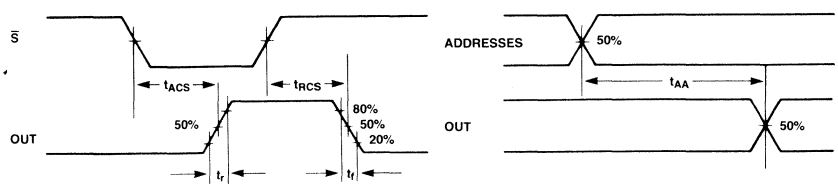
AC Characteristics

(Full Guaranteed Operating Ranges, Output Load = 50Ω to −2.0V and 30pF to GND, and Airflow ≥ 2.5 m/s, unless otherwise noted.)

Read Cycle

		MBM10470A-10			MBM10470A-15			MBM10470A-20			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
Address access time	t_{AA}			10			15			20	ns
Chip select access time	t_{ACS}			6			8			15	ns
Chip select recovery time	t_{RCS}			6			8			15	ns

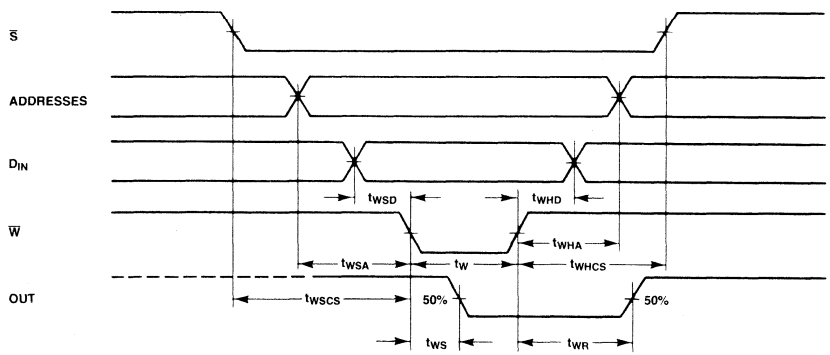
Read Cycle Timing Diagrams



Write Cycle

Parameter	Symbol	MBM10470A-10 Min	MBM10470A-10 Typ	MBM10470A-10 Max	MBM10470A-15 Min	MBM10470A-15 Typ	MBM10470A-15 Max	MBM10470A-20 Min	MBM10470A-20 Typ	MBM10470A-20 Max	Unit
Write pulse width	t_W	12			15			15			ns
Write disable time	t_{WS}			6			8			15	ns
Write recovery time	t_{WR}			10			10			15	ns
Address set up time	t_{WSA}	1			1			3			ns
Chip select set up time	t_{WSCS}	1			1			2			ns
Data set up time	t_{WSD}	1			1			2			ns
Address hold time	t_{WHA}	2			2			2			ns
Chip select hold time	t_{WHCS}	2			2			2			ns
Data hold time	t_{WHD}	2			2			2			ns

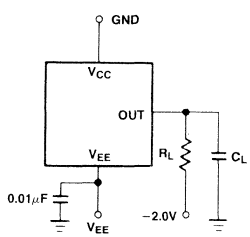
Write Cycle Timing Diagram

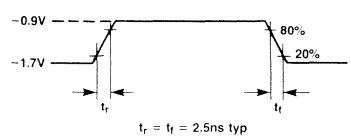


Rise Time and Fall Time

Parameter	Symbol	MBM10470A-10 Min	MBM10470A-10 Typ	MBM10470A-10 Max	MBM10470A-15 Min	MBM10470A-15 Typ	MBM10470A-15 Max	MBM10470A-20 Min	MBM10470A-20 Typ	MBM10470A-20 Max	Unit
Output rise time	t_r		1.5			1.5			1.5		ns
Output fall time	t_f		1.5			1.5			1.5		ns

AC Test Conditions





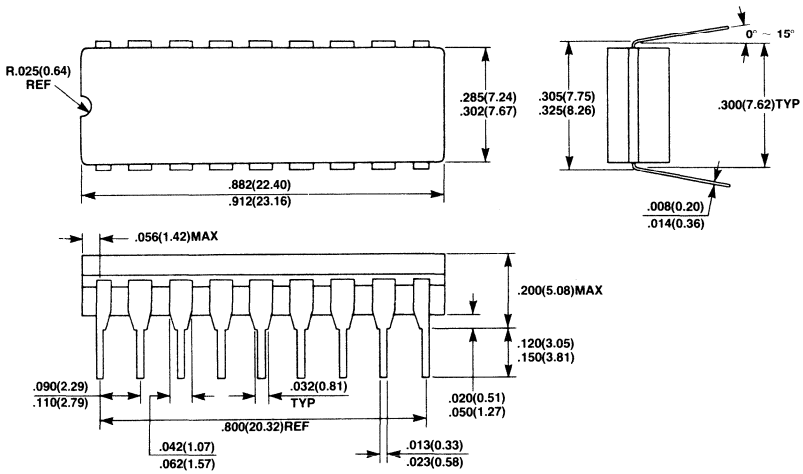
$t_r = t_f = 2.5$ns typ

OUTPUT LOAD: $R_L = 50\Omega$
$C_L = 30$pF
(INCLUDING PROBE AND STRAY CAPACITANCE)

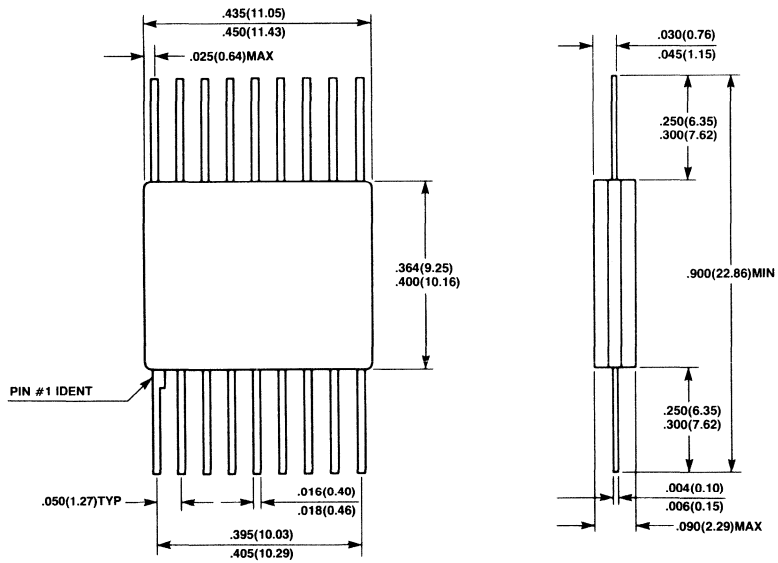
NOTE: ALL TIMING MEASUREMENTS REFERENCED TO 50% INPUT LEVELS.

Package Dimensions
Dimensions in inches
(millimeters)

18-Lead Ceramic (Cerdip) Dual In-Line Package
(Case No.: DIP-18C-C01)

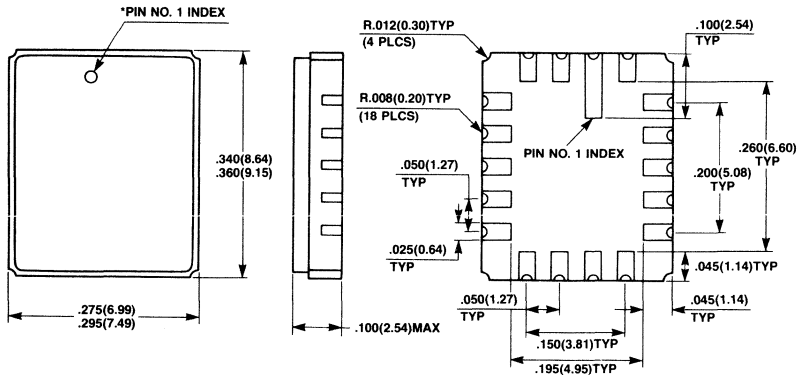


18-Lead Ceramic (CERDIP) Flat Package
(Case No.: FPT-18C-C01)



Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

18-Pad Ceramic (Frit Seal) Leadless Chip Carrier
(Case No.: LCC-18C-F01)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

FUJITSU

MBM100470A-10, MBM100470A-15

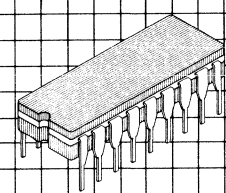
4096-Bit Bipolar ECL Random Access Memory

Description

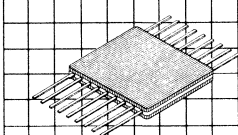
The Fujitsu MBM100470A is a fully decoded 4096-bit ECL read/write access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 4096 words by one bit, and it features on-chip voltage/temperature compensation for improved noise margin.

The MBM100470A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon), processing.

Operation for the MBM100470A is specified over a temperature range of from 0° to 85°C (T_A for DIP, T_C for Flat Package). It also features 18-pin Ceramic DIP and Flat Package, and is fully compatible with industry-standard 100K-series ECL families.



Ceramic Package
DIP-18C-C01



Ceramic Package
FPT-18C-C01

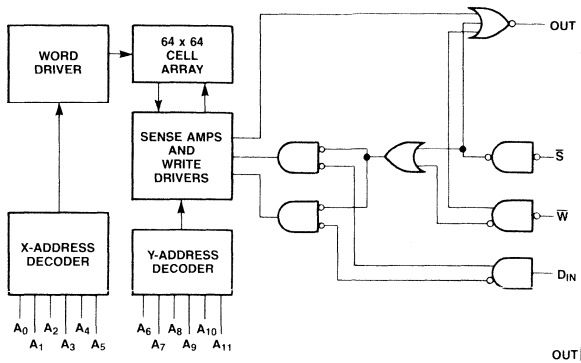
LCC-18C-F01

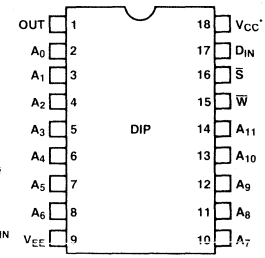
Features

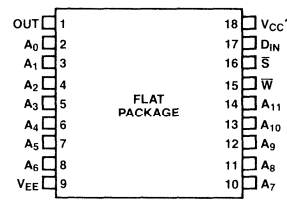
- **4096 words x 1 bit organization**
- **On-chip voltage/ temperature compensation for improved noise margin**
- **Fully compatible with industry-standard 100K-series ECL families**
- **Address access time: 10 nsec. max. (MBM100470A-10) 15 nsec. max. (MBM100470A-15)**
- **Chip select access time: 6 nsec. max. (MBM100470A-10) 8 nsec. max. (MBM100470A-15)**
- **Open emitter output for ease of memory expansion**
- **Low power dissipation of 0.19mW/bit**
- **DOPOS and IOP-II processing**
- **Pin compatible with the F100470**

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

MBM100470A Block Diagram and Pin Assignments







*VCC GROUNDED

TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{S}$	$\overline{W}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	OUT	READ

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE

Functional Description

The Fujitsu MBM100470A is fully decoded 4096-bit read/write random access memory organized as 4096 words by one bit. Memory cell selection is achieved by means of a 12-bit address designated $A_0 \sim A_{11}$. The active low Chip Select ($\overline{S}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{W}$) input. With $\overline{W}$ and $\overline{S}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{W}$ is held high, while $\overline{S}$ is held low. Data at the addressed location is then transferred to OUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
V_{EE} pin potential to ground pin	V_{EE}	+0.5 to −7.0	V
Input voltage	V_{IN}	+0.5 to V_{EE}	V
Output current (DC, output high)	I_{OUT}	−30	mA
Temperature under bias	T_A for DIP	−55 to +125	°C
	T_C for flat package	−55 to +125	
Storage temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Guaranteed Operating Conditions
(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP / Case Temperature for Flat Package
Supply voltage	V_{EE}	−5.7	−4.5	−4.2	V	0°C to 85°C

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input pin capacitance	C_{IN}		4		pF
Output pin capacitance	C_{OUT}		6		pF

DC Characteristics

(V_{CC} = 0V, V_{EE} = −4.5V, Output Load = 50Ω and 30pF to −2.0V, T_A = 0°C to 85°C for DIP, T_C = 0°C to 85°C for Flat Package, Airflow ≥ 2.5 m/s, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Output high voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	−1025		−880	mV
Output low voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	−1810		−1620	mV
Output high voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	−1035			mV
Output low voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			−1610	mV
Input high voltage (guaranteed input voltage high for all inputs)	V_{IH}	−1165		−880	mV
Input low voltage (guaranteed input voltage low for all inputs)	V_{IL}	−1810		−1475	mV
Input high current ($V_{IN} = V_{IH\ max}$)	I_{IH}			220	μA
Input low current ($V_{IN} = V_{IL\ min}$)	I_{IL}	−50			μA
$\overline{S}$ input low current ($V_{IN} = V_{IL\ min}$)	I_{IL}	0.5		170	μA
Power supply current (all inputs and output open)	I_{EE}	−200			mA

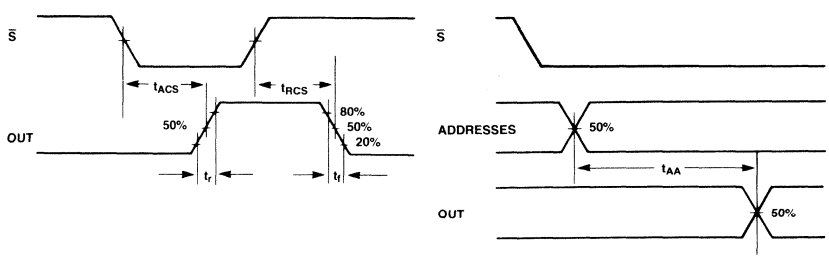
AC Characteristics

(V_{CC} = 0V, V_{EE} = −4.5V ± 5%, Ouput Load = 50Ω to −2.0V and 30pF to GND, T_A = 0°C to 85°C for DIP, T_C = 0°C to 85°C for Flat Package, Airflow ≥ 2.5 m/s, unless otherwise noted.)

Read Cycle

		MBM100470A-10			MBM100470A-15			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit
Address access time	t_{AA}			10			15	ns
Chip select access time	t_{ACS}			6			8	ns
Chip select recovery time	t_{RCS}			6			8	ns

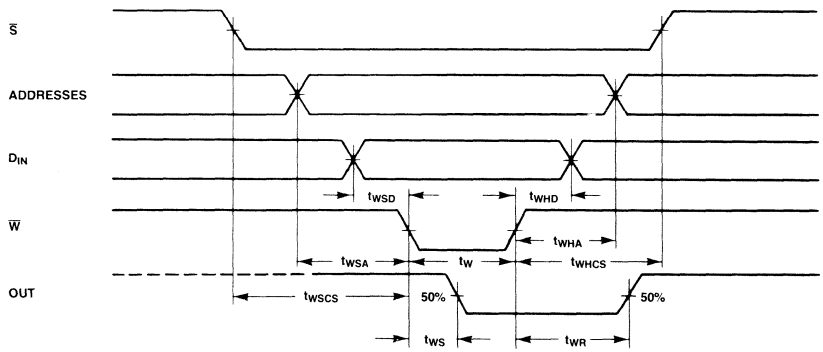
Read Cycle Timing Diagrams



Write Cycle

Parameter	Symbol	MBM100470A-10 Min	Typ	Max	MBM100470A-15 Min	Typ	Max	Unit
Write pulse width	t_W	12			15			ns
Write disable time	t_{WS}			6			8	ns
Write recovery time	t_{WR}			12			12	ns
Address set up time	t_{WSA}	1			1			ns
Chip select set up time	t_{WSCS}	1			1			ns
Data set up time	t_{WSD}	1			1			ns
Address hold time	t_{WHA}	2			2			ns
Chip select hold time	t_{WHCS}	2			2			ns
Data hold time	t_{WHD}	2			2			ns

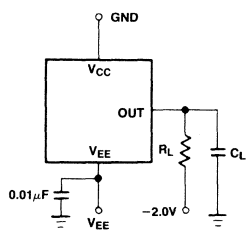
Write Cycle Timing Diagram

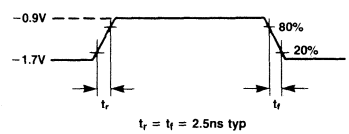


Rise Time and Fall Time

Parameter	Symbol	Min	Typ	Max	Unit
Output rise time	t_r		1.5		ns
Output fall time	t_f		1.5		ns

AC Test Conditions



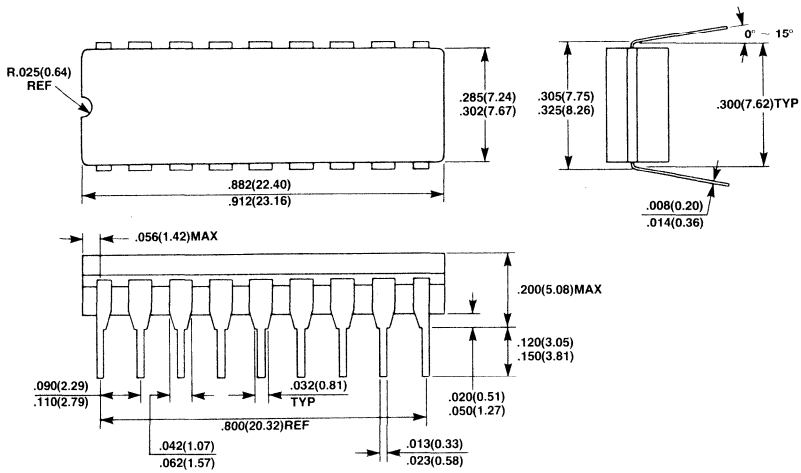


OUTPUT LOAD: $R_L = 50\Omega$
$C_L = 30pF$
(INCLUDING PROBE AND STRAY CAPACITANCE)

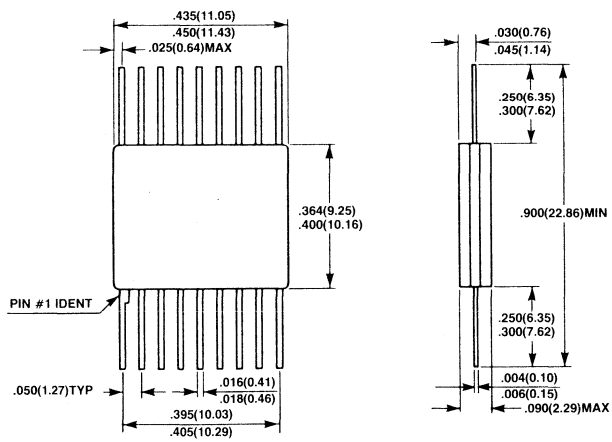
NOTE: ALL TIMING MEASUREMENTS REFERENCED TO 50% INPUT LEVELS.

Package Dimensions
Dimensions in inches
(millimeters)

18-Lead Ceramic (CERDIP) Dual In-Line Package
(Case No.: DIP-18C-C01)



18-Lead Ceramic (CERDIP) Flat Package
(Case No.: FPT-18C-C01)



FUJITSU

MBM10474A-10, MBM10474A-15

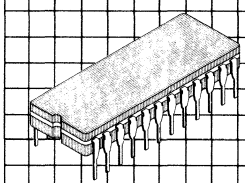
4096-Bit Bipolar ECL Random Access Memory

Description

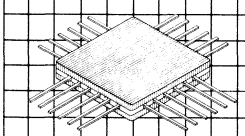
The Fujitsu MBM10474A is a fully decoded 4096-bit ECL read/write random access memory designed for high speed scratch pad, control and buffer storage applications. This device is organized as 1024 words by 4 bits, and it features on-chip voltage compensation for improved noise margin.

The MBM10474A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

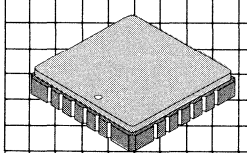
Operation for the MBM10474A is specified over a temperature range of from 0°C to 75°C (T_A for DIP, T_C for Flat Package and LCC). It also features 24-pin Ceramic DIP, Flat Package, or LCC, and is fully compatible with industry standard 10K-series ECL families.



Ceramic Package
DIP-24C-C05



Ceramic Package
FPT-24C-C02



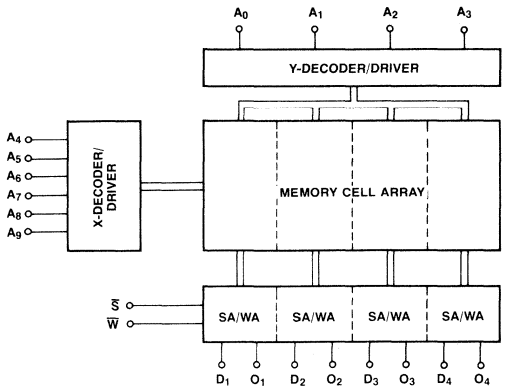
Ceramic Package
LCC-24C-F02

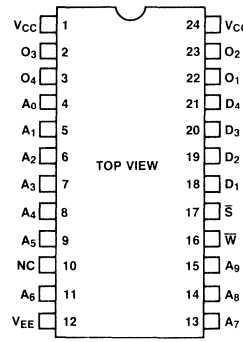
Features

- **1024 words × 4 bits organization**
- **On-chip voltage compensation for improved noise margin**
- **Fully compatible with industry standard 10K-series ECL families**
- **Address access time:**
  10 ns max. (MBM10474A-10)
  15 ns max. (MBM10474A-15)
- **Chip select access time:**
  6 ns max. (MBM10474A-10)
  8 ns max. (MBM10474A-15)
- **Open emitter output for ease of memory expansion**
- **Low power dissipation of**
  0.26 mW/bit typ. (MBM10474A-10)
  0.20 mW/bit typ. (MBM10474A-15)
- **DOPOS and IOP-II**

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

MBM10474A Block Diagram and Pin Assignments



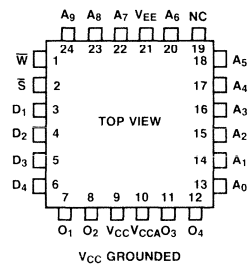


Dual Inline Package

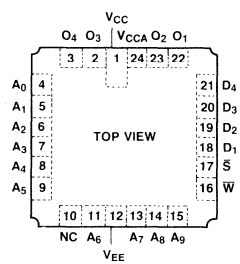
TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{S}$	$\overline{W}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	OUT	READ

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE



Flatpack



Leadless Chip Carrier

Functional Description

The Fujitsu MBM10474A is a fully decoded 4096 bit read/write random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designed A_0 through A_9. The active low Chip Select ($\overline{S}$) input is provided for memory expansion. The read and write operations are controlled by the state of the Enable ($\overline{W}$) input. With $\overline{W}$ and $\overline{S}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{W}$ is held high, while $\overline{S}$ is held low. Data at the addressed location is then transferred to OUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
V_{EE} pin potential to ground pin	V_{EE}	+0.5 to −7.0	V
Input voltage	V_{IN}	+0.5 to V_{EE}	V
Output current (DC, output high)	I_{OUT}	−30	mA
Temperature under bias	T_A for DIP	−55 to +125	°C
	T_C for flat package and LCC	−55 to +125	°C
Storage temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Guaranteed Operating Conditions
(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply voltage	V_{EE}	−5.46	−5.2	−4.94	V	0°C to 75°C

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input pin capacitance	C_{IN}		4	5	pF
Output pin capacitance	C_{OUT}		6	8	pF

DC Characteristics
(V_{CC} = 0V, V_{EE} = −5.2V, Output Load = 50Ω to −2.0V, T_A = 0°C to 75°C for DIP, Airflow ≥2.5m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

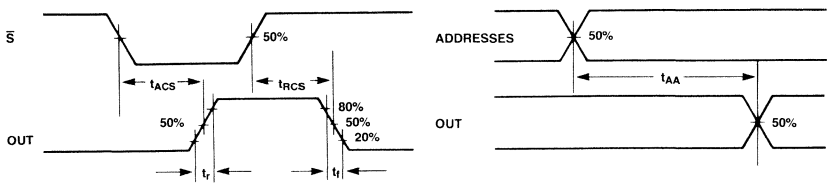
Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Output high voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	−1000 −960 −900		−840 −810 −720	mV	0°C 25°C 75°C
Output low voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	−1870 −1850 −1830		−1665 −1650 −1625	mV	0°C 25°C 75°C
Output high voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	−1020 −980 −920			mV	0°C 25°C 75°C
Output low voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			−1645 −1630 −1605	mV	0°C 25°C 75°C
Input high voltage (guaranteed input voltage high for all inputs)	V_{IH}	−1145 −1105 −1045		−840 −810 −720	mV	0°C 25°C 75°C
Input low voltage (guaranteed input voltage low for all inputs)	V_{IL}	−1870 −1850 −1830		−1490 −1475 −1450	mV	0°C 25°C 75°C
Input high current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA	0°C to 75°C
Input low current (V_{IN} = $V_{IL\ min}$)	I_{IL}	−50			μA	0°C to 75°C
$\overline{S}$ input low current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power supply current (all inputs and output open) MBM10474A-10 / MBM10474A-15	I_{EE}	−230 / −200			mA	0°C to 75°C

AC Characteristics
(V_{CC} = 0V, V_{EE} = −5.2 ±5%, Output Load = 50Ω to −2.0V and 30pF to GND, T_A = 0°C to 75°C for DIP, Airflow ≥ 2.5 m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Read Cycle

Parameter	Symbol	MBM10474A-10 Min	Typ	Max	MBM10474A-15 Min	Typ	Max	Unit
Address access time	t_{AA}	2	7	10	3	10	15	ns
Chip select access time	t_{ACS}	1.5	3	6	2	4	8	ns
Chip select recovery time	t_{RCS}	1.5	3	6	2	4	8	ns

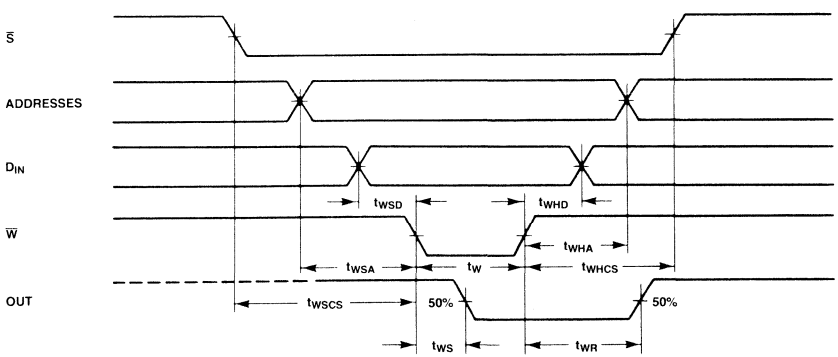
Read Cycle Timing Diagram



Write Cycle

Parameter	Symbol	MBM10470A-10 Min	Typ	Max	MBM10474A-15 Min	Typ	Max	Unit
Write pulse width	t_W	12			15			ns
Write disable time	t_{WS}			6			8	ns
Write recovery time	t_{WR}			10			15	ns
Address set up time	t_{WSA}	2			2			ns
Chip select set up time	t_{WSCS}	1			2			ns
Data set up time	t_{WSD}	1			2			ns
Address hold time	t_{WHA}	1			3			ns
Chip select hold time	t_{WHCS}	1			2			ns
Data hold time	t_{WHD}	1			2			ns

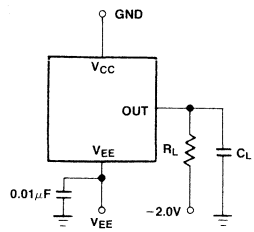
Write Cycle Timing Diagram

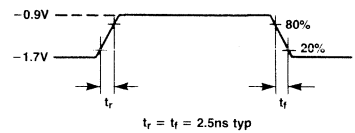


Rise Time and Fall Time

Parameter	Symbol	Min	Typ	Max	Unit
Output rise time	t_r	1		3.5	ns
Output fall time	t_f	1		3.5	ns

AC Test Conditions





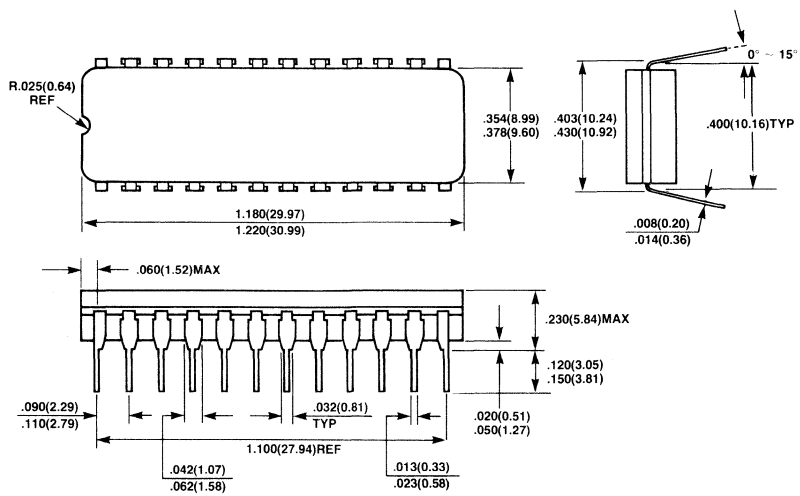
OUTPUT LOAD: $R_L = 50\Omega$
$C_L = 30pF$
(INCLUDING PROBE AND STRAY CAPACITANCE)

NOTE: ALL TIMING MEASUREMENTS REFERENCED TO 50% INPUT LEVELS.

Package Dimensions

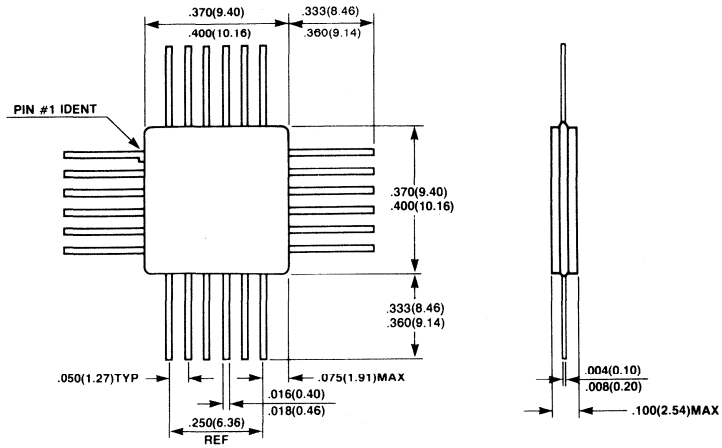
Dimensions in inches
(millimeters)

24-Lead Ceramic (CERDIP) Dual In-Line Package
(Case No.: DIP-24C-C05)

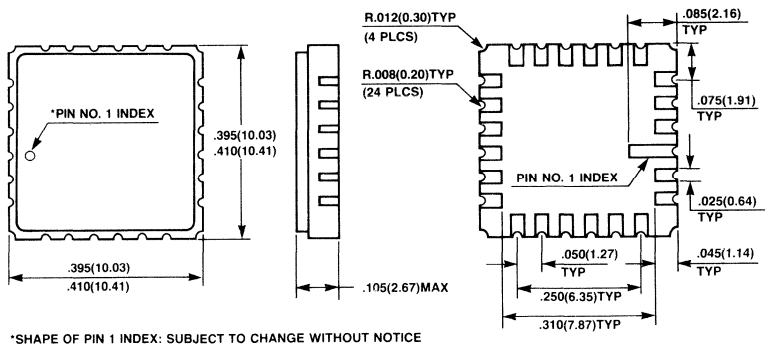


Package Dimensions
(continued)
Dimensions in inches
(millimeters)

24-Lead Ceramic (CERDIP) Flat Package
(Case No.: FPT-24C-C02)



24-Pad Ceramic (FRIT SEAL) Leadless Chip Carriers
(Case No: LCC-24C-F02)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

MBM100474A-10, MBM100474A-15

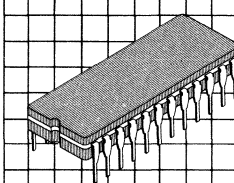
4096-Bit Bipolar ECL Random Access Memory

Description

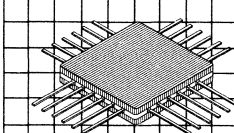
The Fujitsu MBM100474A is a fully decoded 4096-bit ECL read/write random access memory designed for high speed scratch pad, control and buffer storage applications. This device is organized as 1024 words by 4 bits, and it features on-chip voltage/temperature compensation for improved noise margin.

The MBM100474A offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

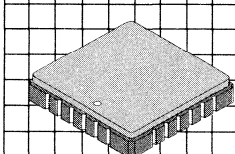
Operation for the MBM100474A is specified over a temperature range of from 0°C to 85°C (T_A for DIP, T_C for Flat Package and LCC). It also features 24-pin Ceramic DIP, Flat Package, or LCC, and is fully compatible with industry standard 100K-series ECL families.



Ceramic Package DIP-24C-C05



Ceramic Package LCC-24C-F02



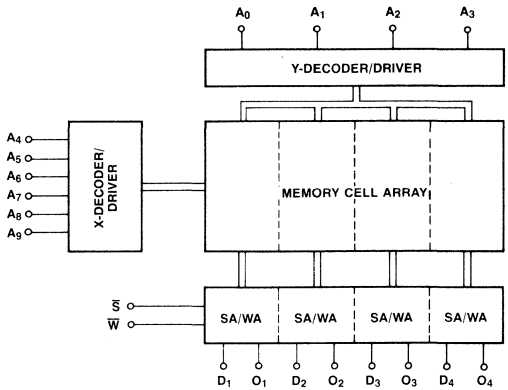
Ceramic Package LCC-24C-F02

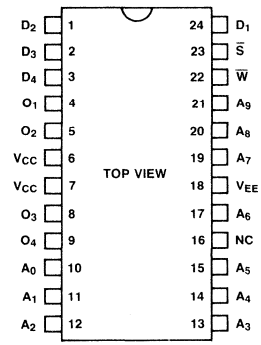
Features

- **1024 words × 4 bits organization**
- **On-chip voltage temperature compensation for improved noise margin**
- **Fully compatible with industry standard 100K-series ECL families**
- **Address access time: 10 ns max. (MBM100474A-10) 15 ns max. (MBM100474A-15)**
- **Chip select access time: 6 ns max. (MBM100474A-10) 8 ns max. (MBM100474A-15)**
- **Open emitter output for ease of memory expansion**
- **Low power dissipation of 0.22 mW/bit (MBM100474A-10) 0.20 mW/bit (MBM100474A-15)**
- **DOPOS and IOP-II**

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

MBM100474A Block Diagram and Pin Assignments



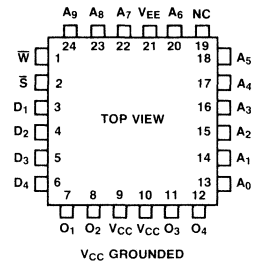


Dual Inline Package

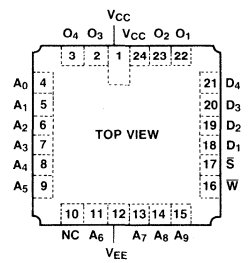
TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{S}$	$\overline{W}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	OUT	READ

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE



Flatpack



Leadless Chip Carrier

Functional Description

The Fujitsu MBM100474A is a fully decoded 4096 bit read/write random access memory organized as 1024 words by 4 bits. Memory cell selection is achieved by means of a 10-bit address designed A_0 through A_9. The active low Chip Select ($\overline{S}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{W}$) input. With $\overline{W}$ and $\overline{S}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{W}$ is held high, while $\overline{S}$ is held low. Data at the addressed location is then transferred to OUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
V_{EE} pin potential to ground pin	V_{EE}	+0.5 to −7.0	V
Input voltage	V_{IN}	+0.5 to V_{EE}	V
Output current (DC, output high)	I_{OUT}	−30	mA
Temperature under bias	T_A for DIP	−55 to +125	°C
	T_C for flat package and LCC	−55 to +125	°C
Storage temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Guaranteed Operating Conditions
(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply voltage	V_{EE}	−5.7	−4.5	−4.2	V	0°C to 85°C

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input pin capacitance	C_{IN}		4	5	pF
Output pin capacitance	C_{OUT}		6	8	pF

DC Characteristics
(V_{CC} = 0V, V_{EE} = −4.5V, Output Load = 50Ω to −2.0V, T_A = 0°C to 85°C for DIP, Airflow ≥2.5m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Output high voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)		V_{OH}	−1025		−880	mV
Output low voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)		V_{OL}	−1810		−1620	mV
Output high voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)		V_{OHC}	−1035			mV
Output low voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)		V_{OLC}			−1610	mV
Input high voltage (guaranteed input voltage high for all inputs)		I_{IH}	−1165		−880	mV
Input low voltage (guaranteed input voltage low for all inputs)		I_{IL}	−1810		−1475	mV
Input high current ($V_{IN} = V_{IH\ max}$)		I_{IH}			220	μA
Input low current ($V_{IN} = V_{IL\ min}$)		I_{IL}	−50			μA
$\overline{S}$ input low current ($V_{IN} = V_{IL\ min}$)		I_{IL}	0.5		170	μA
Power supply current (all inputs and output open)	MBM100474A-10	I_{EE}	−230			mA
	MBM100474A-15		−200			

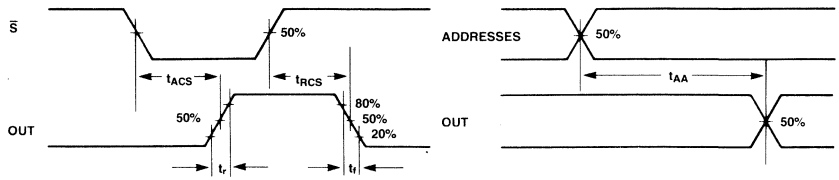
AC Characteristics

(V_{CC} = 0V, V_{EE} = −4.5 ±5%, Output Load = 50Ω to −2.0V and 30pF to GND, T_A = 0°C to 85°C for DIP, Airflow ≥ 2.5 m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Read Cycle

Parameter	Symbol	MBM100474A-10 Min	Typ	Max	MBM100474A-15 Min	Typ	Max	Unit
Address access time	t_{AA}	2	7	10	3	10	15	ns
Chip select access time	t_{ACS}	1.5	3	6	2	4	8	ns
Chip select recovery time	t_{RCS}	1.5	3	6	2	4	8	ns

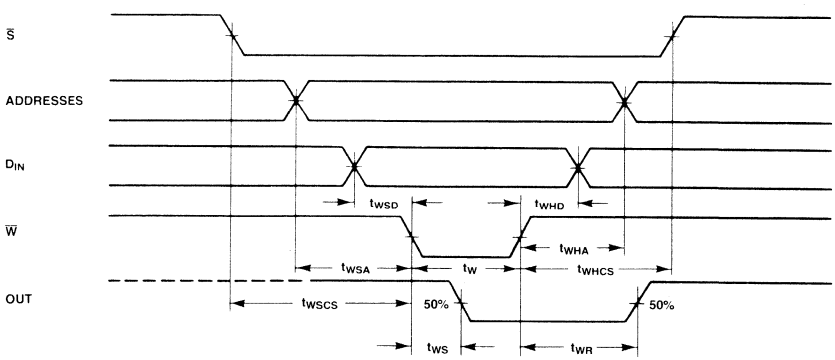
Read Cycle Timing Diagram



Write Cycle

Parameter	Symbol	MBM100474A-10 Min	Typ	Max	MBM100474A-15 Min	Typ	Max	Unit
Write pulse width	t_W	12			15			ns
Write disable time	t_{WS}			6			8	ns
Write recovery time	t_{WR}			10			15	ns
Address set up time	t_{WSA}	2			2			ns
Chip select set up time	t_{WSCS}	1			2			ns
Data set up time	t_{WSD}	1			2			ns
Address hold time	t_{WHA}	1			3			ns
Chip select hold time	t_{WHCS}	1			2			ns
Data hold time	t_{WHD}	1			2			ns

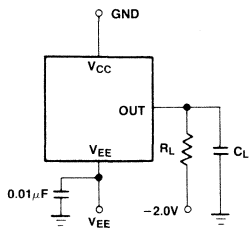
Write Cycle Timing Diagram

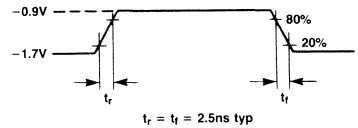


Rise Time and Fall Time

Parameter	Symbol	Min	Typ	Max	Unit
Output rise time	t_r	1		3.5	ns
Output fall time	t_f	1		3.5	ns

AC Test Conditions





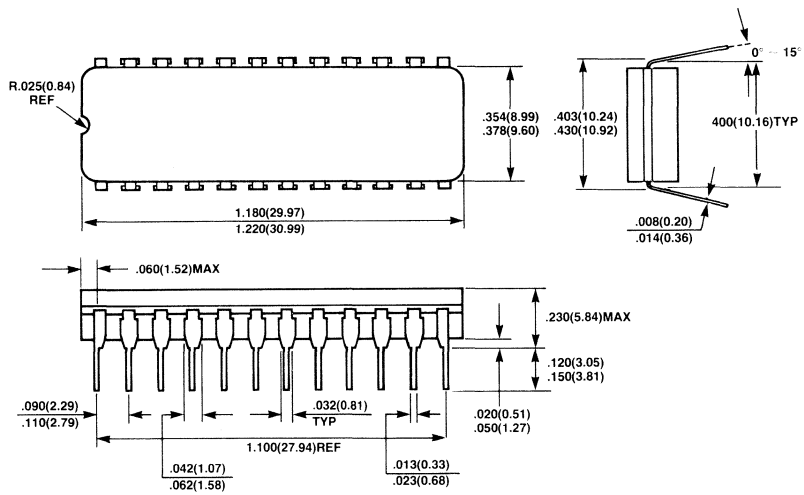
OUTPUT LOAD: $R_L = 50\Omega$
$C_L = 30pF$
(INCLUDING PROBE AND STRAY CAPACITANCE)

NOTE: ALL TIMING MEASUREMENTS REFERENCED TO 50% INPUT LEVELS.

Package Dimensions

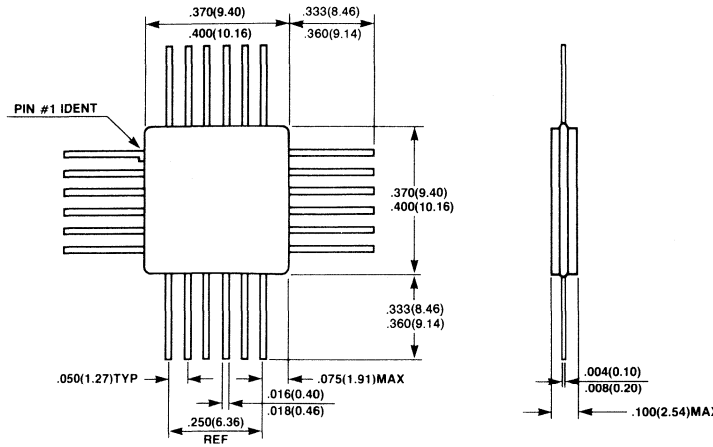
Dimensions in inches
(millimeters)

24-Lead Ceramic (CERDIP) Dual In-Line Package
(Case No.: DIP-24C-C05)

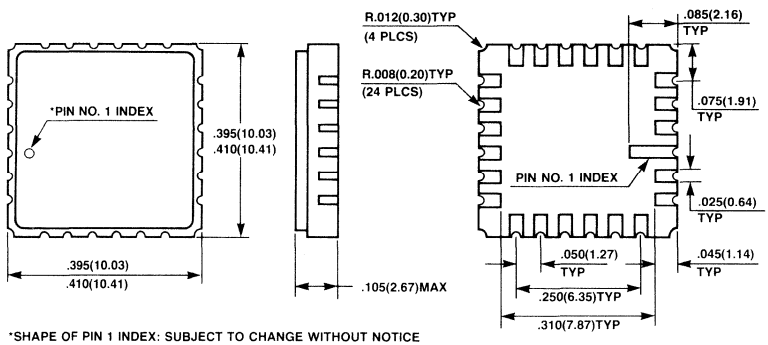


Package Dimensions
Dimensions in inches
(millimeters)

24-Lead Ceramic (CERDIP) Flat Package
(Case No.: FPT-24C-C02)



24-Pad Ceramic (FRIT SEAL) Leadless Chip Carriers
(Case No: LCC-24C-F02)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

MBM10480-15, MBM10480-25

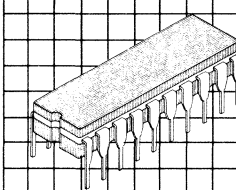
16384-Bit Bipolar ECL Random Access Memory

Description

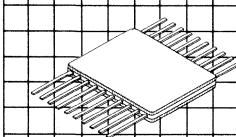
The Fujitsu MBM10480 is a fully decoded 16384-bit ECL read/write random access memory designed for main memory, control and buffer storage applications. This device is organized as 16384 words by one bit, and it features on-chip voltage compensation for improved noise margin.

The MBM10480 offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon), processing.

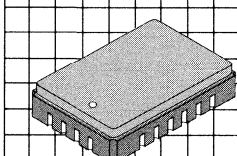
Operation for the MBM10480 is specified over a temperature range of from 0°C to 75°C (T_A for DIP, T_C for Flat Package and LCC). It also features 20-pin Ceramic DIP, Flat Package, and LCC, and is fully compatible with industry standard 10K-series ECL families.



Ceramic Package
DIP-20C-C03



Ceramic Package
FPT-20C-C01



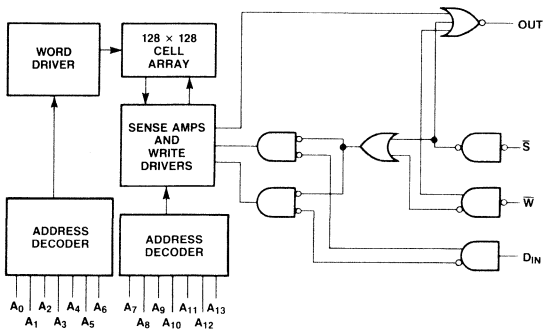
Ceramic Package
LCC-20C-F01

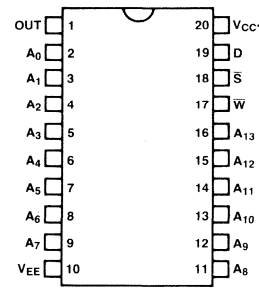
Features

- **16384 words × 1 bit organization**
- **On-chip voltage compensation for improved noise margin**
- **Fully compatible with industry standard 10K-series ECL families**
- **Address access time:**
  15 ns max. (MBM10480-15)
  25 ns max. (MBM10480-25)
- **Chip select access time:**
  8 ns max. (MBM10480-15)
  10 ns max. (MBM10480-25)
- **Open emitter output for ease of memory expansion**
- **Low power dissipation of 0.05 mW/bit**
- **DOPOS and IOP-II**
- **Pin compatible with the F10480**

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

MBM10480
Block Diagram and Pin Assignments





Dual In-Line Package

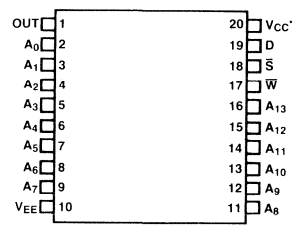
TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{S}$	$\overline{W}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	OUT	READ

H = HIGH VOLTAGE LEVEL

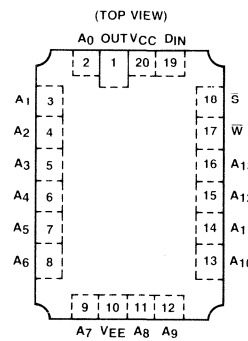
L = LOW VOLTAGE LEVEL

X = DON'T CARE



*VCC GROUNDED

Flat Package



Leadless Chip Carrier

Functional Description

The Fujitsu MBM10480 is a fully decoded 16384 bit read/write random access memory organized as 16384 words by one bit. Memory cell selection is achieved by means of a 14-bit address designed A_0 through A_{13}. The active low Chip Select ($\overline{S}$) input is provided for memory expansion. The read and write operations are controlled by the state of the Enable ($\overline{W}$) input. With $\overline{W}$ and $\overline{S}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{W}$ is held high, while $\overline{S}$ is held low. Data at the addressed location is then transferred to OUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
V_{EE} pin potential to ground pin	V_{EE}	+0.5 to −7.0	V
Input voltage	V_{IN}	+0.5 to V_{EE}	V
Output current (DC, output high)	I_{OUT}	−30	mA
Temperature under bias	T_A for DIP	−55 to +125	°C
	T_C for flat package and LCC	−55 to +125	°C
Storage temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Guaranteed Operating Conditions
(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply voltage	V_{EE}	−5.46	−5.2	−4.94	V	0°C to 75°C

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input pin capacitance	C_{IN}		5		pF
Output pin capacitance	C_{OUT}		6		pF

DC Characteristics
(V_{CC} = 0V, V_{EE} = −5.2V, Output Load = 50Ω and 30pF to −2.0V, T_A = 0°C to 75°C for DIP, Airflow >2.5m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Output high voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	−1000		−840	mV	0°C
		−960		−810		25°C
		−900		−720		75°C
Output low voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	−1870		−1665	mV	0°C
		−1850		−1650		25°C
		−1830		−1625		75°C
Output high voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	−1020			mV	0°C
		−980				25°C
		−920				75°C
Output low voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			−1645	mV	0°C
				−1630		25°C
				−1605		75°C
Input high voltage (guaranteed input voltage high for all inputs)	V_{IH}	−1145		−840	mV	0°C
		−1105		−810		25°C
		−1045		−720		75°C
Input low voltage (guaranteed input voltage low for all inputs)	V_{IL}	−1870		−1490	mV	0°C
		−1850		−1475		25°C
		−1830		−1450		75°C
Input high current ($V_{IN} - V_{IH\ min}$)	I_{IH}			220	μA	0°C to 75°C
Input low current ($V_{IN} = V_{IL\ min}$)	I_{IL}	−50			μA	0°C to 75°C
$\overline{S}$ input low current ($V_{IN} = V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power supply current (all inputs and output open) — MBM10480-15	I_{EE}	−220			mA	0°C to 75°C
Power supply current (all inputs and output open) — MBM10480-25	I_{EE}	−220			mA	0°C to 75°C

AC Characteristics

(V_{CC} = 0V, V_{EE} = −5.2 ±5%, Output Load = 50Ω to −2.0V and 30pF to GND, T_A = 0°C to 75°C for DIP, Airflow ≥ 2.5 m/s, T_C = 0°C to 75°C for Flat Package and LCC, unless otherwise noted.)

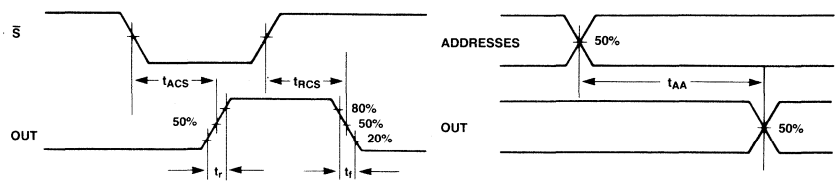
Read Cycle

Parameter	Symbol	MBM10480-15 Min	MBM10480-15 Typ	MBM10480-15 Max	MBM10480-25 Min	MBM10480-25 Typ	MBM10480-25 Max	Unit
Address access time	t_{AA}			15			25	ns
Chip select access time	t_{ACS}			8			10	ns
Chip select recovery time	t_{RCS}			8			10	ns

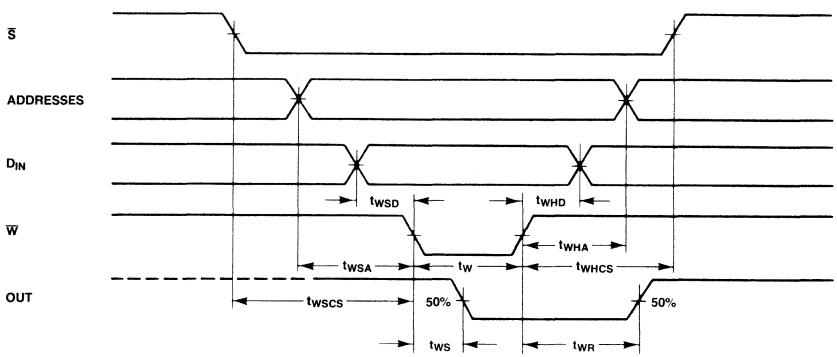
Write Cycle

Parameter	Symbol	MBM10480-15 Min	MBM10480-15 Typ	MBM10480-15 Max	MBM10480-25 Min	MBM10480-25 Typ	MBM10480-25 Max	Unit
Write pulse width	t_W	15			25			ns
Write disable time	t_{WS}			8			10	ns
Write recovery time	t_{WR}			18			20	ns
Address set up time	t_{WSA}	2			5			ns
Chip select set up time	t_{WSCS}	2			5			ns
Data set up time	t_{WSD}	2			5			ns
Address hold time	t_{WHA}	3			5			ns
Chip select hold time	t_{WHCS}	3			5			ns
Data hold time	t_{WHD}	3			5			ns

Read Cycle Timing Diagram



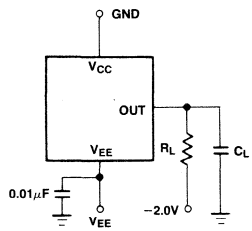
Write Cycle Timing Diagram

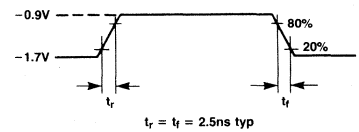


Rise Time and Fall Time

Parameter	Symbol	Min	Typ	Max	Unit
Output rise time	t_r		3		ns
Output fall time	t_f		3		ns

AC Test Conditions





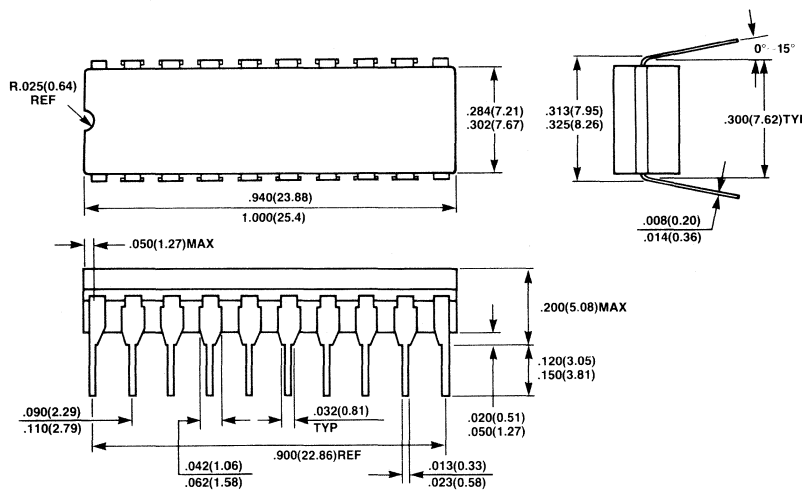
OUTPUT LOAD: $R_L = 50\Omega$
$C_L = 30pF$
(INCLUDING PROBE AND STRAY CAPACITANCE)

NOTE: ALL TIMING MEASUREMENTS REFERENCED TO 50% INPUT LEVELS.

Package Dimensions

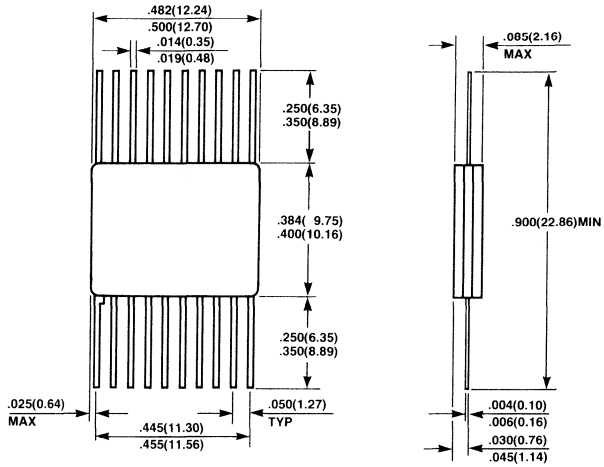
Dimensions in inches (millimeters)

20-Lead Ceramic (CERDIP) Dual In-Line Package (Case No.: DIP-20C-C03)

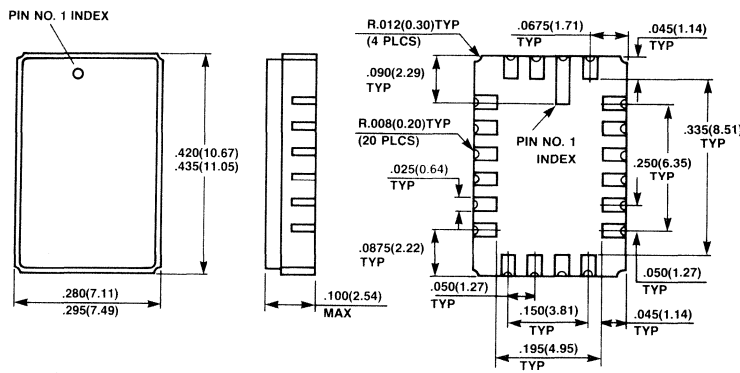


Package Dimensions
(continued)
Dimensions in inches
(millimeters)

20-Lead Ceramic (CERDIP) Flat Package
(Case No.: FPT-20C-C01)



20-Pad Ceramic (FRIT SEAL) Leadless Chip Carrier
(Case No: LCC-20C-F01)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

FUJITSU

MBM100480-15, MBM100480-25

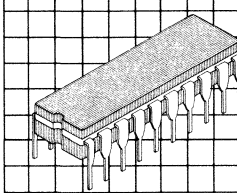
16384-Bit Bipolar ECL Random Access Memory

Description

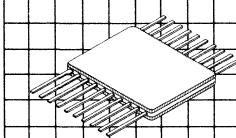
The Fujitsu MBM100480 is a fully decoded 16384-bit ECL read/write random access memory designed for main memory, control and buffer storage applications. This device is organized as 16384 words by one bit, and it features on-chip voltage/temperature compensation for improved noise margin.

The MBM100480 offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon), processing.

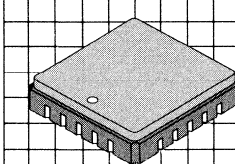
Operation for the MBM100480 is specified over a temperature range of from 0°C to 85°C (T_A for DIP, T_C for Flat Package and LCC). It also features 20-pin Ceramic DIP, Flat Package, and LCC, and is fully compatible with industry standard 100K-series ECL families.



Ceramic Package
DIP-20C-C03



Ceramic Package
FPT-20C-C01



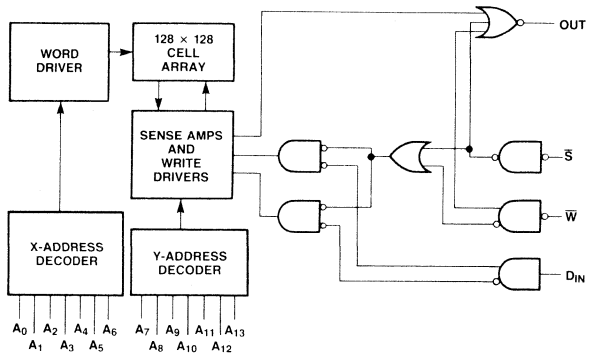
Ceramic Package
LCC-20C-F01

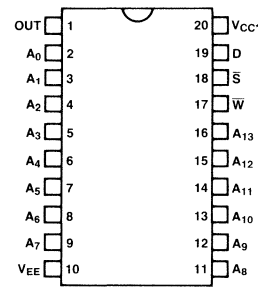
Features

- **16384 words × 1 bit organization**
- **On-chip voltage/temperature compensation for improved noise margin**
- **Fully compatible with industry standard 100K-series ECL families**
- **Address access time: 15 ns max. (MBM100480-15) 25 ns max. (MBM100480-25)**
- **Chip select access time: 8 ns max. (MBM100480-15) 10 ns max. (MBM100480-25)**
- **Open emitter output for ease of memory expansion**
- **Low power dissipation of 0.04 mW/bit**
- **DOPOS and IOP-II**
- **Pin compatible with the F100480**

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

MBM100480 Block Diagram and Pin Assignments





Dual In-Line Package

TRUTH TABLE

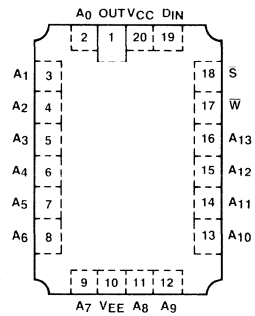
INPUT			OUTPUT	MODE
$\overline{S}$	$\overline{W}$	D_{IN}		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	OUT	READ

H = HIGH VOLTAGE LEVEL

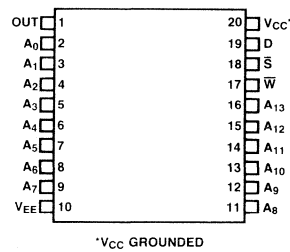
L = LOW VOLTAGE LEVEL

X = DON'T CARE

(TOP VIEW)



Leadless Chip Carrier



Flat Package

Functional Description

The Fujitsu MBM100480 is a fully decoded 16384 bit read/write random access memory organized as 16384 words by one bit. Memory cell selection is achieved by means of a 14-bit address designed A_0 through A_{13}. The active low Chip Select ($\overline{S}$) input is provided for memory expansion. The read and write operations are controlled by the state of the Enable ($\overline{W}$) input. With $\overline{W}$ and $\overline{S}$ held low, the data at D_{IN} is written into the addressed location. To read, $\overline{W}$ is held high, while $\overline{S}$ is held low. Data at the addressed location is then transferred to OUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
V_{EE} pin potential to ground pin	V_{EE}	+0.5 to −7.0	V
Input voltage	V_{IN}	+0.5 to V_{EE}	V
Output current (DC, output high)	I_{OUT}	−30	mA
Temperature under bias	T_A for DIP	−55 to +125	°C
	T_C for flat package and LCC	−55 to +125	°C
Storage temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Guaranteed Operating Conditions
(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply voltage	V_{EE}	−5.7	−4.5	−4.2	V	0°C to 85°C

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input pin capacitance	C_{IN}		5		pF
Output pin capacitance	C_{OUT}		6		pF

DC Characteristics
(V_{CC} = 0V, V_{EE} = −4.5V, Output Load = 50Ω and 30pF to −2.0V, T_A = 0°C to 85°C for DIP, Airflow >2.5m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

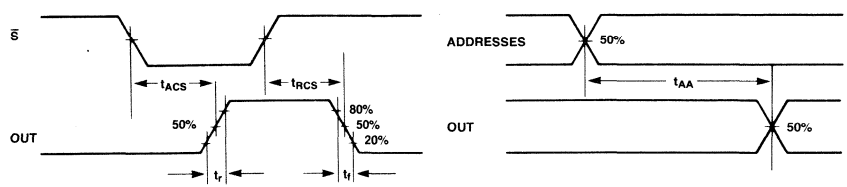
Parameter		Symbol	Min	Typ	Max	Unit
Output high voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)		V_{OH}	−1025		−880	mV
Output low voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)		V_{OL}	−1810		−1620	mV
Output high voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)		V_{OHC}	−1035			mV
Output low voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)		V_{OLC}			−1610	mV
Input high voltage (guaranteed input voltage high for all inputs)		V_{IH}	−1165		−880	mV
Input low voltage (guaranteed input voltage low for all inputs)		V_{IL}	−1810		−1475	mV
Input high current (V_{IN} = $V_{IH\ max}$)		I_{IH}			220	μA
Input low current (V_{IN} = $V_{IL\ min}$)		I_{IL}	−50			μA
$\overline{S}$ input low current (V_{IN} = $V_{IL\ min}$)		I_{IL}	0.5		170	μA
Power supply current (all inputs and output open)	MBM100480-15	I_{EE}	−220			mA
	MBM100480-25		−220			

AC Characteristics
(V_{CC} = 0V, V_{EE} = −4.5 ±5%, Output Load = 50Ω to −2.0V and 30pF to GND, T_A = 0°C to 85°C for DIP, Airflow ≥ 2.5 m/s, T_C = 0°C to 85°C for Flat Package and LCC, unless otherwise noted.)

Read Cycle

Parameter	Symbol	MBM100480-15 Min	MBM100480-15 Typ	MBM100480-15 Max	MBM100480-25 Min	MBM100480-25 Typ	MBM100480-25 Max	Unit
Address access time	t_{AA}			15			25	ns
Chip select access time	t_{ACS}			8			10	ns
Chip select recovery time	t_{RCS}			8			10	ns

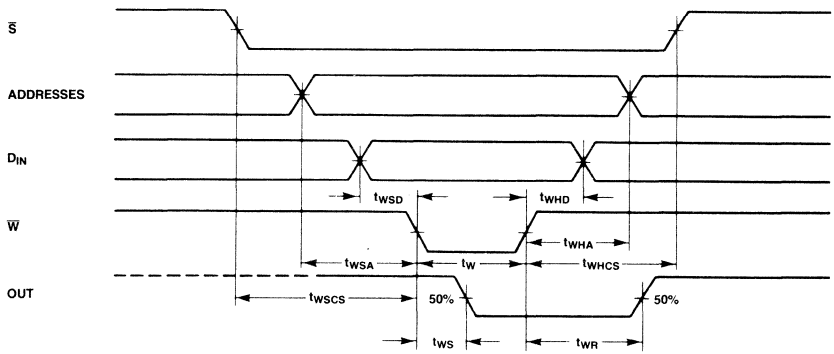
Read Cycle Timing Diagram



Write Cycle

Parameter	Symbol	MBM100480-15 Min	Typ	Max	MBM100480-25 Min	Typ	Max	Unit
Write pulse width	t_W	15			25			ns
Write disable time	t_{WS}			8			10	ns
Write recovery time	t_{WR}			18			20	ns
Address set up time	t_{WSA}	2			5			ns
Chip select set up time	t_{WSCS}	2			5			ns
Data set up time	t_{WSD}	2			5			ns
Address hold time	t_{WHA}	3			5			ns
Chip select hold time	t_{WHCS}	3			5			ns
Data hold time	t_{WHD}	3			5			ns

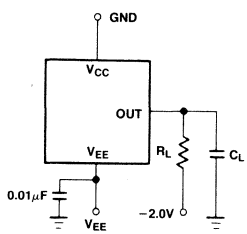
Write Cycle Timing Diagram

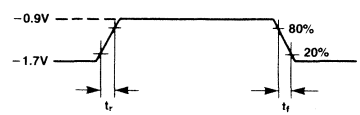


Rise Time and Fall Time

Parameter	Symbol	Min	Typ	Max	Unit
Output rise time	t_r		3		ns
Output fall time	t_f		3		ns

AC Test Conditions





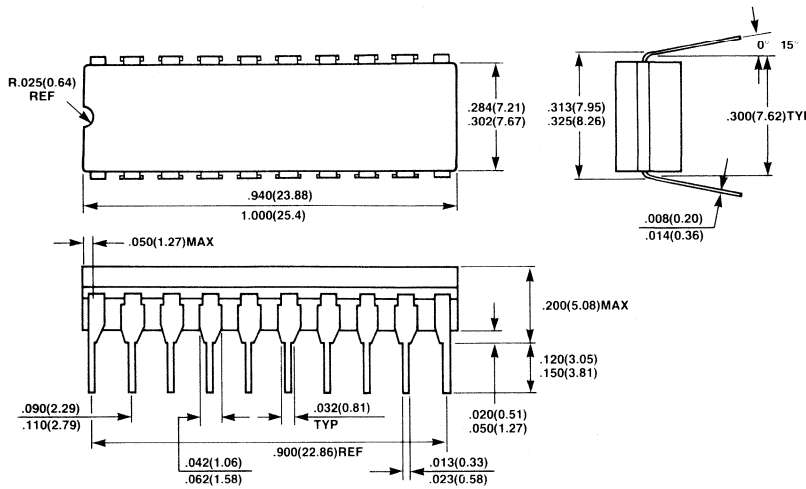
$t_r = t_f = 2.5$ns typ

OUTPUT LOAD: $R_L = 50\Omega$
$C_L = 30$pF
(INCLUDING PROBE AND STRAY CAPACITANCE)

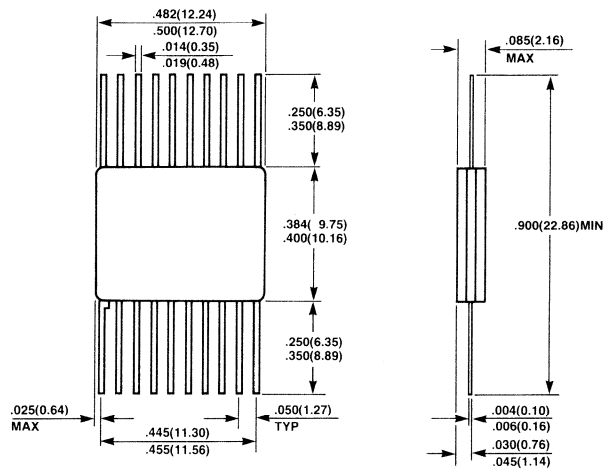
NOTE: ALL TIMING MEASUREMENTS REFERENCED TO 50% INPUT LEVELS.

Package Dimensions
Dimensions in inches
(millimeters)

20-Lead Ceramic (CERDIP) Dual In-Line Package
(Case No.: DIP-20C-C03)

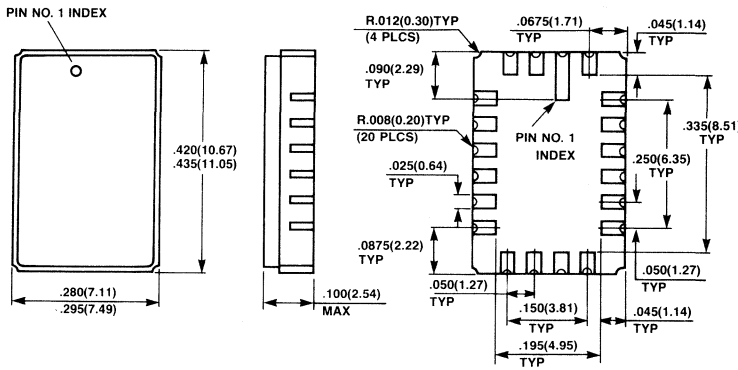


20-Lead Ceramic (CERDIP) Flat Package
(Case No.: FPT-20C-C01)



Package Dimensions
(continued)
Dimensions in inches
(millimeters)

20-Pad Ceramic (FRIT SEAL) Leadless Chip Carrier
(Case No: LCC-20C-F01)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

MBM10484-15

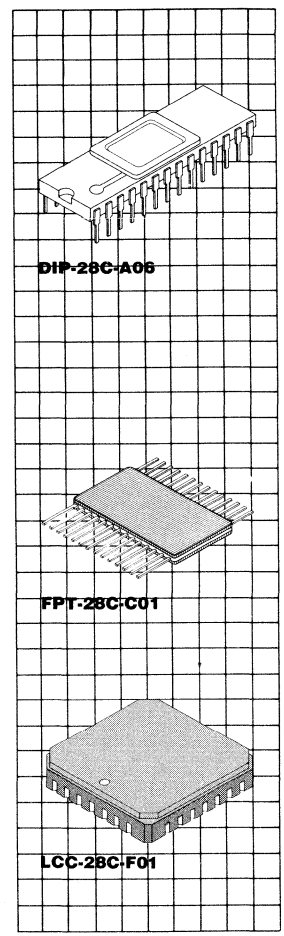
16384-Bit Bipolar ECL Random Access Memory

Description

The Fujitsu MBM10484 is a fully decoded 16,384-bit ECL read/write random access memory designed for main memory, control, and buffer storage applications. The device is organized as 4,096 words by 4-bits, and it features on-chip voltage compensation for improved noise margin.

The MBM10484 offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon), processing.

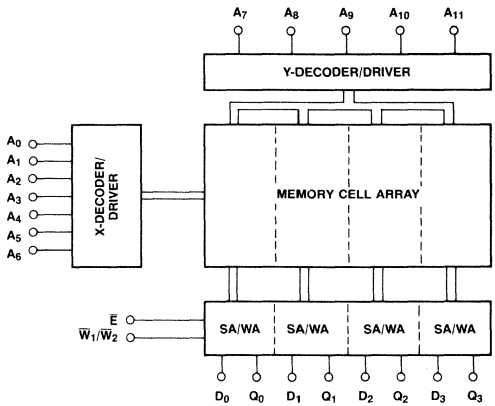
Operation for the MBM10484 is specified over a temperature range of 0°C to 75°C (T_A for DIP, T_C for Flat Package). The MBM10484-15 features a 28-pin Ceramic DIP or Flat Package, and is fully compatible with industry standard 10K-series ECL families.

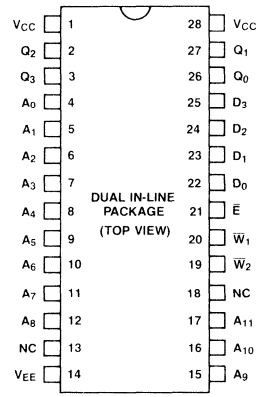


Features

- **4096 words × 4-bits organization**
- **On-chip voltage compensation for improved noise margin**
- **Fully compatible with industry standard 10K-series ECL families**
- **Address access time: 15 ns max.**
- **Chip select access time: 8 ns max.**
- **Open emitter output for ease of memory expansion**
- **Low power dissipation of 0.07 mW/bit**
- **DOPOS and IOP-II**

MBM10484 Block Diagram and Pin Assignment





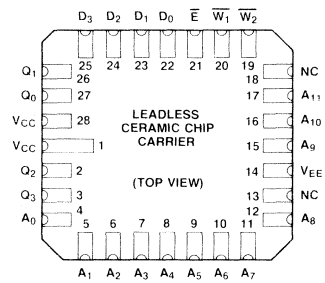
TRUTH TABLE

INPUT			Q	MODE
$\overline{E}$	$\overline{W}_1/\overline{W}_2$	IN		
H	X	X	L	DISABLED
L	*L	H	L	WRITE "H"
L	*L	L	L	WRITE "L"
L	*H	X	OUT	READ

*L = BOTH $\overline{W}_1$ AND $\overline{W}_2$ ARE LOW.
*H = EITHER $\overline{W}_1$ OR $\overline{W}_2$ IS HIGH, OR BOTH $\overline{W}$'S ARE HIGH.

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE

FPT Pinout is Equivalent



Functional Description

The Fujitsu MBM10484 is a fully decoded 16384-bit read/write random access memory organized as 4096 words by 4-bits. Memory cell selection is achieved by means of a 12-bit address designed A_0 through A_{11}. The active low Chip Enable ($\overline{E}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{W}$) inputs. With $\overline{W}$ and $\overline{E}$ held low, the data at IN (D_0-D_3) is written into the addressed location.

To read, $\overline{W}$ are/is held high, while $\overline{E}$ is held low. Data at the addressed location is then transferred to Q_{OUT} (Q_0–Q_3) and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
V_{EE} pin potential to ground pin	V_{EE}	+0.5 to −7.0	V
Input voltage	V_{IN}	+0.5 to V_{EE}	V
Output current (DC, output high)	I_{OUT}	−30	mA
Temperature under bias	T_A for DIP	−55 to +125	°C
	T_C for flat package	−55 to +125	°C
Storage temperature	T_{STG}	−65 to +125	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Guaranteed Operating Conditions
(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package
Supply voltage	V_{EE}	−5.46	−5.2	−4.94	V	0°C to 75°C

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input pin capacitance	C_{IN}		4		pF
Output pin capacitance	C_{OUT}		6		pF

DC Characteristics
(V_{CC} = 0V, V_{EE} = −5.2V, Output Load = 50Ω to −2.0V, T_A = 0°C to 75°C for DIP, Airflow >2.5m/s, T_C = 0°C to 75°C for Flat Package, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Output high voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	−1000 −960 −900		−840 −810 −720	mV	0°C 25°C 75°C
Output low voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	−1870 −1850 −1830		−1665 −1650 −1625	mV	0°C 25°C 75°C
Output high voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	−1020 −980 −920			mV	0°C 25°C 75°C
Output low voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			−1645 −1630 −1605	mV	0°C 25°C 75°C
Input high voltage (guaranteed input voltage high for all inputs)	V_{IH}	−1145 −1105 −1045		−840 −810 −720	mV	0°C 25°C 75°C
Input low voltage (guaranteed input voltage low for all inputs)	V_{IL}	−1870 −1850 −1830		−1490 −1475 −1450	mV	0°C 25°C 75°C
Input high current ($V_{IN} = V_{IH\ max}$)	I_{IH}			220	μA	0°C to 75°C
Input low current ($V_{IN} = V_{IL\ min}$)	I_{IL}	−50			μA	0°C to 75°C
$\overline{E}$ input low current ($V_{IN} = V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power supply current (all inputs and outputs open)	I_{EE}	−240			mA	0°C to 75°C

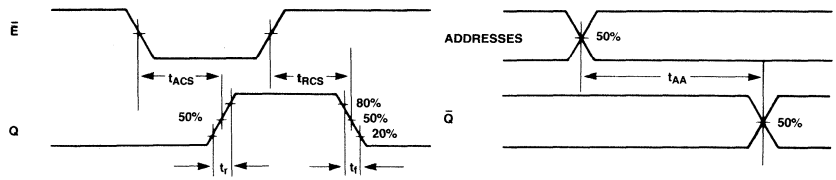
AC Characteristics
(V_{CC} = 0V, V_{EE} = −5.2 ±5%, Output Load = 50Ω to −2.0V and 30pF to GND, T_A = 0°C to 75°C for DIP, Airflow >2.5 m/s, T_C = 0°C to 75°C for Flat Package, unless otherwise noted.)

Read Cycle

Parameter	Symbol	Min	Typ	Max	Unit
Address access time	t_{AA}		12.0	15.0	ns
Chip enable access time	t_{ACS}			8.0	ns
Chip enable recovery time	t_{RCS}			8.0	ns

AC Characteristics
(continued)
(V_{CC} = 0V, V_{EE} = −5.2 ±5%, Output Load = 50Ω to −2.0V and 30pF to GND, T_A = 0°C to 75°C for DIP, Airflow ≥2.5 m/s, T_C = 0°C to 75°C for Flat Package, unless otherwise noted.)

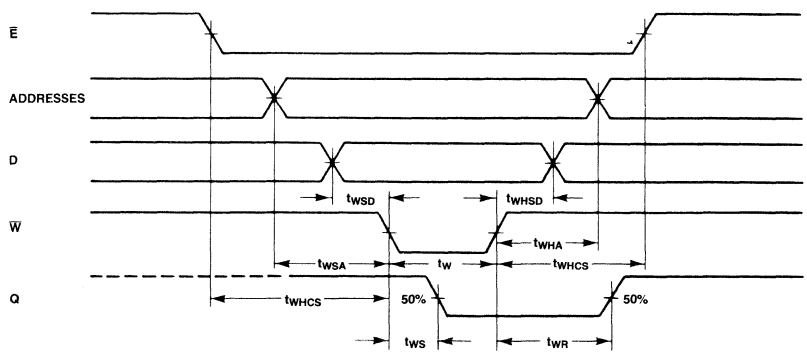
Read Cycle Timing Diagram



Write Cycle

Parameter	Symbol	Min	Typ	Max	Unit
Write pulse width	t_W	15.0			ns
Write disable time	t_{WS}			8.0	ns
Write recovery time	t_{WR}			17.0	ns
Address set up time	t_{WSA}	3.0			ns
Chip enable set up time	t_{WSCS}	3.0			ns
Data set up time	t_{WSD}	3.0			ns
Address hold time	t_{WHA}	2.0			ns
Chip enable hold time	t_{WHCS}	2.0			ns
Data hold time	t_{WHD}	2.0			ns

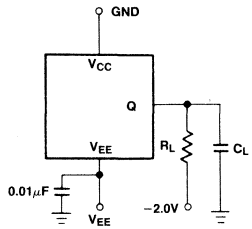
Write Cycle Timing Diagram

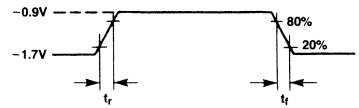


Rise Time and Fall Time

Parameter	Symbol	Min	Typ	Max	Unit
Output rise time	t_r		2.5		ns
Output fall time	t_f		2.5		ns

AC Test Conditions





$t_r = t_f = 2.5ns$ typ

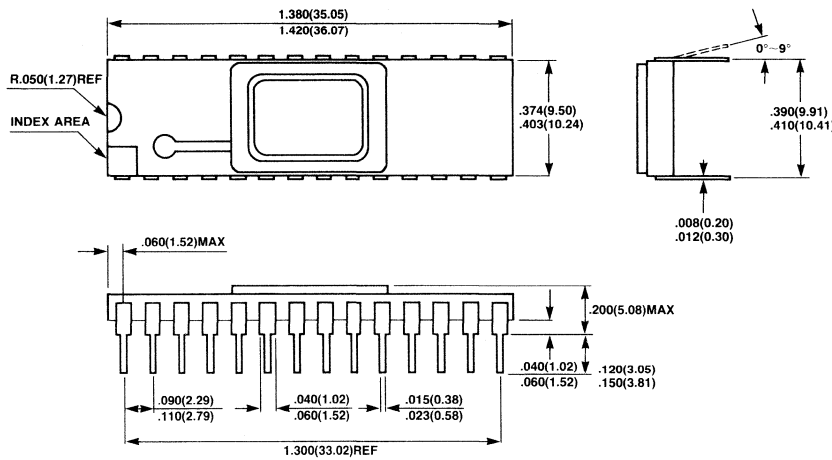
OUTPUT LOAD: $R_L = 50\Omega$
$C_L = 30pF$
(INCLUDING PROBE AND STRAY CAPACITANCE)

NOTE: ALL TIMING MEASUREMENTS REFERENCED TO 50% INPUT LEVELS.

Package Dimensions

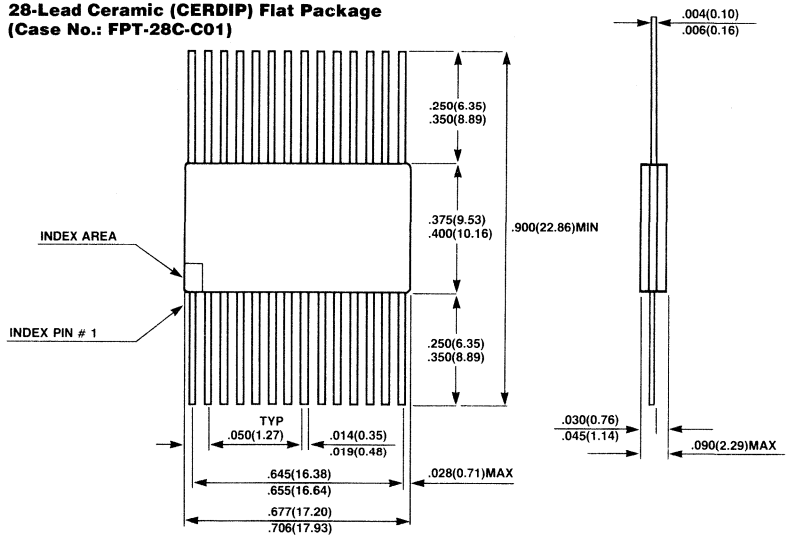
Dimensions in inches
(millimeters)

28-Lead Ceramic (Metal Seal) Dual In-Line Package (Case No.: Dip-28C-A06)

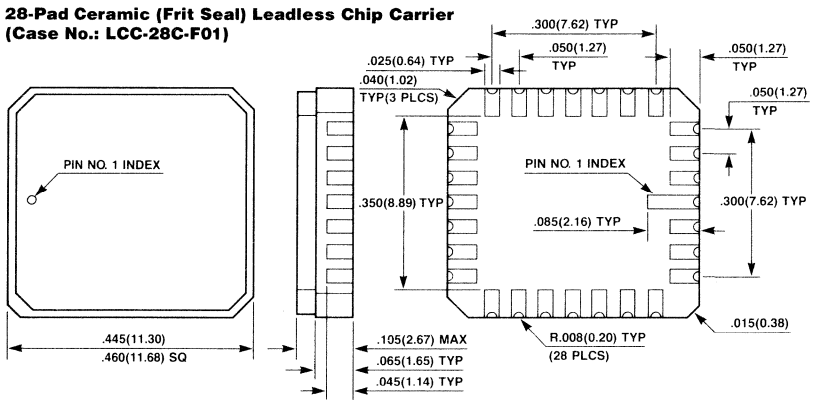


Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

28-Lead Ceramic (CERDIP) Flat Package
(Case No.: FPT-28C-C01)



28-Pad Ceramic (Frit Seal) Leadless Chip Carrier
(Case No.: LCC-28C-F01)



FUJITSU

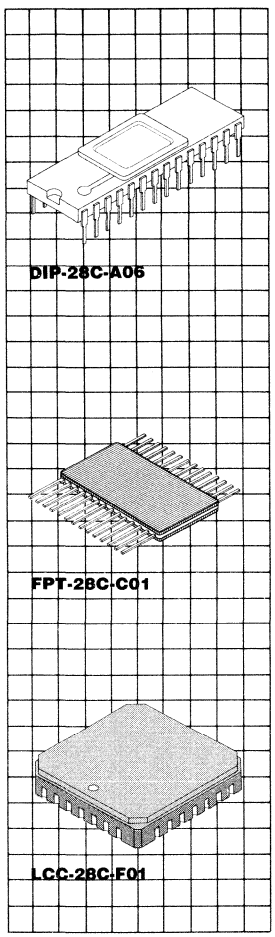
MBM100484-15
16384-Bit Bipolar ECL Random Access Memory

Description

The Fujitsu MBM100484 is a fully decoded 16,384-bit ECL read/write random access memory designed for main memory, control, and buffer storage applications. The device is organized as 4,096 words by 4-bits, and it features on-chip voltage and temperature compensation for improved noise margin.

The MBM100484 offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon), processing.

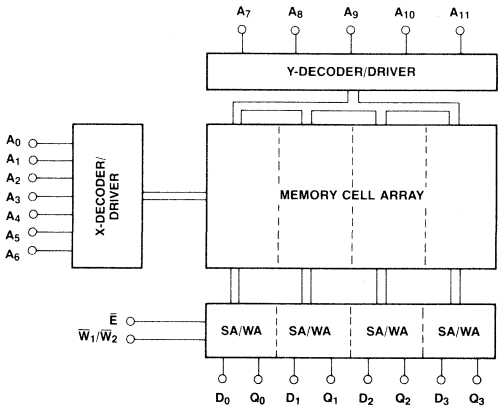
Operation for the MBM100484 is specified over a temperature range of 0°C to 85°C (T_A for DIP, T_C for Flat Package). The device also features 28-pin Ceramic DIP or Flat Package, and is fully compatible with industry standard 100K-series ECL families.

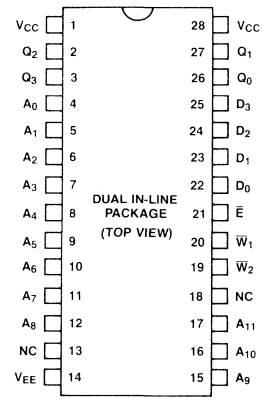


Features

- **4096 words × 4-bits organization**
- **On-chip voltage and temperature compensation for improved noise margin**
- **Fully compatible with industry standard 100K-series ECL families**
- **Address access time: 15 ns max.**
- **Chip select access time: 8 ns max.**
- **Open emitter output for ease of memory expansion**
- **Low power dissipation of 0.06 mW/bit**
- **DOPOS and IOP-II**

MBM100484 Block Diagram and Pin Assignment





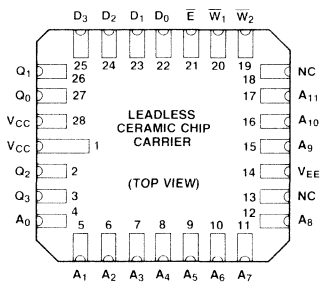
TRUTH TABLE

INPUT			Q	MODE
$\overline{E}$	$\overline{W}_1/\overline{W}_2$	IN		
H	X	X	L	DISABLED
L	*L	H	L	WRITE "H"
L	*L	L	L	WRITE "L"
L	*H	X	OUT	READ

*L = BOTH $\overline{W}_1$ AND $\overline{W}_2$ ARE LOW.
*H = EITHER $\overline{W}_1$ OR $\overline{W}_2$ IS HIGH, OR BOTH $\overline{W}$'S ARE HIGH.

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE

FPT Pinout is Equivalent



Functional Description

The Fujitsu MBM100484 is a fully decoded 16384 bit read/write random access memory organized as 4096 words by 4 bit. Memory cell selection is achieved by means of a 12-bit address designed A_0 through A_{11}. The active low Chip Enable ($\overline{E}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{W}$) inputs. With $\overline{W}$ and $\overline{E}$ held low, the data at D_{IN} (D_0–D_3) is written into the addressed location. To read, $\overline{W}$ are/is held high, while $\overline{E}$ is held low. Data at the addressed location is then transferred to Q_{OUT} (Q_0–Q_3) and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
V_{EE} pin potential to ground pin	V_{EE}	+0.5 to −7.0	V
Input voltage	V_{IN}	+0.5 to V_{EE}	V
Output current (DC, output high)	I_{OUT}	−30	mA
Temperature under bias	T_A for DIP	−55 to +125	°C
	T_C for flat package	−55 to +125	°C
Storage temperature	T_{STG}	−65 to +125	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Guaranteed Operating Conditions
(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package
Supply voltage	V_{EE}	−5.7	−4.5	−4.2	V	0°C to 85°C

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input pin capacitance	C_{IN}		4		pF
Output pin capacitance	C_{OUT}		6		pF

DC Characteristics
(V_{CC} = 0V, V_{EE} = −4.5V, Output Load = 50Ω to −2.0V, T_A = 0°C to 85°C for DIP, Airflow >2.5m/s, T_C = 0°C to 85°C for Flat Package, unless otherwise noted.)

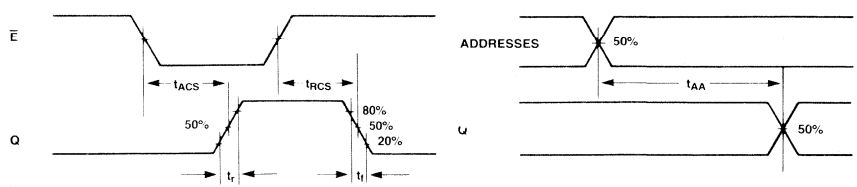
Parameter	Symbol	Min	Typ	Max	Unit
Output high voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	−1025		−880	mV
Output low voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	−1810		−1620	mV
Output high voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	−1035			mV
Output low voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			−1610	mV
Input high voltage (guaranteed input voltage high for all inputs)	V_{IH}	−1165		−880	mV
Input low voltage (guaranteed input voltage low for all inputs)	V_{IL}	−1810		−1475	mV
Input high current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA
Input low current (V_{IN} = $V_{IL\ min}$)	I_{IL}	−50			μA
$\overline{E}$ input low current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA
Power supply current (all inputs and outputs open)	I_{EE}	−240			mA

AC Characteristics
(V_{CC} = 0V, V_{EE} = −4.5 ±5%, Output Load = 50Ω to −2.0V and 30pF to GND, T_A = 0°C to 85°C for DIP, Airflow ≥2.5 m/s, T_C = 0°C to 85°C for Flat Package, unless otherwise noted.)

Read Cycle

Parameter	Symbol	Min	Typ	Max	Unit
Address access time	t_{AA}		12.0	15.0	ns
Chip enable access time	t_{ACS}			8.0	ns
Chip enable recovery time	t_{RCS}			8.0	ns

Read Cycle Timing Diagram



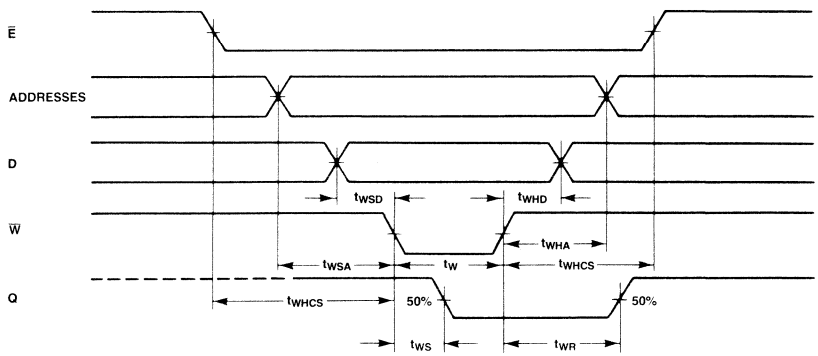
AC Characteristics

(continued)
(V_{CC} = 0V, V_{EE} = −4.5 ±5%, Output Load = 50Ω to −2.0V and 30pF to GND, T_A = 0°C to 85°C for DIP, Airflow ≥2.5 m/s, T_C = 0°C to 85°C for Flat Package, unless otherwise noted.)

Write Cycle

Parameter	Symbol	Min	Typ	Max	Unit
Write pulse width	t_W	15.0			ns
Write disable time	t_{WS}			8.0	ns
Write recovery time	t_{WR}			17.0	ns
Address set up time	t_{WSA}	3.0			ns
Chip enable set up time	t_{WSCS}	3.0			ns
Data set up time	t_{WSD}	3.0			ns
Address hold time	t_{WHA}	2.0			ns
Chip enable hold time	t_{WHCS}	2.0			ns
Data hold time	t_{WHD}	2.0			ns

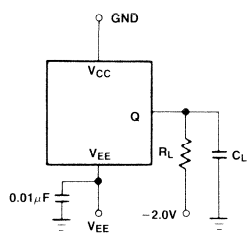
Write Cycle Timing Diagram

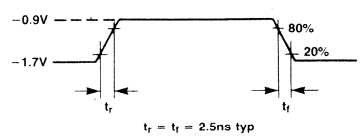


Rise Time and Fall Time

Parameter	Symbol	Min	Typ	Max	Unit
Output rise time	t_r		2.5		ns
Output fall time	t_f		2.5		ns

AC Test Conditions



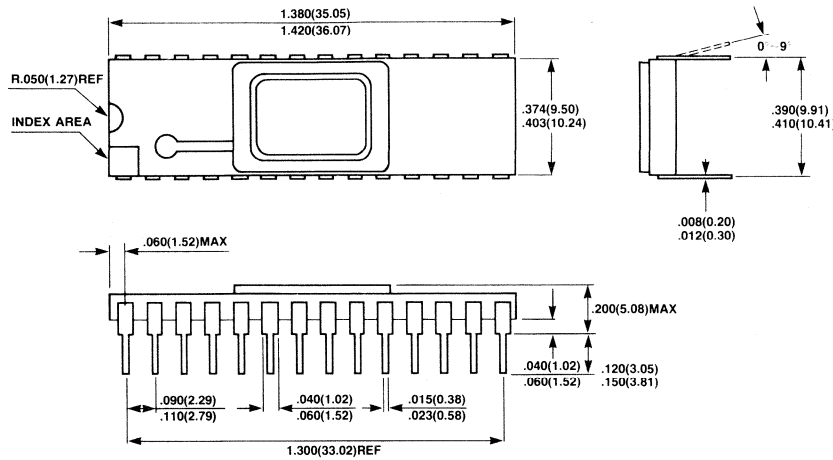


OUTPUT LOAD: R_L = 50Ω
C_L = 30pF
(INCLUDING PROBE AND STRAY CAPACITANCE)

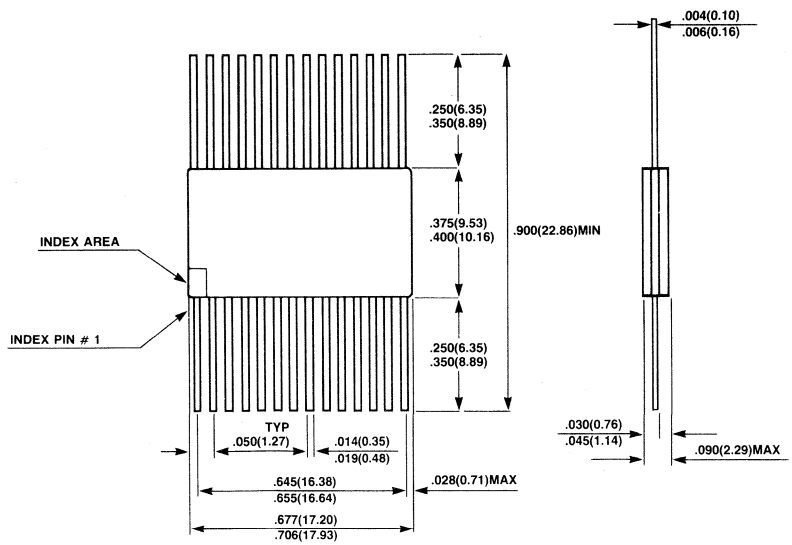
NOTE: ALL TIMING MEASUREMENTS REFERENCED TO 50% INPUT LEVELS.

Package Dimensions
Dimensions in inches
(millimeters)

28-Lead Ceramic (Metal Seal) Dual In-Line Package
(Case No.: DIP-28C-A06)

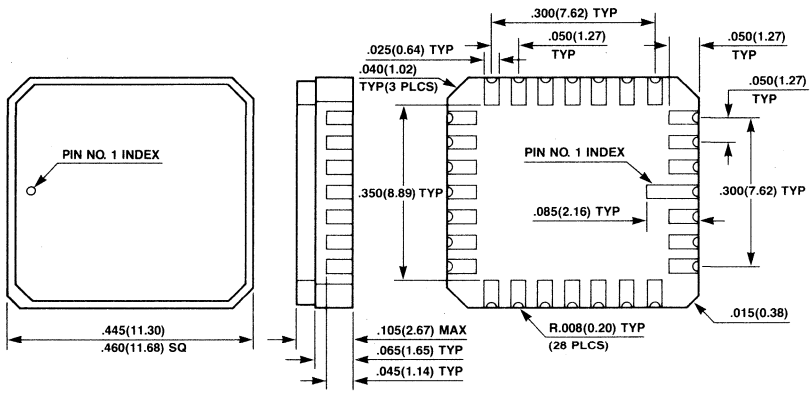


28-Lead Ceramic (CERDIP) Flat Package
(Case No.: FPT-28C-C01)



Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

28-Pad Ceramic (Frit Seal) Leadless Chip Carrier
(Case No.: LCC-28C-F01)



FUJITSU

MBM10490

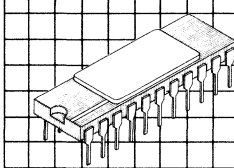
65,536-Bit Bipolar ECL Random Access Memory

Description

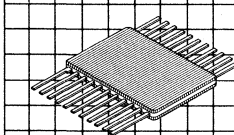
The Fujitsu MBM10490 is a fully decoded 65,536-bit ECL read/write random access memory designed for main memory, control, and buffer storage applications. The device is organized as 65,536 words by 1-bit, and it features on-chip voltage compensation for improved noise margin.

The MBM10490 offers extremely small cell and chip size, realized through the use of Fujitsu's patented IOP-II (Isolation by Oxide and polysilicon) and fine lithography processing.

Operation for the MBM10490 is specified over a temperature range of 0°C to 75°C (T_A for DIP, T_C for Flat Package). It also features 22-pin Ceramic DIP or Flat Package, and is fully compatible with the industry standard 10K-series ECL families.



DIP-22C-A02



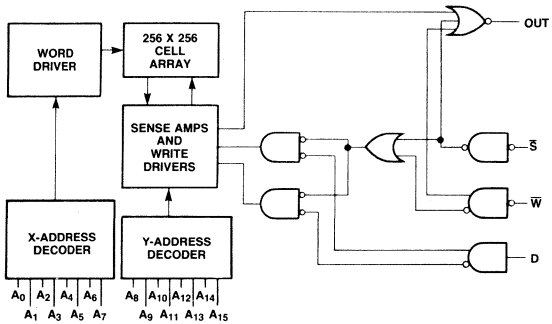
FPT-22C-C01

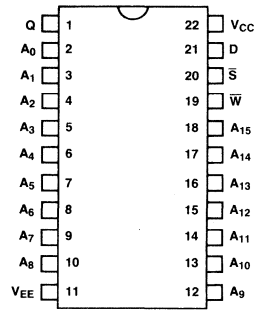
Features

- **65,536 words x 1-bit organization**
- **On-chip voltage compensation for improved noise margin**
- **Fully compatible with industry standard 10K-series ECL families**
- **Address access time:**
  15 ns max. (MBM10490-15)
  25 ns max. (MBM10490-25)
- **Open emitter output for ease of memory expansion**
- **Low power dissipation of:**
  0.024 mW/bit max. (MBM10490-15)
  0.014 mW/bit max. (MBM10490-25)
- **DOPOS and IOP-II**

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

MBM10490 Block Diagram and Pin Assignments

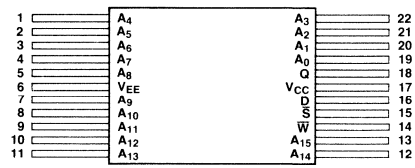




TRUTH TABLE

INPUT			OUTPUT	MODE
S̄	W̄	IN		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	OUT	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't Care



Functional Description

The Fujitsu MBM10490 is a fully decoded 65,536-bit read/write random access memory organized as 65,536 words by 1-bit. Memory cell selection is achieved by means of a 16-bit address designed A_0 through A_{15}. The active low Chip Select ($\overline{S}$) input is provided for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{W}$) input. With $\overline{W}$ and $\overline{S}$ held low, the data at D is written into the addressed location. To read, $\overline{W}$ is held high, while $\overline{S}$ is held low. Data at the addressed location is then transferred to Q and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
V_{EE} pin potential to ground pin	V_{EE}	+0.5 to −7.0	V
Input voltage	V_{IN}	+0.5 to V_{EE}	V
Output current (DC, output high)	I_{OUT}	−30	mA
Temperature under bias	T_A for DIP	−55 to +125	°C
	T_C for flat-package	−55 to +125	°C
Storage temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Capacitance

Parameter	Symbol	Min	Max	Unit
Input pin capacitance DIP/FPT	C_{IN}	2.0/1.0	5.0/4.0	pF
Output pin capacitance DIP/FPT	C_{OUT}	3.0/2.0	6.0/4.0	pF

Guaranteed Operating Conditions

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package
Supply voltage	V_{EE}	−5.46	−5.2	−4.94	V	0°C to 75°C

DC Characteristics

(V_{CC} = 0V, V_{EE} = −5.2V, Output Load = 50Ω to −2.0V, T_A = 0°C to 75°C for DIP, T_C = 0°C to 75°C for Flat Package, Airflow ≥2.5m/s, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A/T_C
Output high voltage (V_{IN} = V_{IH} max. or V_{IL} min.)	V_{OH}	−1000 −960 −900		−840 −810 −720	mV	0°C 25°C 75°C
Output low voltage (V_{IN} = V_{IH} max. or V_{IL} min.)	V_{OL}	−1870 −1850 −1830		−1665 −1650 −1625	mV	0°C 25°C 75°C
Output high voltage (V_{IN} = V_{IH} min. or V_{IL} max.)	V_{OHC}	−1020 −980 −920			mV	0°C 25°C 75°C
Output low voltage (V_{IN} = V_{IH} min. or V_{IL} max.)	V_{OLC}			−1645 −1630 −1605	mV	0°C 25°C 75°C
Input high voltage (guaranteed input voltage high for all inputs)	V_{IH}	−1145 −1105 −1045		−840 −810 −720	mV	0°C 25°C 75°C
Input low voltage (guaranteed input voltage low for all inputs)	V_{IL}	−1870 −1850 −1830		−1490 −1475 −1450	mV	0°C 25°C 75°C
Input high current (V_{IN} = V_{IH} max.)	I_{IH}			110	μA	0°C to 75°C
$\overline{S}$ input high current (V_{IN} = V_{IH} max.)	I_{IH}			220	μA	0°C to 75°C
Input low current (V_{IN} = V_{IL} min.)	I_{IL}	−50		90	μA	0°C to 75°C
$\overline{S}$ input low current (V_{IN} = V_{IL} min.)	I_{IL}	0.5		170	μA	0°C to 75°C
Power supply current (all inputs and outputs open) MBM10490-15	I_{EE}	−300			mA	0°C to 75°C
Power supply current (all inputs and outputs open) MBM10490-25	I_{EE}	−200			mA	0°C to 75°C

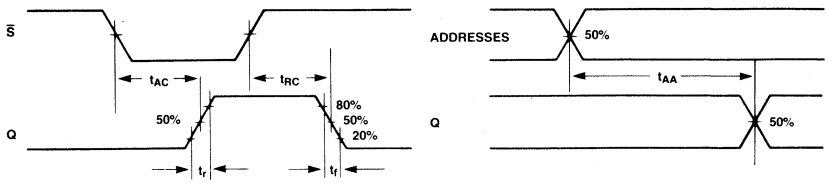
AC Characteristics

(V_{CC} = 0V, V_{EE} = −5.2V ±5%, Output Load = 50Ω to −2.0V and 30 pF to GND, T_A = 0°C to 75°C for DIP, T_C = 0°C to 75°C for Flat Package, Airflow ≥2.5 m/s, unless otherwise noted.)

Read Cycle

Parameter	Symbol	MBM10490-15 Min	MBM10490-15 Typ	MBM10490-15 Max	MBM10490-25 Min	MBM10490-25 Typ	MBM10490-25 Max	Unit
Address access time	t_{AA}			15			25	ns
Chip select access time	t_{AC}			10			15	ns
Chip select recovery time	t_{RC}			10			15	ns

Read Cycle Timing Diagram



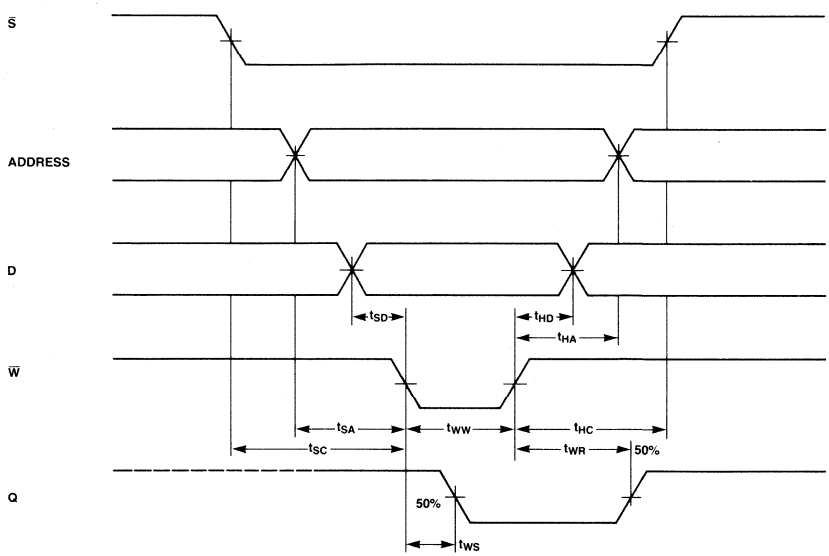
Write Cycle

Parameter	Symbol	MBM10490-15 Min	MBM10490-15 Typ	MBM10490-15 Max	MBM10490-25 Min	MBM10490-25 Typ	MBM10490-25 Max	Unit
Write pulse width	t_{WW}	15			20			ns
Write disable time	t_{WS}			10			20	ns
Write recovery time	t_{WR}			17			25	ns
Address set up time	t_{SA}	2			3			ns
Chip select set up time	t_{SC}	2			3			ns
Data set up time	t_{SD}	2			3			ns
Address hold time	t_{HA}	1			2			ns
Chip select hold time	t_{HC}	1			2			ns
Data hold time	t_{HD}	1			2			ns

AC Characteristics

(Continued)
(V_{CC} = 0V, V_{EE} = −5.2V ±5%, Output Load = 50Ω to −2.0V and 30 pF to GND, T_A = 0°C to 75°C for DIP, T_C = 0°C to 75°C for Flat Package, Airflow ≥2.5 m/s, unless otherwise noted.)

Write Cycle Timing Diagram

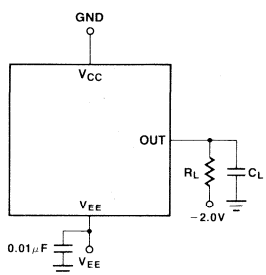


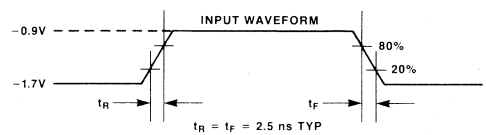
Rise Time and Fall Time

Parameter	Symbol	Min	Max	Unit
Output rise time −15/−25	t_r	1.0/1.0	2.0/3.0	ns
Output fall time −15/−25	t_f	1.0/1.0	2.0/3.0	ns

AC Test Conditions

OUTPUT LOAD:
R_L = 50Ω
C_L = 30 pF
(INCLUDING PROBE AND STRAY CAPACITANCE)



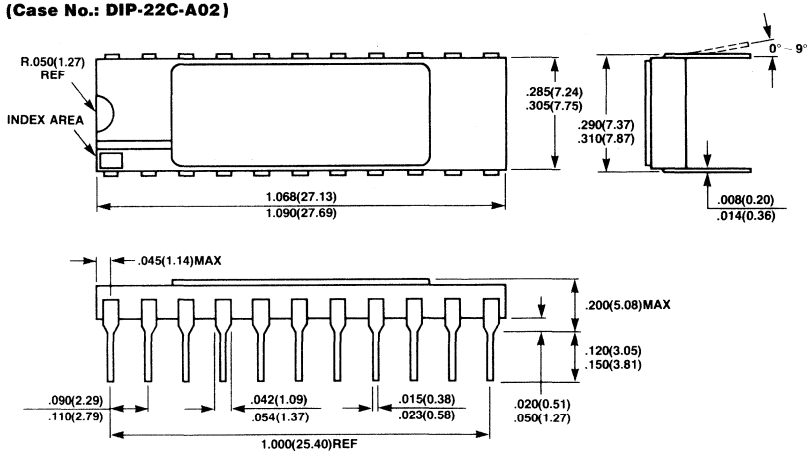


NOTE: ALL TIMING MEASUREMENTS REFERENCED 50% INPUT LEVELS.

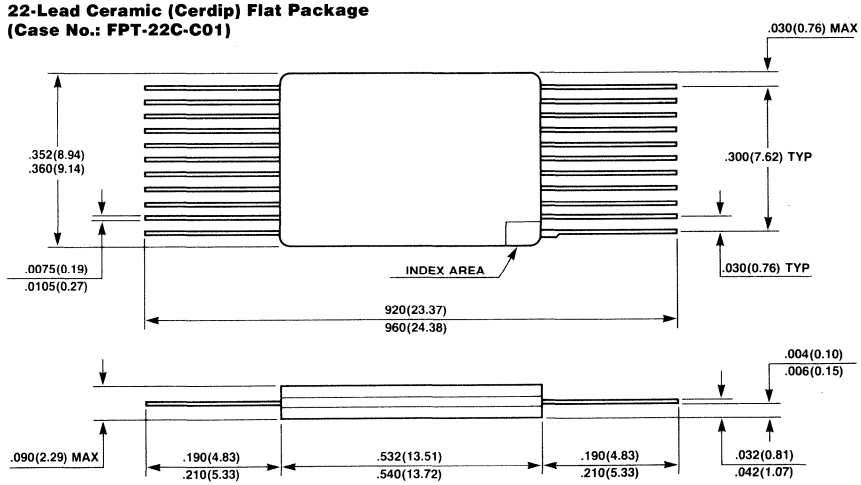
Package Dimensions

Dimensions in Inches
(millimeters)

22-Lead Ceramic (Metal Seal) Dual In-Line Package (Case No.: DIP-22C-A02)



22-Lead Ceramic (Cerdip) Flat Package (Case No.: FPT-22C-C01)



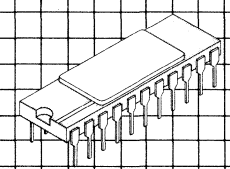
MBM100490
65,536-Bit Bipolar ECL Random Access Memory

Description

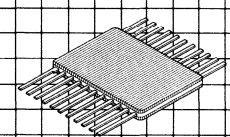
The Fujitsu MBM100490 is a fully decoded 65,536-bit ECL read/write random access memory designed for main memory, control, and buffer storage applications. The device is organized as 65,536 words by 1-bit, and it features on-chip voltage and temperature compensation for improved noise margin.

The MBM100490 offers extremely small cell and chip size, realized through the use of Fujitsu's patented IOP-II (Isolation by Oxide and polysilicon) and fine lithography processing.

Operation for the MBM100490 is specified over a temperature range of 0°C to 85°C (T_A for DIP, T_C for Flat Package). It also features 22-pin Ceramic DIP or Flat Package, and is fully compatible with the industry standard 100K-series ECL families.



DIP-22C-A02



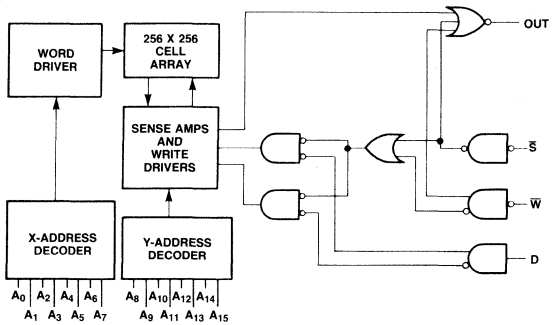
FPT-22C-C01

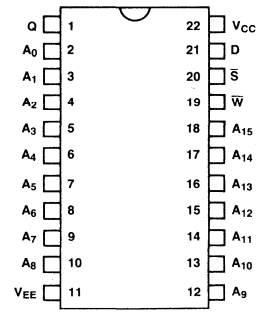
Features

- **65,536 words x 1-bit organization**
- **On-chip voltage and temperature compensation for improved noise margin**
- **Fully compatible with industry standard 100K-series ECL families**
- **Address access time:**
  15 ns max. (MBM100490-15)
  25 ns max. (MBM100490-25)
- **Open emitter output for ease of memory expansion**
- **Low power dissipation of:**
  0.021 mW/bit max. (MBM100490-15)
  0.014 mW/bit max. (MBM100490-25)
- **DOPOS and IOP-II**

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

MBM100490 Block Diagram and Pin Assignments

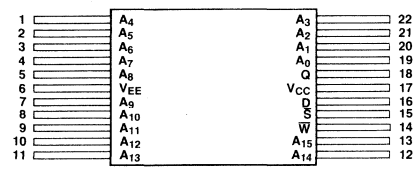




TRUTH TABLE

INPUT			OUTPUT	MODE
S̄	W̄	IN		
H	X	X	L	DISABLED
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	OUT	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't Care



Functional Description

The Fujitsu MBM100490 is a fully decoded 65,536-bit read/write random access memory organized as 65,536 words by 1-bit. Memory cell selection is achieved by means of a 16-bit address designed A_0 through A_{15}. The active low Chip Select ($\overline{S}$) input is provied for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{W}$) input. With $\overline{W}$ and $\overline{S}$ held low, the data at D is written into the addressed location. To read, $\overline{W}$ is held high, while $\overline{S}$ is held low. Data at the addressed location is then transferred to Q and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
V_{EE} pin potential to ground pin	V_{EE}	+0.5 to −7.0	V
Input voltage	V_{IN}	+0.5 to V_{EE}	V
Output current (DC, output high)	I_{OUT}	−30	mA
Temperature under bias	T_A for DIP	−55 to +125	°C
	T_C for flat-package	−55 to +125	°C
Storage temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur it ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Capacitance

Parameter	Symbol	Min	Max	Unit
Input pin capacitance DIP/FPT	C_{IN}	2.0/1.0	5.0/4.0	pF
Output pin capacitance DIP/FPT	C_{OUT}	3.0/2.0	6.0/4.0	pF

Guaranteed Operating Conditions
(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package
Supply voltage	V_{EE}	−4.7	−4.5	−4.2	V	0°C to 85°C

DC Characteristics
(V_{CC} = 0V, V_{EE} = −4.5V, Output Load = 50Ω to −2.0V, T_A = 0°C to 85°C for DIP, T_C = 0°C to 85°C for Flat Package, Airflow ≤2.5m/s, unless otherwise noted)

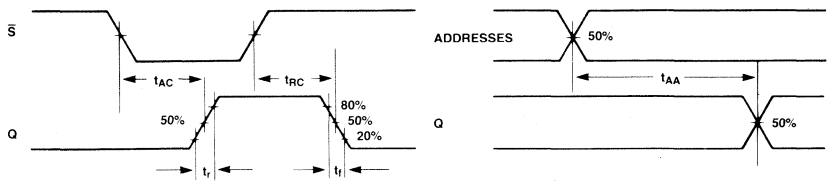
Parameter		Symbol	Min	Typ	Max	Unit	
Output high voltage (V_{IN} = V_{IH} max. or V_{IL} min.)		V_{OH}	−1025		−880	mV	
Output low voltage (V_{IN} = V_{IH} max. or V_{IL} min.)		V_{OL}	−1810		−1620	mV	
Output high voltage (V_{IN} = V_{IH} min. or V_{IL} max.)		V_{OHC}	−1035			mV	
Output low voltage (V_{IN} = V_{IH} min. or V_{IL} max.)		V_{OLC}			−1610	mV	
Input high voltage (guaranteed input voltage high for all inputs)		V_{IH}	−1165		−880	mV	
Input low voltage (guaranteed input voltage low for all inputs)		V_{IL}	−1810		−1475	mV	
Input high current (V_{IN} = V_{IH} max.)		I_{IH}			110	μA	0°C to 85°C
$\overline{S}$ input high current (V_{IN} = V_{IH} max.)		I_{IH}			220	μA	0°C to 85°C
Input low current (V_{IN} = V_{IL} min.)		I_{IL}	−50			μA	0°C to 85°C
$\overline{S}$ input low current (V_{IN} = V_{IL} min.)		I_{IL}	0.5		170	μA	0°C to 85°C
Power supply current (all inputs and outputs open)	MBM100490-15	I_{EE}	−300			mA	0°C to 85°C
	MBM100490-25		−200				

AC Characteristics
(V_{CC} = 0V, V_{EE} = −4.5V ±5%, Output Load = 50Ω to −2.0V and 30 pF to GND, T_A = 0°C to 85°C for DIP, T_C = 0°C to 85°C for Flat Package, Airflow ≥2.5 m/s, unless otherwise noted.)

Read Cycle

Parameter	Symbol	MBM100490-15 Min	Typ	Max	MBM100490-25 Min	Typ	Max	Unit
Address access time	t_{AA}			15			25	ns
Chip select access time	t_{AC}			10			15	ns
Chip select recovery time	t_{RC}			10			15	ns

Read Cycle Timing Diagram



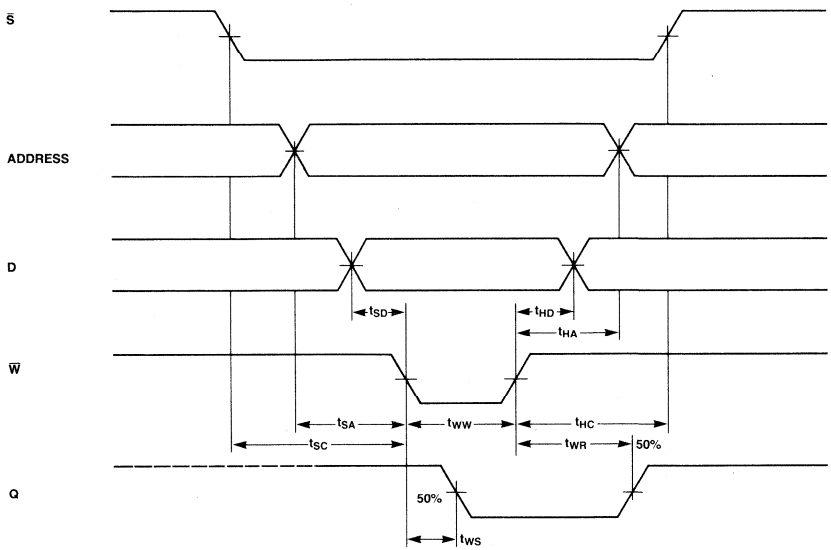
Write Cycle

Parameter	Symbol	MBM100490-15 Min	Typ	Max	MBM100490-25 Min	Typ	Max	Unit
Write pulse width	t_{WW}	15			20			ns
Write disable time	t_{WS}			10			20	ns
Write recovery time	t_{WR}			17			25	ns
Address set up time	t_{SA}	2			3			ns
Chip select set up time	t_{SC}	2			3			ns
Data set up time	t_{SD}	2			3			ns
Address hold time	t_{HA}	1			2			ns
Chip select hold time	t_{HC}	1			2			ns
Data hold time	t_{HD}	1			2			ns

AC Characteristics

(Continued)
(V_{CC} = 0V, V_{EE} = −4.5V ±5%, Output Load = 50Ω to −2.0V and 30 pF to GND, T_A = 0°C to 85°C for DIP, T_C = 0°C to 85°C for Flat Package, Airflow ≥2.5 m/s, unless otherwise noted.)

Write Cycle Timing Diagram

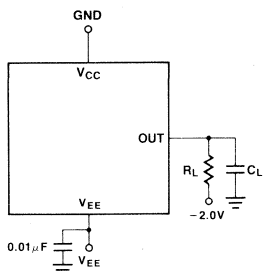


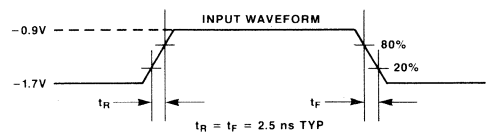
Rise Time and Fall Time

Parameter	Symbol	Min	Max	Unit
Output rise time	t_r −15/−25	1.0/1.0	2.0/3.0	ns
Output fall time	t_f −15/−25	1.0/1.0	2.0/3.0	ns

AC Test Conditions

OUTPUT LOAD:
R_L = 50Ω
C_L = 30 pF
(INCLUDING PROBE AND STRAY CAPACITANCE)

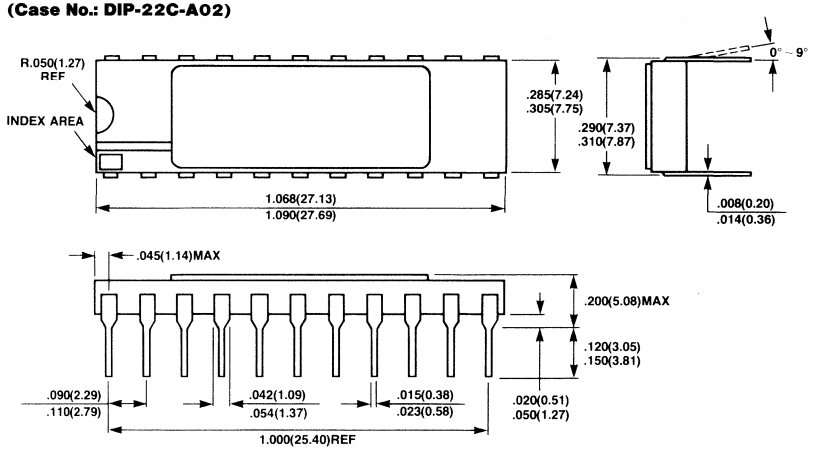




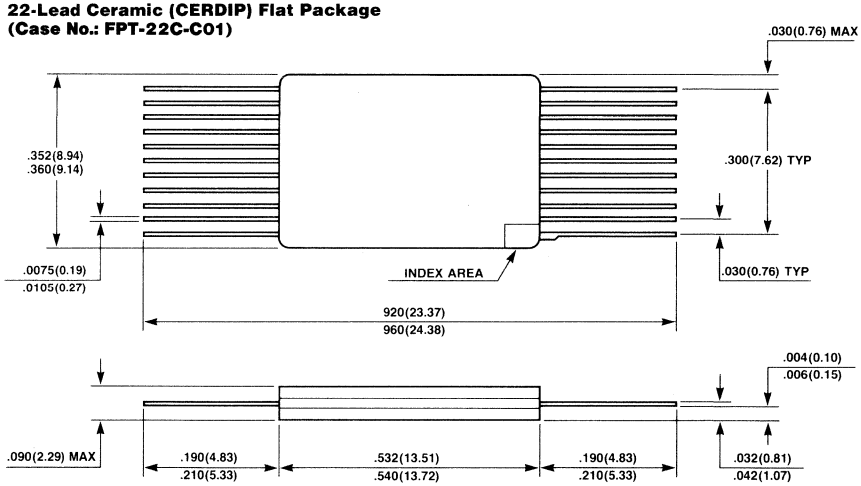
NOTE: ALL TIMING MEASUREMENTS REFERENCED 50% INPUT LEVELS.

Package Dimensions
Dimensions in Inches
(millimeters)

22-Lead Ceramic (Metal Seal) Dual In-Line Package
(Case No.: DIP-22C-A02)



22-Lead Ceramic (CERDIP) Flat Package
(Case No.: FPT-22C-C01)



FUJITSU

MB70801-15

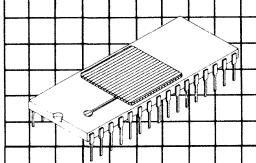
4,608-Bit Bipolar Random Access Memory

Description

The Fujitsu MB70801-15 is a fully decoded 4608-bit ECL read/write random access memory designed for high-speed scratch pad, control and buffer storage applications. This device is organized as 512 words by 9-bits, and it features on-chip voltage compensation for improved noise margin.

The MB70801-15 offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon), processing. As a result, very fast access time with high yields and outstanding device reliability are achieved in volume production.

Operation for the MB70801-15 is specified over a temperature range of 0° to 75°C (ambient). It also features metal-sealed 32-pin dual-in-line packaging, and it is fully compatible with industry-standard 10K-series ECL families.



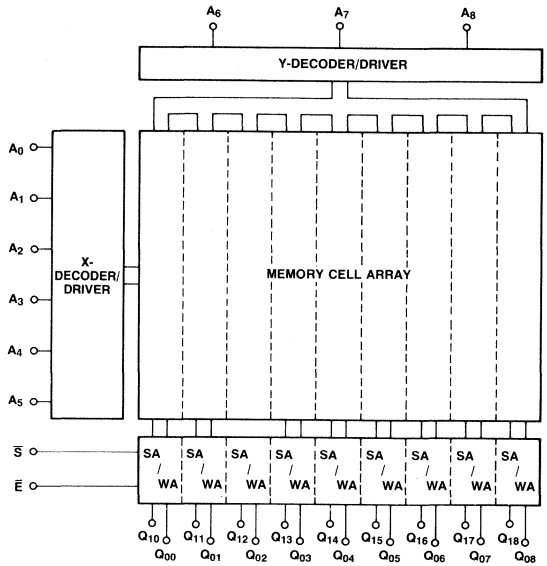
Ceramic Package DIP-32C-A01

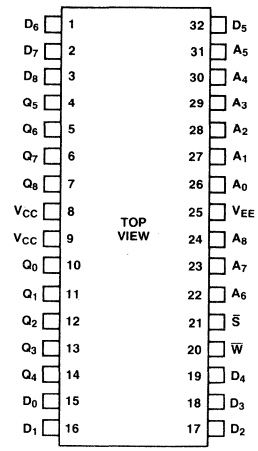
Features

- **512 words x 9-bits organization**
- **On-chip voltage compensation for improved noise margin**
- **Fully compatible with industry-standard 10K-series ECL families**
- **Address access time: 15 ns max. 12 ns typ.**
- **Chip select access time: 10 ns max. 6 ns typ.**
- **Open emitter output for ease of memory expansion**
- **Low power dissipation of 0.25 mW/bit typ.**
- **DOPOS and IOP-II processing**

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

MB70801-15 Block Diagram and Pin Assignment





TRUTH TABLE

INPUT			OUTPUT (Q)	MODE
$\overline{S}$	$\overline{W}$	IN		
H	X	X	L	DISABLE
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	OUT	READ

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
V_{EE} pin potential to ground pin	V_{EE}	+0.5 to −7.0	V
Input voltage	V_{IN}	+0.5 to V_{EE}	V
Output current (DC, output high)	I_{OUT}	−30	mA
Temperature under bias	T_A	−55 to +125	°C
Storage temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Functional Description

The Fujitsu MB70801-15 is a fully decoded 4,608 bit read/write random access memory organized as 512 words by 9 bits. Memory cell selection is achieved by means of a 9-bit address designated A_0 through A_8. The active low Chip Select ($\overline{S}$) input is provied for memory expansion. The read and write operations are controlled by the state of the active low Write Enable ($\overline{W}$) input. With $\overline{W}$ and $\overline{S}$ held low, the data at IN is written into the address location. To read, $\overline{W}$ is held high, while $\overline{S}$ is held low. Data at the addressed location is then transferred to OUT and read out non-inverted. Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

Guaranteed Operating Conditions

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Supply voltage	V_{EE}	−5.46	−5.2	−4.94	V	0°C to 75°C

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input pin capacitance	C_{IN}		4	6	pF
Output pin capacitance	C_{OUT}		6	8	pF

DC Characteristics

(V_{CC} = 0V, V_{EE} = −5.2V, Output Load = 50Ω to −2.0V, unless otherwise noted.)

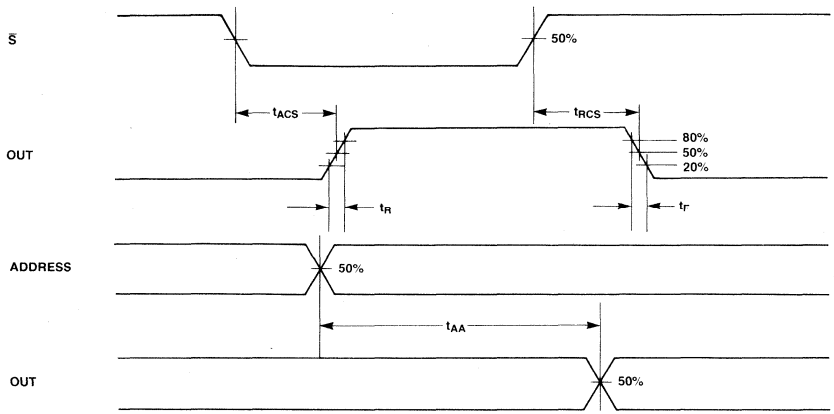
Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output high voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	−1000 −960 −900		−840 −810 −720	mV	0°C 25°C 75°C
Output low voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	−1870 −1850 −1830		−1665 −1650 −1625	mV	0°C 25°C 75°C
Output high voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	−1020 −980 −920			mV	0°C 25°C 75°C
Output low voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			−1645 −1630 −1605	mV	0°C 25°C 75°C
Input high voltage (guaranteed input voltage high for all inputs)	V_{IH}	−1145 −1105 −1045		−840 −810 −720	mV	0°C 25°C 75°C
Input low voltage (guaranteed input voltage low for all inputs)	V_{IL}	−1870 −1850 −1830		−1490 −1475 −1450	mV	0°C 25°C 75°C
Input high current ($V_{IN} = V_{IH\ max}$)	I_{IH}			220	μA	0°C to 75°C
Input low current ($V_{IN} = V_{IL\ min}$)	I_{IL}	−50			μA	0°C to 75°C
$\overline{S}$ input low current ($V_{IN} = V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power supply current (all inputs and outputs open)	I_{EE}	−260			mA	0°C to 75°C

AC Characteristics
(Full Guaranteed Operating Ranges, Output Load = 50Ω to −2.0V and 30pF to GND and Airflow ≥2.5 m/s unless otherwise noted.)

Read Cycle

Parameter	Symbol	Min	Typ	Max	Unit
Address access time	t_{AA}	4	12	15	ns
Chip select access time	t_{ACS}	2	6	10	ns
Chip select recovery time	t_{RCS}	2	6	10	ns

Read Cycle Timing Diagram

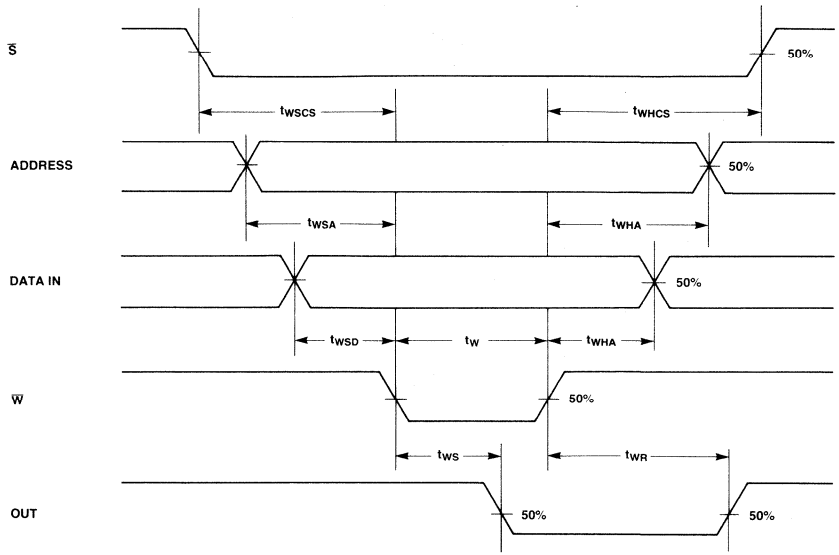


Write Cycle

Parameter	Symbol	Min	Typ	Max	Unit
Write pulse width	t_W	12			ns
Write disable time	t_{WS}			10	ns
Write recovery time	t_{WR}			12	ns
Address set up time	t_{WSA}	2.5			ns
Chip select set up time	t_{WSCS}	1.5			ns
Data set up time	t_{WSD}	1.5			ns
Address hold time	t_{WHA}	0.5			ns
Chip select hold time	t_{WHCS}	1.5			ns
Data hold time	t_{WHD}	1.5			ns

AC Characteristics
(Continued)

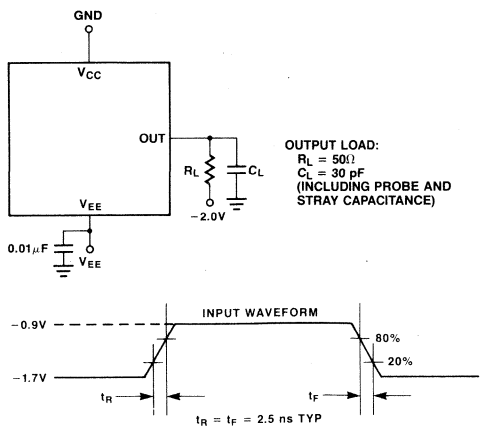
Write Cycle Timing Diagram



Rise Time and Fall Time

Parameter	Symbol	Min	Typ	Max	Unit
Output rise time	t_r	1.0	2.0	5.0	ns
Output fall time	t_f	1.0	2.0	5.0	ns

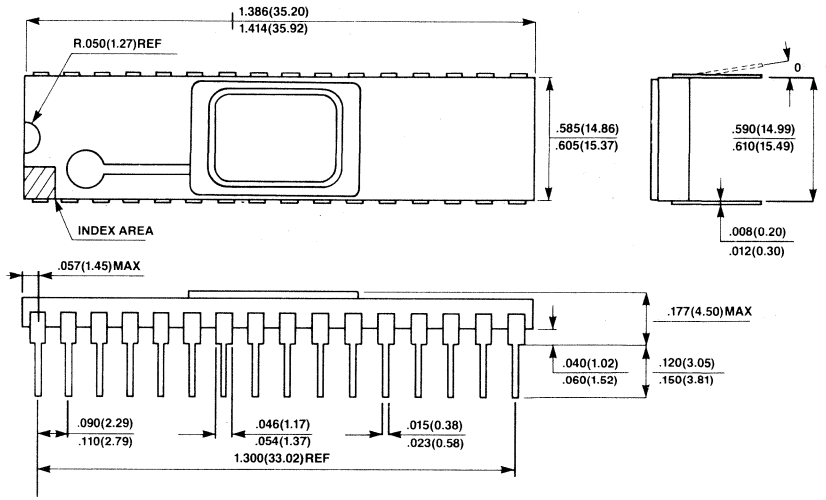
AC Test Conditions



NOTE: ALL TIMING MEASUREMENTS REFERENCED 50% INPUT LEVELS.

Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

32-Lead Ceramic (Metal Seal) Dual In-Line Package
(Case No.: DIP-32C-A01)



FUJITSU

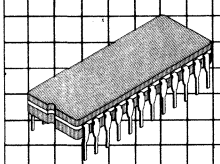
MB70802-20
4,608-Bit Buffer Address Array

Description

The Fujitsu MB70802 is a 4608-bit ECL read/write buffer address array which can be used for wider tag addresses or deeper tag memories. The device is organized as a high speed 512 words by 9-bits static RAM array, parity generator/checker, and 9-bit high speed comparator. It also features on-chip voltage compensation for improved noise margin.

The MB70802 offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon), processing. As a result, very fast access time, high yields, and outstanding device reliability are achieved in volume production.

Operation for the MB70802 is specified over a temperature range of from 0° to 75°C (ambient). It also features standard ceramic 24-pin dual-in-line packaging, and it is fully compatible with industry-standard 10K-series ECL families.



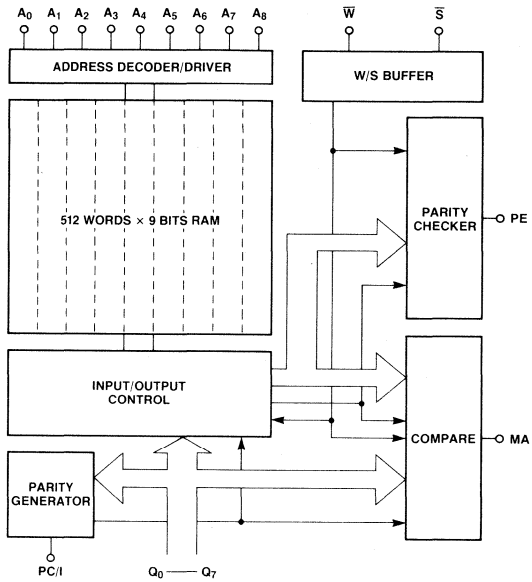
DIP-24C-C05

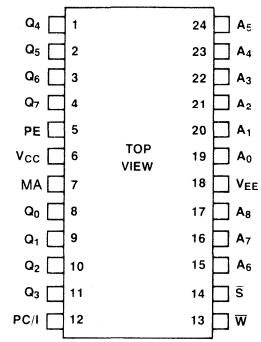
Features

- **512 words x 9-bits organization**
- **On-chip parity generator/checker**
- **9-bit high speed comparator.**
- **On-chip voltage compensation for improved noise margin**
- **Fully compatible with industry-standard 10K-series ECL families**
- **Parity Error address access time:**
  20 ns max.
  18 ns typ.
- **Match address access time:**
  20 ns max.
  18 ns typ.
- **Match data in access time:**
  15 ns max.
  12 ns typ.
- **Chip select access time:**
  10 ns max.
  6 ns typ.
- **Open emitter output for ease of memory expansion**
- **Low power dissipation of 0.25 mW/bit typ.**
- **DOPOS and IOP-II processing**

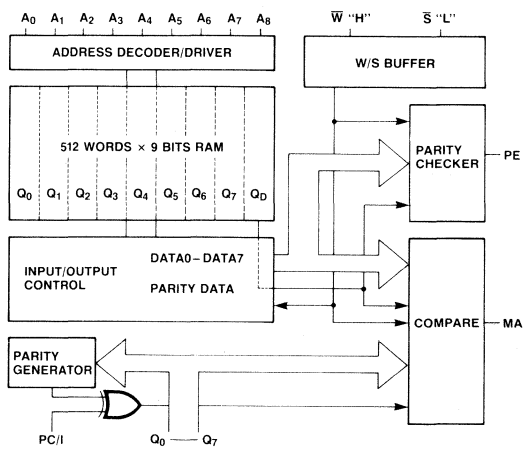
Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

MB70802 Block Diagrams and Pin Assignment



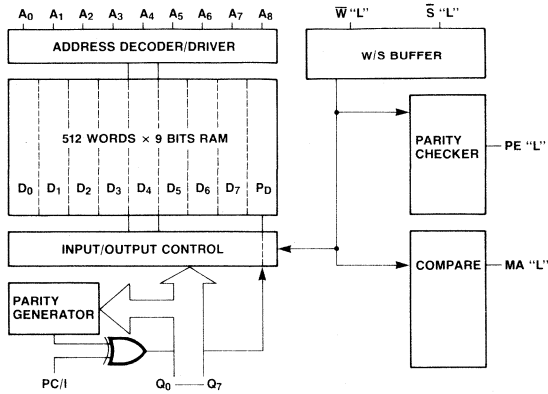


Read Operating Data—Signal Flow



MB70802 Block Diagram and Pin Assignment
(Continued)

Write Operating Data—Signal Flow



TRUTH TABLE

INPUT				OUTPUT		
PC/I	$\overline{S}$	$\overline{W}$	D_I	MATCH	PE	
X	H	X	X	L	L	DISABLE
PI	L	L	D_I	L	L	WRITE "D_I"
PI	L	H	D_I	L	PI	EQUAL (READ)
PI	L	H	D_I	L	$\overline{PI}$	UNDEFINED ERROR (READ)
PI	L	H	D_I	H	PI	NOT EQUAL (READ)
PI	L	H	D_I	H	$\overline{PI}$	PARITY ERROR (READ)

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
D_I = DATA IN
PI = H OR L
X = DON'T CARE

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
V_{EE} pin potential to ground pin	V_{EE}	+0.5 to −7.0	V
Input voltage	V_{IN}	+0.5 to V_{EE}	V
Output current (DC, output high)	I_{OUT}	−30	mA
Temperature under bias	T_A	−55 to +125	°C
Storage temperature	T_{stg}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Functional Description

The Fujitsu MB70802 is a 4,608-bit buffer address array organized as a high speed 512 words by 9-bits static RAM array, parity generator/checker, and 9-bit high speed comparator. Word selection is achieved by means of a 9-bit address designated A_0–A_8.

The active low chip select ($\overline{S}$) input is provided for memory array expansion. The read (Compare/Parity Checker) and write operations are controlled by the state of the active low Write Enable ($\overline{W}$) input. With $\overline{W}$ and $\overline{S}$ held low, the 8-bit data on Q_0 to Q_7 and a parity bit data generated by parity generator are written into the addressed location. If a PC/I input holds low (high) under the write operation, a parity error flag is high (low) under the read operation. To read, $\overline{W}$ is held high, while $\overline{S}$ is held low. The 8-bit data and parity bit data are input to all the comparators which perform a match of the nine inputs (one word) against the stored word. If a particular word is identical to the input word, such comparators generate a match signal. Simultaneously, the 9-bit stored data is checked by the parity checker.

Guaranteed Operating Conditions

(Referenced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	T_A
Supply voltage	V_{EE}	−5.46	−5.2	−4.94	V	0°C to 75°C

Capacitance

Parameter	Symbol	Min	Typ	Max	Unit
Input pin capacitance	C_{IN}		4	6	pF
Output pin capacitance	C_{OUT}		6	8	pF

DC Characteristics

(V_{CC} = 0V, V_{EE} = −5.2V, Output Load = 50Ω to −2.0V, unless otherwise noted.)

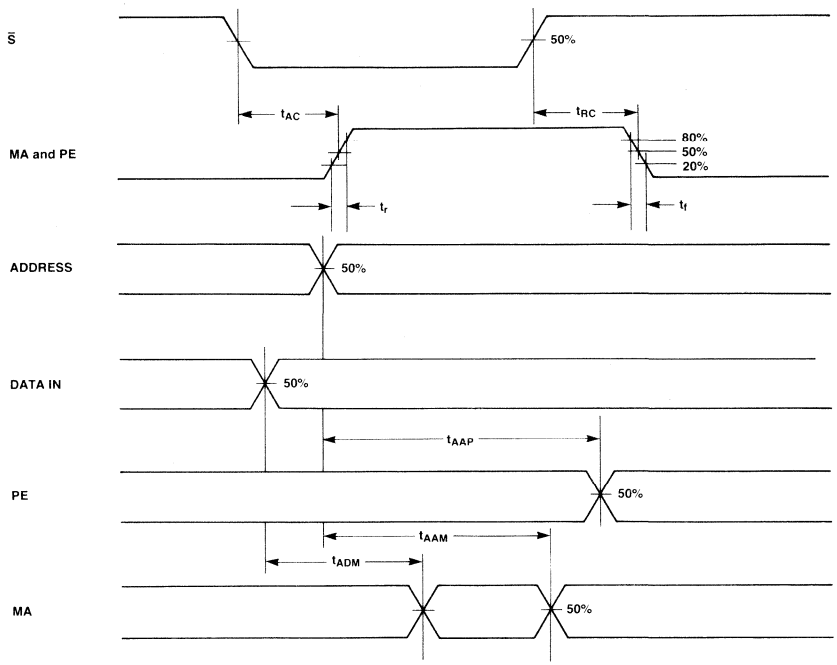
Parameter	Symbol	Min	Typ	Max	Unit	T_A
Output high voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	−1000 −960 −900		−840 −810 −720	mV	0°C 25°C 75°C
Output low voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	−1870 −1850 −1830		−1665 −1650 −1625	mV	0°C 25°C 75°C
Output high voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)	V_{OHC}	−1020 −980 −920			mV	0°C 25°C 75°C
Output low voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			−1645 −1630 −1605	mV	0°C 25°C 75°C
Input high voltage (guaranteed input voltage high for all inputs)	V_{IH}	−1145 −1105 −1045		−840 −810 −720	mV	0°C 25°C 75°C
Input low voltage (guaranteed input voltage low for all inputs)	V_{IL}	−1870 −1850 −1830		−1490 −1475 −1450	mV	0°C 25°C 75°C
Input high current ($V_{IN} = V_{IH\ max}$)	I_{IH}			220	μA	0°C to 75°C
Input low current ($V_{IN} = V_{IL\ min}$)	I_{IL}	−50			μA	0°C to 75°C
$\overline{S}$ and PC/I Input low current ($V_{IN} = V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power supply current (all inputs and outputs open)	I_{EE}	−260			mA	0°C to 75°C

AC Characteristics
(Full Guaranteed Operating Ranges, Output Load = 50Ω to −2.0V and 30pF to GND and Airflow ≥2.5 m/s unless otherwise noted.)

Read Cycle

Parameter	Symbol	Min	Typ	Max	Unit
Parity error address access time	t_{AAP}	4	18	20	ns
Match address access time	t_{AAM}	4	18	20	ns
Match data in access time	t_{ADM}	2	12	15	ns
Chip select access time	t_{AC}	2	6	10	ns
Chip select recovery time	t_{RC}	2	6	10	ns

Read Cycle Timing Diagram

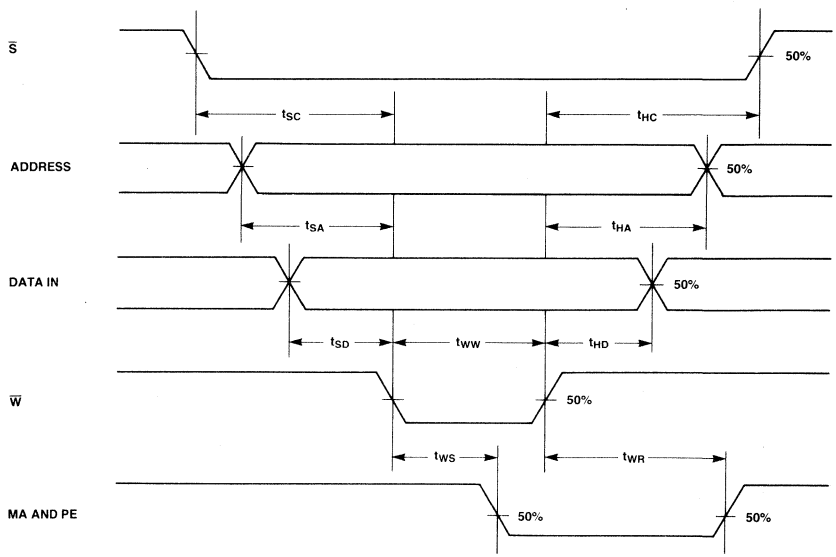


AC Characteristics
(Continued)
(Full Guaranteed Operating Ranges, Output Load = 50Ω to −2.0V and 30pF to GND and Airflow ≥2.5 m/s unless otherwise noted.)

Write Cycle

Parameter	Symbol	Min	Typ	Max	Unit
Write pulse width	t_{WW}	17			ns
Write disable time	t_{WS}			10	ns
Write recovery time	t_{WR}			18	ns
Address set up time	t_{SA}	1.5			ns
Chip select set up time	t_{SC}	1.5			ns
Data set up time	t_{SD}	1.5			ns
Address hold time	t_{HA}	1.5			ns
Chip select hold time	t_{HC}	1.5			ns
Data hold time	t_{HD}	1.5			ns

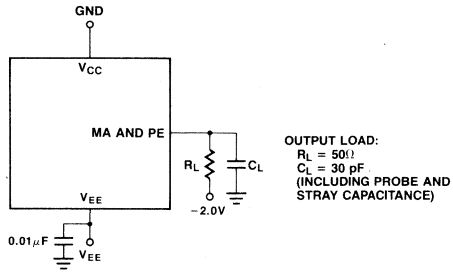
Write Cycle Timing Diagram

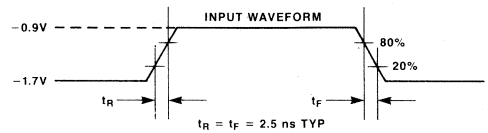


Rise Time and Fall Time

Parameter	Symbol	Min	Typ	Max	Unit
Output rise time	t_r	1.0	2.0	5.0	ns
Output fall time	t_f	1.0	2.0	5.0	ns

AC Test Conditions





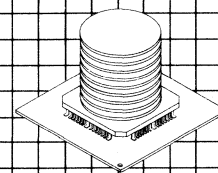
NOTE: ALL TIMING MEASUREMENTS REFERENCED 50% INPUT LEVELS.

MB7700H Series
ECL Bipolar RAM

Description

The Fujitsu MB7700H series are 4K-bit ECL read/write random access memories designed for applications of high-speed scratch pad, control and buffer storage. The device consists of 4-planes of 256 words x 4-bits memory arrays. By means of the metal options, several kinds of organizations for various usages within a system are realized (e.g. 256 words x 16-bits, 512 words x 8-bits and so on).

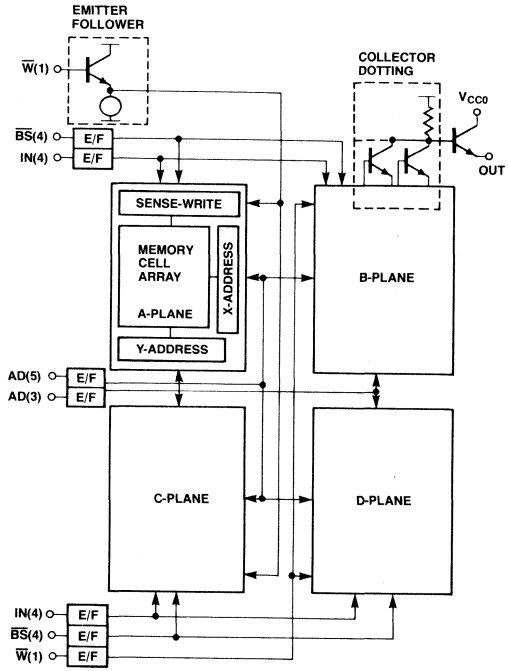
The MB7700H series offers extremely small cell size realized through the use of IOP-II (Isolation by Oxide and Polysilicon) processing. As a result, very fast access times are achieved.

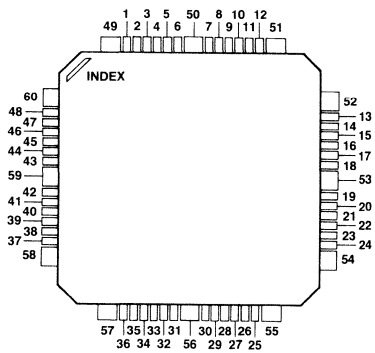


Features

- **256 words x 16-bits organization (basic)**
- **On-chip voltage compensation for improved noise margin**
- **Fully compatible with 10K ECL families**
- **Address access time 5 ns (max.) 4 ns (typ.)**
- **Power dissipation 6W (max.) 3.6W (typ.)**
- **Open emitter output for ease of memory expansion**
- **60 Pin FLAT package**
- **Metal options**

MB7700H Block Diagram and Pin Assignment





TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{BS}$	$\overline{W}$	D		
H	X	X	L	DISABLE
L	L	H	L	WRITE "H"
L	L	L	L	WRITE "L"
L	H	X	O	READ

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE

Pin Assignment Table

Pin No.	Part No. 7701H	7702H	7703H	7704H	7705H	7706H
1	$O_{23.a}$	$O_{3.a}$	$O_{3.a}$	$O_{3.a}$	$O_{3.a}$	$O_{0.ac}$
2	$O_{01.a}$	$O_{2.a}$	$O_{2.a}$	$O_{2.a}$	$O_{2.a}$	$O_{1.ac}$
3	A_0	A_0	A_0	$A_{0.ab}$	A_0	$A_{0.ab}$
4	A_1	A_1	A_1	$A_{1.ab}$	A_1	$A_{1.ab}$
5	A_2	A_2	A_2	$A_{2.ab}$	A_2	A_2
6	A_3	A_3	A_3	$A_{3.ab}$	A_3	A_3
7	$O_{01.b}$	$O_{0.b}$	$O_{0.b}$	$O_{0.b}$	$O_{0.b}$	$D_{0.ab}$
8	$O_{23.b}$	$O_{1.b}$	$O_{1.b}$	$O_{1.b}$	$O_{1.b}$	$D_{1.ab}$
9	$D_{0.b}$	$O_{2.b}$	$O_{2.b}$	$O_{2.b}$	$O_{2.b}$	$D_{2.ab}$
10	$D_{1.b}$	$O_{3.b}$	$O_{3.b}$	$O_{3.b}$	$O_{3.b}$	$D_{3.ab}$
11	A_4	A_4	A_4	$A_{4.ab}$	A_4	A_4
12	A_5	A_5	A_5	$A_{5.ab}$	A_5	A_5
13	A_6	A_6	A_6	$A_{6.ab}$	A_6	A_6
14	A_7	A_7	A_7	$A_{7.ab}$	A_7	A_7
15	$D_{2.b}$	$D_{1.ab}$	$D_{1.b}$	$D_{1.ab}$	$D_{.b}$	N.C.
16	$D_{3.b}$	$D_{0.ab}$	$D_{0.b}$	$D_{0.ab}$	$\overline{BS}_3$	$\overline{BS}_{0.ab}$
17	N.C.	N.C.	$\overline{BS}_{.b}$	$\overline{BS}_{.b}$	$\overline{BS}_2$	$\overline{BS}_{1.ab}$
18	$\overline{W}_{.b}$	$\overline{W}_{.bd}$	$\overline{W}_{.ab}$	$\overline{W}_{.ab}$	$\overline{W}_{.b}$	$\overline{W}_{.bd}$
19	$\overline{W}_{.d}$	$\overline{BS}_{.cd}$	$\overline{BS}_{.d}$	$\overline{BS}_{.d}$	$\overline{W}_{.d}$	N.C.
20	N.C.	N.C.	N.C.	N.C.	N.C.	$\overline{BS}_{3.cd}$
21	$\overline{BS}_2$	$D_{3.cd}$	$D_{3.b}$	$D_{3.cd}$	N.C.	$\overline{BS}_{2.cd}$
22	$\overline{BS}_1$	$D_{2.cd}$	$D_{2.b}$	$D_{2.cd}$	$D_{.d}$	N.C.
23	N.C.	$O_{1.d}$	$O_{1.d}$	$O_{1.d}$	$O_{1.d}$	$O_{3.bd}$
24	N.C.	$O_{0.d}$	$O_{0.d}$	$O_{0.d}$	$O_{0.d}$	$O_{2.bd}$
25	$O_{23.d}$	$O_{3.d}$	$O_{3.d}$	$O_{3.d}$	$O_{3.d}$	$O_{0.bd}$
26	$O_{01.d}$	$O_{2.d}$	$O_{2.d}$	$O_{2.d}$	$O_{2.d}$	$O_{1.bd}$
27	$D_{3.d}$	N.C.	$D_{1.d}$	$A_{0.cd}$	N.C.	$A_{0.cd}$
28	$D_{2.d}$	N.C.	$D_{0.d}$	$A_{1.cd}$	N.C.	$A_{1.cd}$
29	$D_{1.d}$	N.C.	$D_{2.d}$	$A_{2.cd}$	N.C.	N.C.
30	$D_{0.d}$	N.C.	$D_{3.d}$	$A_{3.cd}$	N.C.	N.C.

Pin No.	Part No. 7701H	7702H	7703H	7704H	7705H	7706H
31	$O_{01.c}$	$O_{0.c}$	$O_{0.c}$	$O_{0.c}$	$O_{0.c}$	$D_{0.cd}$
32	$O_{23.c}$	$O_{1.c}$	$O_{1.c}$	$O_{1.c}$	$O_{1.c}$	$D_{1.cd}$
33	$D_{0.c}$	$O_{2.c}$	$O_{2.c}$	$O_{2.c}$	$O_{2.c}$	$D_{2.cd}$
34	$D_{1.c}$	$O_{3.c}$	$O_{3.c}$	$O_{3.c}$	$O_{3.c}$	$D_{3.cd}$
35	N.C.	N.C.	$D_{2.c}$	$A_{4.cd}$	N.C.	N.C.
36	N.C.	N.C.	$D_{3.c}$	$A_{5.cd}$	N.C.	N.C.
37	$D_{3.c}$	N.C.	$D_{1.c}$	$A_{6.cd}$	N.C.	N.C.
38	$D_{2.c}$	N.C.	$D_{0.c}$	$A_{7.cd}$	N.C.	N.C.
39	$\overline{BS}_3$	$D_{1.cd}$	$D_{3.a}$	$D_{1.cd}$	$D_{.c}$	N.C.
40	$\overline{BS}_0$	$D_{0.cd}$	$D_{2.a}$	$D_{0.cd}$	$\overline{BS}_0$	$\overline{BS}_{0.cd}$
41	N.C.	N.C.	$\overline{BS}_{.c}$	$\overline{BS}_{.c}$	$\overline{BS}_1$	$\overline{BS}_{1.cd}$
42	$\overline{W}_{.c}$	$\overline{W}_{.ac}$	$\overline{W}_{.cd}$	$\overline{W}_{.cd}$	$\overline{W}_{.c}$	$\overline{W}_{.ac}$
43	$\overline{W}_{.a}$	$\overline{BS}_{.ab}$	$\overline{BS}_{.a}$	$\overline{BS}_{.a}$	$\overline{W}_{.a}$	N.C.
44	N.C.	N.C.	N.C.	N.C.	N.C.	$\overline{BS}_{3.ab}$
45	$D_{0.a}$	$D_{3.ab}$	$D_{0.a}$	$D_{3.ab}$	N.C.	$\overline{BS}_{2.ab}$
46	$D_{1.a}$	$D_{2.ab}$	$D_{1.a}$	$D_{2.ab}$	$D_{.a}$	N.C.
47	$D_{2.a}$	$O_{1.a}$	$O_{1.a}$	$O_{1.a}$	$O_{1.a}$	$O_{3.ac}$
48	$D_{3.a}$	$O_{0.a}$	$O_{0.a}$	$O_{0.a}$	$O_{0.a}$	$O_{2.ac}$
49	$V_{CC.a}$	$V_{CC.a}$	$V_{CC.a}$	$V_{CC.a}$	$V_{CC.a}$	$V_{CC.a}$
50	V_{CC0}	V_{CC0}	V_{CC0}	V_{CC0}	V_{CC0}	V_{CC0}
51	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
52	V_{EE2}	V_{EE2}	V_{EE2}	V_{EE2}	V_{EE2}	V_{EE2}
53	V_{EE1}	V_{EE1}	V_{EE1}	V_{EE1}	V_{EE1}	V_{EE1}
54	V_{EE2}	V_{EE2}	V_{EE2}	V_{EE2}	V_{EE2}	V_{EE2}
55	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
56	V_{CC0}	V_{CC0}	V_{CC0}	V_{CC0}	V_{CC0}	V_{CC0}
57	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
58	V_{EE2}	V_{EE2}	V_{EE2}	V_{EE2}	V_{EE2}	V_{EE2}
59	V_{EE1}	V_{EE1}	V_{EE1}	V_{EE1}	V_{EE1}	V_{EE1}
60	V_{EE2}	V_{EE2}	V_{EE2}	V_{EE2}	V_{EE2}	V_{EE2}

$V_{CC} = V_{CC0} = 0V$, $V_{EE1} = -3.6V$, $V_{EE2} = -5.2V$

Note: Pin name definition

$O_{1.a}$
- → Plane location
- → Terminal name of plane

$O_{1,2.a}$ → O_1, O_2 dot (between terminals in a plane)

$O_{1.ab}$ → Plane "a", plane "b" dot (between planes)

N.C. Non connection

Absolute Maximum Ratings

Rating	Symbol	Value	Unit
V_{EE1} pin potential to ground pin (V_{CC})	V_{EE1}	+0.5 to −7.0	V
V_{EE2} pin potential to ground pin (V_{CC})	V_{EE2}	+0.5 to −7.0	V
Input voltage	V_{IN}	+0.5 to V_{EE}	V
Output current (DC, output high)	I_{OUT}	−30	mA
Temperature under bias	T_A	−25 to 100	°C
Storage temperature	T_{STG}	−55 to 125	°C

Note: Input pins except (BS) should not be left open.

Guaranteed Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{EE1}	−3.78	−3.60	−3.42	V
Supply voltage	V_{EE2}	−5.46	−5.20	−4.94	V
Case temperature	T_A	0		55	°C

DC Characteristics

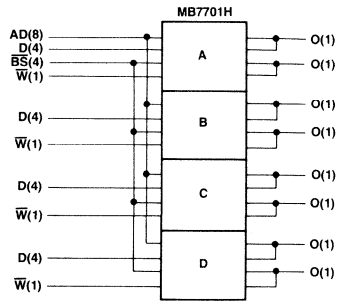
(MB7701/MB7702/MB7703/MB7704/MB7705/MB7706 $V_{CC} = V_{CC0} = 0V$, $V_{EE1} = -3.6V$, $V_{EE2} = -5.2V$ Output Load = 50 Ohm to −2.0V)

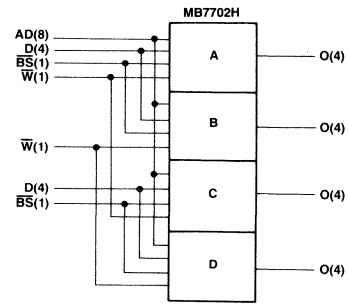
Parameter		Symbol	Min	Typ	Max	Unit	T_A
Output high voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)		V_{OH}	−1000 −960 −925		−840 −810 −755	mV	0°C 25°C 55°C
Output low voltage ($V_{IN} = V_{IH\ max}$ or $V_{IL\ min}$)		V_{OL}	−1870 −1850 −1840		−1630 −1615 −1600	mV	0°C 25°C 55°C
Output high voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)		V_{OHC}	−1020 −980 −945			mV	0°C 25°C 55°C
Output low voltage ($V_{IN} = V_{IH\ min}$ or $V_{IL\ max}$)		V_{OLC}			−1610 −1595 −1580	mV	0°C 25°C 55°C
Input high voltage		V_{IH}	−1145 −1105 −1070		−840 −810 −755	mV	0°C 25°C 55°C
Input low voltage		V_{IL}	−1870 −1850 −1840		−1490 −1475 −1460	mV	0°C 25°C 55°C
Input high current ($V_{IN} = V_{IH\ max}$)	Address	$I_{IH(A)}$			220	μA	0° to 55°C
	Data in	$I_{IH(D)}$			220	μA	
	Write enable	$I_{IH(W)}$			220	μA	
	Block select	$I_{IH(BS)}$			220	μA	
Input low current ($V_{IN} = V_{IL\ min}$)	Address	$I_{IL(A)}$			170	μA	0° to 55°C
	Data in	$I_{IL(D)}$			170	μA	
	Write enable	$I_{IL(W)}$			170	μA	
	Block select	$I_{IL(BS)}$	0.5		170	μA	
Power supply current		I_{EE1}	−480			mA	0° to 55°C
Power supply current		I_{EE2}	−800			mA	0° to 55°C

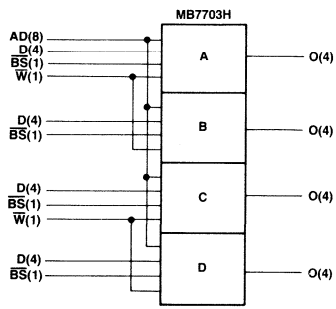
AC Characteristics

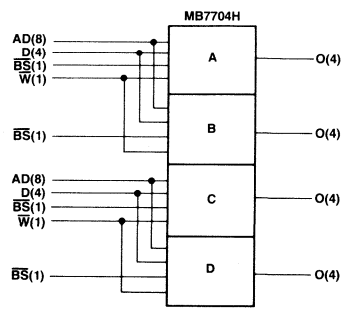
Parameter	Symbol	Min	Typ	Max	Unit
Block select access time	t_{AB}	0.5		3.0	ns
Block select recovery time	t_{RB}	0.5		3.0	ns
Address access time	t_{AA}	1.5		5.0	ns
Write pulse width	t_{WW}	3.5			ns
Address set up time	t_{SA}	1.5			ns
Block select set up time	t_{SB}	1.5			ns
Data set up time	t_{SD}	0.5			ns
Address hold time	t_{HA}	1.5			ns
Block select hold time	t_{HB}	1.5			ns
Data hold time	t_{HD}	2.5			ns
Write disable time	t_{WS}			4.0	ns
Write recovery time	t_{WR}			4.0	ns
Input capacitance	C_{IN}			6.5	pF
Output capacitance	C_{OUT}			8.0	pF

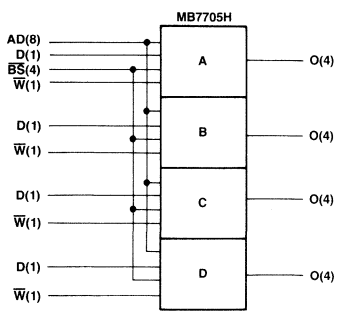
Internal Plane Connection Diagrams

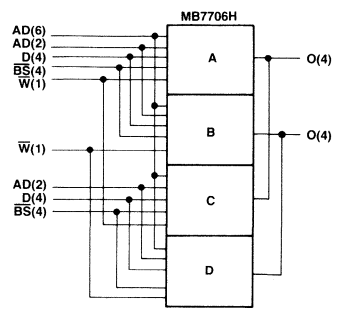








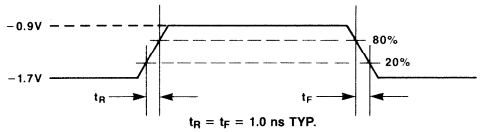




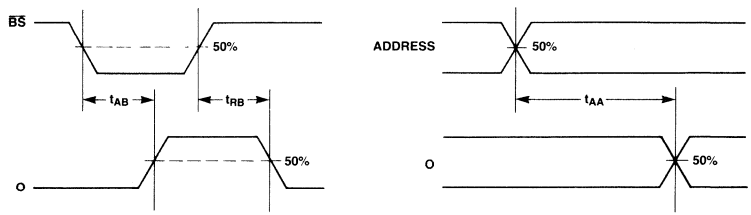
NOTES: *1 VALUES IN ( ) SHOW THE NUMBER OF EXTERNAL PINS HAVING THE SAME PIN NAME.
*2 "A", "B", "C" AND "D" IN THE BOXES SHOW FOUR MEMORY PLANES IN A CHIP.

Timing Diagrams

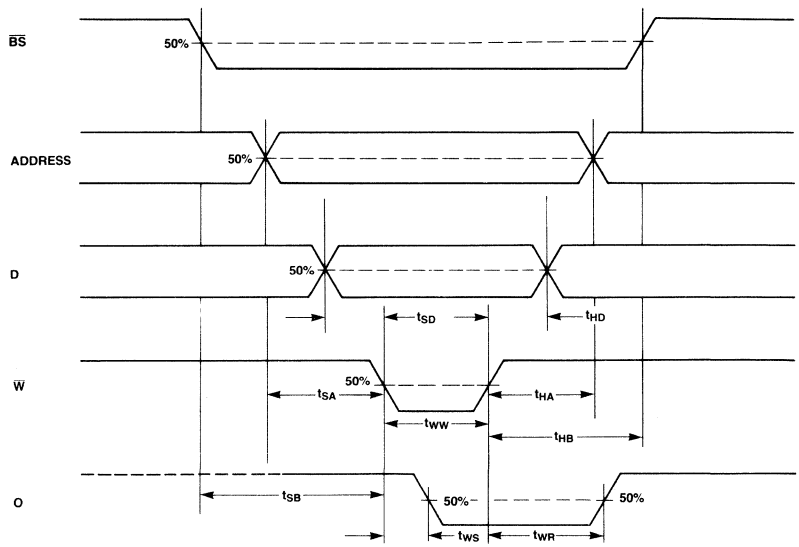
Input Conditions



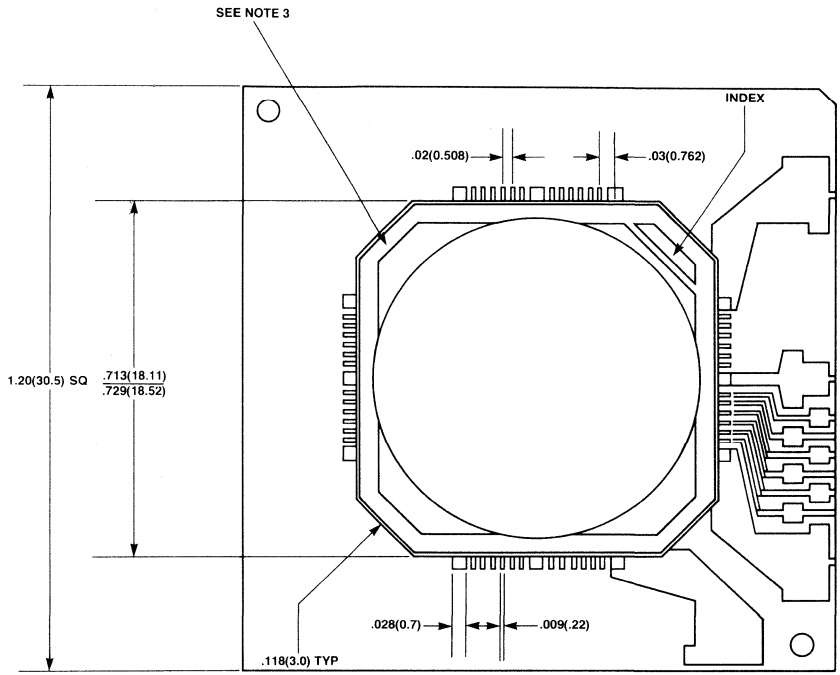
Read Cycle Timing Diagram

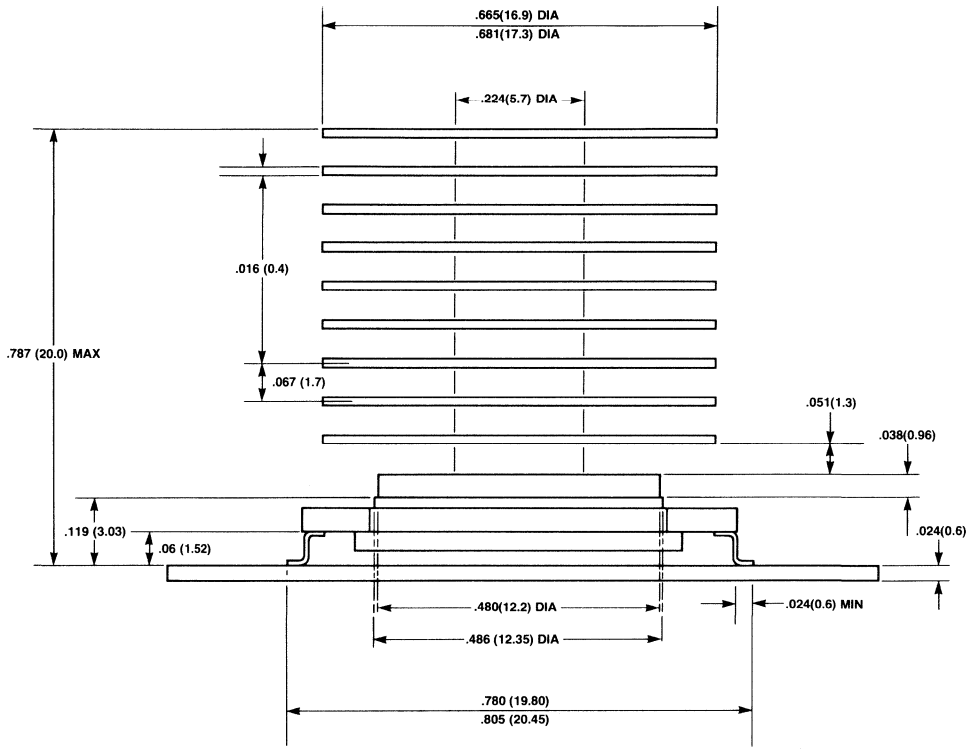


Write Cycle Timing Diagram



Package Dimensions





NOTES: *1 DIMENSIONS IN INCHES AND (MILLIMETERS)
*2 COOLING FIN CENTER IS WITHIN .02(0.5)
*3 BOTTOM PATTERN OF CERAMIC BASE IS CONNECTED TO V_{CC}

FUJITSU
MICROELECTRONICS, INC.

MBM93419

TTL 576-BIT BIPOLAR RANDOM ACCESS MEMORY

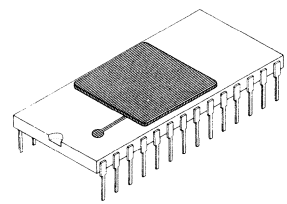
DESCRIPTION

The Fujitsu MBM93419 is a high speed TTL read/write random-access memory, organized as 64 words by 9 bits, with open-collector outputs.

MBM93419 is packaged in a 28-pin dual-in-line package, and is plug-in replaceable with F93419. It is ideally suited for scratchpad, small buffer and other applications where the number of required words is small and the number of required bits per word is relatively large. The ninth bit can provide parity for 8-bit word systems.

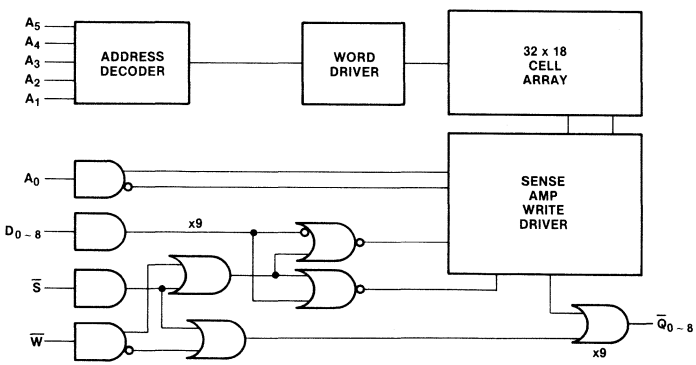
FEATURES

- **Organization: 64 words x 9-bits**
- **+5V Single Power Supply**
- **TTL Inputs and Outputs**
- **Open Collector Outputs**
- **Address Access Time: 45 ns Max.**
- **Chip Select Access Time: 40 ns Max.**
- **Power Dissipation: 1.3mW/bit Typ.**
- **Compatible with F93419**

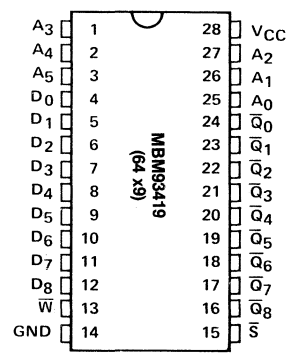


CERAMIC PACKAGE
DIP-28C-A01

MBM93419 BLOCK DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

INPUT			OUTPUT	MODE
$\overline{S}$	$\overline{W}$	D		
H	X	X	H	DISABLED
L	L	H	H	WRITE "H"
L	L	L	H	WRITE "L"
L	H	X	$\overline{D_{OUT}}$	READ

H = HIGH VOLTAGE LEVEL
L = LOW VOLTAGE LEVEL
X = DON'T CARE
*DATA OUTPUT IS THE COMPLEMENT OF DATA INPUT

Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric field. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than the maximum rated voltages to this device.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage (DC)	V_{IN}	−0.5 to +5.5	V
Input Current (DC)	I_{IN}	−12.0 to +5.0	mA
Output Voltage (V_{OUT} = "H")	V_{OUT}	−0.5 to +5.5	V
Output Current (DC, V_{OUT} = "L")	I_{OUT}	+20.0	mA
Storage Temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

GUARANTEED OPERATING RANGES

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature
Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	0°C to +75°C
Input High Voltage	V_{IH}	2.1	—	—	V	
Input Low Voltage	V_{IL}	—	—	0.8	V	

CAPACITANCE

(T_A = 25°C, V_{CC} = 5.0V, V_{IN} = 2.0V, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Pin Capacitance	C_{IN}	—	—	5.0	pF
Output Pin Capacitance	C_{OUT}	—	—	8.0	pF

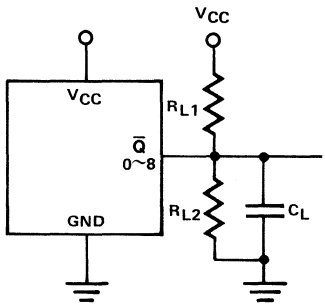
DC CHARACTERISTICS

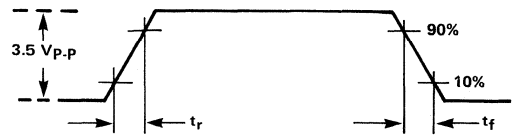
(V_{CC} = 5V ±5%, T_A = 0°C to 75°C, Air Flow ≥ 2.5m/sec, After Warm-up ≥ 2 min.)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Low Voltage	V_{OL}	V_{CC} = Min, I_{OL} = 12mA	—	0.4	0.5	V
Input High Voltage	V_{IH}	—	—	1.6	—	V
Input Low Voltage	V_{IL}	—	—	1.5	—	V
Input Low Current	I_{IL}	V_{CC} = Max, V_{IN} = 0.4V	—	−250	−400	μA
Input High Current	I_{IH1}	V_{CC} = Max, V_{IN} = 4.5V	—	1.0	40	μA
Input High Current	I_{IH2}	V_{CC} = Max, V_{IN} = 5.25V	—	—	1.0	mA
Output Leakage Current	I_{CEX}	V_{CC} = Max, V_{OUT} = 4.5V	—	1.0	100	μA
Input Clamp Diode Voltage	V_{CD}	V_{CC} = Max, V_{OUT} = 4.5V	—	−1.0	−1.5	V
Power Supply Current	I_{CC}	V_{CC} = Max, T_A = 25°C All Input GND	—	160	200	mA

AC CHARACTERISTICS

(V_{CC} = 5V ± 5%, T_A = 0°C to 75°C, Air Flow ≥ 2.5 m/sec, After Warm-up ≥ 2 min.)



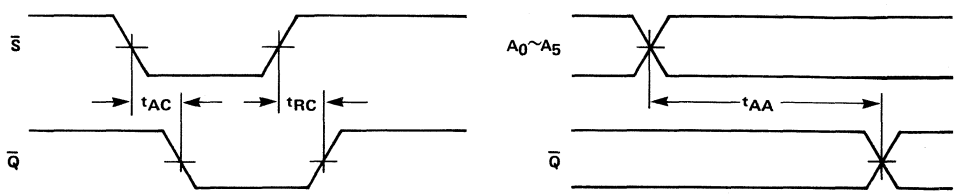


Input Pulse Voltage: 3.5V_{P-P}
Input Pulse Rise and Fall Time: 10ns
Output Load: R_{L1} = 450Ω
R_{L2} = 750Ω
C_L = 30pF (Including Jig)
Timing Measurement Levels: Input = 1.5V
Output = 1.5V

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	—	26	45	ns
Chip Select Access Time	t_{AC}	—	18	40	ns
Chip Select Recovery Time	t_{RC}	—	18	40	ns

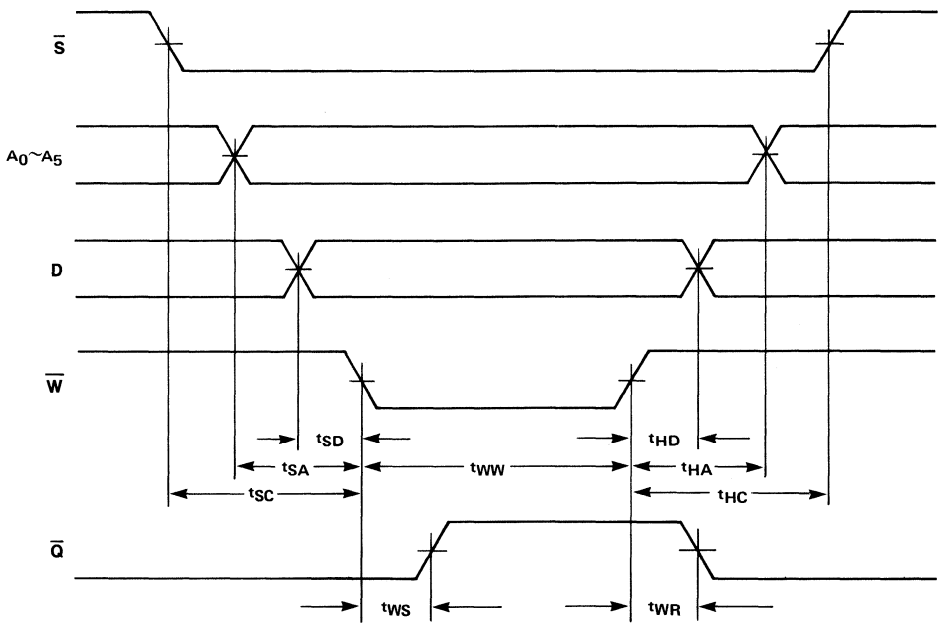
READ CYCLE



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	35	7	—	ns
Write Recovery Time	t_{WR}	—	20	45	ns
Write Delayed Time	t_{WS}	—	20	40	ns
Address Setup Time	t_{SA}	5	0	—	ns
Chip Select Setup Time	t_{SC}	5	0	—	ns
Data Setup Time	t_{SD}	5	0	—	ns
Address Hold Time	t_{HA}	5	0	—	ns
Chip Select Hold Time	t_{HC}	5	0	—	ns
Data Hold Time	t_{HD}	5	0	—	ns

WRITE CYCLE



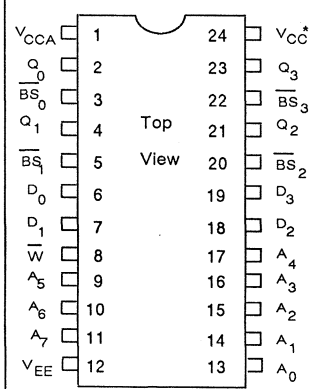
Advanced Information

Bipolar Memory

■ MBM10422A-5
1K Bit ECL RAM

Target Specifications

- **Organization:**
  256 x 4
- **Access Time:**
  5ns (Max)
- **Power Dissipation:**
  1040mW (200mA)
- **Package:**
  24 Pin DIP/FPT
  24 Pad LCC
- **Availability:**
  Samples - 1st Qtr. 1986
  Production - 2nd Qtr. 1986



* V_{CC} grounded

Note:

DIP and Flat Package styles conform to the same pin assignment.

Circuit diagrams utilizing Fujitsu products are included as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described herein any license under the patent rights of Fujitsu Limited or others. Fujitsu Limited reserves the right to change device specifications.

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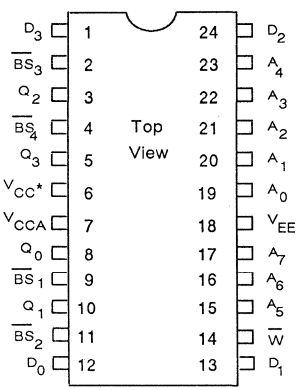
Advanced Information

Bipolar Memory

MBM100422A-5
1K Bit ECL RAM

Target Specifications

- **Organization:**
  256 x 4
- **Access Time:**
  5ns (Max)
- **Power Dissipation:**
  900mW (200mA)
- **Package:**
  24 Pin DIP/FPT
  24 Pad LCC
- **Availability:**
  Samples – 1st Qtr. 1986
  Production – 2nd Qtr. 1986



* V_{CC} grounded

Note:

DIP and Flat Package styles conform to the same pin assignment.

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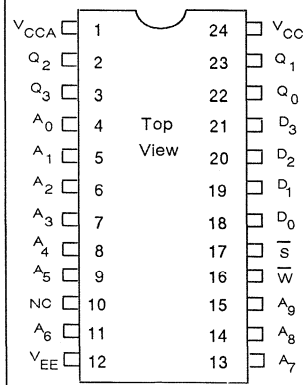
Advanced Information

Bipolar Memory

MBM10474A-5
4K Bit ECL RAM

Target Specifications

- **Organization:**
  1024 x 4
- **Access Time:**
  5ns (Max)
- **Power Dissipation:**
  1560mW (300mA)
- **Package:**
  24 Pin DIP/FPT
  24 Pad LCC
- **Availability:**
  Samples - 1st Qtr. 1986
  Production - 3rd Qtr. 1986



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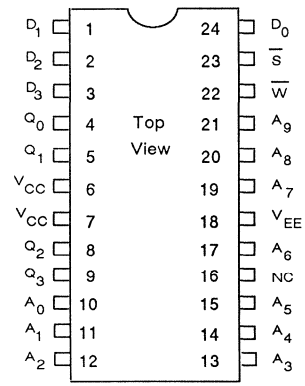
Advanced Information

Bipolar Memory

MBM100474A-5
4K Bit ECL RAM

Target Specifications

- **Organization:**
  1024 x 4
- **Access Time:**
  5ns (Max)
- **Power Dissipation:**
  1350mW (300mA)
- **Package:**
  24 Pin DIP/FPT
  24 Pad LCC
- **Availability:**
  Samples - 2nd Qtr. 1986
  Production - 3rd Qtr. 1986



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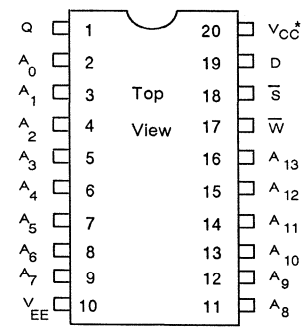
Advanced Information

Bipolar Memory

MBM10480A-10
16K Bit ECL RAM

Target Specifications

- **Organization:**
  16,384 x 1
- **Access Time:**
  10ns (Max)
- **Power Dissipation:**
  1150 mW (220 mA)
- **Package:**
  20 Pin DIP/FPT
  20 Pad LCC
- **Availability:**
  Samples - 3rd Qtr. 1986
  Production - 4th Qtr. 1986



* V_{CC} grounded

Note:

DIP and Flat Package styles conform to the same pin assignment.

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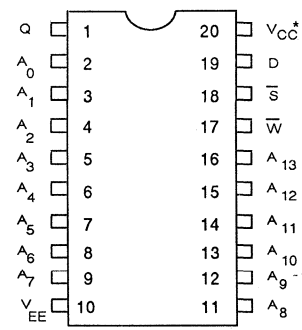
Advanced Information

Bipolar Memory

MBM100480A-10
16K Bit ECL RAM

Target Specifications

- **Organization:**
  16,384 x 1
- **Access Time:**
  10ns (Max)
- **Power Dissipation:**
  1000mW (220mA)
- **Package:**
  20 Pin DIP/FPT
  20 Pad LCC
- **Availability:**
  Samples - 3rd Qtr. 1986
  Production - 4th Qtr. 1986



* V_{CC} grounded

Note:

DIP and Flat Package styles conform to the same pin assignment.

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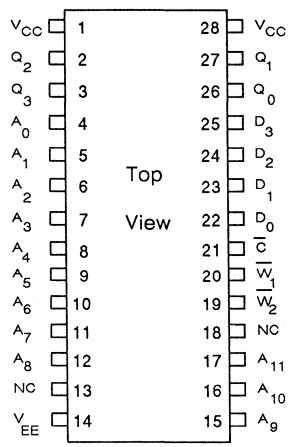
Advanced Information

Bipolar Memory

MBM10484A–10, MBM100484A–10
16K Bit ECL RAM

Target Specifications

- **Organization:**
  4096 x 4
- **Access Time:**
  10ns (Max)
- **Power Dissipation:**
  < 1500mW
- **Package:**
  28 Pin DIP/FPT
  28 Pad LCC
- **Availability:**
  Samples – 4th Qtr. 1986
  Production – 1st Qtr. 1987



Note:

DIP and Flat Package styles conform to the same pin assignment.

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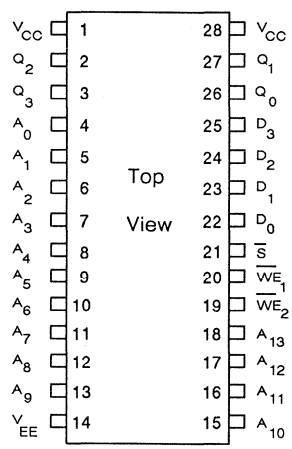
Advanced Information

Bipolar Memory

MBM10494-15, MBM100494-15
64K Bit ECL RAM

Target Specifications

- **Organization:**
  16,384 x 4
- **Access Time:**
  15ns (Max)
- **Power Dissipation:**
  < 1500mW
- **Package:**
  28 Pin DIP/FPT
  28 Pad LCC
- **Availability:**
  Samples - 1st Qtr. 1987
  Production - 3rd Qtr. 1987



Note:

DIP and Flat Package styles conform to the same pin assignment.

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Fujitsu Part No.	Organization	Output	Package Pins	Signetics	AMD	MMI	National	TI	Harris	Fairchild	Hitachi	Motorola	Raytheon	Intel
MB7111	32 x 8	0C	16	N82S23	AM27S18	6330	DM54/74S188	TBP18SA30	HM7602					
MB7112	32 x 8	3S	16	N82S123	AM27S19	6331	DM54/74S288	TBP18S030	HM7603			MCM27S19		
MB7113	256 x 4	0C	16	N82S126	AM27S20	6300	DM54/74S387	TBP24SA10	HM7610					
MB7114	256 x 4	3S	16	N82S129	AM27S21	6301	DM54/74S287	TBP24S10	HM7611					
MB7115	512 x 4	0C	16	N82S130	AM27S12	6305	DM54/74S570		HM7620					
MB7116	512 x 4	3S	16	N82S131	AM27S13	6306	DM54/74S571		HM7621			MCM7621		
MB7117	256 x 8	0C	20			53/6308		TBP28LA22						
MB7118	256 x 8	3S	20			53/6309	DM54/74S471	TBP28L22						
MB7121	1024 x 4	0C	18		AM27S32	53/6352	DM54/74S572	TBP24SA41	HM7642	93452	HN25044			
MB7122	1024 x 4	3S	18	N/S82S137	AM27S33	53/63S441	DM54/74S573	TBP24S41	HM7643	93453	HN25045	MCM7643		
MB7123	512 x 8	0C	20		AM27S28	53/6348	DM54/74S473	TBP28SA42						
MB7124	512 x 8	3S	20	N/S82S147	AM27S29	53/6349	DM54/74S472	TBP28S42	HM7649				29623	
MB7127	2048 x 4	0C	18	N/S82S184	AM27S184	53/6388	DM77/87S184	TBP24SA81						
MB7128	2048 x 4	3S	18	N/S82S185	AM27S185	53/6389	DM77/87S185	TBP24S81	HM7685			MCM7685	29651	
MB7131	1024 x 8	0C	24	N/S82S180	AM27S180	53/6380	DM77/87S180	TBP28SA86		93450	HN25088			
MB7132	1024 x 8	TS	24	N/S82S181	AM27S181	53/6381	DM77/87S281	TBP28S86	HM7681	93451	HN25089	MCM7681	29631	3628
MB7133	4096 x 4	0C	20		AM27540									
MB7134	4096 x 4	3S	20	N/S82HS195	AM27541	53/63S1641	DM77/87S195		HM76165			MCM76165		
MB7137	2048 x 8	0C	24		AM27S190		DM77/87S190	TBP28SA166A		937510	HN25168			
MB7138	2048 x 8	3S	24	N/S82S191	AM27S191	63S1681	DM77/87S191	TBP28S166A	HM76161	932511	HN25169	MCM76161	29681	3636
MB7141	4096 x 8	0C	24											
MB7142	4096 x 8	3S	24	N/S82S321	AM27S43	63S3281	DM77/87S321		HM76321				29671	3632
MB7143	8192 x 8	0C	24							93564				
MB7144	8192 x 8	3S	24	82HS641	AM27S49				HM76641	93565				
MB7151	4096 x 4	0C	20		AM27S40									
MB7152	4096 x 4	3S	20	N/S82S195	AM27S41	53/63S1641	DM77/87S195		HM76165			MCM76161		
MB7226RA	512 x 8	3S	24		AM27S25	53/63RA481	DM87SR25							
MB7232RA	1024 x 8	3S	24		AM27S35	53/63RA881	DM87SR181					MCM27S35		

Commercial Temperature Range (0°C to +75°C)

Device	Organization	Output	Access Time (max)	Power Supply Volts	Power Supply Current (Icc)	Package
MB7111E	32 x 8	0C	35nS	+5V	100mA	16-pin
MB7111H	32 x 8	0C	25nS	+5V	100mA	16-pin
MB7112E	32 x 8	TS	35nS	+5V	100mA	16-pin
MB7112H	32 x 8	TS	25nS	+5V	100mA	16-pin
MB7113E	256 x 4	0C	40nS	+5V	100mA	16-pin
MB7113H	256 x 4	0C	30nS	+5V	100mA	16-pin
MB7114E	256 x 4	TS	40nS	+5V	100mA	16-pin
MB7114H	256 x 4	TS	30nS	+5V	100mA	16-pin
MB7115E	512 x 4	0C	45nS	+5V	120mA	16-pin
MB7115H	512 x 4	0C	35nS	+5V	120mA	16-pin
MB7116E	512 x 4	TS	45nS	+5V	120mA	16-pin
MB7116H	512 x 4	TS	35nS	+5V	120mA	16-pin
MB7117E	256 x 8	0C	45nS	+5V	140mA	20-pin
MB7117H	256 x 8	0C	35nS	+5V	140mA	20-pin
MB7118E	256 x 8	TS	45nS	+5V	140mA	20-pin
MB7118H	256 x 8	TS	35nS	+5V	140mA	20-pin
MB7121E	1K x 4	0C	45nS	+5V	150mA	18-pin
MB7121H	1K x 4	0C	35nS	+5V	150mA	18-pin
MB7122E	1K x 4	TS	45nS	+5V	150mA	18-pin
MB7122H	1K x 4	TS	35nS	+5V	150mA	18-pin
MB7123E	512 x 8	0C	45nS	+5V	170mA	20-pin
MB7123H	512 x 8	0C	35nS	+5V	170mA	20-pin
MB7124E	512 x 8	TS	45nS	+5V	170mA	20-pin
MB7124H	512 x 8	TS	35nS	+5V	170mA	20-pin
MB7127E	2K x 4	0C	55nS	+5V	155mA	18-pin
MB7127H	2K x 4	0C	45nS	+5V	155mA	18-pin
MB7128E	2K x 4	TS	55nS	+5V	155mA	18-pin
MB7128H	2K x 4	TS	45nS	+5V	155mA	18-pin
MB7128Y	2K x 4	TS	35nS	+5V	155mA	18-pin
MB7131E	1K x 8	0C	55nS	+5V	175mA	24-pin
MB7131H	1K x 8	0C	45nS	+5V	175mA	24-pin
MB7132E	1K x 8	TS	55nS	+5V	175mA	24-pin
MB7132H	1K x 8	TS	45nS	+5V	175mA	24-pin
MB7132Y	1K x 8	TS	35nS	+5V	175mA	24-pin
MB7133E	4K x 4	0C	55nS	+5V	170mA	20-pin
MB7133H	4K x 4	0C	45nS	+5V	170mA	20-pin
MB7134E	4K x 4	TS	55nS	+5V	170mA	20-pin
MB7134H	4K x 4	TS	45nS	+5V	170mA	20-pin
MB7134Y	4K x 4	TS	35nS	+5V	170mA	20-pin
MB7137E	2K x 8	0C	55nS	+5V	180mA	24-pin
MB7137H	2K x 8	0C	45nS	+5V	180mA	24-pin
MB7138E	2K x 8	TS	55nS	+5V	180mA	24-pin
MB7138H	2K x 8	TS	45nS	+5V	180mA	24-pin
MB7138Y	2K x 8	TS	35nS	+5V	180mA	24-pin
MB7141E	4K x 8	0C	65nS	+5V	185mA	24-pin
MB7141H	4K x 8	0C	55nS	+5V	185mA	24-pin
MB7142E	4K x 8	TS	65nS	+5V	185mA	24-pin
MB7142H	4K x 8	TS	55nS	+5V	185mA	24-pin
MB7143E	8K x 8	0C	65nS	+5V	190mA	24-pin
MB7143H	8K x 8	0C	55nS	+5V	190mA	24-pin
MB7144E	8K x 8	TS	65nS	+5V	190mA	24-pin
MB7144H	8K x 8	TS	55nS	+5V	190mA	24-pin
MB7151E	4K x 4	0C	55nS	+5V	170mA	20-pin
MB7151H	4K x 4	0C	45nS	+5V	170mA	20-pin
MB7152E	4K x 4	TS	55nS	+5V	170mA	20-pin
MB7152H	4K x 4	TS	45nS	+5V	170mA	20-pin
MB7152Y	4K x 4	TS	35nS	+5V	170mA	20-pin
MB7226RA/RS-20	512 x 8	TS	20nS	+5V	170mA	24-pin
MB7226RA/RS-25	512 x 8	TS	25nS	+5V	170mA	24-pin
MB7232RA/RS-20	1K x 8	TS	20nS	+5V	185mA	24-pin
MB7232RA/RS-25	1K x 8	TS	25nS	+5V	185mA	24-pin

Extended Temperature Range (−55°C to +125°C)

Device	Organization	Output	Access Time (max)	Power Supply Volts	Power Supply Current (Icc)	Package
MB7128E-W	2K x 4	TS	55nS	+5V	155mA	18-pin
MB7132E-W	1K x 8	TS	55nS	+5V	175mA	24-pin
MB7138E-W	2K x 8	TS	55nS	+5V	180mA	24-pin
MB7142E-W	4K x 8	TS	65nS	+5V	185mA	24-pin
MB7144E-W	8K x 8	TS	70nS	+5V	190mA	24-pin

Fujitsu also offers a family of DEAP PROMs available in extended temperature range (−55°C to +125°C). These PROMs are of the same generic family as the commercial temperature range product and utilize the same programming methods and more elaborate testing procedures. This product is available processed to Mil. Std. 883B or 883C.

Fujitsu PROM Technology

The Fujitsu MB7100 and MB7200 series Schottky PROMs are fabricated using Schottky TTL, passive isolation technology known as Isolation by Oxide and Poly-silicon (IOP). The isolation is achieved by a thin-epitaxial and Shallow V-Grooving (SVG), Diffused Eutectic Aluminum Process (DEAP™) technology with fine emitter. It uses a pulse programming method which achieves high-speed operation, high-speed programming, high programmability and high reliability.

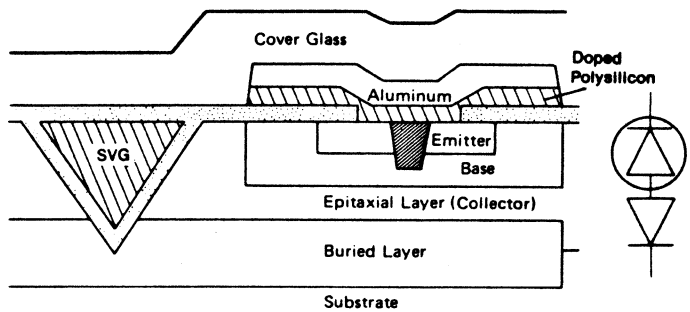
The memory cell is originally structured with an open-base NPN transistor and then programmed by shorting the base-emitter junction, i.e. shorted junction type cell which is achieved by eutectically melting aluminum and silicon adjacent to the P-N junction of the cell diode with relatively low temperatures.

Fast programming time of typically 150 μs/bit is achieved with a fine emitter cell which requires less programming energy. The result is negligible thermal stress. This high reliability feature eliminates aluminum migration in the programmed cell. Further, Fujitsu's advanced technology allows very high programmability.

Special Factory Testing

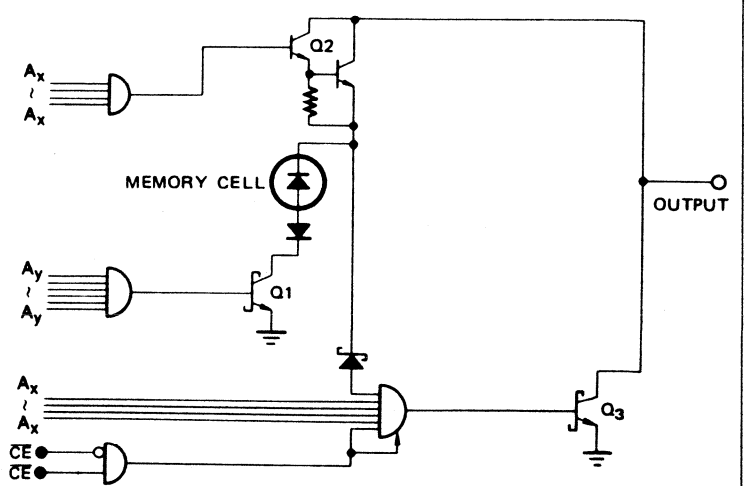
Extra rows and extra columns of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

Programmed Cell (Cross Section)



Programmed by Diffused Eutectic Aluminum Process

Internal Programming Circuit



Fujitsu PROM Technology

The Fujitsu MB7100 series Schottky PROM is fabricated using Schottky TTL passive isolation technology known as Isolation by Oxide and Poly-silicon (IOP), which is achieved by thin-epitaxial and Shallow V-Grooving (SVG), Diffused Eutectic Aluminum Process (DEAP) technology with fine emitter and pulse programming method which achieve high-speed operation, high-speed programming, high programmability and high reliability.

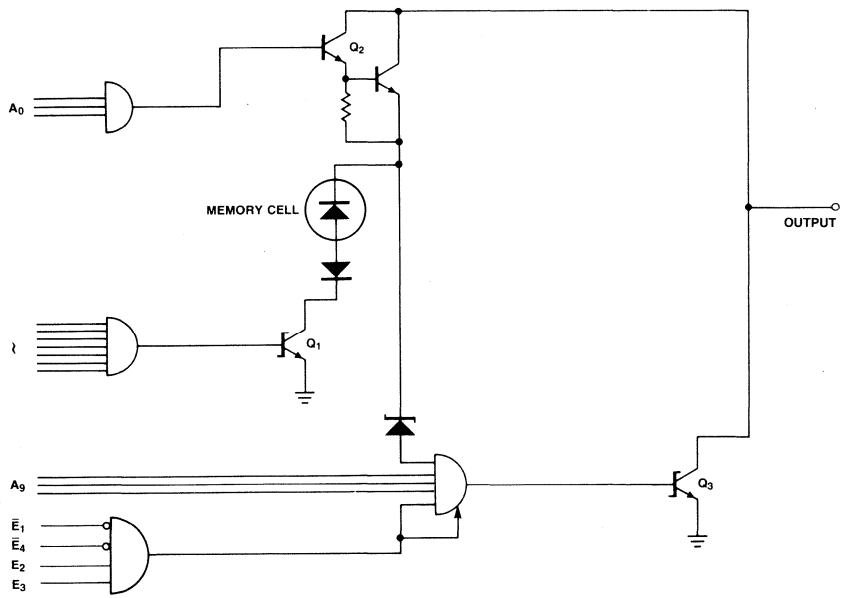
Special Factory Testing

Extra rows and extra columns of test cells, plus additional circuitry built into the PROM chip, allow improved factory testing of DC, AC and programming characteristics. These test cells and test circuitry provide enhanced correlation between programmed and unprogrammed circuits in order to guarantee high programmability and reliability.

One memory cell is originally structured with a base-open NPN transistor and then programmed by shorting the base-emitter junction, i.e. shorted junction type cell which is achieved by eutectically melting aluminum and silicon adjacent to the P-N junction of cell diode with relatively low temperature, i.e., DEAP technology.

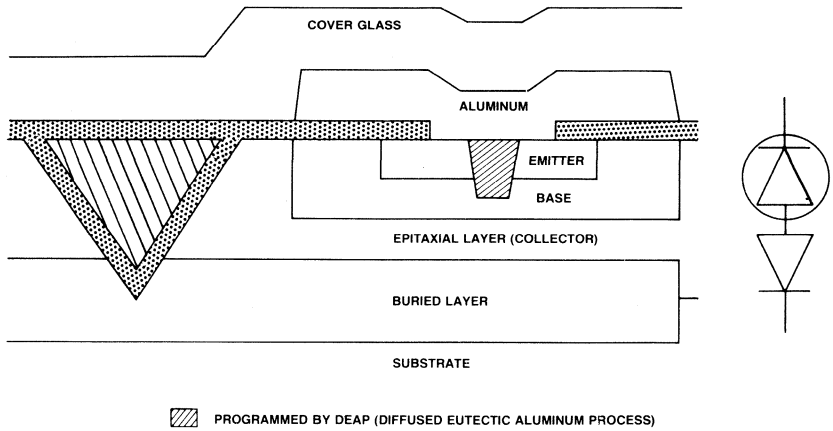
Fast programming time of typically 150 μs/bit is achieved with a fine emitter cell which requires less programming energy; the result is negligible thermal stress. This high reliability feature virtually eliminates aluminum migration in the programmed cell. Further, Fujitsu advanced technology allows very high programmability.

Internal Programming Circuit



Programming Information
(Continued)

Programmed Cell (Cross Section)



Programming

The device is manufactured with outputs low (positive logic "zero") in all storage cells. To make an output high at a particular cell, a junction must be changed from a blocking state to a conducting state. This procedure is called programming.

A logic "one" can be permanently programmed into a selected bit location. The desired bit for programming is selected using ten address inputs to turn on transistors Q1 and Q2. By applying the PV_{CE} pulse voltage, the chip is disabled and transistor Q3 is held off. Then, a train of programming pulses applied to the desired output flows through the junction into transister Q1. This programming current changes the junction to the conducting state. The pulse train is stopped as soon as the output voltage indicates that the selected bit is in the logic one state.

To assure that the element is programmed properly, two additional programming pulses are applied immediately after an output voltage indicates conduction in the programmed bit.

One output must be programmed at a time since the internal decoding circuit is capable of sinking only one unit of programming current at a time.

Verification

After the device has been programmed, the correct program pattern can be verified when all chip enables are taken enable. To guarantee full supply voltage and full temperature range operation, a programmed device should source 2.4 mA at V_{OH} = 2.4V and V_{CC} = 7V at 25°C ambient temperature.

Reliability

Fujitsu utilizes an extensive testing procedure to ensure device performance prior to shipment. However, 100% programmability is not guaranteed, and it is imperative that this specification be rigorously adhered to in order to achieve a satisfactory programming yield. Fujitsu will not accept responsibility for any device found defective if it was not programmed according to this specification. Devices returned to Fujitsu as defective must be accompanied by a complete truth table with clearly indicated locations of supposedly defective memory cells.

Programming Procedure

1. Apply power: V_{CC} = PV_{CC}, GND = 0V.
2. Select the desired bit.
3. Read the output to confirm the voltage V_O = low. (In the case of V_O = high, select the next desired bit.)
4. Apply a 20V pulse voltage to the PV_{CE} input.
5. Apply a programming pulse with amplitude of 125 mA and duration of t_{PW} (11 μs) after a delay of t_{SP} (4 μs).
6. Read the output V_O after a delay of t_{PR} (10 μs).
   a) In the case of V_O = low, repeat steps "4", "5" and "6" with cycle time of t_{CYC} (50 μs).
   b) In the case of V_O = high, apply 2 additional programming pulses to provide a highly reliable memory cell.
7. Select the next desired bit after a delay of t_{HA} (2 μs).

Notes: *1 Programming must be done bit by bit.
*2 Ambient temperature during programming must be room temperature. (25°C ± 2°C)

Programming Information
(Continued)

DC Specifications
(T_A = 25°C)

Parameter	Symbol		Min	Typ	Max	Unit
Input low voltage	V_{IL}		0		0.8	V
Input high voltage	V_{IH}		2.0		5.25	V
Power supply voltage	PV_{CC}	P:	6.7	7.0	7.3	V
		R:	4.75	5.0	5.25	
Programming pulse current	I_{PRG}		120		130	mA
PV_{CE} pulse voltage	PV_{CE}		20	20	22	V
Programming pulse clamp voltage	V_{PRG}		20	20	22	V
PV_{CE} pulse clamp current	PI_{CE}		230		260	mA
Reference voltage for a prog. "1"	V_{REF}		1.0	1.5	2.0	V

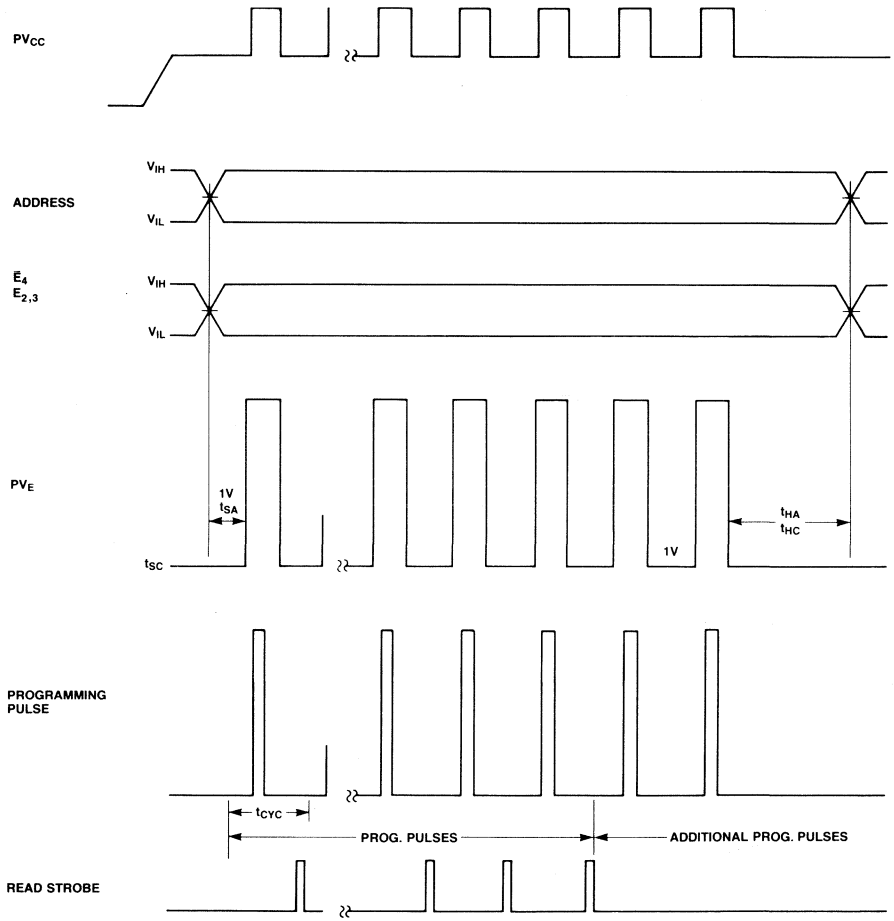
AC Specifications
(T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Programming pulse cycle time	t_{CYC}	40	50	60	μs
Programming pulse width*1	t_{PW}	10	11	12	μs
Programming pulse rise time*2	t_r			2	μs
PV_{CE} pulse rise time*2	t_r			2	μs
PV_{CC} pulse rise time*3	t_r			2	μs
Programming pulse fall time*4	t_f			2	μs
PV_{CE} pulse fall time*4	t_f			2	μs
PV_{CC} pulse fall time*5	t_f			2	μs
Address input set-up time	t_{SA}	2			μs
Chip enable input set-up time	t_{SC}	2			μs
PV_{CE} set-up time*6	t_{SP}	4			μs
Address input hold time	t_{HA}	2			μs
Chip enable input hold time	t_{HC}	2			μs
PV_{CE} hold time*7	t_{HP}	2			μs
PV_{CE} pulse trailing edge to read strobe time*8	t_{PR}	10			μs
Programming pulse number				100	Times
Programming time/bit		120	150	6120	μs/bit
Additional programming pulse number		2	2	2	Times

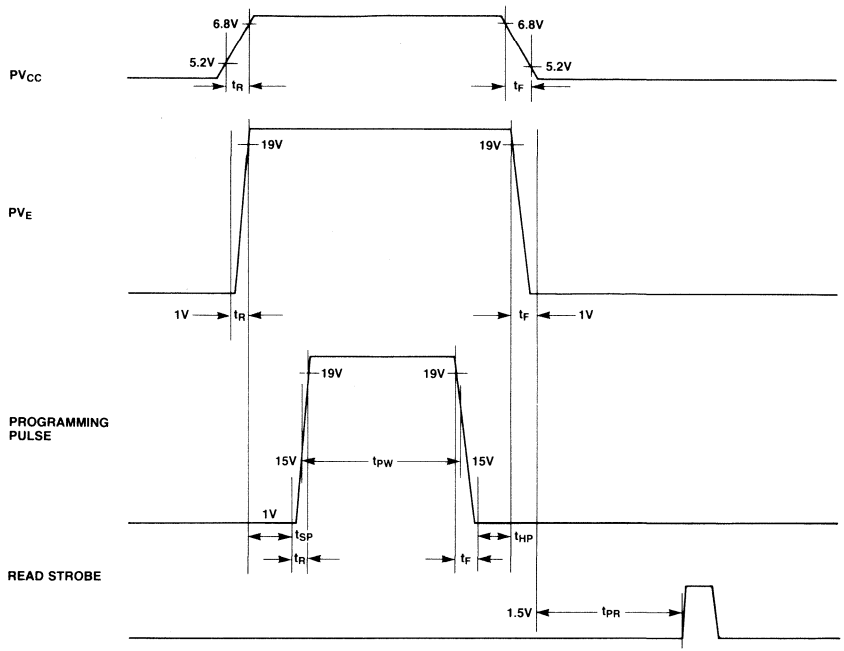
Notes: *1 Stipulated 200Ω load and 15V.
*2 From 1V to 19V (200Ω load).
*3 From 5.2V to 6.8V (30Ω load).
*4 From 19V to 1V (200Ω load).
*5 From 6.8V to 5.2V (30Ω load).
*6 From PV_E pulse 19V to programming pulse 1V.
*7 From programming pulse 1V to PV_E pulse 19V.
*8 From PV_E pulse 1V to read strobe.

Programming Information
(Continued)

Typical Waveforms

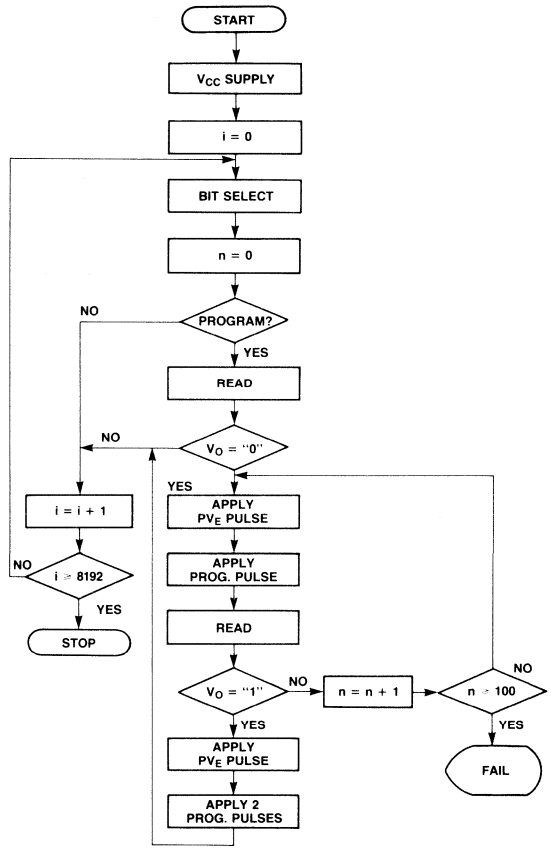


One Detailed Programming Cycle



Programming Information
(Continued)

Programming Flow Chart



Fujitsu Approved PROM Programmers

The Fujitsu MB7100 and MB7200 series PROM family is being supported by several commercial PROM Programmer manufacturers. Fujitsu, in order to guarantee not only programmability but long term reliability, has an active program to qualify all PROM programmer manufacturer's products before they are approved.

In order to support customers, Fujitsu Microelectronics will pre-program parts for qualification. Contact your local Fujitsu representative for details.

Programmer Manufacturer	Fujitsu Part Number	Programming Module	LCC Support Status	Socket Adapter
Data I/O System 19/29	7100 Series	950-0059-001	LCC Support TBA	None (Unipak II)
Data I/O System 22	7100 Series 7200 Series	Factory Configurable	LCC Support TBA	Configuration Dependant
Advantest T310/TR4928	7100 Series	PZ3871/3871A	LCC Support TBA	— Not Used
Minato Electronics 1850/70	7100 Series	5SP-71XX (XX = PROM type)	No Current LCC Support	— Included in Module
Toyo/Aval PKW7000	7100 Series	UN-721F	No Current LCC Support	Included in Module
Kontron MPP-80S/ EPP-80S	MB7121/22 MB7123/24 MB7127/28 MB7131/32 MB7133/34 MB7137/38 MB7141/42	MOD-23 MOD-23 MOD-23 MOD-23 MOD-23 MOD-23 MOD-23	No Current LCC Support	24-2 24-6 4-4 4-5 20 22 22-11
Stag Microsystems PPZ	MB7121/22 MB7123/24 MB7127/28 MB7131/32 MB7133/34 MB7137/38 MB7141/42 MB7143/44	ZM2000	No Current LCC Support	Included in Module

Note: Contact Manufacturer for LCC info

The DEAP™ Technique

Introduction

A PROM device is composed of a programmable memory cell array and peripheral circuitry for input, output and programming. Fujitsu's memory cell consists of an emitter-base junction as the programmable element and a collector-base junction as the switching element. Programming is based on a technique referred to as DEAP™ DEAP™ is an acronym for Diffused Eutectic Aluminum Process. Briefly described, the Fujitsu designed DEAP™ programming technique utilizes an aluminum and a polysillicon layer sitting on top of an emitter-base diode. During programming a reverse current is applied to the emitter sufficient to raise the temperature of the junction. When the temperature increases to a certain point, an aluminum-silicon eutectic is formed from the aluminum and polysilicon layers on top of the emitter-base junction. This eutectic when formed, is diffused from the surface of the emitter down through the emitter-base juction thus shorting the junction out. Once the eutectic has shorted out the juction, power dissipation at the juction decreases rapidly, also causing the temperature to decrease rapidly. This phenomenon results in no further diffusion of the aluminum-silicon eutectic, therfore the collector-base junction has been protected from any damage. After the cell has cooled down, two additional programming pulses are applied to the cell to provide a highly reliable and uniform resistive short.

What Makes DEAP™ Better?

Bipolar PROMs of today utilize two basic programming technologies. The first and most widely used is the fusible link. Several types of fuse materials are used to achieve this method of programming. The most common types of fuse materials are nichrome, titanaium-tungsten and polysilicon. A second technology of programming bipolar PROMs and a more advantageous one is the Fujitsu DEAP™ technique. A brief description of each technology is necessary to explain why DEAP™ is better.

The fusible link technology can be referred to as a "surface" technology. The fusible link normally sits on the surface of the silicon and occupies a considerable amount of silicon real estate. To make a small die and highly dense device with a fusible link technology requires a major effort in device masking during manufacturing. When programming a fusible link, a section of the fuse is blown open just like a common electrical fuse. A closer look will show that the fuse material has been melted at the gap and splattered about. This fuse splattering causes fragments of fuse material to be scattered on the surface. This is not a ''clean" operation. On some PROMs, the passivation layer could be ruptured and expose the die to possible contamination. On other PROMs, an opening is designed above the fuse gap in the passivation layer so the fuse is deliberately exposed. These openings or windows are potential reliability factors in that moisture, salts or stray fuse material fragments can reach the die through these openings.

Generally after blowing a fusible link, the gap that has been created is very narrow. Because of the short width of the gap a very high electric field can exist across the gap. Due to this electric field, atoms can migrate across the gap and eventually partially reconnect the fuse of memory cells where programming has taken place. This action is referred to as "growback". Generally this problem becomes apparent under accelerated life testing or after many hours of operation.

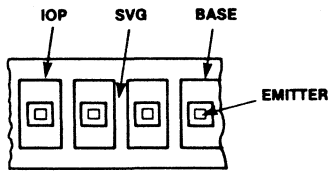
The Fujitsu DEAP™ programming technique is not a "surface" technology but a "subsurface" technology. The programmable element is vertical and not horizontal like fusible link. There are several advantages to this type of approach. The memory cell can be designed to be much smaller with the same manufacturing tolerances resulting in smaller die sizes and faster access times. Since DEAP™ is a "subsurface" technology, there is no need for openings in the passivation layer as with fuses and the passivation cannot be ruptured. This way there will be no chance for contaminates to be exposed to the die. The DEAP™ technique exhibits no splatter fuse material whatsoever. The DEAP™ programming technique has no "growback" mechanism like fusible link because the shorting mechanism is self limiting and extremely reliable.

How About Reliability?

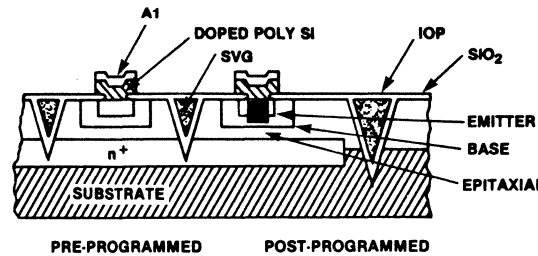
Later in this booklet, you'll see specific data on reliability. However, the DEAP™ technology with its fully passivated die and subsurface eutectic process means high reliability as well as fast access time and small die size.

DEAP™ Cell Structure

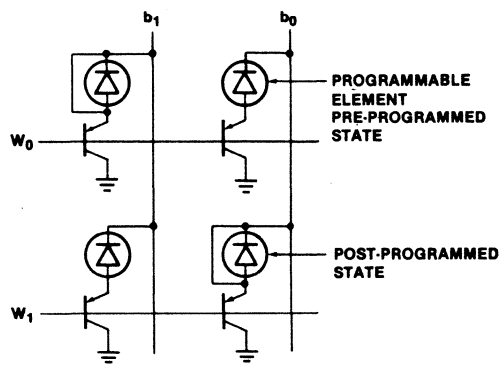
Top view



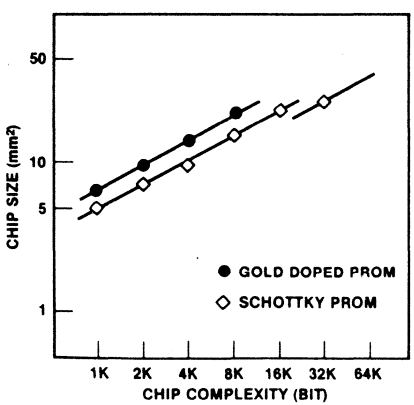
Cross Section

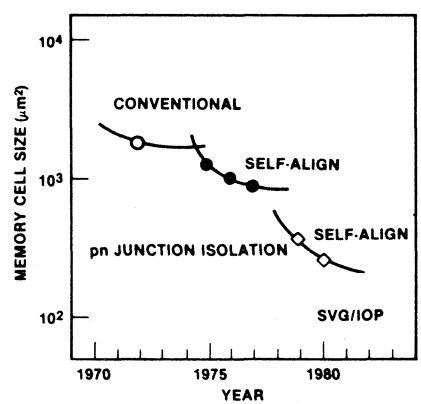


Electrical Equivalent



PROM Cell Technologies





FUJITSU

MB7111E/H, MB7112E/H
Programmable Schottky 256-Bit Read Only Memory

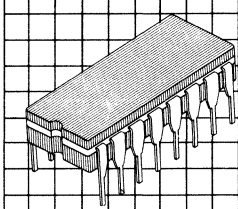
Description

The Fujitsu MB7111 and MB7112 are high speed Schottky TTL electrically field programmable read only memories organized as 32 words by 8-bits. With uncommitted collector outputs provided on the MB7111 and three-state outputs on the MB7112, memory expansion is simple.

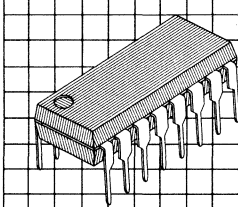
The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP (Diffused Eutectic Aluminum Process) according to simple programming procedures.

The sophisticated passive isolation termed SVG (Shallow V-Groove) with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.



Ceramic Package
DIP-16C-C02



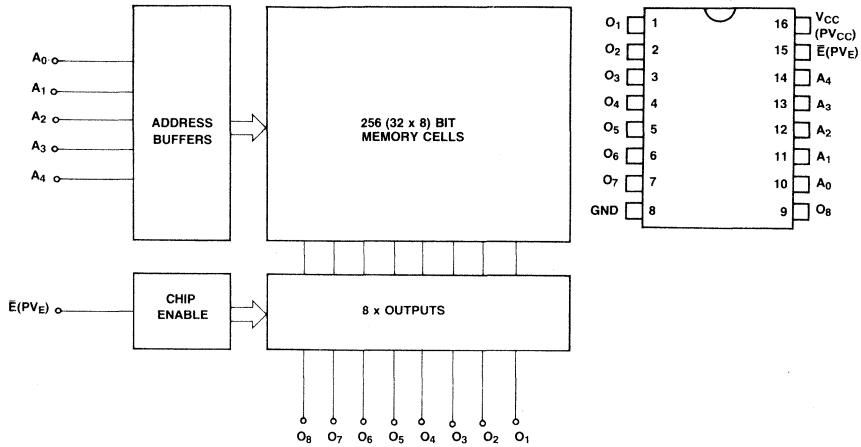
Plastic Package
DIP-16P-M02

Features

- **Single +5V supply voltage**
- **32 words x 8-bits organization, fully decoded**
- **Proven high programmability and reliability**
- **Programming by DEAP (Diffused Eutectic Aluminum Process)**
- **Simplified and lower power programming**
- **Low current PNP inputs**
- **AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques**
- **Fast access time, 15 ns typ.**
  H: 25 ns max.
  E: 35 ns max.
- **TTL compatible inputs and outputs**
- **Open collector outputs (MB7111)**
- **3-state outputs (MB7112)**
- **One chip enable lead for simplified memory expansion**
- **Standard 16-pin DIP package**
- **JEDEC approved pin out**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB7111/7112 Block Diagram and Pin Assignment



Absolute Maximum Ratings

(See Note)

Parameter		Symbol	Rating	Unit
Power supply voltage		V_{CC}	−0.5 to +7.0	V
Power supply voltage (during programming)		V_{CC}	−0.5 to +7.5	V
Input voltage		V_{IN}	−1.5 to +5.5	V
Input voltage (during programming)		V_{IPRG}	22.5	V
Output voltage (during programming)		V_{OPRG}	−0.5 to +22.5	V
Input current		I_{IN}	−20	mA
Input current (during progrmaming)		I_{IPRG}	+270	mA
Output current		I_{OUT}	+100	mA
Output current (during programming)		I_{OPRG}	+150	mA
Storage temperature	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−40 to +125	
Output voltage		V_{OUT}	−0.5 to V_{CC}	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Guaranteed Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Input low voltage	V_{IL}	0		0.8	V
Input high voltage	V_{IH}	2.0		5.5	V
Ambient temperature	T_A	0		75	°C

Capacitance

(f = 1 MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			10	pF
Output capacitance	C_O			12	pF

DC Characteristics

(Full guaranteed operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Input leakage current (V_{IH} = 5.5V)		I_R			40	μA
Input low current (V_{IL} = 0.45V)		I_F			−250	μA
Output low voltage (I_{OL} = 10 mA)		V_{OL}			0.45	V
Output low voltage (I_{OL} = 16 mA)		V_{OL}			0.50	V
Output leakage current (V_O = 2.4V, chip disabled)	MB7111	I_{OLK}			40	μA
Output leakage current (V_O = 2.4V, chip disabled)	MB7112	I_{OIH}			40	μA
Output leakage current (V_O = 0.45V, chip disabled)	MB7112	I_{OIL}			−40	μA
Input clamp voltage (I_{IN} = −18 mA)		V_{IC}			−1.2	V
Power supply current (V_{IN} = GND)		I_{CC}		70	100	mA
Output high voltage (I_O = −2.4 mA)	MB7112	V_{OH}*1	2.4			V
Output short circuit current (V_O = GND)	MB7112	I_{OS}*1	−15		−60	mA

Note: *1 Denotes guaranteed characteristics of the output high-level (ONE) state when the chip is enabled ($V_{\overline{E}}$ = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

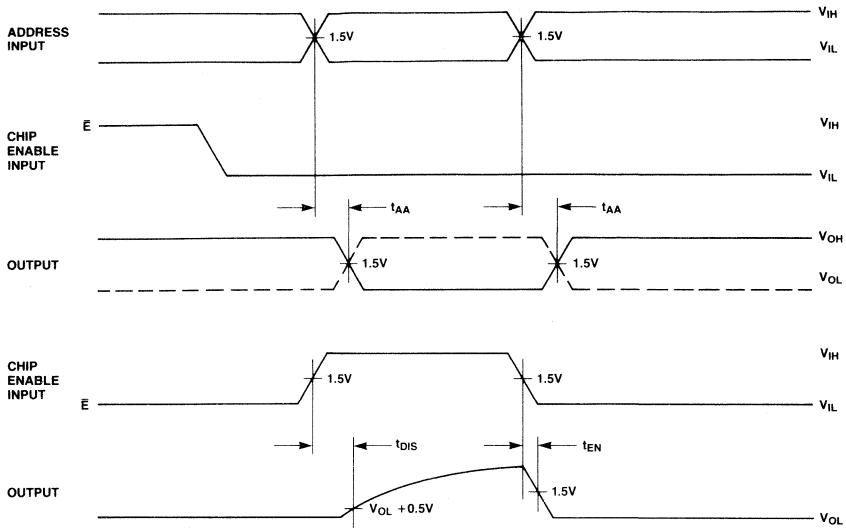
AC Characteristics

(Full guaranteed operating conditions unless otherwise noted.)

		MB7111/MB7112E		MB7111/MB7112H		
Parameter	Symbol	Typ	Max	Typ	Max	Unit
Access time (via address input)	t_{AA}	15	35	15	25	ns
Output disable time	t_{DIS}		25*1		20*1	ns
Output enable time	t_{EN}		20		20	ns

Note: *1 Using Wired-OR outputs, this value is equivalent to the output enable time (t_{EN}) of the device.

Operation Timing Diagram

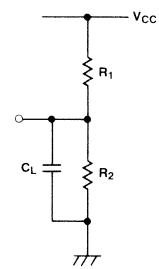


NOTE: OUTPUT DISABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO REACH A HIGH IMPEDANCE STATE WHEN CHIP ENABLE GOES HIGH. OUTPUT ENABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO BECOME ACTIVE WHEN CHIP ENABLE GOES LOW. THE HIGH IMPEDANCE STATE IS DEFINED AS A POINT ON THE OUTPUT WAVEFORM, THAT IS 0.5V FROM THE ACTIVE OUTPUT LEVEL.

AC Test Conditions

Input Conditions

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5 ns from 1V to 2V
Frequency ..... 1 MHz



TRUTH TABLE

	MB7133/MB7134		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30 pF
t_{DIS}	300Ω	600Ω	30 pF
t_{EN}	300Ω	600Ω	30 pF

Input/Output Circuit Information

Input

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of the input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

Open-Collector Output

Open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30 mA for the MB7112 (3-state) compared to 0 mA for the MB7111 (open-collector).

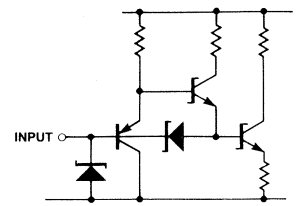
Three-State Output

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

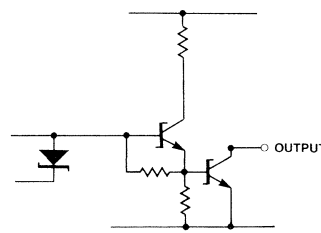
If two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously, with short circuit current from one enabled device flowing through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should ensure that this condition does not exist.

In the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the output circuit decreases the load on the Chip Enable circuit.

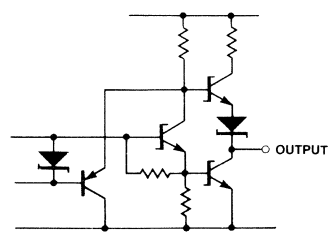
MB7111/7112 Input



MB7111 Output

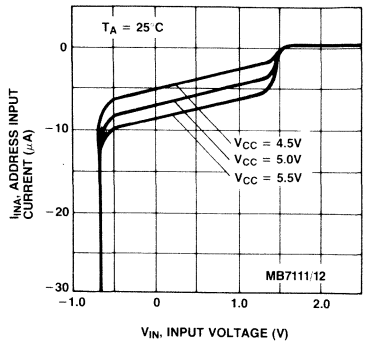


MB7112 Output

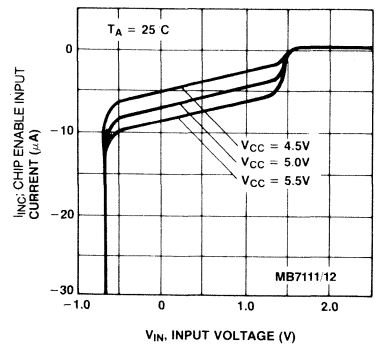


Typical Characteristics Curves

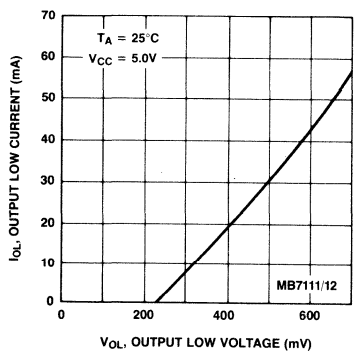
I_{INA} Input Current vs. V_{IN} Input Voltage



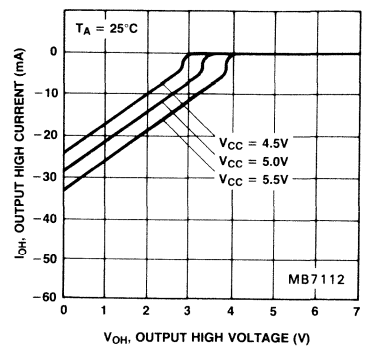
I_{INC} Input Current vs. V_{IN} Input Voltage



I_{OL} Output Low Current vs. V_{OL} Output Low Voltage

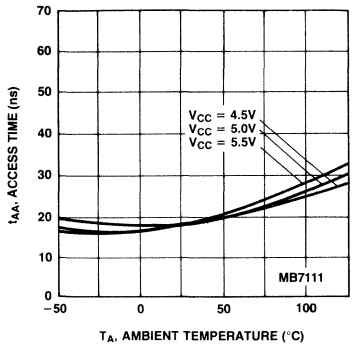


I_{OH} Output High Current vs. V_{OH} Output High Voltage

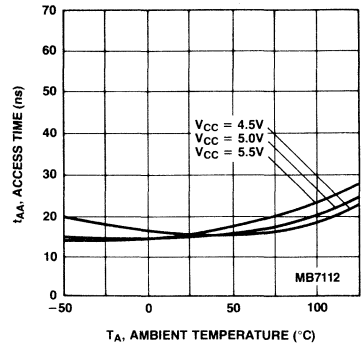


Typical Characteristics Curves
(Continued)

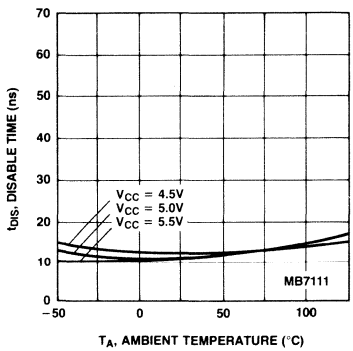
t_{AA} Access Time vs. Ambient Temperature



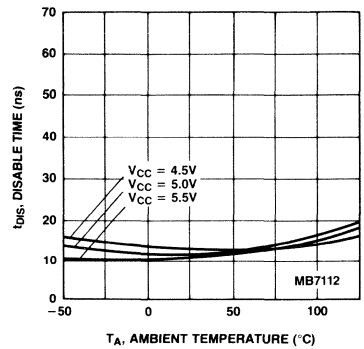
t_{AA} Access Time vs. Ambient Temperature



t_{DIS} Disable Time vs. Ambient Temperature

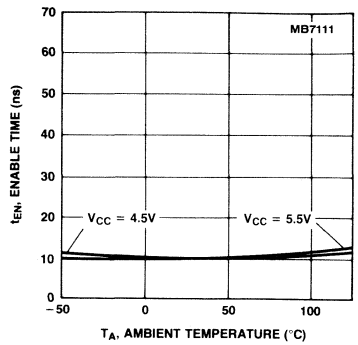


t_{DIS} Disable Time vs. Ambient Temperature

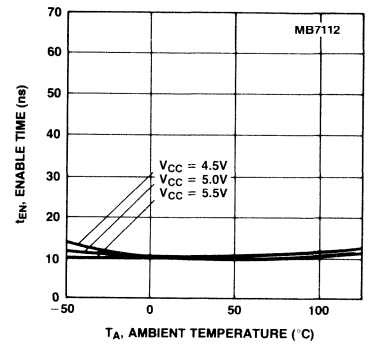


Typical Characteristics Curves
(Continued)

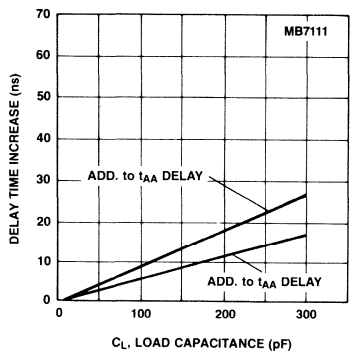
t_{EN} Enable Time vs. Ambient Temperature



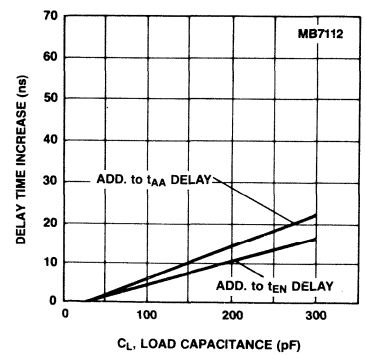
t_{EN} Enable Time vs. Ambient Temperature



Delay Time Increase vs. C_L Load Capacitance



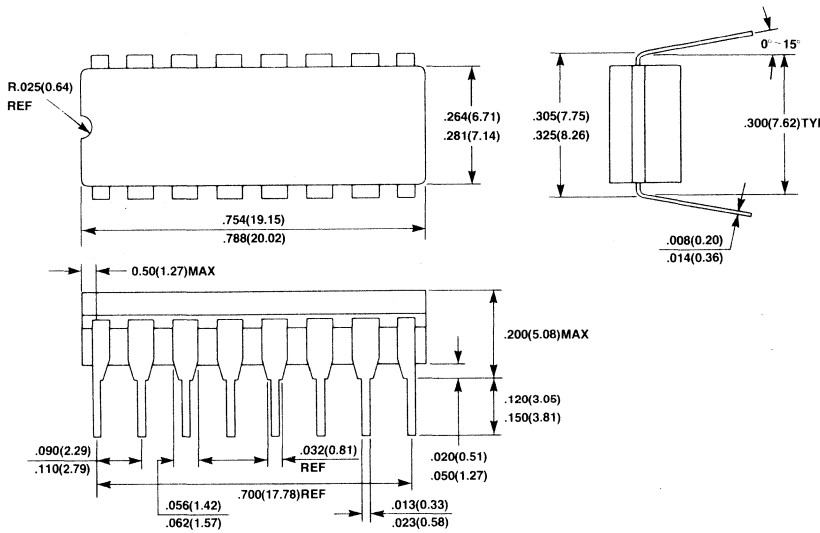
Delay Time Increase vs. C_L Load Capacitance



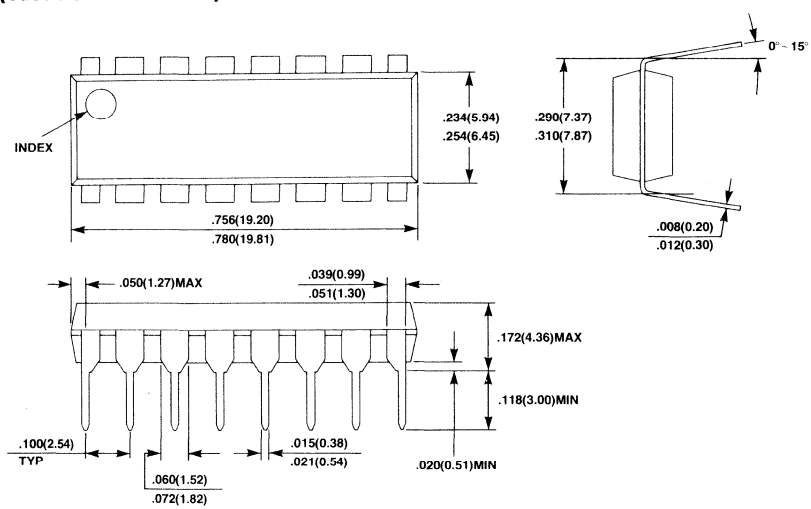
Package Dimensions

Dimensions in inches
(millimeters)

16-Lead Ceramic (CERDIP) Dual In-Line Package (Case No.: DIP-16C-C02)



16-Lead Plastic Dual In-Line Package (Case No.: DIP-16P-M02)



Advanced Information

Availability Q2 '86

Bipolar PROM

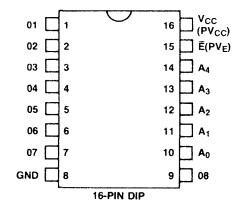
FUJITSU

■ MB7111L/7112L

Low Power 256-Bit
Schottky TTL PROM

Features

- **Organization:**
  32 × 8-bits
- **Process:**
  Schottky TTL
- **Program:**
  Diffused Eutectic Aluminum Process (DEAP)
- **Output:**
  Open Collector (MB7111)
  Three-State (MB7112)
- **Power Supply:**
  +5V ±5%
- **Power Dissipation:**
  200 mW max.
- **Address Access Time:**
  55 ns max.
- **Package:**
  16-pin DIP



16-PIN DIP

FUJITSU

MB7113E/H, MB7114E/H
Programmable Schottky 1,024-Bit Read Only Memory

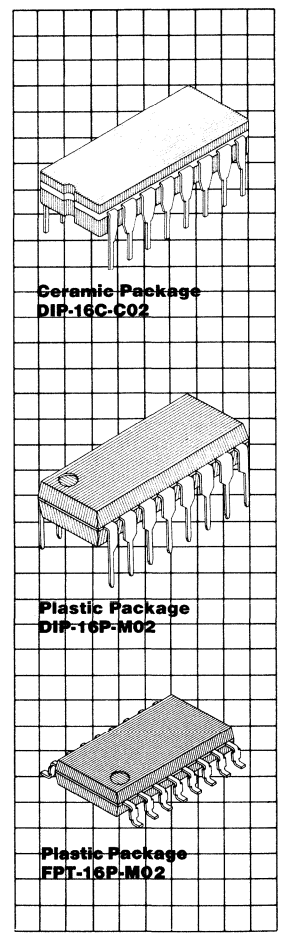
Description

The Fujitsu MB7113 and MB7114 are high speed Schottky TTL electrically field programmable read only memories organized as 256 words by 4-bits. With uncommitted collector outputs provided on the MB7113 and three-state outputs on the MB7114, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP (Diffused Eutectic Aluminum Process) according to simple programming procedures.

The sophisticated passive isolation termed SVG (Shallow V-Groove) with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

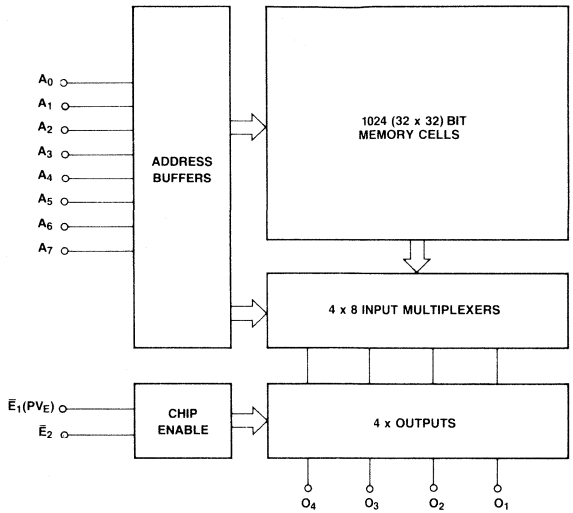


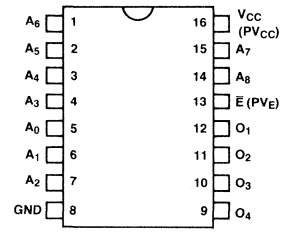
Features

- **Single +5V supply voltage**
- **256 words x 4-bits organization, fully decoded**
- **Proven high programmability and reliability**
- **Programming by DEAP (Diffused Eutectic Aluminum Process)**
- **Simplified low power programming**
- **Low current PNP inputs**
- **AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques**
- **Fast access time, 20 ns typ.**
  H: 30 ns max.
  E: 40 ns max.
- **TTL compatible inputs and outputs**
- **Open collector outputs (MB7113)**
- **3-state outputs (MB7114)**
- **Two chip enables lead for simplified memory expansion**
- **Standard 16-pin DIP package**
- **JEDEC approved pin out**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB7113/7114 Block Diagram and Pin Assignments





Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Power supply voltage		V_{CC}	−0.5 to +7.0	V
Power supply voltage (during programming)		V_{CC}	−0.5 to +7.5	V
Input voltage		V_{IN}	−1.5 to +5.5	V
Input voltage (during programming)		V_{IPRG}	22.5	V
Output voltage (during programming)		V_{OPRG}	−0.5 to +22.5	V
Input current		I_{IN}	−20	mA
Input current (during programming)		I_{IPRG}	+270	mA
Output current		I_{OUT}	+100	mA
Output current (during programming)		I_{OPRG}	+150	mA
Storage temperature	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−40 to +125	
Output voltage		V_{OUT}	−0.5 to V_{CC}	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Guaranteed Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Input low voltage	V_{IL}	0		0.8	V
Input high voltage	V_{IH}	2.0		5.5	V
Ambient temperature	T_A	0		75	°C

Capacitance
(f = 1 MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			10	pF
Output capacitance	C_O			12	pF

DC Characteristics
(Full guaranteed operating conditions unless otherwise noted.)

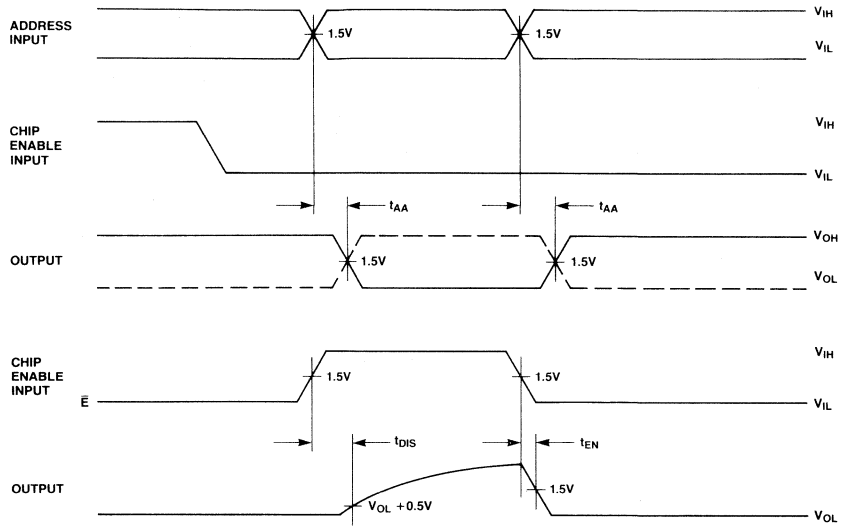
Parameter		Symbol	Min	Typ	Max	Unit
Input leakage current (V_{IH} = 5.5V)		I_R			40	μA
Input load current (V_{IL} = 0.45V)		I_F			−250	μA
Output low voltage (I_{OL} = 10 mA)		V_{OL}			0.45	V
Output low voltage (I_{OL} = 16 mA)		V_{OL}			0.50	V
Output leakage current (V_O = 2.4V, chip disabled)	MB7113	I_{OLK}			40	μA
Output leakage current (V_O = 2.4V, chip disabled)	MB7114	I_{OIH}			40	μA
Output leakage current (V_O = 0.5V, chip disabled)	MB7114	I_{OIL}			−40	μA
Input clamp voltage (I_{IN} = −18 mA)		V_{IC}			−1.2	V
Power supply current (V_{IN} = OPEN or GND)		I_{CC}		60*2	100	mA
Output high voltage (I_O = −2.4 mA)	MB7114	V_{OH}*1	2.4			V
Output short circuit current (V_O = GND)	MB7114	I_{OS}*1	−15		−60	mA

Notes: *1 Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{\overline{E}}$ = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.
*2 This value denotes conditions at T_A = 25°C and V_{CC} = +5.0V.

AC Characteristics
(Full guaranteed operating conditions unless otherwise noted.)

Parameter	Symbol	MB7113/MB7114E Typ	MB7113/MB7114E Max	MB7113/7114H Typ	MB7113/7114H Max	Unit
Access time (via address input)	t_{AA}	20	40	20	30	ns
Output disable time	t_{DIS}	15	25	15	25	ns
Output enable time	t_{EN}	15	25	15	25	ns

Operation Timing Diagram

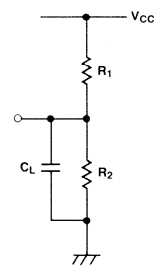


NOTE: OUTPUT DISABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO REACH A HIGH IMPEDANCE STATE WHEN SOME OF THE CHIP ENABLES ARE TAKEN HIGH (DISABLED). OUTPUT ENABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO BECOME ACTIVE WHEN THE CHIP ENABLES ARE TAKEN LOW (ENABLED). THE HIGH IMPEDANCE STATE IS DEFINED AS A POINT ON THE OUTPUT WAVEFORM EQUAL TO A ΔV OF 0.5V FROM THE ACTIVE OUTPUT LEVEL.

AC Test Conditions

Input Conditions

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5 ns from 1V to 2V
Frequency ..... 1 MHz



TRUTH TABLE

	MB7113/MB7114		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30 pF
t_{DIS}	300Ω	600Ω	30 pF
t_{EN}	300Ω	600Ω	30 pF

Input/Output Circuit Information

Input

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

Open-Collector Output

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30 mA for the MB7114 (3-state) compared to 0 mA for the MB7113 (open-collector).

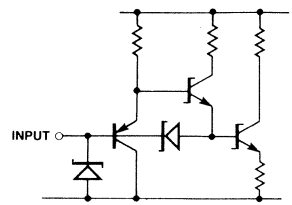
Three-State Output

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

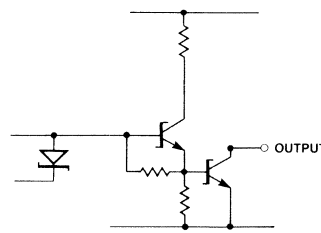
In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor provided in the output circuit is effective to decrease a load for the Chip Enable circuit.

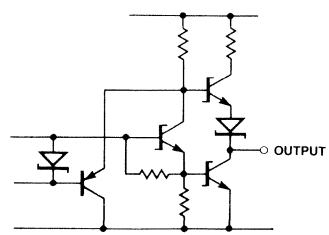
MB7113/MB7114 Input



MB7113 Output

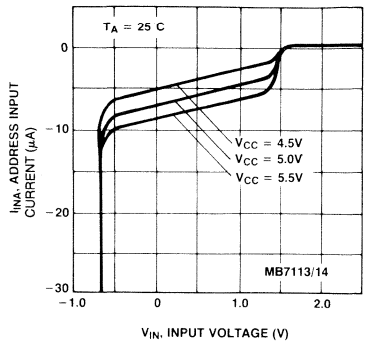


MB7114 Output

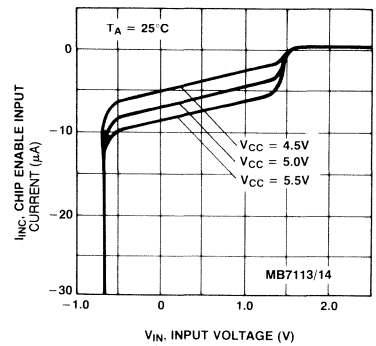


Typical Characteristics Curves

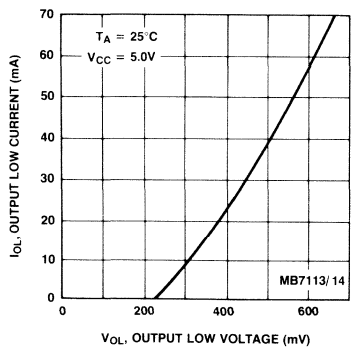
I_{INA} Input Current vs. V_{IN} Input Voltage



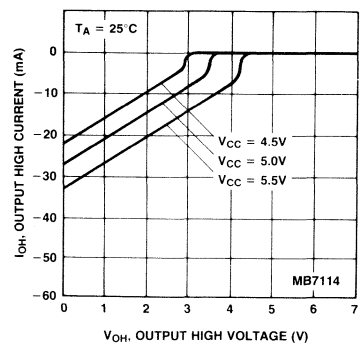
I_{INC} Input Current vs. V_{IN} Input Voltage



I_{OL} Output Low Current vs. V_{OL} Output Low Voltage

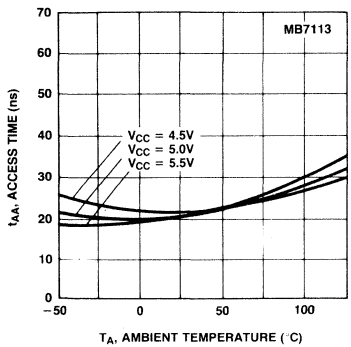


I_{OH} Output High Current vs. V_{OH} Output High Voltage

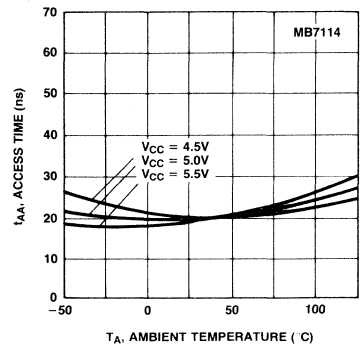


Typical Characteristics Curves
(Continued)

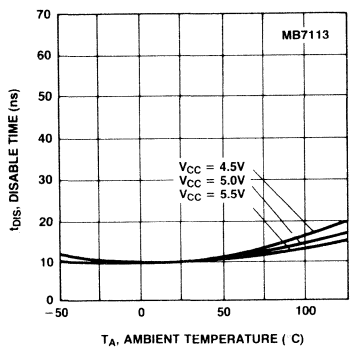
t_{AA} Access Time vs. Ambient Temperature



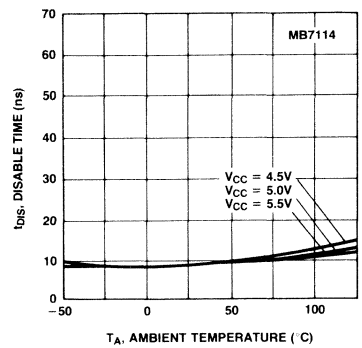
t_{AA} Access Time vs. Ambient Temperature



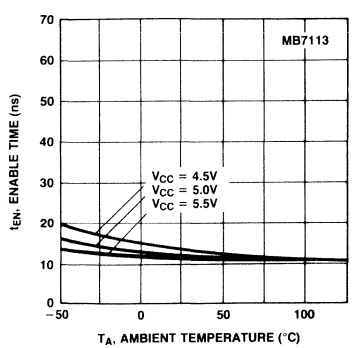
t_{DIS} Disable Time vs. Ambient Temperature



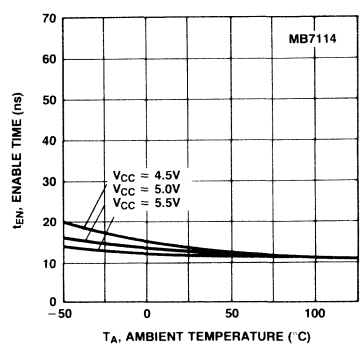
t_{DIS} Disable Time vs. Ambient Temperature



t_{EN} Enable Time vs. Ambient Temperature

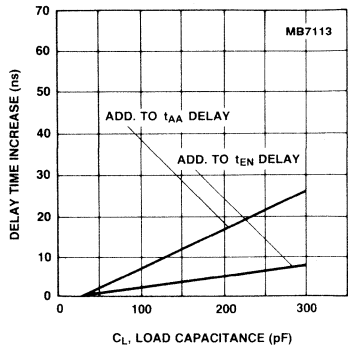


t_{EN} Enable Time vs. Ambient Temperature

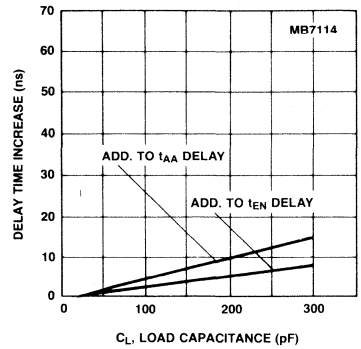


Typical Characteristics Curves
(Continued)

Delay Time Increase vs. C_L Load Capacitance

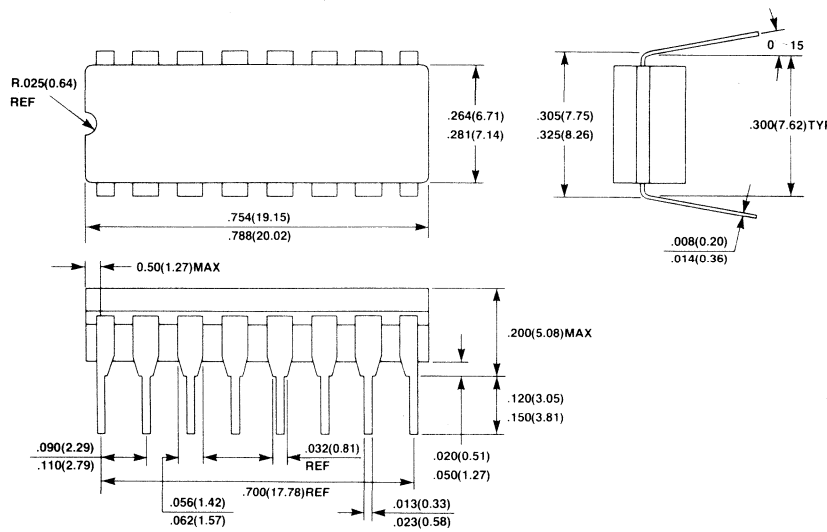


Delay Time Increse vs. C_L Load Capacitance



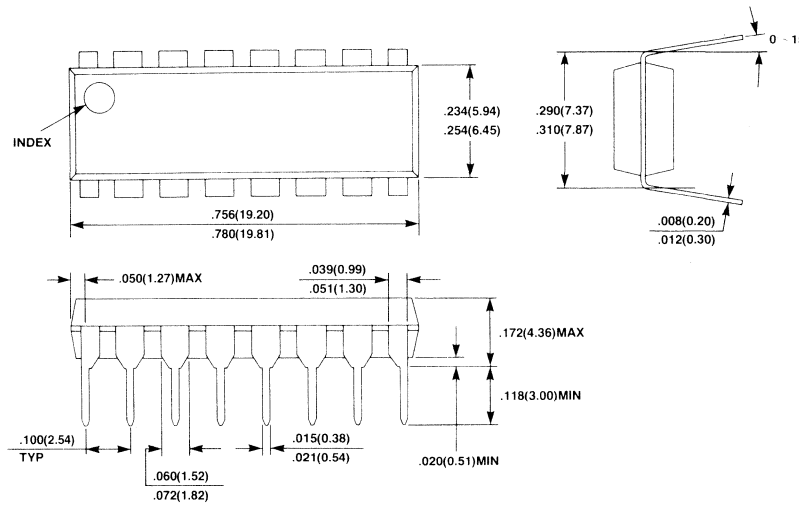
Package Dimensions
Dimensions in inches
(millimeter)

16-Lead Ceramic (CERDIP) Dual In-Line Package (Case No.: DIP-16C-C02)

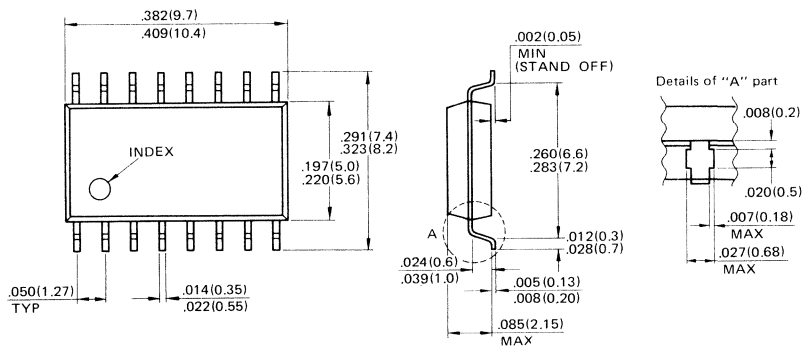


Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

16-Lead Plastic Dual In-Line Package
(Case No.: DIP-16P-M02)



16-Lead Plastic Flat Package
(Case No.: FPT-16P-M02)



Advanced Information

Availability Q2 '86

Bipolar PROM

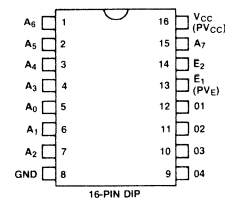
FUJITSU

■ MB7113L/7114L

Low Power 1024-Bit
Schottky TTL PROM

Features

- **Organization:**
  256 × 4-bits
- **Process:**
  Schottky TTL
- **Program:**
  Diffused Eutectic Aluminum Process (DEAP)
- **Output:**
  Open Collector (MB7113)
  Three-State (MB7114)
- **Power Supply:**
  +5V ±5%
- **Power Dissipation:**
  200 mW max.
- **Address Access Time:**
  55 ns max.
- **Package:**
  16-pin DIP



FUJITSU

MB7115E/H, MB7116E/H

Programmable Schottky 2,048-Bit Read Only Memory

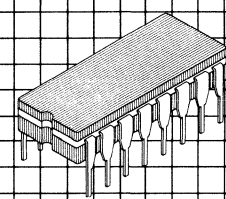
Description

The Fujitsu MB7115 and MB7116 are high speed Schottky TTL electrically field programmable read only memories organized as 512 words by 4-bits. With uncommitted collector outputs provided on the MB7115 and three-state outputs on the MB7116, memory expansion is simple.

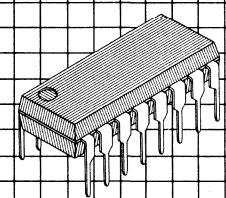
The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP (Diffused Eutectic Aluminum Process) according to simple programming procedures.

The sophisticated passive isolation termed SVG (Shallow V-Groove) with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.



Ceramic Package
DIP-16C-C02



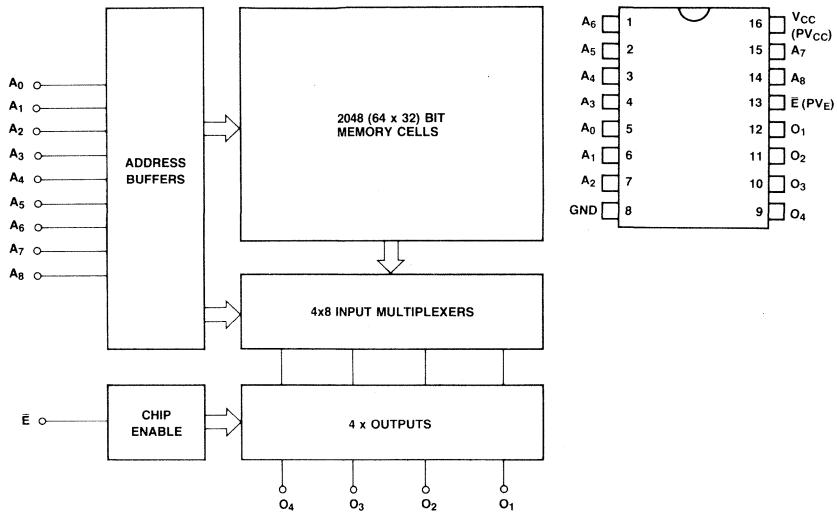
Plastic Package
DIP-16P-M02

Features

- **Single +5V supply voltage**
- **512 words x 4-bits organization, fully decoded**
- **Proven high programmability and reliability**
- **Programming by DEAP (Diffused Eutectic Aluminum Process)**
- **Simplified low power programming**
- **Low current PNP inputs**
- **AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques**
- **Fast access time, 20 ns typ.**
  H: 35 ns max.
  E: 45 ns max.
- **TTL compatible inputs and outputs**
- **Open collector outputs (MB7115)**
- **3-state outputs (MB7116)**
- **Chip enable lead for simplified memory expansion**
- **Standard 16-pin DIP package**
- **JEDEC approved pin out**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB7115/7116 Block Diagram and Pin Assignments



Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Power supply voltage		V_{CC}	−0.5 to +7.0	V
Power supply voltage (during programming)		V_{CC}	−0.5 to +7.5	V
Input voltage		V_{IN}	−1.5 to +5.5	V
Input voltage (during programming)		V_{IPRG}	22.5	V
Output voltage (during programming)		V_{OPRG}	−0.5 to +22.5	V
Input current		I_{IN}	−20	mA
Input current (during programming)		I_{IPRG}	+270	mA
Output current		I_{OUT}	+100	mA
Output current (during programming)		I_{OPRG}	+150	mA
Storage temperature	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−40 to +125	
Output voltage		V_{OUT}	−0.5 to V_{CC}	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Guaranteed Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Input low voltage	V_{IL}	0		0.8	V
Input high voltage	V_{IH}	2.0		5.5	V
Ambient temperature	T_A	0		75	°C

Capacitance
(f = 1 MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			10	pF
Output capacitance	C_O			12	pF

DC Characteristics
(Full guaranteed operating conditions unless otherwise noted.)

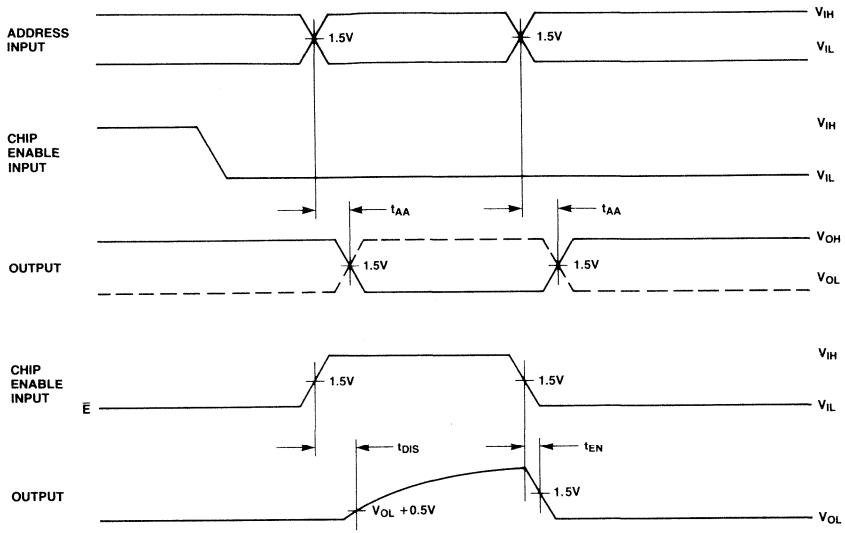
Parameter		Symbol	Min	Typ	Max	Unit
Input leakage current (V_{IH} = 5.5V)		I_R			40	μA
Input load current (V_{IL} = 0.45V)		I_F			−250	μA
Output low voltage (I_{OL} = 10 mA)		V_{OL}			0.45	V
Output low voltage (I_{OL} = 16 mA)		V_{OL}			0.50	V
Output leakage current (V_O = 2.4V, chip disabled)	MB7115	I_{OLK}			40	μA
Output leakage current (V_O = 2.4V, chip disabled)	MB7116	I_{OIH}			40	μA
Output leakage current (V_O = 0.5V, chip disabled)	MB7116	I_{OIL}			−40	μA
Input clamp voltage (I_{IN} = −18 mA)		V_{IC}			−1.2	V
Power supply current (V_{IN} = OPEN or GND)		I_{CC}		70*2	120	mA
Output high voltage (I_O = −2.4 mA)	MB7116	V_{OH}*1	2.4			V
Output short circuit current (V_O = GND)	MB7116	I_{OS}*1	−15		−60	mA

Notes: *1 Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{\overline{E}}$ = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.
*2 This value denotes conditions at T_A = 25°C and V_{CC} = +5.0V.

AC Characteristics
(Full guaranteed operating conditions unless otherwise noted.)

Parameter	Symbol	E Typ	E Max	H Typ	H Max	Unit
Access time (via address input)	t_{AA}	20	45	20	35	ns
Output disable time	t_{DIS}	15	30	15	30	ns
Output enable time	t_{EN}	15	30	15	30	ns

Operation Timing Diagram

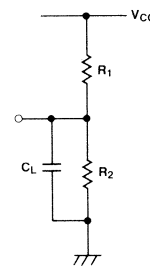


NOTE: OUTPUT DISABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO REACH A HIGH IMPEDANCE STATE WHEN THE CHIP ENABLE IS TAKEN HIGH (DISABLED). OUTPUT ENABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO BECOME ACTIVE WHEN THE CHIP ENABLE IS TAKEN LOW (ENABLED). THE HIGH IMPEDANCE STATE IS DEFINED AS A POINT ON THE OUTPUT WAVEFORM EQUAL TO A ΔV of 0.5V FROM THE ACTIVE OUTPUT LEVEL.

AC Test Conditions

Input Conditions

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5 ns from 1V to 2V
Frequency ..... 1 MHz



TRUTH TABLE

	MB7115/MB7116		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30 pF
t_{DIS}	300Ω	600Ω	30 pF
t_{EN}	300Ω	600Ω	30 pF

Input/Output Circuit Information

Input

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

Open-Collector Output

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30 mA for the MB7116 (3-state) compared to 0 mA for the MB7115 (open-collector).

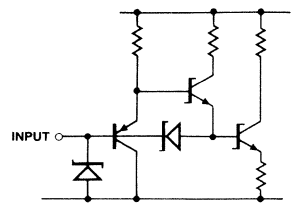
Three-State Output

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

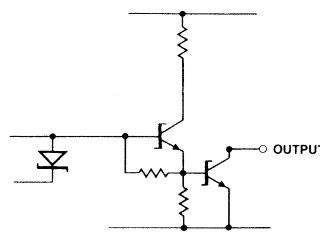
In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor provided in the output circuit is effective to decrease a load for the Chip Enable circuit.

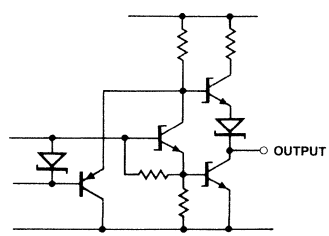
MB7115/MB7116 Input



MB7115 Output

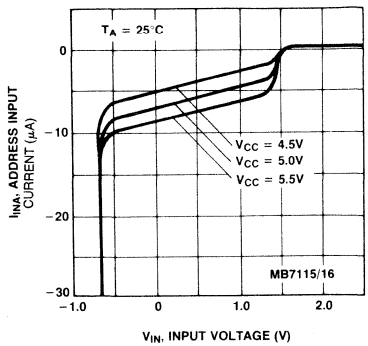


MB7116 Output

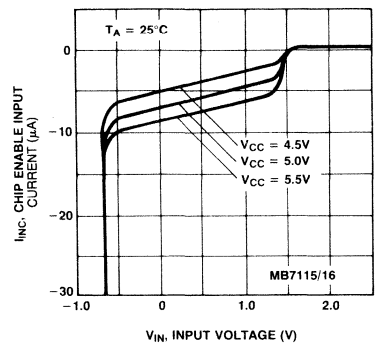


Typical Characteristics Curves

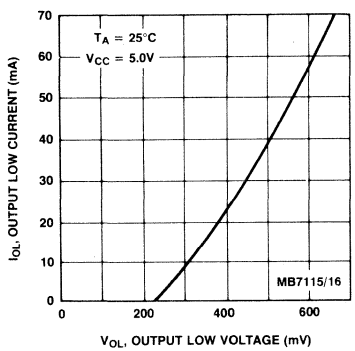
I_{INA} Input Current vs. V_{IN} Input Voltage



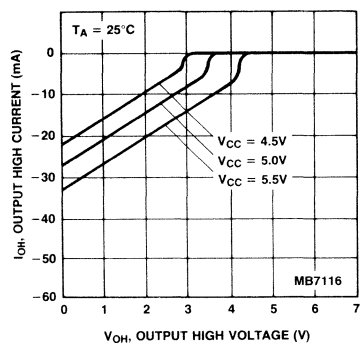
I_{INC} Input Current vs. V_{IN} Input Voltage



I_{OL} Output Low Current vs. V_{OL} Output Low Voltage

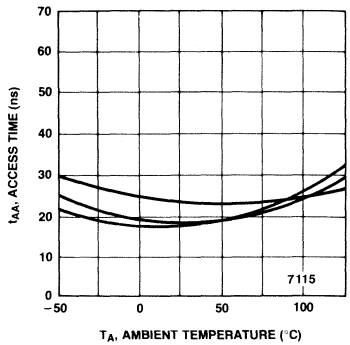


I_{OH} Output High Current vs. V_{OH} Output High Voltage

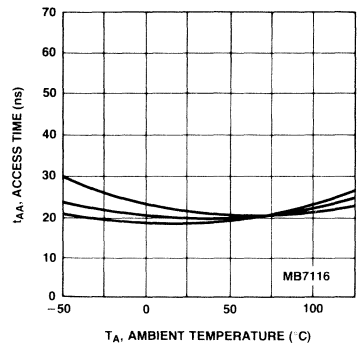


Typical Characteristics Curves
(Continued)

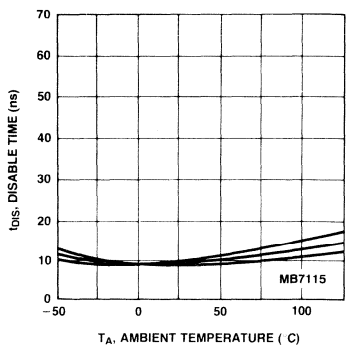
t_{AA} Access Time vs. Ambient Temperature



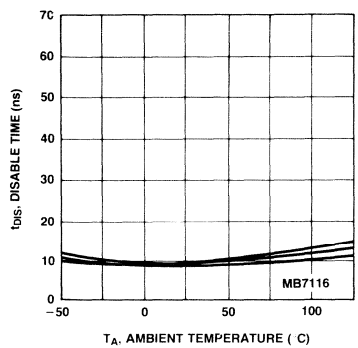
t_{AA} Access Time vs. Ambient Temperature



t_{DIS} Disable Time vs. Ambient Temperature

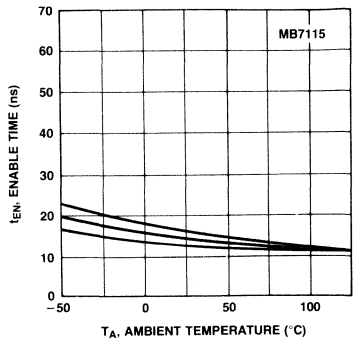


t_{DIS} Disable Time vs. Ambient Temperature

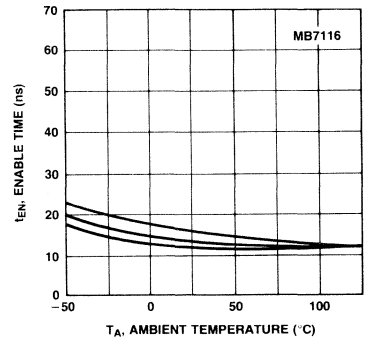


Typical Characteristics Curves
(Continued)

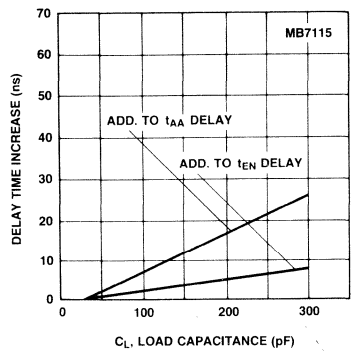
t_{EN} Enable Time vs. Ambient Temperature



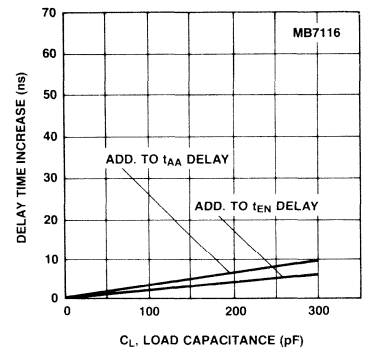
t_{EN} Enable Time vs. Ambient Temperature



Delay Time Increase vs. C_L Load Capacitance

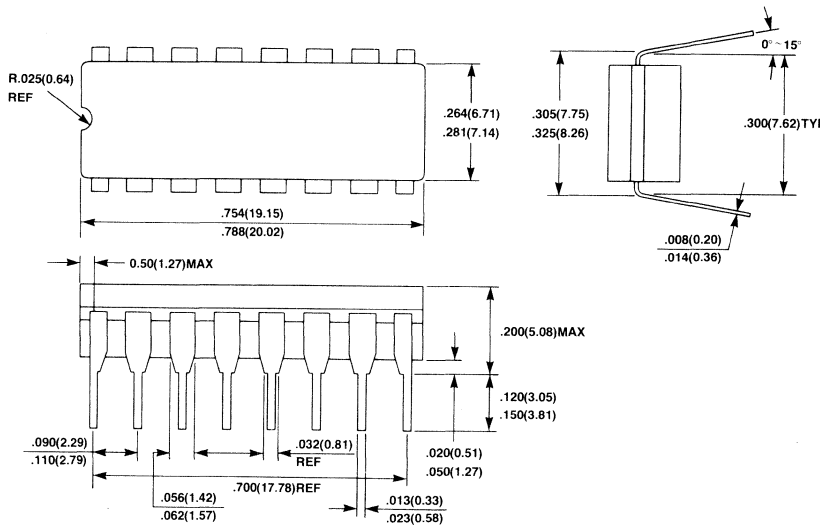


Delay Time Increse vs. C_L Load Capacitance

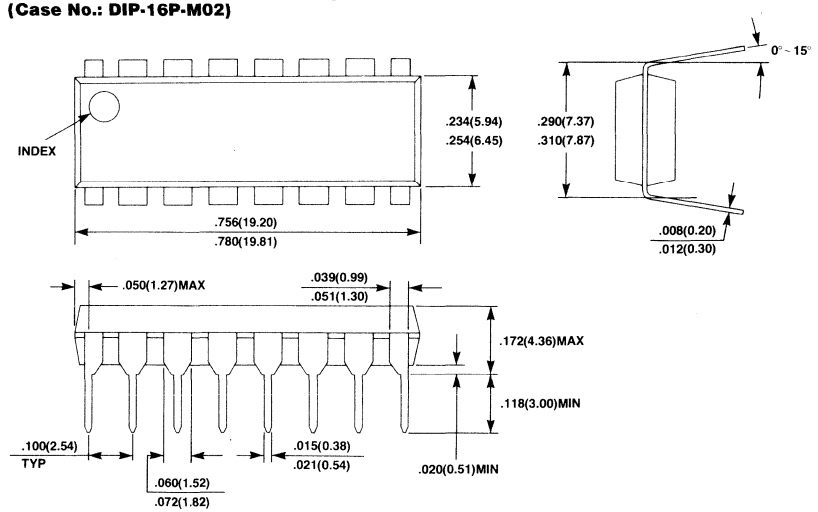


Package Dimensions
Dimensions in inches
(millimeter)

16-Lead Ceramic (CERDIP) Dual In-Line Package
(Case No.: DIP-16C-C02)



16-Lead Plastic Dual In-Line Package
(Case No.: DIP-16P-M02)



MB7117E/H, MB7118E/H

Schottky TTL 2048-Bit Bipolar Programmable Read-Only Memory

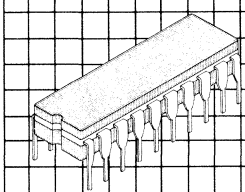
Description

The Fujitsu MB7117 and MB7118 are high speed Schottky TTL electrically field programmable read only memories organized as 256 words by 8-bits. With uncommitted collector outputs provided on the MB7117 and three-state outputs on the MB7118 memory expansion is simple.

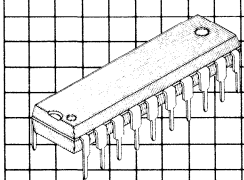
The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP™ (Diffused Eutectic Aluminum Process) according to simple programming procedures.

The sophisticated passive isolation termed IOP (Isolation by Oxide and Polysilicon) with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

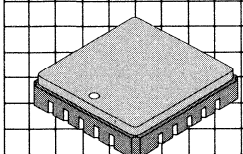
Extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.



Cerdip Package
DIP-20C-C01



Plastic Package
DIP-20P-M02

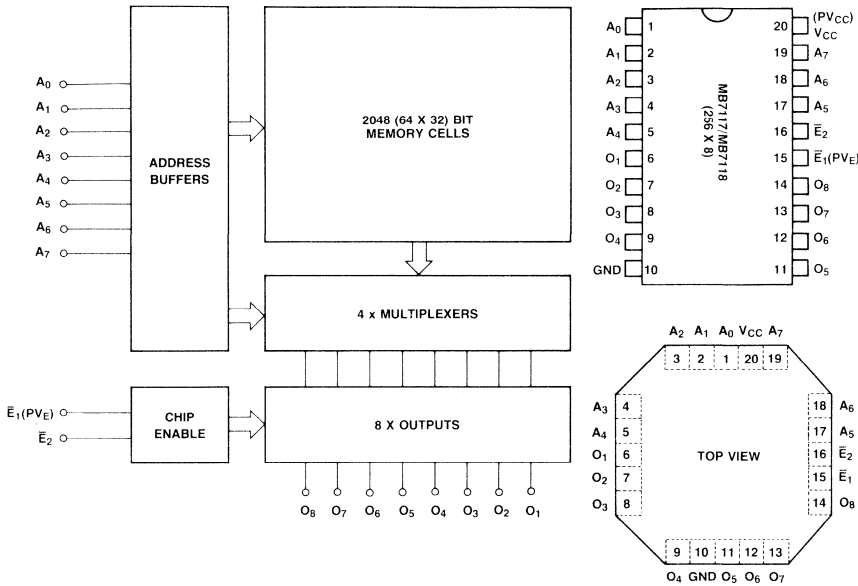


LCC-20C-F02

Features

- **Single +5V supply voltage**
- **Organized as 256 words by 8-bits, fully decoded**
- **Proven higher programmability and reliability**
- **Programming by DEAP™ (Diffused Eutectic Aluminum Process)**
- **Simplified, low power programming**
- **Low current PNP inputs**
- **AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques**
- **Fast access time, 25 nsec typ.**
  E—45 nsec max.
  H—35 nsec max.
- **TTL compatible inputs and outputs**
- **Open collector outputs, MB7117**
- **Three-state outputs, MB7118**
- **Two chip enables for simplified memory expansion**
- **Standard 20-pin DIP package**
- **JEDEC approved pin out**

MB7117E/H, MB7118E/H Block Diagram and Pin Assignment



Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Power supply voltage		V_{CC}	−0.5 to +7.0	V
Power supply voltage (druing programming)		V_{CC}	−0.5 to +7.5	V
Input voltage		V_{IN}	−1.5 to +5.5	V
Input voltage (during programming)		V_{PRG}	22.5	V
Output voltage (during programming)		V_{PRG}	0.5 to +22.5	V
Input current		I_{IN}	−20	mA
Input current (during programming)		I_{PRG}	+270	mA
Output current		I_{OUT}	+100	mA
Output current (during Programming)		I_{PRG}	+150	mA
Storage temperature	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−40 to +125	
Output voltage		V_{OUT}	−0.5 to V_{CC}	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Guaranteed Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Input low voltage	V_{IL}	0		0.8	V
Input high voltage	V_{IH}	2.0		5.5	V
Ambient temperature	T_A	0		75	°C

Capacitance
(f = 1MHz, V_{CC} = + 5V, V_{IN} = +2V, T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			10	pF
Output capacitance	C_O			12	pF

DC Characteristics
(Full guaranteed operating conditions unless otherwise noted.)

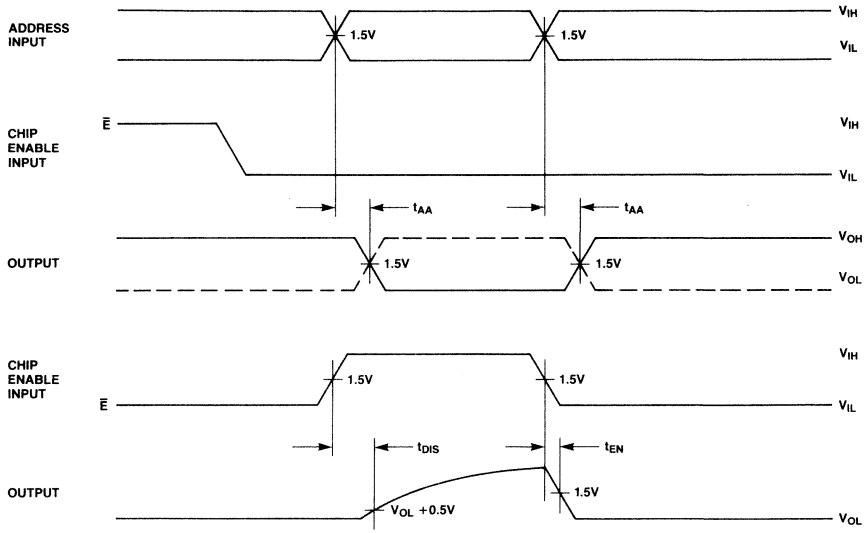
Parameter		Symbol	Min	Typ	Max	Unit
Input leakage current (V_{IH} = 5.5V)		I_R			40	μA
Input load current (V_{IL} = 0.45V)		I_F			−250	μA
Output low voltage (I_{OL} = 10mA)		V_{OL}			0.45	V
Output low voltage (I_{OL} = 16mA)		V_{OL}			0.50	V
Output leakage current (V_O = 2.4V, chip disabled)	MB7117	I_{OLK}			40	μA
Output leakage current (V_O = 2.4V, chip disabled)	MB7118	I_{OIH}			40	μA
Output leakage current (V_O = 0.45V, chip disabled)	MB7118	I_{OIL}			−40	μA
Input clamp voltage (I_{IN} = −18mA)		V_{IC}			−1.2	V
Power supply current (V_{IN} = OPEN or GND)		I_{CC}		80	140	mA
Output high voltage (I_O = −2.4mA)	MB7118	V_{OH} *1	2.4			V
Output short circuit current (V_O = GND)	MB7118	I_{OS} *1	−15		−60	mA

Note: *1 Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{\overline{IE}}$ = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

AC Characteristics
(Full guaranteed operating conditions unless otherwise noted.)

Parameter	Symbol	MB7117E/ MB7118E Typ	MB7117E/ MB7118E Max	MB7117H/ MB7118H Typ	MB7117H/ MB7118H Max	Unit
Access time (via address input)	t_{AA}	25	45	25	35	ns
Output disable time	t_{DIS}		30		30	ns
Output enable time	t_{EN}		30		30	ns

Operation Timing Diagram

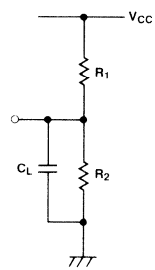


NOTE: OUTPUT DISABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO REACH A HIGH RESISTANCE STATE WHEN THE CHIP ENABLE IS TAKEN HIGH (DISABLED). OUTPUT ENABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO BECOME ACTIVE WHEN ALL OF CHIP ENABLES ARE TAKEN LOW (ENABLED). THE HIGH RESISTANCE STATE IS DEFINED AS A POINT ON THE OUTPUT WAVEFORM EQUAL TO A ΔV OF 0.5V FROM THE ACTIVE OUTPUT LEVEL.

AC Test Conditions

Input Conditions
Amplitude: 0V to 3V
Rise and Fall Time: 5 ns from 1V to 2V
Frequency: 1MHz

	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF
t_{DIS}	300Ω	600Ω	30pF
t_{EN}	300Ω	600Ω	30pF



Input/Output Circuit Information

Input Circuit

Schottky TTL circuit technology is used in the input circuit to achieve high-speed operation. A PNP transistor in the first stage of the input circuit improves input high/low current characteristics remarkably. The input circuit also includes a protection diode for reliable operation.

Open Collector Output

The open collector output is often utilized in high-speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high-frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB7118 (three-state) compared to 0mA for the MB7117 (open-collector).

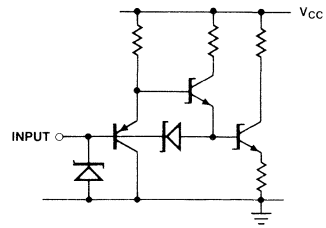
Three-State Output

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high-impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

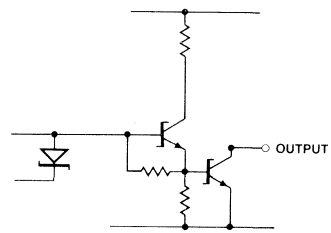
In the case where two devices are on at the same time, the possibility exists that they may be in opposite (one a ONE and one a ZERO) impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor is also provided in the output circuit and is effective in decreasing a load for the Chip Enable circuit.

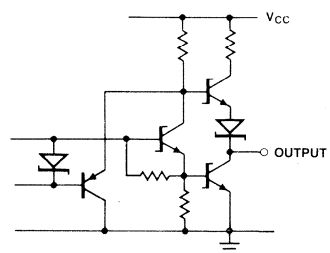
MB7117/MB7118 Input Circuit



MB7117 Output Circuit

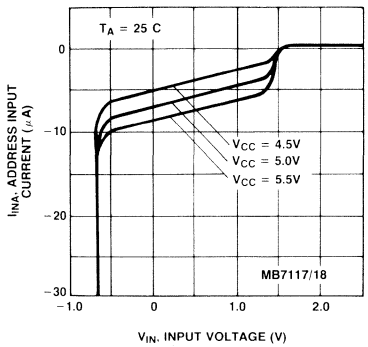


MB7118 Output Circuit

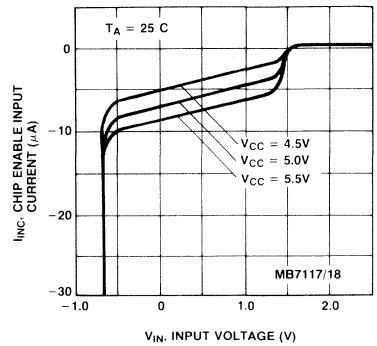


Typical Characteristics Curves

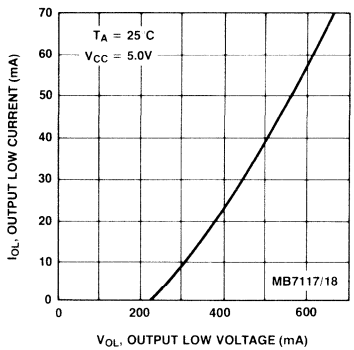
I_{INA} Input Current vs. V_{IN} Input Voltage



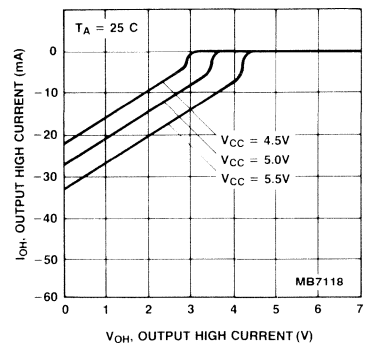
I_{INC} Input Current vs. V_{IN} Input Voltage



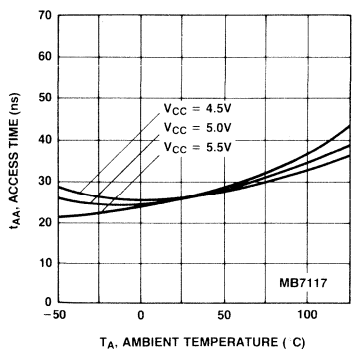
I_{OL} Output Low Current vs. V_{OL} Output Low Voltage



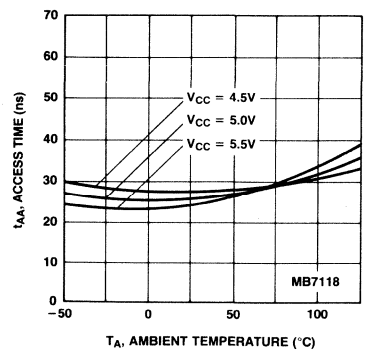
I_{OH} Output High Current vs. V_{OH} Output High Voltage



t_{AA} Access Time vs. Ambient Temperature

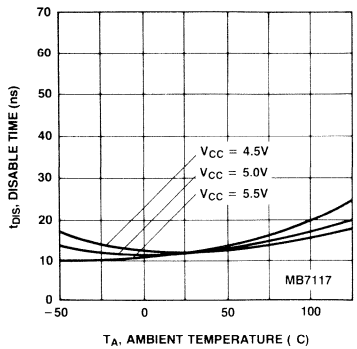


t_{AA} Access Time vs. Ambient Temperature

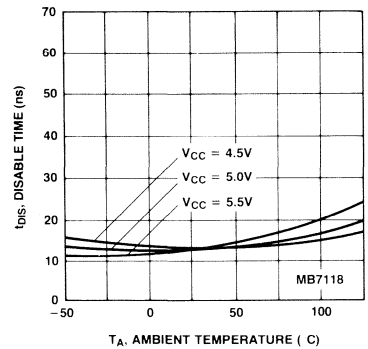


Typical Characteristics Curves
(Continued)

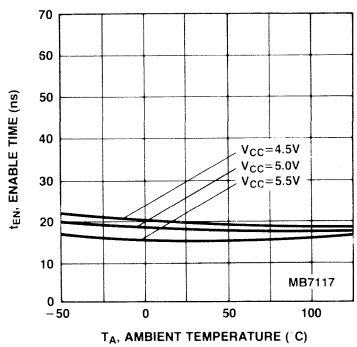
t_{DS} Disable Time vs. Ambient Temperature



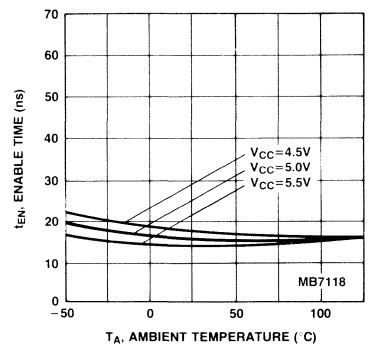
t_{DIS} Disable Time vs. Ambient Temperature



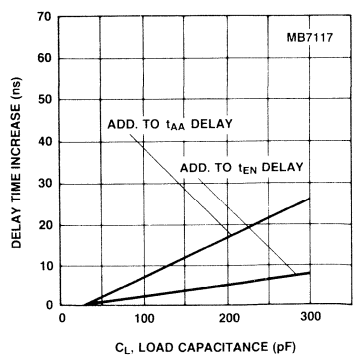
t_{EN} Enable Time vs. Ambient Temperature



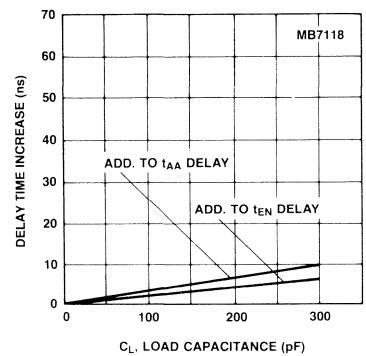
t_{EN} Enable Time vs. Ambient Temperature



Delay Time Increase vs. C_L Load Capacitance



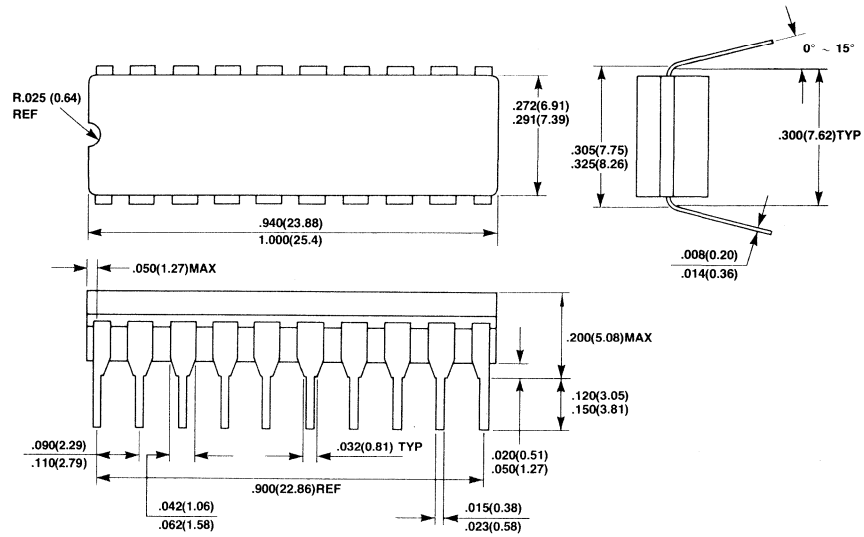
Delay Time Increase vs. C_L Load Capacitance



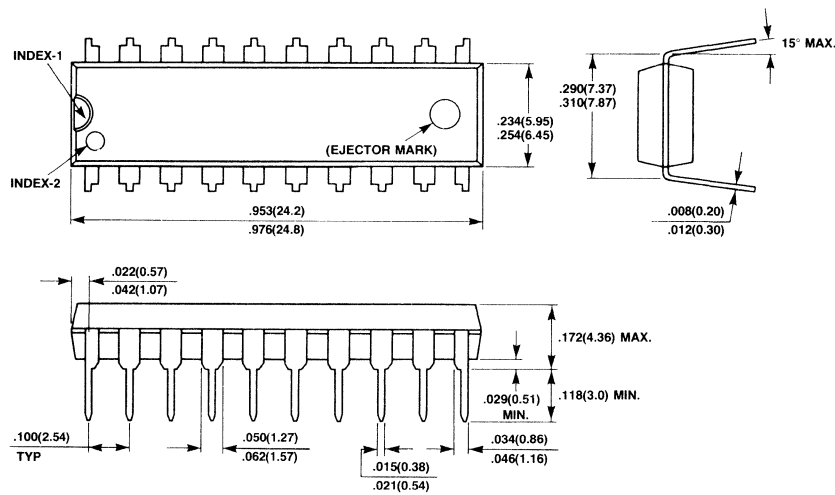
Package Dimensions

Dimensions in inches
(millimeters)

20-Pin Cerdip Dual In-Line Package
DIP-20C-C01

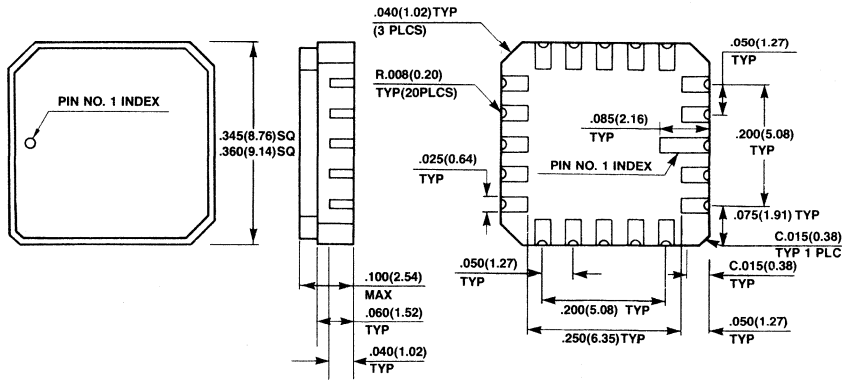


20-Pin Plastic Dual In-Line Package
DIP-20P-M02



Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

20-Pad Ceramic (Frit Seal) Leadless Chip Carrier
(Case No.: LCC-20C-FO2)



FUJITSU

MB7121E/H, MB7122E/H/Y

Programmable Schottky 4,096-Bit Read Only Memory

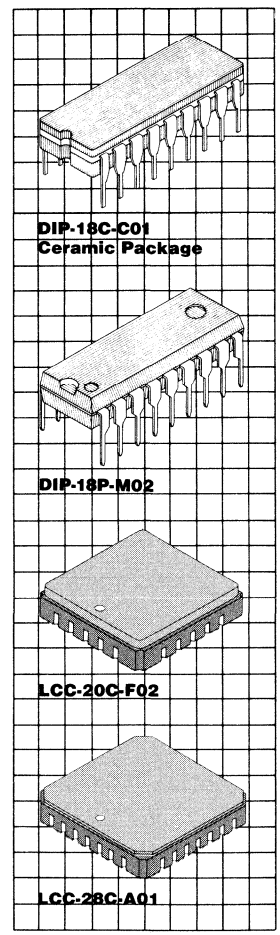
Description

The Fujitsu MB7121 and MB7122 are high speed Schottky TTL electrically field programmable read only memories organized as 1024 words by 4-bits. With uncommitted collector outputs provided on the MB7121 and three-state outputs on the MB7122, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP (Diffused Eutectic Aluminum Process) according to simple programming procedures.

The sophisticated passive isolation termed IOP (Isolation by Oxide and Poly-silicon) with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

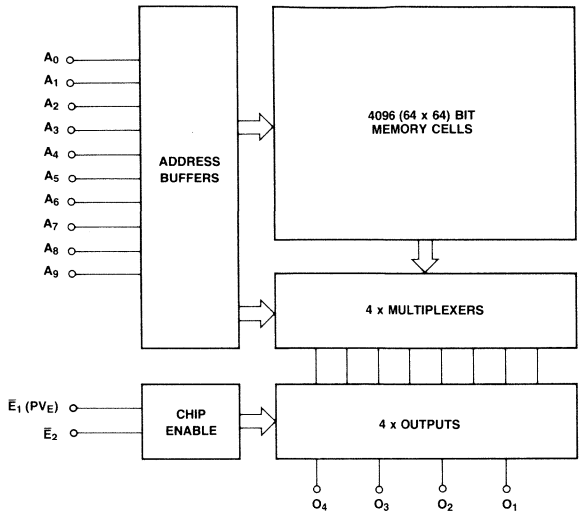


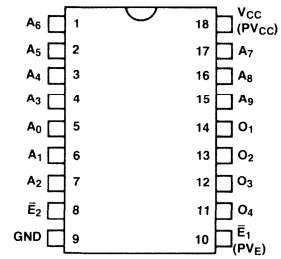
Features

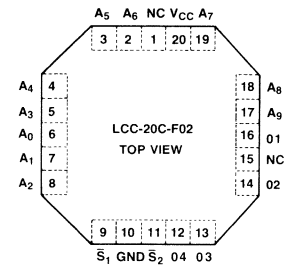
- **Single +5V supply voltage**
- **1,024 words x 4-bits organization, fully decoded**
- **Proven high programmability and reliability**
- **Programming by DEAP (Diffused Eutectic Aluminum Process)**
- **Simplified, low power programming**
- **Low current PNP inputs**
- **AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques**
- **Fast access time, 25 ns typ.**
  MB7122Y: 30 ns max.
  H: 35 ns max.
  E: 45 ns max.
- **TTL compatible inputs and outputs**
- **Open collector outputs (MB7121)**
- **3-state outputs (MB7122)**
- **Two chip enable leads for simplified memory expansion**
- **Standard 18 pin DIP package**
- **JEDEC approved pin out**

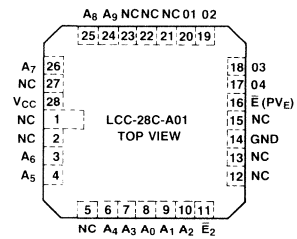
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB7122 Block Diagram and Pin Assignments









Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Power supply voltage		V_{CC}	−0.5 to +7.0	V
Power supply voltage (during programming)		V_{CC}	−0.5 to +7.5	V
Input voltage		V_{IN}	−1.5 to +5.5	V
Input voltage (during programming)		V_{PRG}	22.5	V
Output voltage (during programming)		V_{PRG}	−0.5 to +22.5	V
Input current		I_{IN}	−20	mA
Input current (during programming)		I_{PRG}	+270	mA
Output current		I_{OUT}	+100	mA
Output current (during programming)		I_{PRG}	+150	mA
Storage temperature	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−40 to +125	
Output voltage		V_{OUT}	−0.5 to V_{CC}	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Guaranteed Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Input low voltage	V_{IL}			0.8	V
Input high voltage	V_{IH}	2.0			V
Ambient temperature	T_A	0		75	°C

Capacitance

(f = 1 MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			10	pF
Output capacitance	C_O			12	pF

DC Characteristics

(Full guaranteed operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Input leakage current (V_{IH} = 5.5V)		I_R			40	μA
Input load current (V_{IL} = 0.45V)		I_F			−250	μA
Output low voltage (I_{OL} = 10 mA)		V_{OL}			0.45	V
Output low voltage (I_{OL} = 16 mA)		V_{OL}			0.50	V
Output leakage current (V_O = 2.4V, chip disabled)	MB7121	I_{OLK}			40	μA
Output leakage current (V_O = 2.4V, chip disabled)	MB7122	I_{OIH}			40	μA
Output leakage current (V_O = 0.5V, chip disabled)	MB7122	I_{OIL}			−40	μA
Input clamp voltage (I_{IN} = −18 mA)		V_{IC}			−1.2	V
Power supply current (V_{IN} = OPEN or GND)		I_{CC}		105	150	mA
Output high voltage (I_O = −2.4 mA)	MB7122	V_{OH} *1	2.4			V
Output short circuit current (V_O = GND)	MB7122	I_{OS} *1	−15		−60	mA

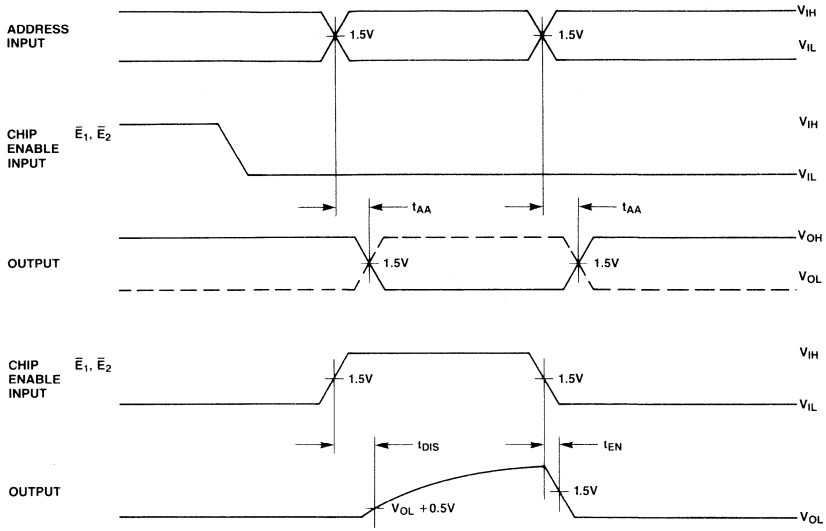
Note: *1 Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled (V_{ICE} = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

AC Characteristics

(Full guaranteed operating conditions unless otherwise noted.)

Parameter	Symbol	MB7121/7122E		MB7121/7122H		MB7122Y		Unit
		Typ	Max	Typ	Max	Typ	Max	
Access time (via address input)	t_{AA}	25	45	25	35	25	30	ns
Output disable time	t_{DIS}		30		30		25	ns
Output enable time	t_{EN}		30		30		25	ns

Operation Timing Diagram

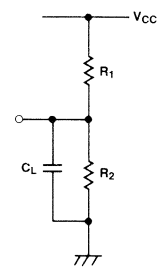


NOTE: OUTPUT DISABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO REACH A HIGH RESISTANCE STATE WHEN THE CHIP ENABLE IS TAKEN HIGH. OUTPUT ENABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO BECOME ACTIVE WHEN THE CHIP ENABLE IS TAKEN LOW. THE HIGH RESISTANCE STATE IS DEFINED AS A POINT ON THE OUTPUT WAVEFORM EQUAL TO A ΔV OF 0.5V FROM THE ACTIVE OUTPUT LEVEL.

AC Test Conditions

Input Conditions

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5 ns from 1V to 2V
Frequency ..... 1 MHz



TRUTH TABLE

	MB7121/MB7122		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30 pF
t_{DIS}	300Ω	600Ω	30 pF
t_{EN}	300Ω	600Ω	30 pF

Input/Output Circuit Information

Input

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

Open-Collector Output

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30 mA for the MB7122 (3-state) compared to 0 mA for the MB7121 (open-collector).

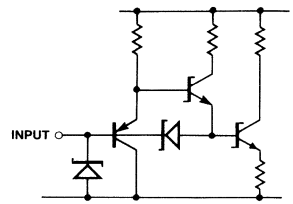
Three-State Output

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

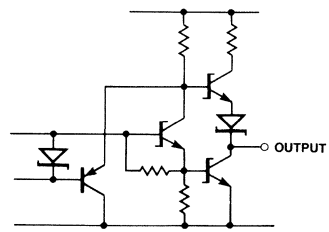
In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor provided in the output circuit is effective to decrease a load for the Chip Enable circuit.

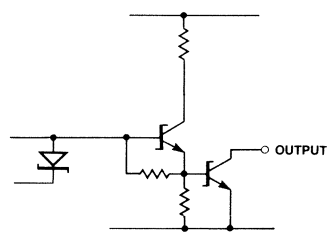
MB7121/MB7122 Input



MB7121 Output

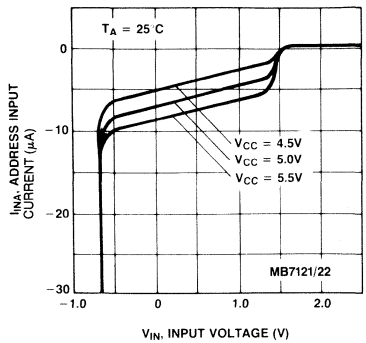


MB7122 Output

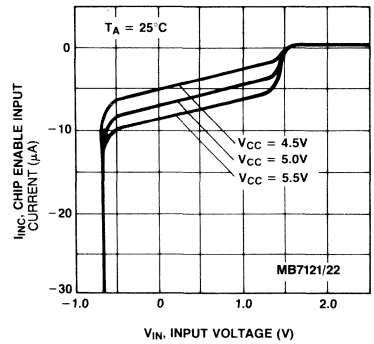


Typical Characteristics Curves

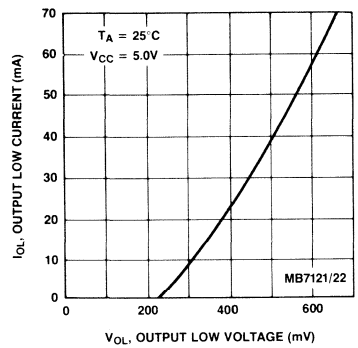
I_{INA} Input Current vs. V_{IN} Input Voltage



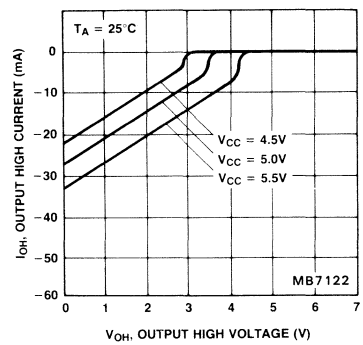
I_{INC} Input Current vs. V_{IN} Input Voltage



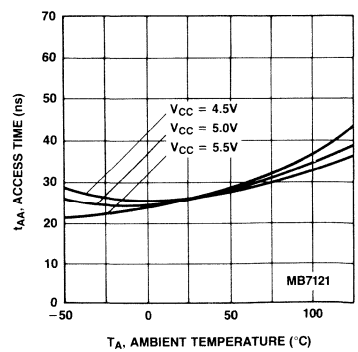
I_{OL} Output Low Current vs. V_{OL} Output Low Voltage



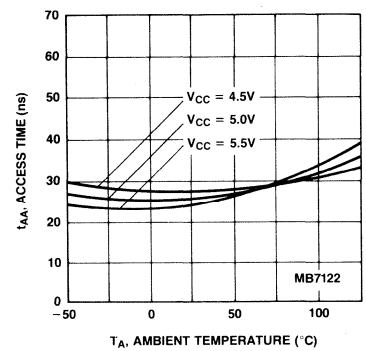
I_{OH} Output High Current vs. V_{OH} Output High Voltage



t_{AA} Access Time vs. Ambient Temperature

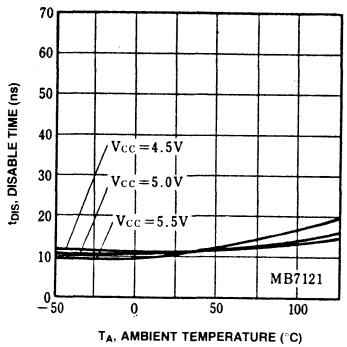


t_{AA} Access Time vs. Ambient Temperature

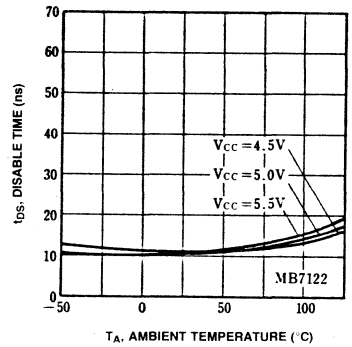


Typical Characteristics Curves
(Continued)

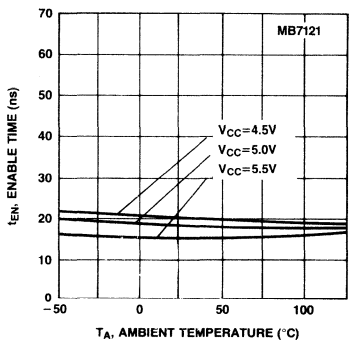
t_{DS} Disable Time vs. Ambient Temperature



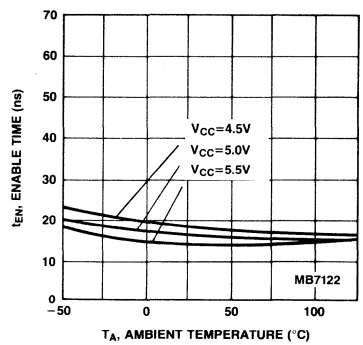
t_{DIS} Disable Time vs. Ambient Temperature



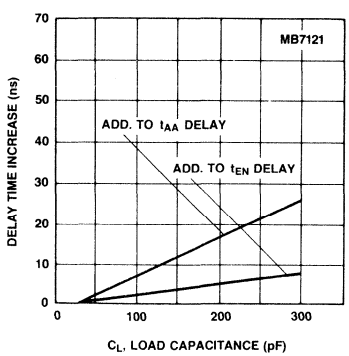
t_{EN} Enable Time vs. Ambient Temperature



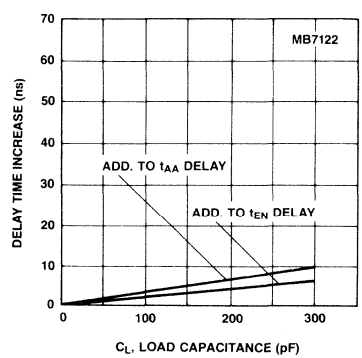
t_{EN} Enable Time vs. Ambient Temperature



Delay Time Increase vs. C_L Load Capacitance



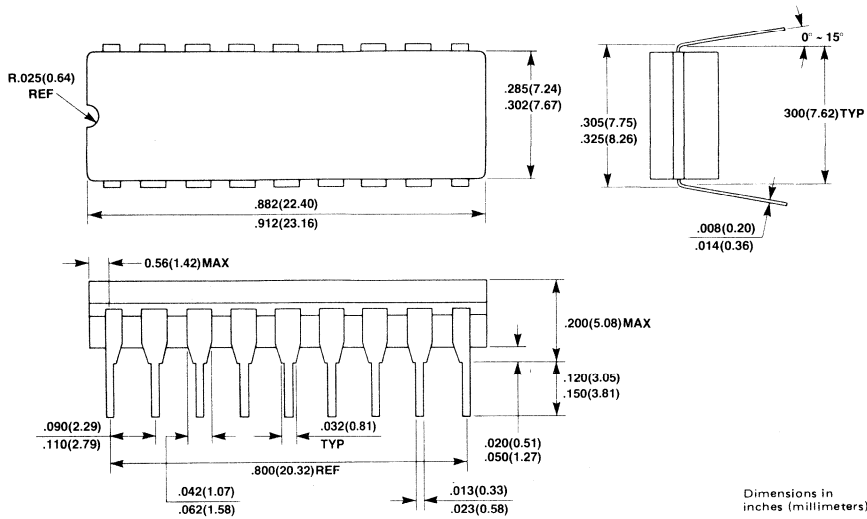
Delay Time Increase vs. C_L Load Capacitance



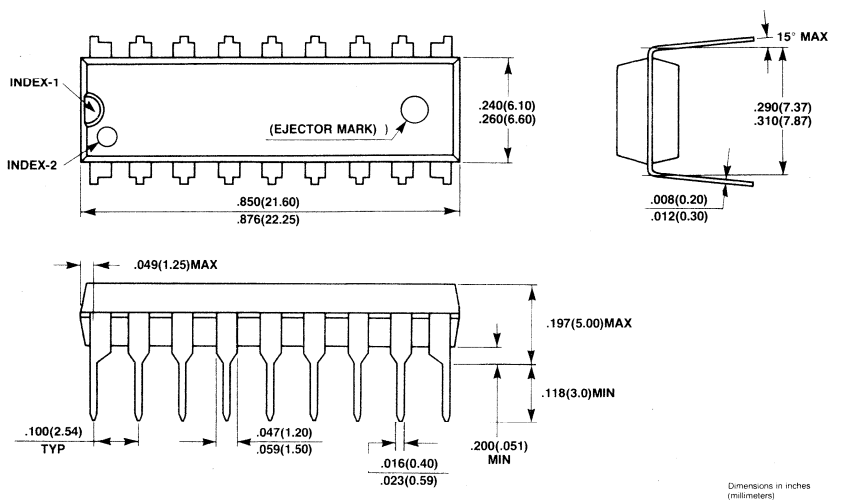
Package Dimensions

Dimensions in inches (millimeters)

18-Lead Ceramic (CERDIP) Dual In-Line Package (Case No.: DIP-18C-C01)

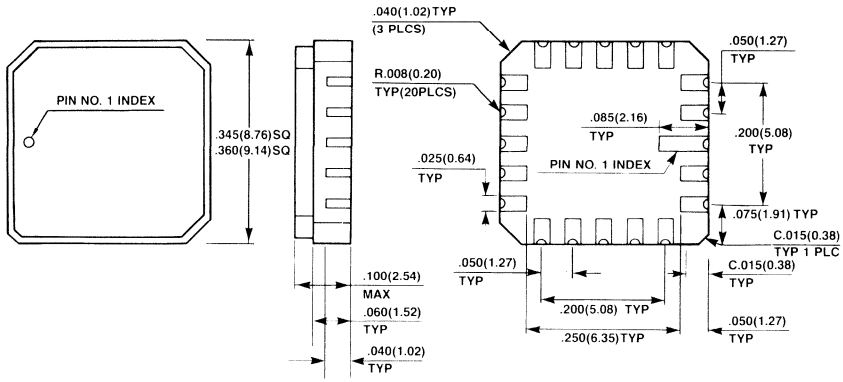


18-Lead Plastic Dual-In-Line Package (Case No.: DIP-18P-M02)

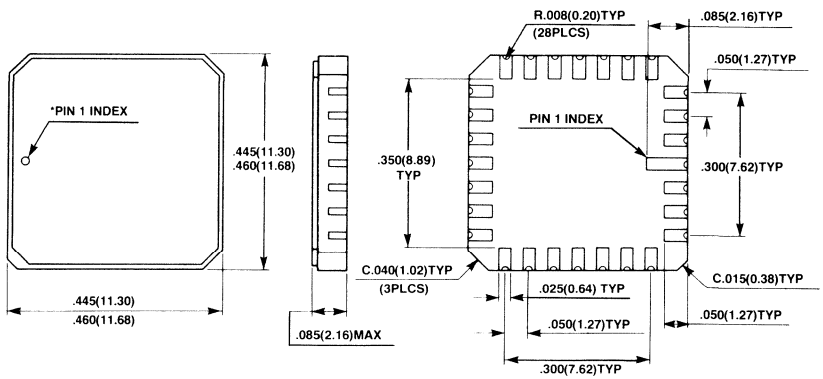


Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

20-Pad Ceramic (Frit Seal) Leadless Chip Carrier
(Case No.: LCC-20C-F02)



28-Pad Ceramic (Metal Seal) Leadless Chip Carrier
(Case No.: LCC-28C-A01)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

FUJITSU

MB7123E/H, MB7124E/H
Programmable Schottky 4096-Bit Read Only Memory

Description

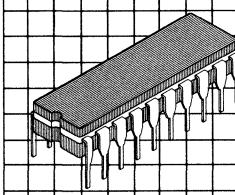
The Fujitsu MB7123 (open collector) and MB7124 (three-state) are high-speed, Schottky TTL electrically field programmable read-only memories organized as 512 words by 8-bits.

Fujitsu PROMS utilize a unique Shallow V-Groove (SVG) passive isolation process which, combined with a very thin epitaxial layer and the Schottky TTL process, provides small die sizes and very fast access times.

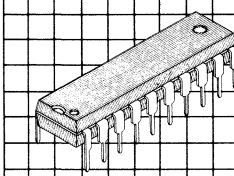
The memory is fabricated with all cells low, the "zero" value for positive logic. Logical "one" for a cell is achieved by programming. Individual cells are programmed to a logical "one" using the highly reliable Diffused Eutectic Aluminum Process (DEAP).

High programming yields are insured through the use of special test cells to verify programmability on each device prior to shipment.

Two guaranteed maximum access time options are available: the 7123 or 7124 "E" versions guarantee 45 ns maximum access time; the 7123 or 7124 "H" versions guarantee 35 ns maximum access time.



Ceramic Package
DIP-20C-C01



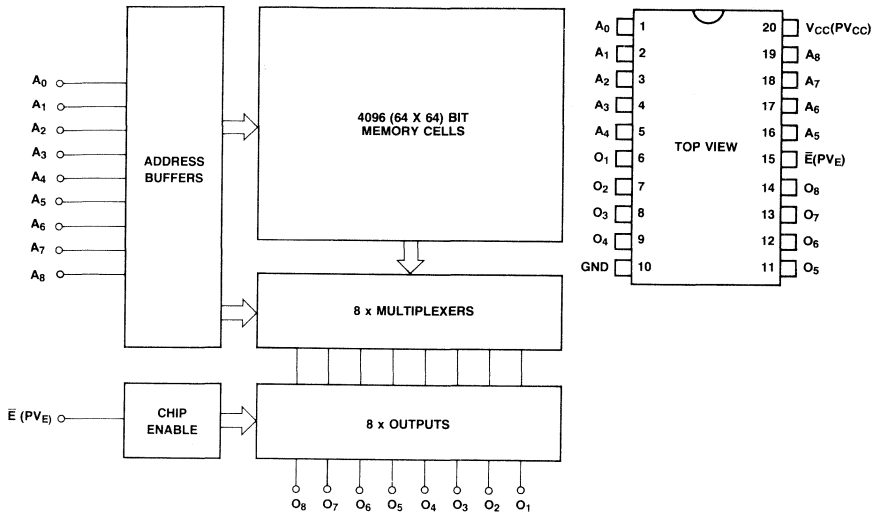
Plastic Package
DIP-20P-M02

Features

- **Single +5V power supply requirement**
- **512 words x 8-bits; fully decoded**
- **High levels of programmability and reliability proven in use**
- **Unique, reliable DEAP programming process**
- **Low power, simplified programming techniques**
- **Low current PNP inputs**
- **AC characteristics guaranteed over the full operating range**
- **Fast. 25 ns typical access time with two guaranteed options:**
  7123/7124 E: 45 ns max.
  7123/7124 H: 35 ns max.
- **TTL compatible inputs and outputs; open collector or three-state**
- **Single Chip Enable input**
- **JEDEC standard pinout; 20-pin package**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB7123/7124 Block Diagram and Pin Assignment



Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Power supply voltage		V_{CC}	−0.5 to +7.0	V
Power supply voltage (during programming)		V_{CC}	−0.5 to +7.5	V
Input voltage		V_{IN}	−1.5 to +5.5	V
Input voltage (during programming)		V_{PRG}	22.5	V
Output voltage (during programming)		V_{PRG}	−0.5 to +22.5	V
Input current		I_{IN}	−20	mA
Input current (during programming)		I_{PRG}	+270	mA
Output current		I_{OUT}	+100	mA
Output current (during programming)		I_{PRG}	+150	mA
Storage temperature	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−40 to +125	
Output voltage		V_{OUT}	−0.5 to V_{CC}	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Guaranteed Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Input low voltage	V_{IL}			0.8	V
Input high voltage	V_{IH}	2.0			V
Ambient temperature	T_A	0		75	°C

Capacitance
($f = 1$ MHz, $V_{CC} = +5V$, $V_{IN} = +2V$, $T_A = 25°C$)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			10	pF
Output capacitance	C_O			12	pF

DC Characteristics
(Full guaranteed operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Input leakage current ($V_{IH} = 5.5V$)		I_R			40	μA
Input load current ($V_{IL} = 0.45V$)		I_F			−250	μA
Output low voltage ($I_{OL} = 10$ mA)		V_{OL}			0.45	V
Output low voltage ($I_{OL} = 16$ mA)		V_{OL}			0.50	V
Output leakage current ($V_O = 2.4V$, chip disabled)	MB7123	I_{OLK}			40	μA
Output leakage current ($V_O = 2.4V$, chip disabled)	MB7124	I_{OIH}			40	μA
Output leakage current ($V_O = 0.45V$, chip disabled)	MB7124	I_{OIL}			−40	μA
Input clamp voltage ($I_{IN} = -18$ mA)		V_{IC}			−1.2	V
Power supply current (V_{IN} = OPEN or GND)		I_{CC}		120	170	mA
Output high voltage*1 ($I_O = -2.4$ mA)	MB7124	V_{OH}	2.4			V
Output short circuit current*1 (V_O = GND)	MB7124	I_{OS}	15		−60	mA

Note: *1 Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{ICE} = 0.4V$) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

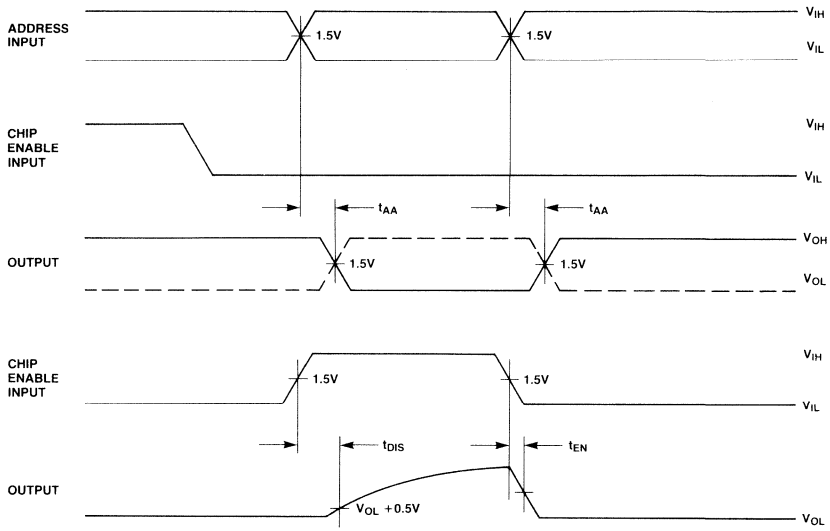
AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	E		H		Unit
		Typ	Max	Typ	Max	
Access time (via address input)	t_{AA}	25	45	25	35	ns
Output disable time	t_{DIS}	15	30	15	30	ns
Output enable time	t_{EN}	15	30	15	30	ns

AC Characteristics

(Recommended operating conditions unless otherwise noted.)

Operation Timing Diagram



NOTE: OUTPUT DISABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO REACH A HIGH RESISTANCE STATE WHEN THE CHIP ENABLE IS TAKEN HIGH. OUTPUT ENABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO BECOME ACTIVE WHEN THE CHIP ENABLE IS TAKEN LOW. THE HIGH RESISTANCE STATE IS DEFINED AS A POINT ON THE OUTPUT WAVEFORM EQUAL TO A ΔV OF 0.5V FROM THE ACTIVE OUTPUT LEVEL.

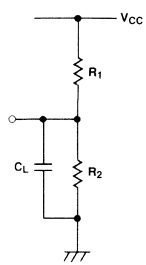
AC Test Conditions

Input Conditions

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5 ns from 1V to 2V
Frequency ..... 1 MHz

TRUTH TABLE

	MB7123/7124		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30 pF
t_{DIS}	300Ω	600Ω	30 pF
t_{EN}	300Ω	600Ω	30 pF



Input/Output Circuit Information

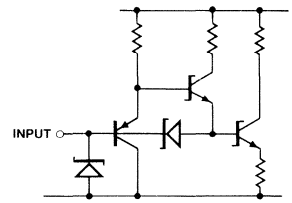
Input

Schottky TTL circuit technology is used in the input circuit to achieve high-speed operation. The PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. A protection diode protects against voltage transients.

Open-Collector Output

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30 mA for the MB7124 (three-state) compared to 0 mA for the MB7123 (open-collector).

MB7123/7124 Input



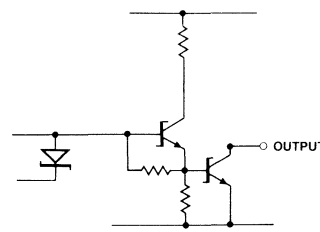
Three-State Output

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

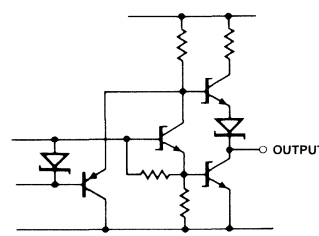
In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor provided in the output circuit decreases the load for the Chip Enable circuit.

MB7123 Output

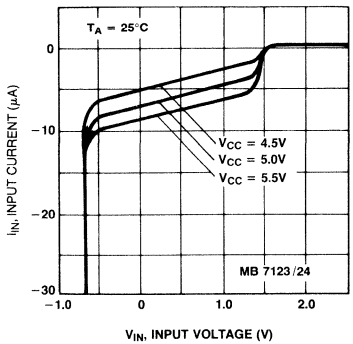


MB7124 Output

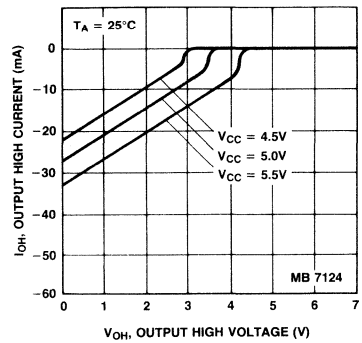


Typical Characteristics Curves

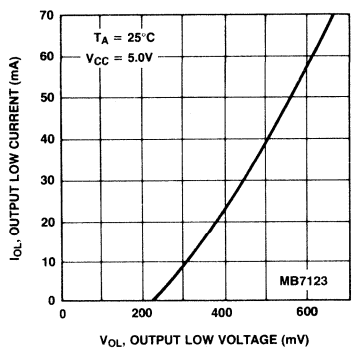
I_{IN} Input Current vs. V_{IN} Input Voltage



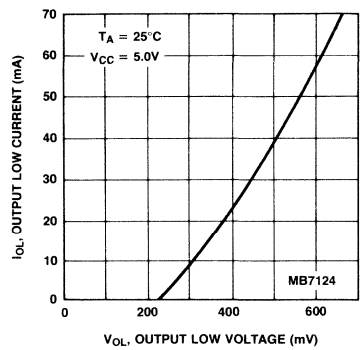
I_{OH} Output High Current vs. V_{OH} Output High Voltage



I_{IL} Output Low Current vs. V_{OL} Output Low Voltage

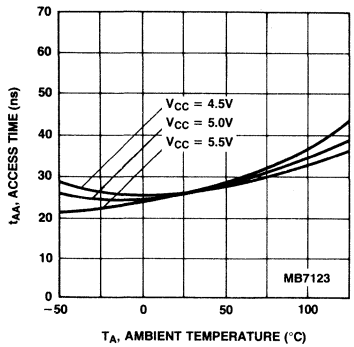


I_{OL} Output Low Current vs. V_{OL} Output Low Voltage

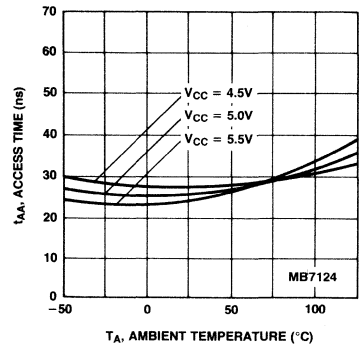


Typical Characteristics Curves
(Continued)

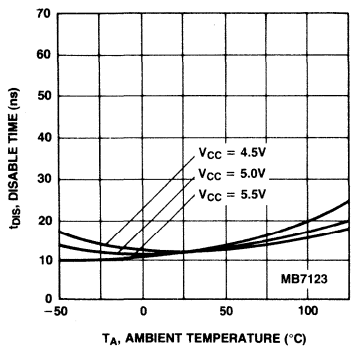
t_{AA} Access Time vs. Ambient Temperature



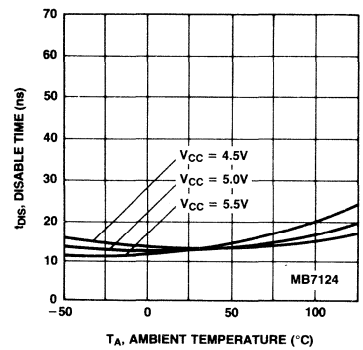
t_{AA}, Access Time vs. Ambient Temperature



t_{DIS} Disable Time vs. Ambient Temperature

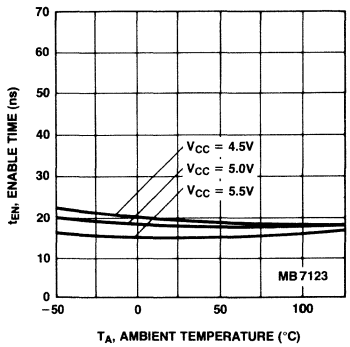


t_{DIS} Disable Time vs. Ambient Temperature

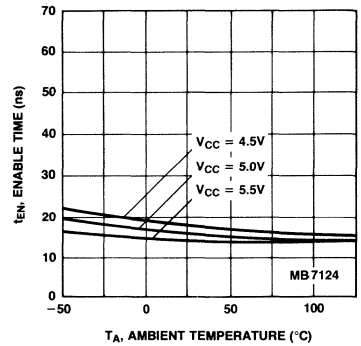


Typical Characteristics Curves
(Continued)

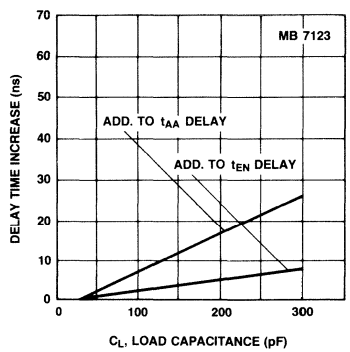
t_{EN} Enable Time vs. Ambient Temperature



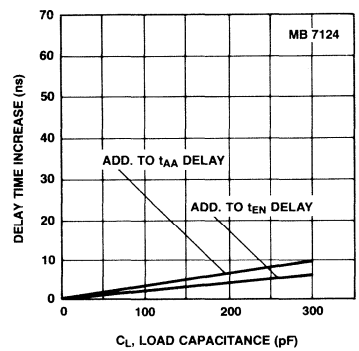
t_{EN} Enable Time vs. Ambient Temperature



Delay Time Increase vs. C_L Load Capacitance

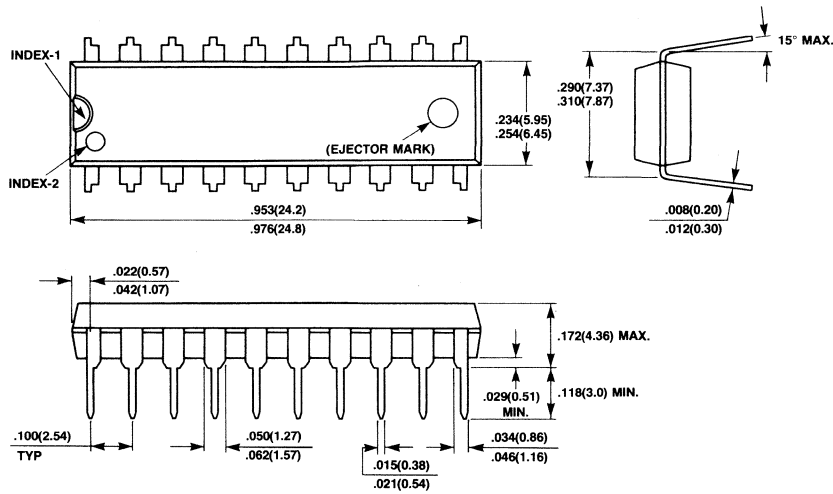


Delay Time Increase vs. C_L Load Capacitance

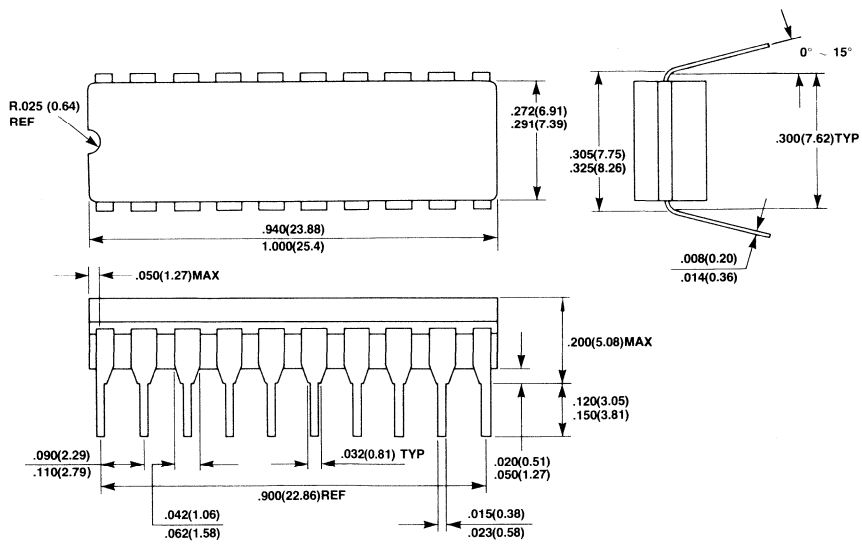


Package Dimensions
Dimensions in inches
(millimeters)

20-Lead Plastic Dual In-Line Package
(Case No.: DIP-20P-M02)



20-Lead Ceramic (CERDIP) Dual In-Line Package
(Case No.: DIP-20C-C01)



FUJITSU

MB7127E/H, MB7128E/H/Y

High Speed Schottky TTL 8,192-Bit PROM

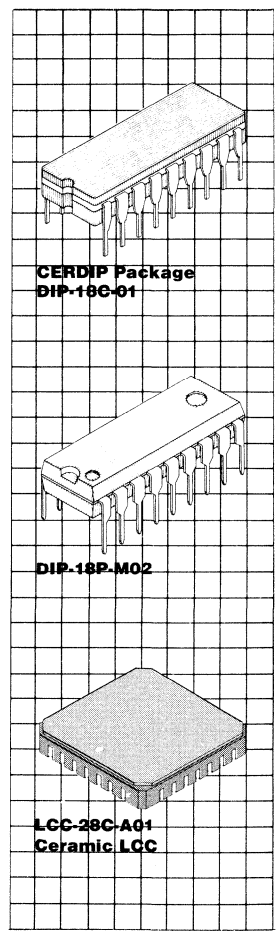
Description

The Fujitsu MB7127/MB7128 are high speed Schottky TTL electrically field programmable read only memories. With open collector outputs on the MB7127 and three-state outputs on the MB7128, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP™ (Diffused Eutectic Aluminum Process) during a simple programming procedure.

The sophisticated passive isolation termed IOP (Isolation by Oxide and Poly-silicon) with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmabily.

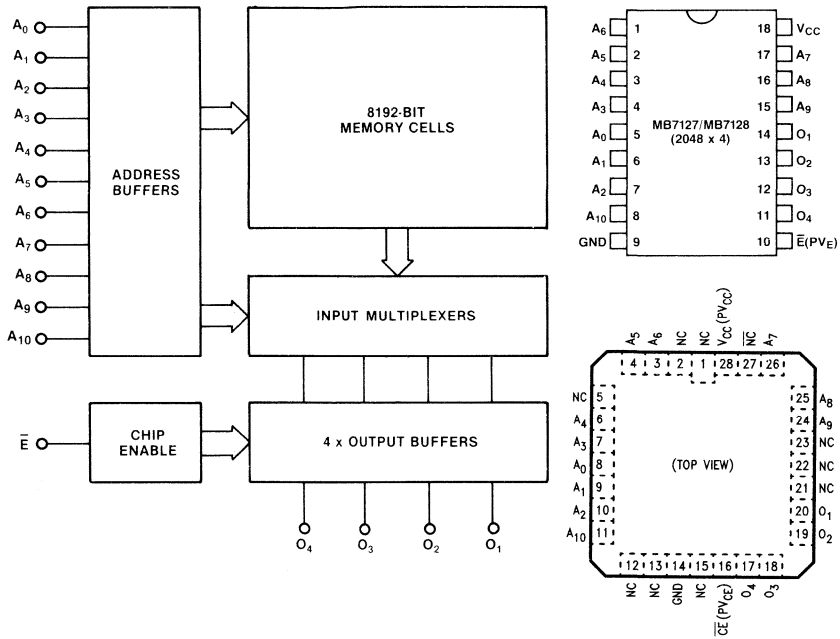


Features

- **Organization: 2,048 x 4-bits**
- **TTL compatible input/output**
- **Fast access time, 30 ns typ.**
  MB7127/MB7128E:
  55 ns max.
  MB7127/MB7128H:
  45 ns max.
  MB7128Y: 35 ns max.
- **Low power dissipation:**
  155 mA max.
- **Single +5V supply voltage**
- **Proven high programmability and reliability of DEAP™ (Diffused Eutectic Aluminum Process) PROM**
- **Chip enable leads for simple memory expansion**
- **Simplified, low power programming**
- **Low current PNP inputs**
- **3-state outputs on MB7128**
- **Open collector outputs on MB7127**
- **Standard 18-pin DIP package**
- **MB7128 pin compatible with industry standard products, 82S185, HM7685, 63S841**
- **MB7127 pin compatible with 82S184, HM7684, 63S840, 27S184**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

MB7127/MB7128 Block Diagram and Pin Assignment



Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Power supply voltage	V_{CC}	−0.5 to +7.0	V
Power supply voltage (during programming)	V_{CC}	−0.5 to +7.5	V
Input voltage	V_{IN}	−1.5 to +5.5	V
Input voltage (during programming)	V_{IPRG}	22.5	V
Output voltage (during programming)	V_{OPRG}	−0.5 to +22.5	V
Input current	I_{IN}	−20	mA
Input current (during programming)	I_{IPRG}	+270	mA
Output current	I_{OUT}	+100	mA
Output current (during programming)	I_{OPRG}	+150	mA
Storage temperature	T_{STG}	−65 to +150	°C
Output voltage	V_{OUT}	−0.5 to $+V_{CC}$	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Input low voltage	V_{IL}	0.0		0.8	V
Input high voltage	V_{IH}	2.0		V_{CC}	V
Ambient temperature	T_A	0		75	°C

Capacitance
(f = 1 MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			10	pF
Output capacitance	C_O			15	pF

DC Characteristics
(Full guaranteed operating ranges unless otherwise noted.)

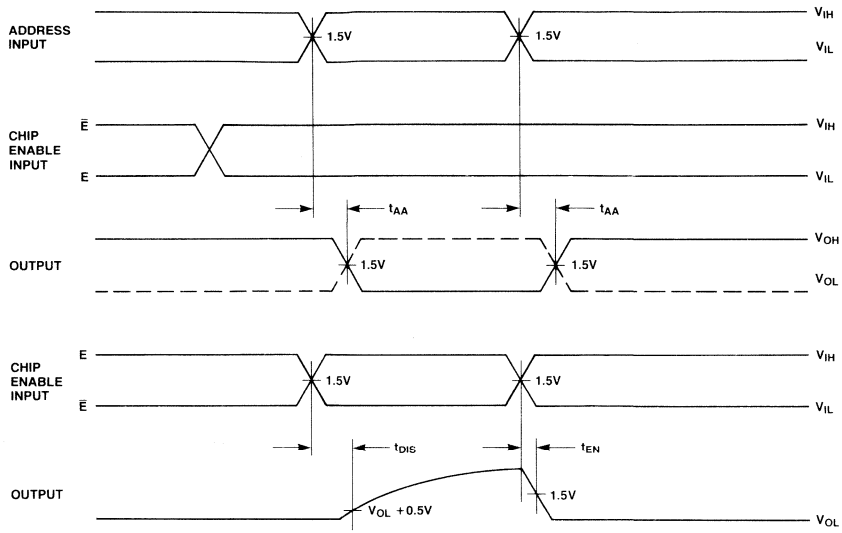
Parameter		Symbol	Min	Typ	Max	Unit
Input leakage current (V_{IH} = 5.5V)		I_R			40	μA
Input load current (V_{IL} = 0.45V)		I_F			−250	μA
Output low voltage (I_{OL} = 10 mA)		V_{OL}			0.45	V
Output low voltage (I_{OL} = 16 mA)		V_{OL}			0.50	V
Output leakage current (V_O = 2.4V, chip disabled)	MB7127	I_{OLK}			40	μA
Output leakage current (V_O = 2.4V, chip disabled)	MB7128	I_{OIH}			40	μA
Output leakage current (V_O = 0.45V, chip disabled)	MB7128	I_{OIL}			−40	μA
Input clamp voltage (I_{IN} = −18 mA)		V_{IC}			−1.2	V
Power supply current (V_{IN} = OPEN or GND)		I_{CC}		110	155	mA
Output high voltage (I_O = −2.4 mA)	MB7128	V_{OH} *1	2.4			V
Output short circuit current (V_O = GND)	MB7128	I_{OS} *1	−15		−60	mA

Note:: *1 Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled (V_{CE} = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

AC Characteristics
(Full guaranteed operating ranges unless otherwise noted.)

		MB7127E/ MB7128E		MB7127H MB7128H		MB7128Y		
Parameter	**Symbol**	**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Unit**
Access time (via address input)	t_{AA}	30	55	30	45	26	35	ns
Output disable time	t_{DIS}		40		30		25	ns
Output enable time	t_{EN}		40		30		25	ns

Operation Timing Diagram



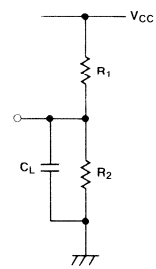
NOTE: OUTPUT DISABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO REACH A HIGH RESISTANCE STATE WHEN THE CHIP ENABLE IS DISABLED. OUTPUT ENABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO BECOME ACTIVE WHEN THE CHIP ENABLE IS ENABLED. THE HIGH RESISTANCE STATE IS DEFINED AS A POINT ON THE OUTPUT WAVEFORM EQUAL TO A ΔV OF 0.5V FROM THE ACTIVE OUTPUT LEVEL.

AC Test Conditions

Input Conditions

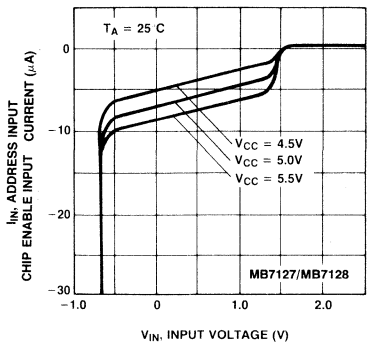
Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5 ns from 1V to 2V
Frequency ..... 1 MHz

MB7127/MB7128		
R_1	R_2	C_L
300Ω	600Ω	30 pF

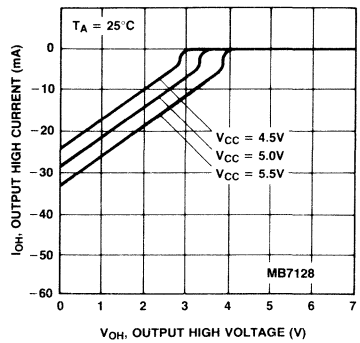


Typical Characteristics Curves

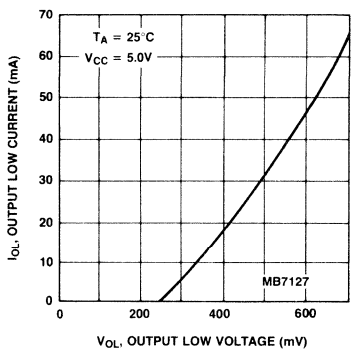
I_{IN} Input Current vs. V_{IN} Input Voltage



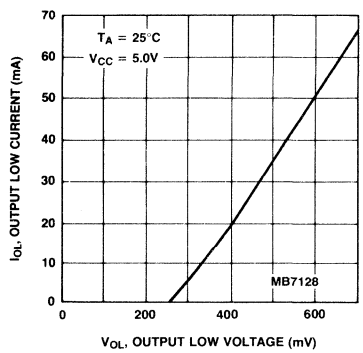
I_{OH} Output High Current vs. V_{OH} Output High Voltage



I_{OL} Output Low Current vs. V_{OL} Output Low Voltage

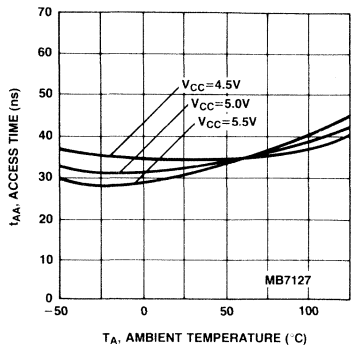


I_{OL} Output Low Current vs. V_{OL} Output Low Voltage

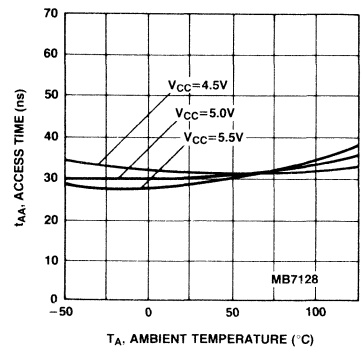


Typical Characteristics Curves
(Continued)

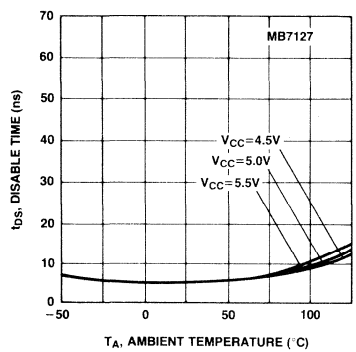
t_{AA} Access Time vs. Ambient Temperature



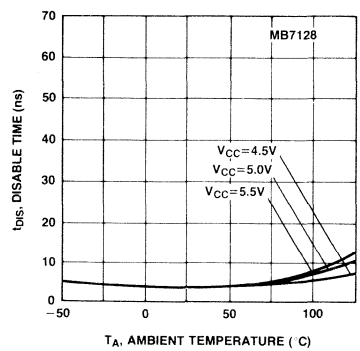
t_{AA} Access Time vs. Ambient Temperature



t_{DS} Disable Time vs. Ambient Temperature

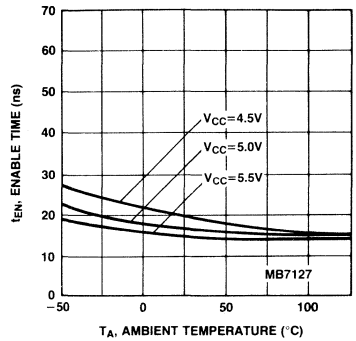


t_{DIS} Disable Time vs. Ambient Temperature

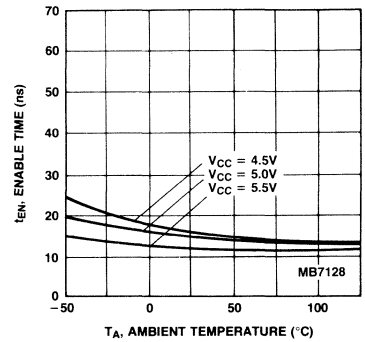


Typical Characteristics Curves
(Continued)

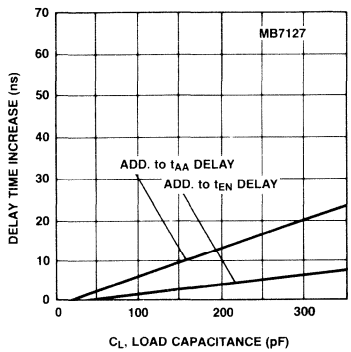
t_{EN} Enable Time vs. Ambient Temperature



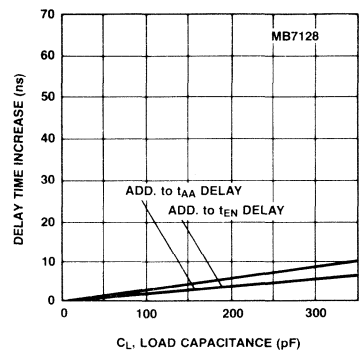
t_{EN} Enable Time vs. Ambient Temperature



Delay Time Increase vs. C_L Load Capacitance



Delay Time Increase vs. C_L Load Capacitance



MB7127/MB7128 Bit Map

	A_8 A_9 A_2 A_{10}
O_1	0 0 0 0 ~ 1 1 1 0
O_2	0 0 0 0 ~ 1 1 1 0
O_3	0 0 0 0 ~ 1 1 1 0
O_4	0 0 0 0 ~ 1 1 1 0

A_7	0	0
A_6	0	0
A_5	0	1
A_4	1	0
A_1	0	1
A_0	0	1
A_3	0	1

~

Multiplexer

A_8	A_9	A_2	A_{10}
0	0	0	0
0	0	0	1
0	0	1	1
0	0	1	0
0	1	1	0
0	1	1	1
0	1	0	1
0	1	0	0
1	0	1	0
1	0	1	1
1	0	0	1
1	0	0	0
1	1	0	0
1	1	0	1
1	1	1	1
1	1	1	0

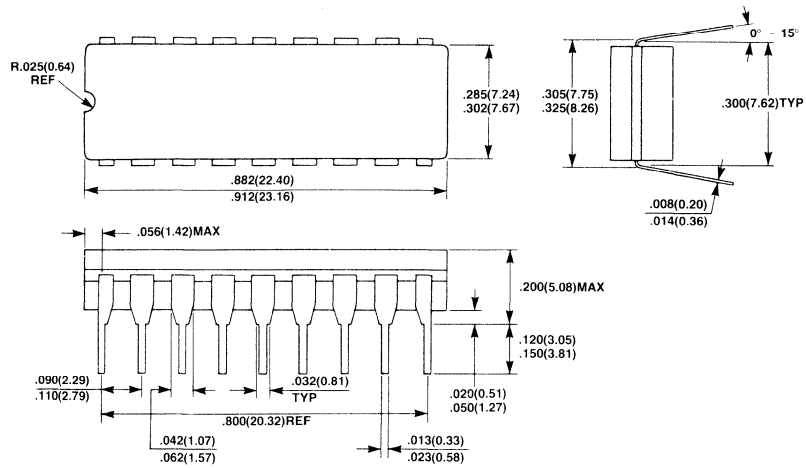
Decoder/Driver

A_7	01100110	01100110	01100110	01100110	01100110	01100110	01100110	01100110
A_6	00111100	11000011	11000011	00111100	11000011	00111100	00111100	11000011
A_5	00001111	00001111	00001111	00001111	00001111	00001111	00001111	00001111
A_4	11111111	00000000	11111111	00000000	11111111	00000000	11111111	00000000
A_1	00000000	00000000	11111111	11111111	00000000	00000000	11111111	11111111
A_0	00000000	00000000	00000000	00000000	11111111	11111111	11111111	11111111
A_3	00000000	00000000	00000000	00000000	00000000	00000000	00000000	00000000

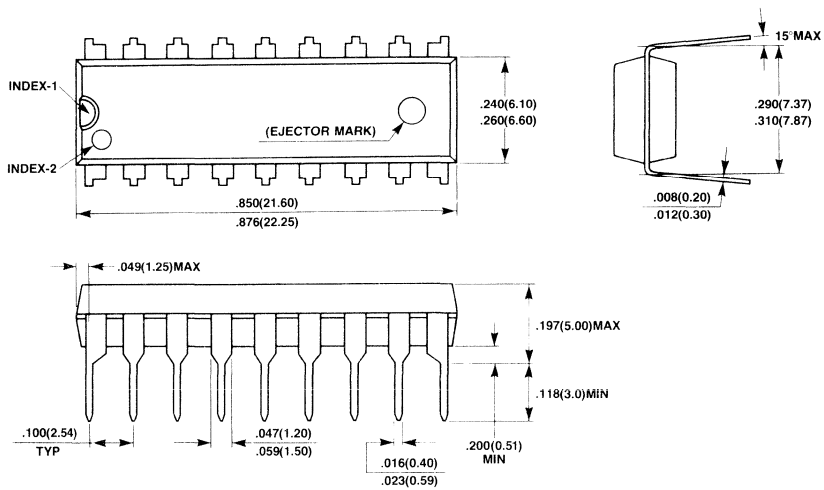
A_7	01100110	01100110	01100110	01100110	01100110	01100110	01100110	01100110
A_6	11000011	00111100	00111100	11000011	00111100	11000011	11000011	00111100
A_5	00001111	00001111	00001111	00001111	00001111	00001111	00001111	00001111
A_4	11111111	00000000	11111111	00000000	11111111	00000000	11111111	00000000
A_1	00000000	00000000	11111111	11111111	00000000	00000000	11111111	11111111
A_0	00000000	00000000	00000000	00000000	11111111	11111111	11111111	11111111
A_3	11111111	11111111	11111111	11111111	11111111	11111111	11111111	11111111

Package Dimensions
Dimensions in inches
(millimeters)

18-Lead Ceramic (CERDIP) Dual In-Line Package
(Case No.: DIP-18C-C01)

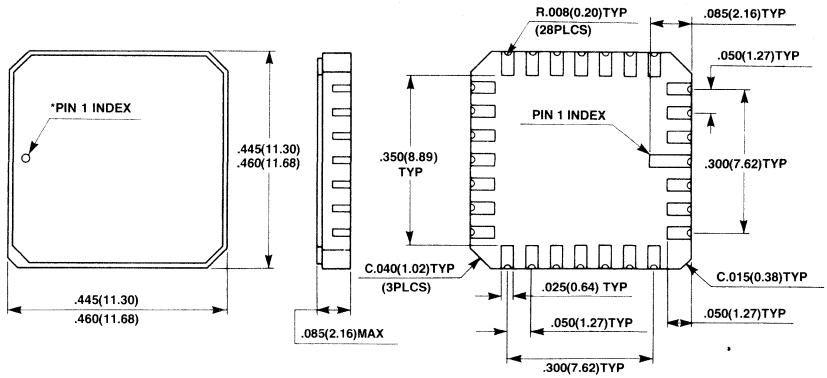


18-Lead Plastic Dual In-Line Package
(Case No.: DIP-18P-M02)



Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

28-Pad Ceramic (Metal Seal) Leadless Chip Carrier
(Case No.: LCC-28C-A01)



FUJITSU

MB7128E-W
High Speed Schottky TTL 8,192-Bit PROM

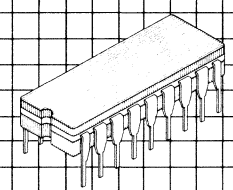
Description

The Fujitsu MB7128E-W is a high speed Schottky TTL electrically field programmable read only memory. With three-state outputs on the MB7128E-W, memory expansion is simple.

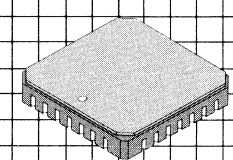
The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP™ (Diffused Eutectic Aluminum Process) during a simple programming procedure.

The sophisticated passive isolation termed IOP (Isolation by Oxide and Poly-silicon) with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.



CERDIP Package
DIP-18C-C01



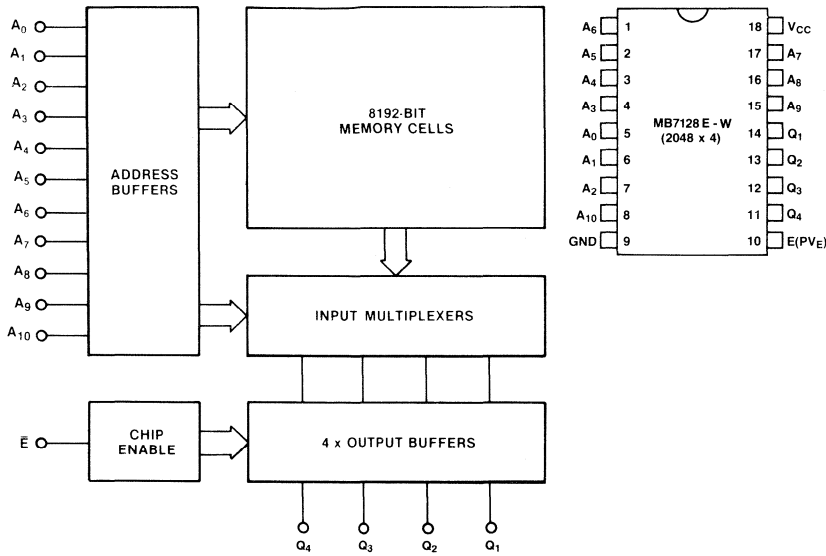
Leadless Chip Carrier
LCC-28C-A01

Features

- **Extended temperature ranges: −55°C to +125°C**
- **Organization: 2,048 words x 4-bits**
- **TTL compatible input/output**
- **Fast access time: 55 ns max. 30 ns typ.**
- **Single +5V supply voltage**
- **Proven high programmability and reliability of DEAP™ (Diffused Eutectic Aluminum Process) PROM**
- **Simplified, low power programming**
- **Low current PNP inputs**
- **MB7128E-W: Three-state outputs**
- **Chip enable inputs for easy memory expansion**
- **Standard 18-pin DIP package**
- **Also available in 28-pad LCC**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

MB7128E-W Block Diagram and Pin Assignment



Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Power supply voltage	V_{CC}	−0.5 to +7.0	V
Power supply voltage (during programming)	V_{CC}	−0.5 to +7.5	V
Input voltage	V_{IN}	−1.5 to 5.5	V
Input voltage (during programming)	V_{IPRG}	22.5	V
Output voltage (during programming)	V_{OPRG}	−0.5 to +22.5	V
Input current	I_{IN}	−20	mA
Input current (during programming)	I_{IPRG}	+270	mA
Output current	I_{OUT}	+100	mA
Output current (during programming)	I_{OPRG}	+150	mA
Storage temperature	T_{STG}	−65 to +150	°C
Output voltage	V_{OUT}	−0.5 to $+V_{CC}$	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.50	5.0	5.50	V
Input low voltage	V_{IL}	0.0		0.8	V
Input high voltage	V_{IH}	2.0		V_{CC}	V
Ambient temperature	T_A	−55		+125	°C

Capacitance
(f = 1 MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			10	pF
Output capacitance	C_O			15	pF

DC Characteristics
(Full guaranteed operating ranges unless otherwise noted.)

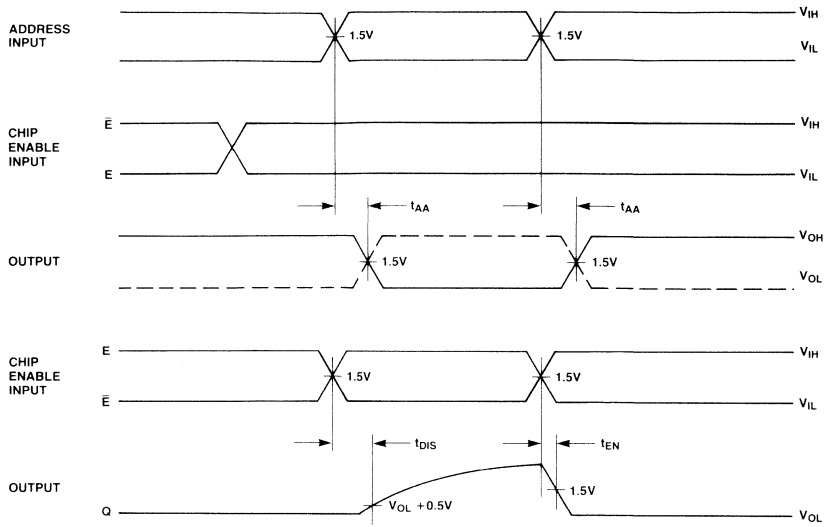
Parameter	Symbol	Min	Typ	Max	Unit
Input leakage current (V_{IH} = 5.5)	I_R			40	μA
Input load current (V_{IL} = 0.45V)	I_F			−250	μA
Output low voltage (I_{OL} = 16 mA)	V_{OL}			0.50	V
Output leakage current (V_O = 2.4V, chip disabled)	I_{OIH}			40	μA
Output leakage current (V_O = 0.45V, chip disabled)	I_{OIL}			−40	μA
Input clamp voltage (I_{In} = −18 mA)	V_{IC}			−1.2	V
Power supply current (V_{IN} = OPEN or GND)	I_{CC}		110	155	mA
Output high voltage (I_O = −2.4 mA)	V_{OH} *1	2.4			V
Output short circuit current (V_O = GND)	I_{OS} *1	−15		−60	mA

Note: *1 Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled (V_{CE} = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

AC Characteristics
(Full guaranteed operating ranges unless otherwise noted.)

Parameter	Symbol	Typ	Max	Unit
Address access time	t_{AA}	30	55	ns
Output disable time	t_{DIS}		40	ns
Output enable time	t_{EN}		40	ns

Operation Timing Diagram



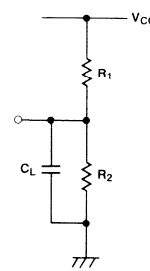
NOTE: OUTPUT DISABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO REACH A HIGH RESISTANCE STATE WHEN THE CHIP ENABLE IS DISABLED. OUTPUT ENABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO BECOME ACTIVE WHEN THE CHIP ENABLE IS ENABLED. THE HIGH RESISTANCE STATE IS DEFINED AS A POINT ON THE OUTPUT WAVEFORM EQUAL TO A ΔV OF 0.5V FROM THE ACTIVE OUTPUT LEVEL.

AC Test Conditions

Input Conditions

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5 ns from 1V to 2V
Frequency ..... 1 MHz

MB7128E-W		
R_1	R_2	C_L
300Ω	600Ω	30 pF



Input/Output Circuit Information

Input

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of the input circuit improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

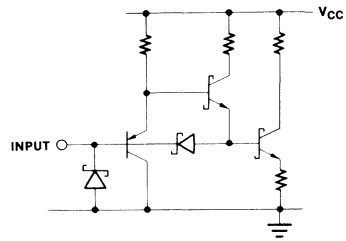
Three-State Output

A "three-state" output is a logic element which has three distinct output states of LOW, HIGH, and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line drive capacity), plus the ability to connect to bus-organized systems.

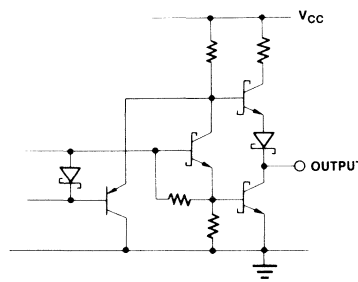
In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor is provided in the output circuit to decrease load on the Chip Enable circuit.

MB7128E-W Input Circuit

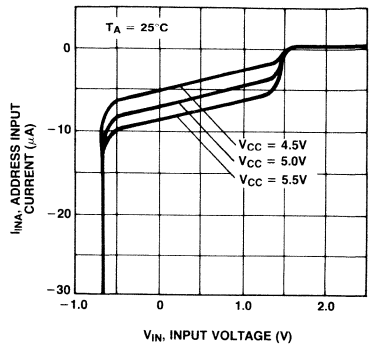


MB7128E-W Output Circuit

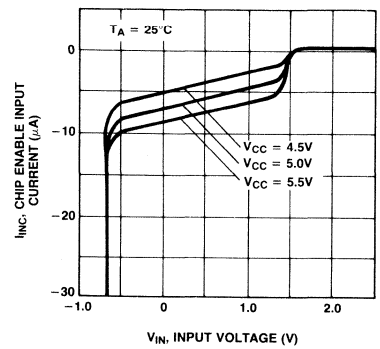


Typical Characteristics Curves

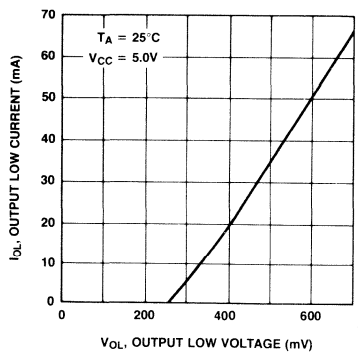
I_{INA} Input Current vs. V_{IN} Input Voltage



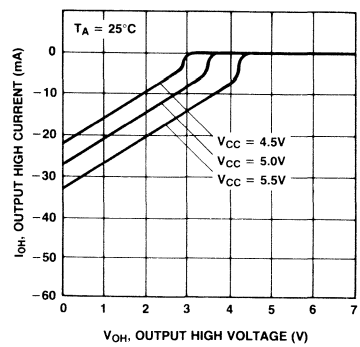
I_{INC} Input Current vs. V_{IN} Input Voltage



I_{OL} Output Low Current vs. V_{OL} Output Low Voltage

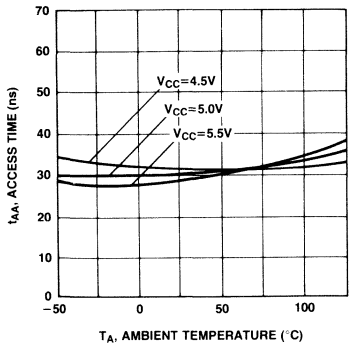


I_{OH} Output High Current vs. V_{OH} Output High Voltage

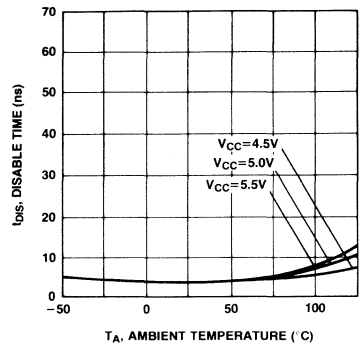


Typical Characteristics Curves
(Continued)

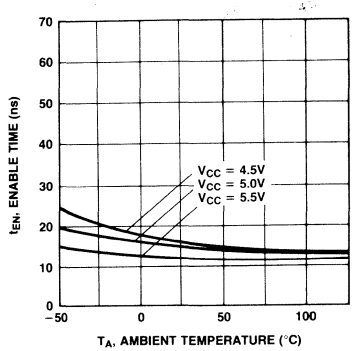
t_{AA} Access Time vs. T_A Ambient Temperature



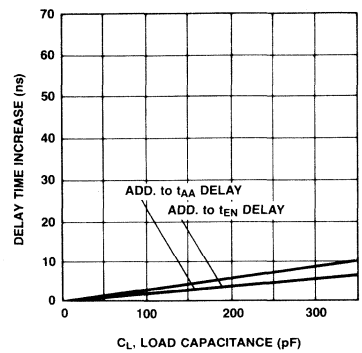
t_{DIS} Disable Time vs. T_A Ambient Temperature



t_{EN} Enable Time vs. T_A Ambient Temperature

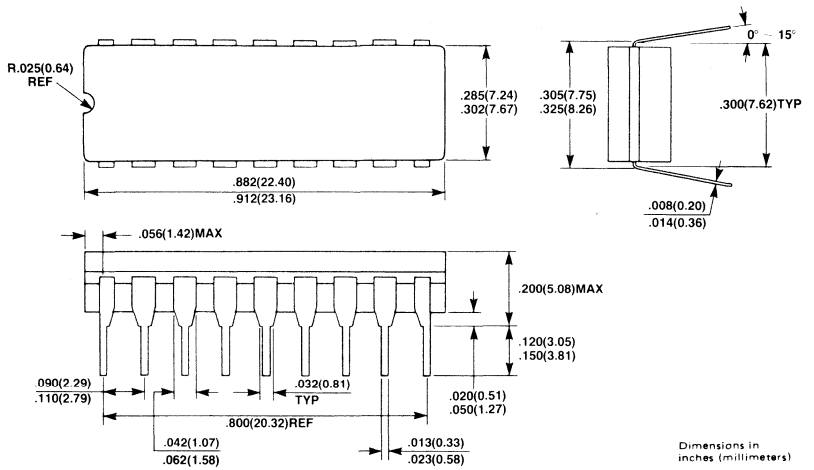


Delay Time Increase vs. C_L Load Capacitance

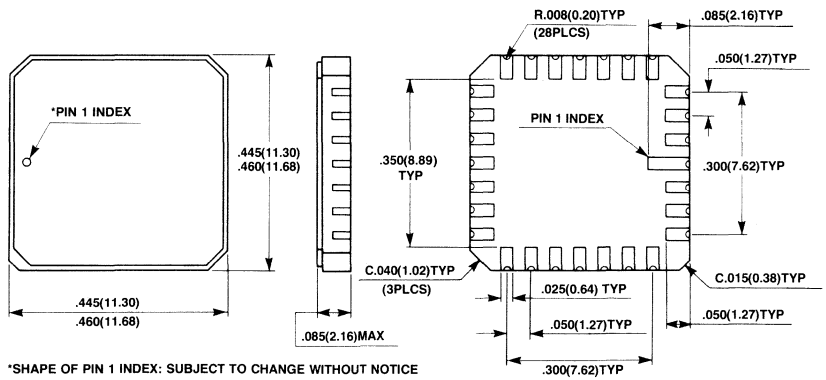


Package Dimensions
Dimensions in inches
(millimeters)

18-Lead Ceramic (CERDIP) Dual In-Line Package (Case No.: DIP-18C-C01)



28-Pad Ceramic (Metal Seal) Leadless Chip Carrier (Case No.: LCC-28C-A01)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

FUJITSU

■ MB7131E/H, MB7132E/H/Y, MB7131E-SK/H-SK, MB7132E-SK/H-SK/Y-SK

Programmable Schottky 8,192-Bit Read Only Memory

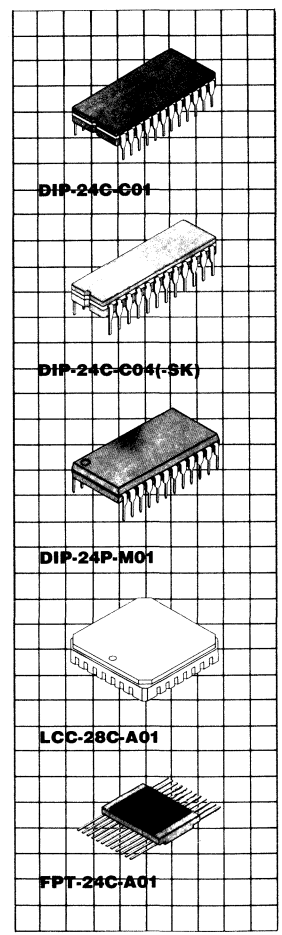
Description

The Fujitsu MB7131 and MB7132 are high speed Schottky TTL electrically field programmable read only memories organized as 1024 words by 8-bits. With uncommitted collector outputs provided on the MB7131 and three-state outputs on the MB7132, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP (Diffused Eutectic Aluminum Process) according to simple programming procedures.

The sophisticated passive isolation termed IOP (Isolation by Oxide and Poly-silicon) with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

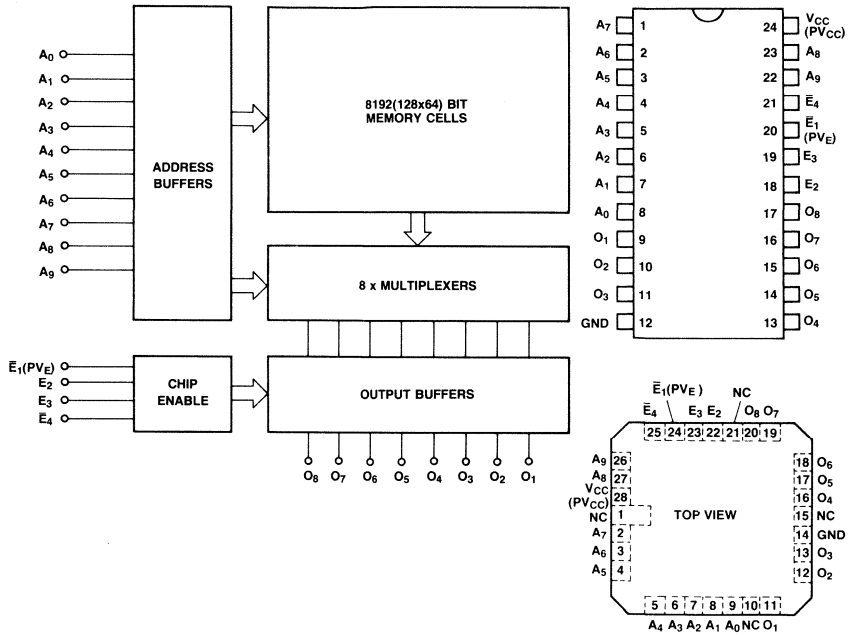


Features

- **Single +5V supply voltage**
- **1024 words x 8-bits organization, fully decoded**
- **Proven high programmability and reliability**
- **Programming by DEAP (Diffused Eutectic Aluminum Process)**
- **Simplified and lower power programming**
- **Low current PNP inputs**
- **AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques**
- **Fast access time, 30 ns typ**
  Y: 35 ns max. (MB7132)
  H: 45 ns max.
  E: 55 ns max.
- **TTL compatible inputs and outputs**
- **Open collector outputs (MB7131)**
- **3 state outputs (MB7132)**
- **Four chip enable leads for simplified memory expansion**
- **300/600 mil 24-pin DIP package**
- **JEDEC approved pin out**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB7131/7132 Block Diagram and Pin Assignments



Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Power supply voltage	V_{CC}	−0.5 to +7.0	V
Power supply voltage (during programming)	V_{CC}	−0.5 to +7.5	V
Input voltage	V_{IN}	−1.5 to 5.5	V
Input voltage (during programming)	V_{PRG}	22.5	V
Output voltage (during programming)	V_{PRG}	−0.5 to +22.5	V
Input current	I_{IN}	−20	mA
Input current (during programming)	I_{PRG}	+270	mA
Ouput current	I_{OUT}	+100	mA
Output current (during programming)	I_{PRG}	+150	mA
Storage temperature	T_{STG}	−65 to +150	°C
Output voltage	V_{OUT}	−0.5 to V_{CC}	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Guaranteed Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Input low voltage	V_{IL}	0		0.8	V
Input high voltage	V_{IH}	2.0		5.5	V
Ambient temperature	T_A	0		75	°C

Capacitance
($f = 1$ MHz, $V_{CC} = +5V$, $V_{IN} = +2V$, $T_A = 25°C$)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			10	pF
Output capacitance	C_O			15	pF

DC Characteristics
(Full guaranteed operating conditions unless otherwise noted.)

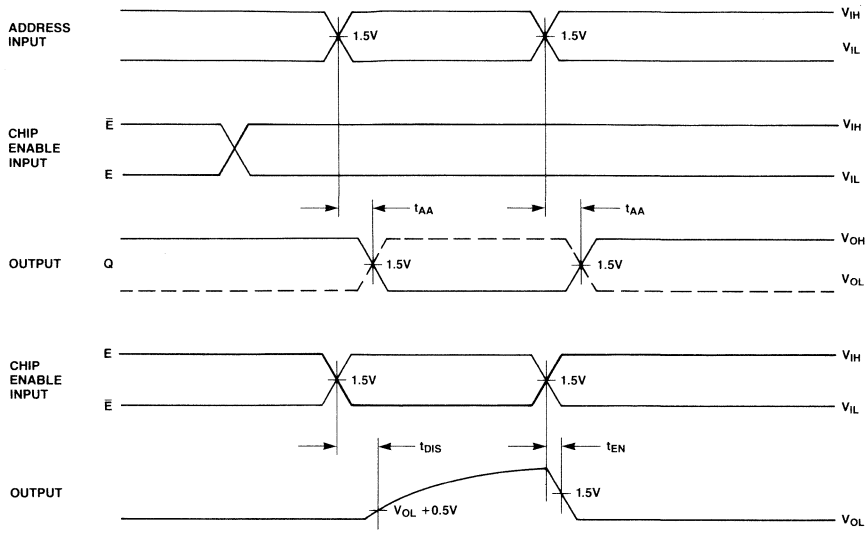
Parameter		Symbol	Min	Typ	Max	Unit
Input leakage current ($V_{IH} = 5.5V$)		I_R			40	μA
Input load current ($V_{IL} = 0.45V$)		I_F			−250	μA
Output low voltage ($I_{OL} = 10$ mA)		V_{OL}			0.45	V
Output low voltage ($I_{OL} = 16$ mA)		V_{OL}			0.50	V
Output leakage current ($V_O = 2.4V$, chip disabled)	MB7131	I_{OLK}			40	μA
Output leakage current ($V_O = 2.4V$, chip disabled)	MB7132	I_{OIH}			40	μA
Output leakage current ($V_O = 0.5V$, chip disabled)	MB7132	I_{OIL}			−40	μA
Input clamp voltage ($I_{IN} = -18$ mA)		V_{IC}			−1.2	V
Power supply current (V_{IN} = OPEN or GND)		I_{CC}		125	175	mA
Output high voltage ($I_O = -2.4$ mA)	MB7132	V_{OH}*1	2.4			V
Output short circuit current (V_O = GND)	MB7132	I_{OS}*1	−15		−60	mA

Note: *1 Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{ICE} = 0.4V$, $V_{ICE} = 2.4V$) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

AC Characteristics
(Full guaranteed operating conditions unless otherwise noted.)

		E		H		MB7132Y/-SK		
Parameter	Symbol	Typ	Max	Typ	Max	Typ	Max	Unit
Access time (via address input)	t_{AA}	30	55	30	45	26	35	ns
Output disable time	t_{DIS}		40		30		25	ns
Output enable time	t_{EN}		40		30		25	ns

Operation Timing Diagram

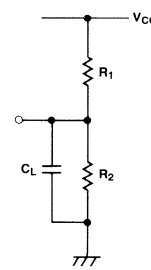


NOTE: OUTPUT DISABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO REACH A HIGH RESISTANCE STATE WHEN THE CHIP ENABLE IS TAKEN HIGH. OUTPUT ENABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO BECOME ACTIVE WHEN THE CHIP ENABLE IS TAKEN LOW. THE HIGH RESISTANCE STATE IS DEFINED AS A POINT ON THE OUTPUT WAVEFORM EQUAL TO A ΔV OF 0.5V FROM THE ACTIVE OUTPUT LEVEL.

AC Test Conditions

Input Conditions

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5 ns from 1V to 2V
Frequency ..... 1 MHz



TRUTH TABLE

	MB7131/MB7132		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30 pF
t_{DIS}	300Ω	600Ω	30 pF
t_{EN}	300Ω	600Ω	30 pF

Input/Output Circuit Information

Input

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

Open-Collector Output

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30 mA for the MB7132 (3-state) compared to 0 mA for the MB7131 (open-collector).

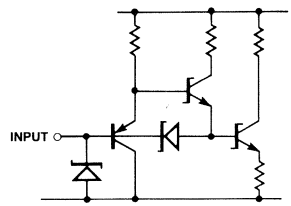
Three-State Output

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

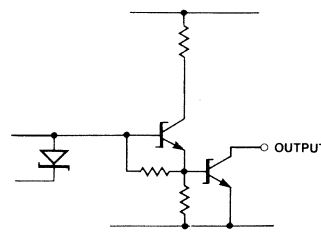
In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor provided in the output circuit is effective to decrease a load for the Chip Enable circuit.

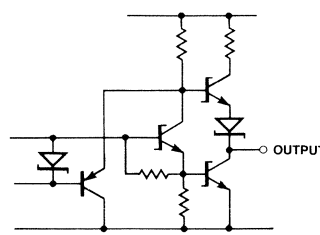
MB7131/7132 Input



MB7131 Output

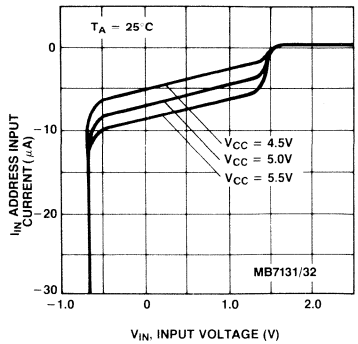


MB7132 Output

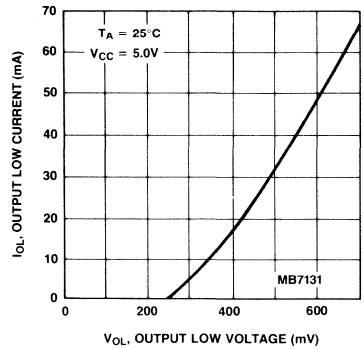


Typical Characteristics Curves

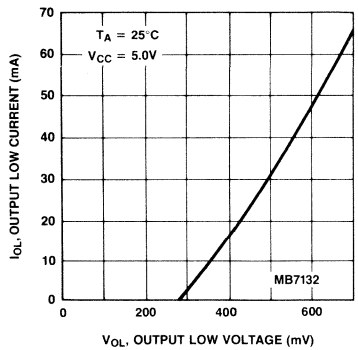
I_{IN} Input Current vs. V_{IN} Input Voltage



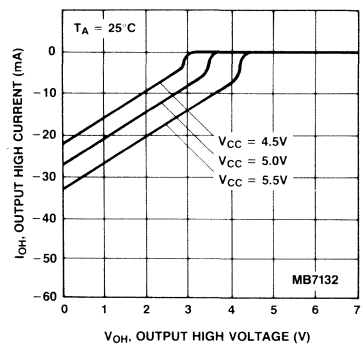
I_{OL} Output Low Current vs. V_{OL} Output Low Voltage



I_{OL} Output Low Current vs. V_{OL} Output Low Voltage

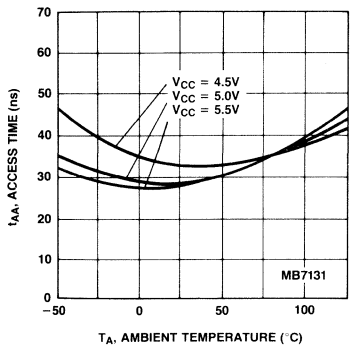


I_{OH} Output High Current vs. V_{OH} Output High Voltage

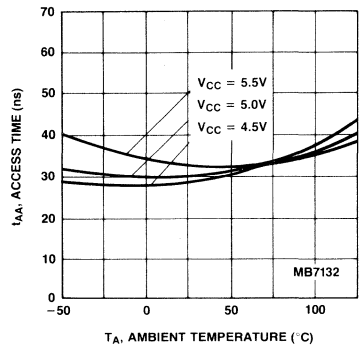


Typical Characteristics Curves
(Continued)

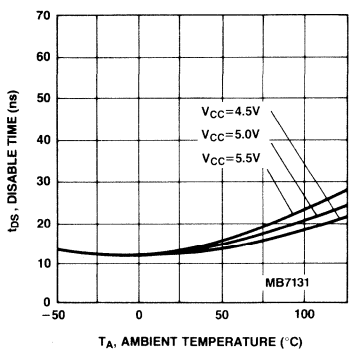
t_{AA} Access Time vs. Ambient Temperature



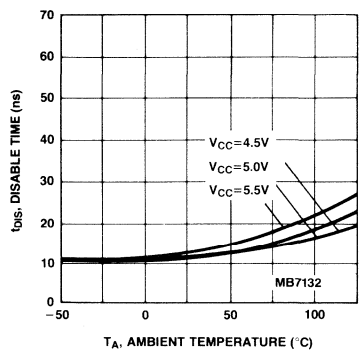
t_{AA} Access Time vs. Ambient Temperature



t_{DS} Disable Time vs. Ambient Temperature

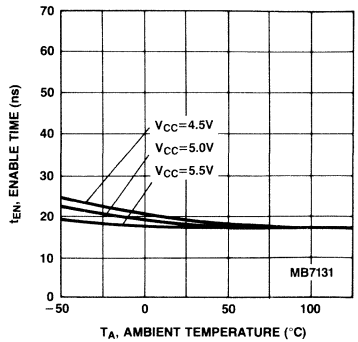


t_{DIS} Disable Time vs. Ambient Temperature

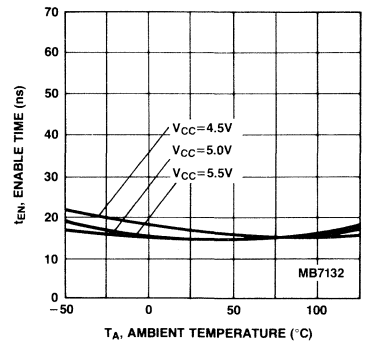


Typical Characteristics Curves
(Continued)

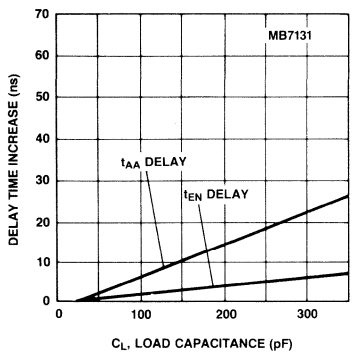
t_{EN} Enable Time vs. Ambient Temperature



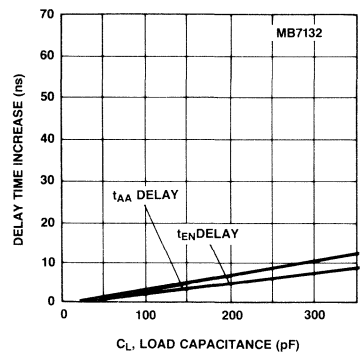
t_{EN} Enable Time vs. Ambient Temperature



Delay Time Increase vs. C_L Load Capacitance



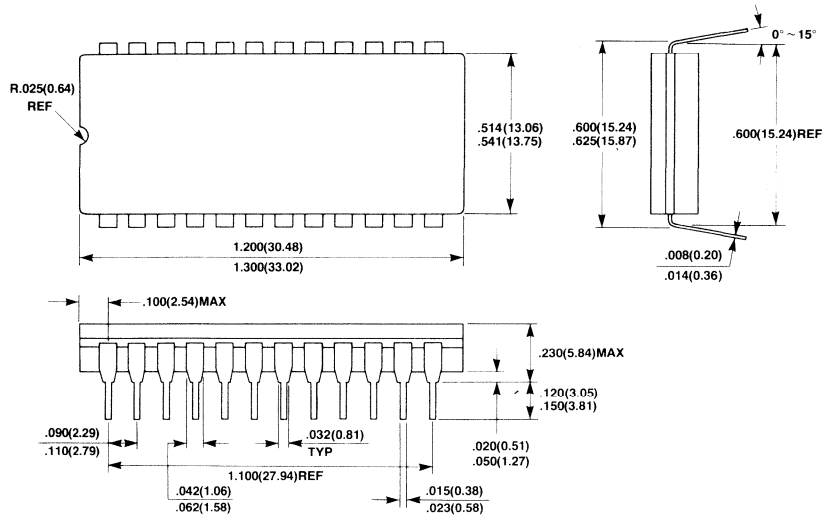
Delay Time Increase vs. C_L Load Capacitance



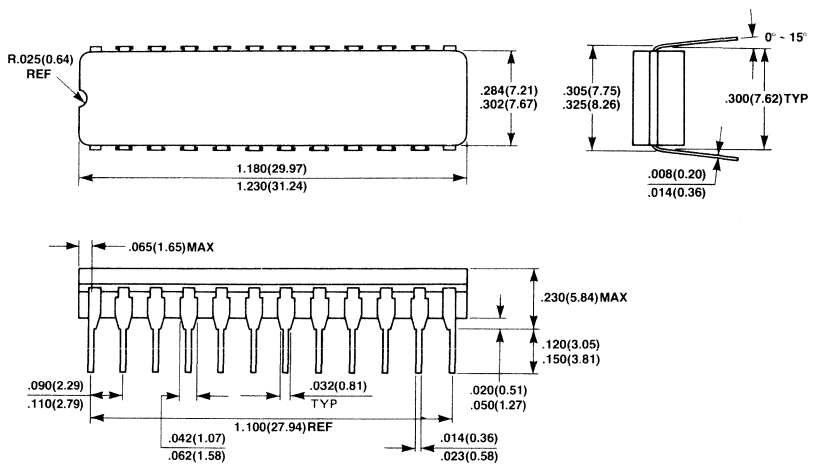
Package Dimensions

Dimensions in inches
(millimeters)

24-Lead Ceramic (CERDIP) Dual In-Line Package (Case No.: DIP-24C-C01)

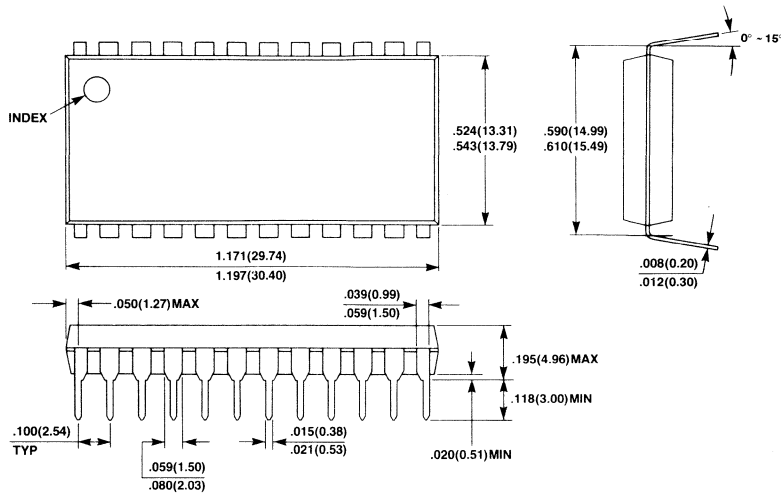


24-Lead Ceramic (CERDIP) Dual In-Line Package (-SK) (Case No.: DIP-24C-C04)

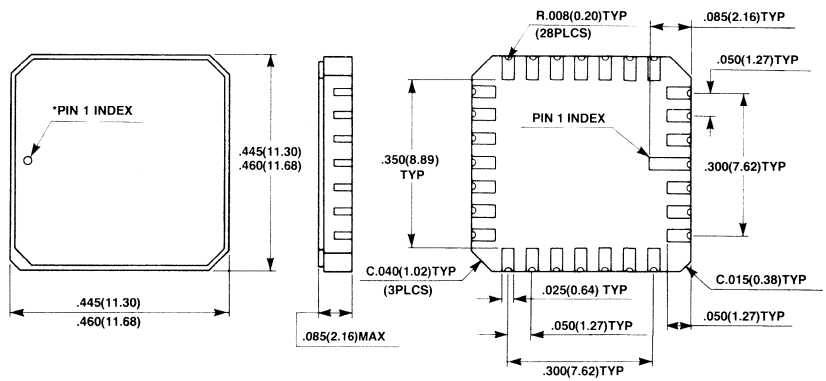


Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

24-Lead Plastic Dual In-Line Package
(Case No.: DIP-24P-M01)



28-Pad Ceramic (Metal Seal) Leadless Chip Carrier
(Case No.: LCC-28C-A01)

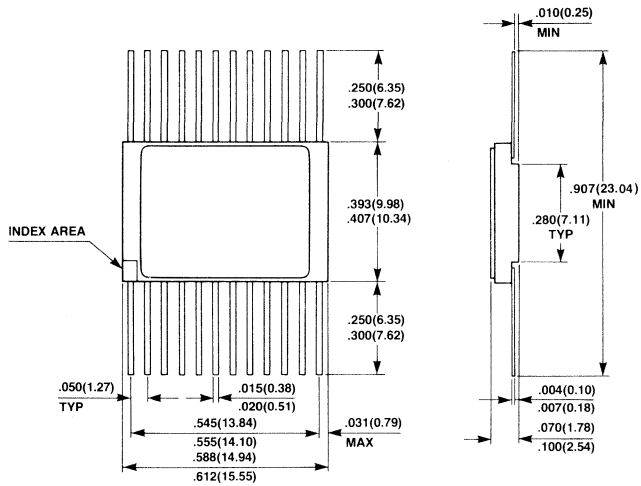


Dimensions in inches
(millimeters)

*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

24-Lead Ceramic (Metal Seal) Flat Package
(Case No.: FPT-24C-A01)



FUJITSU

MB7133E/H, MB7134E/H/Y

Programmable Schottky 16,384-Bit Read Only Memory

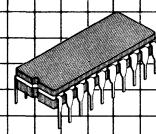
Description

The Fujitsu MB7133 and MB7134 are high speed Schottky TTL electrically field programmable read only memories organized as 4096 words by 4-bits. With uncommitted collector output provided on the MB7133 and three-state outputs on the MB7134, memory expansion is simple.

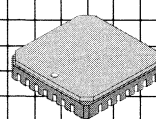
The memory is fabricated with all logic "zeros" (positive logic). Logic Level "ones" can be programmed by the highly reliable DEAP (Diffused Eutectic Aluminum Process) according to simple programming procedures.

The sophisticated passive isolation termed IOP (Isolation by Oxide and Polysilicon) with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

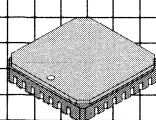
The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.



DIP-20C-C03



LCC-28C-A01



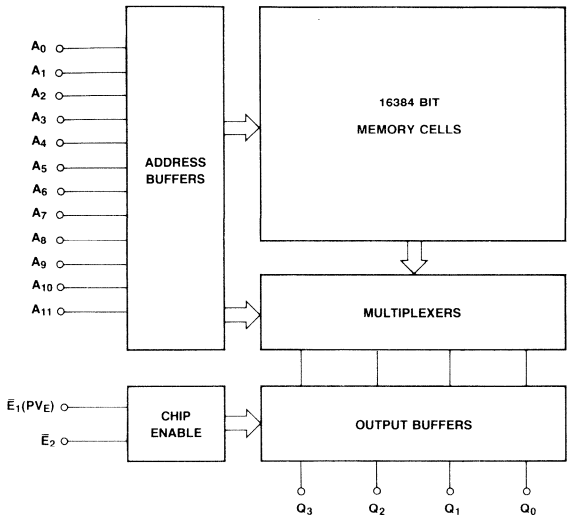
LCC-28C-A02

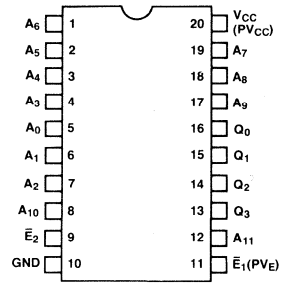
Features

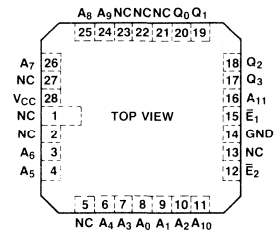
- **Single +5V supply voltage**
- **4096 words x 4-bits organization, fully decoded**
- **Proven high programmability and reliability**
- **Programming by DEAP (diffused eutectic aluminum process)**
- **Simplified, low power programming**
- **Low current PNP inputs**
- **AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques**
- **Fast access time, 35 ns typ**
  MB7134Y: 35 ns max.
  H: 45 ns max.
  E: 55 ns max.
- **TTL compatible inputs and outputs**
- **Open collector (MB7133)**
- **3-state outputs (MB7134)**
- **Two chip enable inputs for simplified memory expansion**
- **300 mil 20-pin DIP package**

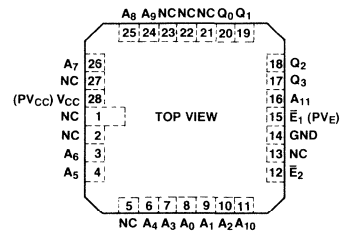
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB7134 Block Diagram and Pin Assignments









Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Power supply voltage	V_{CC}	−0.5 to +7.0	V
Power supply voltage (during programming)	V_{CC}	−0.5 to +7.5	V
Input voltage	V_{IN}	−1.5 to 5.5	V
Input voltage (during programming)	V_{PRG}	22.5	V
Output voltage (during programming)	V_{PRG}	−0.5 to +22.5	V
Input current	I_{IN}	−20	mA
Input current (during programming)	I_{PRG}	+270	mA
Output current	I_{OUT}	+100	mA
Output current (during programming)	I_{PRG}	+150	mA
Storage temperature	T_{STG}	−65 to +150	°C
Output voltage	V_{OUT}	−0.5 to V_{CC}	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Guaranteed Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Input low voltage	V_{IL}	0		0.8	V
Input high voltage	V_{IH}	2.0		5.5	V
Ambient temperature	T_A	0		75	°C

Capacitance
($f = 1$ MHz, $V_{CC} = +5V$, $V_{IN} = +2V$, $T_A = 25°C$)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			10	pF
Output capacitance	C_Q			15	pF

DC Characteristics
(Full guaranteed operating conditions unless otherwise noted.)

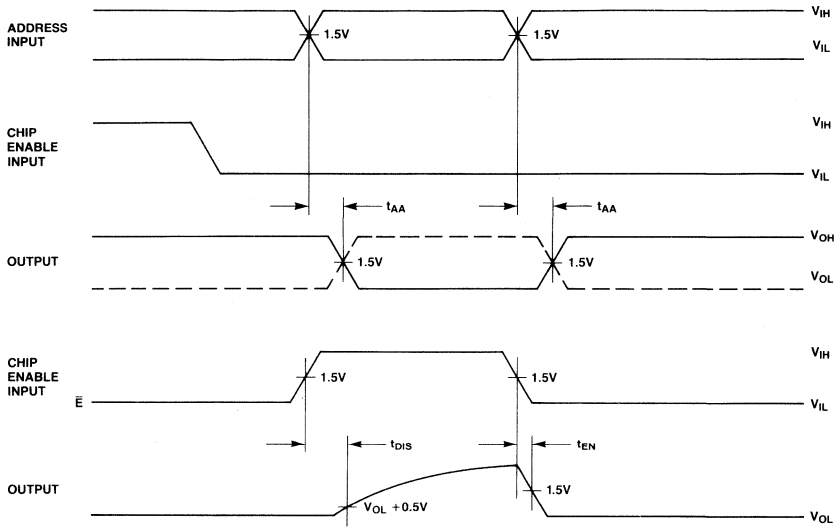
Parameter		Symbol	Min	Typ	Max	Unit
Input leakage current ($V_{IH} = 5.5V$)		I_{R1}			40	μA
Input load current ($V_{IL} = 0.45V$)		I_F			−250	μA
Output low voltage ($I_{OL} = 10$ mA)		V_{OL}			0.45	V
Output low voltage ($I_{OL} = 16$ mA)		V_{OL}			0.50	V
Output leakage current ($V_O = 2.4V$, chip disabled)	MB7133	I_{OLK}			40	μA
	MB7134	I_{OIH}			40	μA
Output leakage current ($V_O = 0.45V$, chip disabled)	MB7134	I_{OIL}			−40	μA
Input clamp voltage ($I_{IN} = -18$ mA)		V_{IC}			−1.2	V
Power supply current (V_{IN} = OPEN or GND)		I_{CC}		120	170	mA
Output high voltage ($I_O = -2.4$ mA)	MB7134	V_{OH} *1	2.4			V
Output short circuit current (V_O = GND)	MB7134	I_{OS} *1	−15		−60	mA

Note: *1 Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{\overline{IE}} = 0.4V$) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

AC Characteristics
(Full guaranteed operating conditions unless otherwise noted.)

Parameter	Symbol	MB7133/7134E Typ	MB7133/7134E Max	MB7133/7134H Typ	MB7133/7134H Max	MB7134Y Typ	MB7134Y Max	Unit
Access time (via address input)	t_{AA}	35	55	35	45	28	35	ns
Output disable time	t_{DIS}		40		40		30	ns
Output enable time	t_{EN}		40		40		30	ns

Operation Timing Diagram

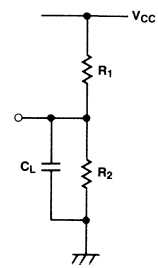


NOTE: OUTPUT DISABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO REACH A HIGH RESISTANCE STATE WHEN THE CHIP ENABLE IS DISABLED. OUTPUT ENABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO BECOME ACTIVE WHEN THE CHIP ENABLE IS ENABLED. THE HIGH RESISTANCE STATE IS DEFINED AS A POINT ON THE OUTPUT WAVEFORM EQUAL TO A ΔV OF 0.5V FROM THE ACTIVE OUTPUT LEVEL.

AC Test Conditions

Input Conditions

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5 ns from 1V to 2V
Frequency ..... 1 MHz



TRUTH TABLE

	MB7133/MB7134		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30 pF
t_{DIS}	300Ω	600Ω	30 pF
t_{EN}	300Ω	600Ω	30 pF

Input/Output Circuit Information

Input

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of the input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

Open Collector Output

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30 mA for the MB7134 (3-state) compared to 0 mA for the MB7133 (open collector).

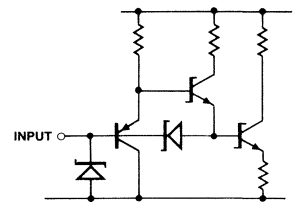
Three-State Output

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

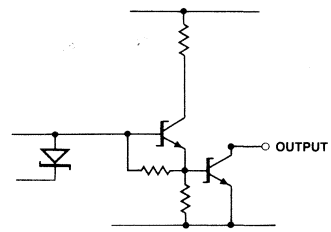
In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the systems designer should consider these factors to ensure that this condition does not exist.

In the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor provided in the output circuit is effective to decrease a load for the Chip Enable circuit.

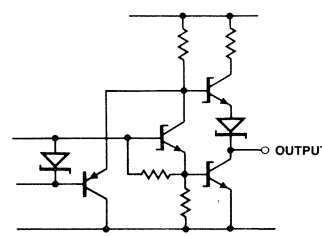
MB7133/MB7134 Input



MB7133 Output

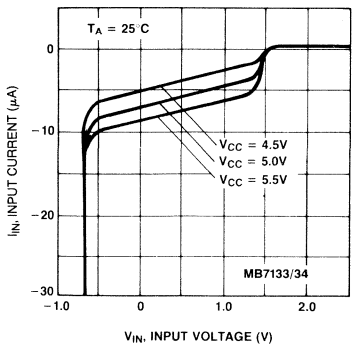


MB7134 Output

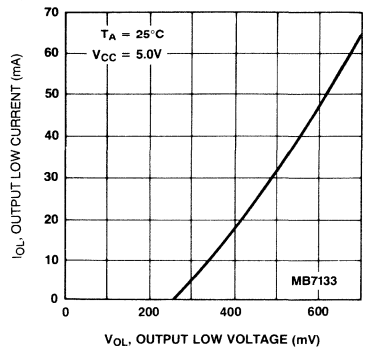


Typical Characteristics Curves

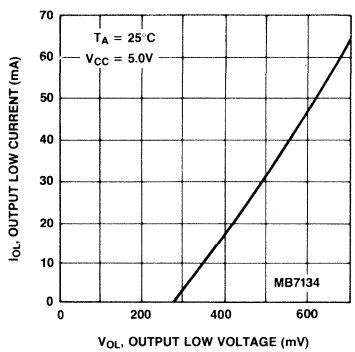
I_{IN} Input Current vs. V_{IN} Input Voltage



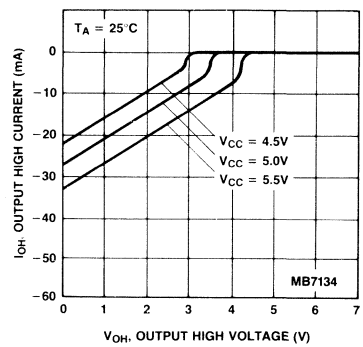
I_{OL} Output Low Current vs. V_{OL} Output Low Voltage



I_{OL} Output Low Current vs. V_{OL} Output Low Voltage

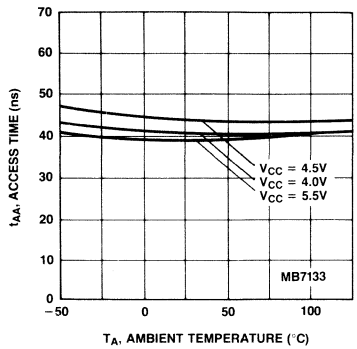


I_{OH} Output High Current vs. V_{OH} Output High Voltage

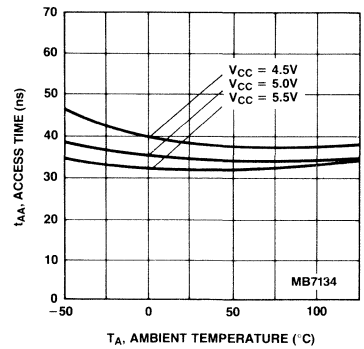


Typical Characteristics Curves
(Continued)

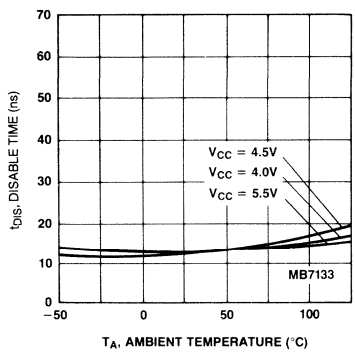
t_{AA} Access Time vs. Ambient Temperature



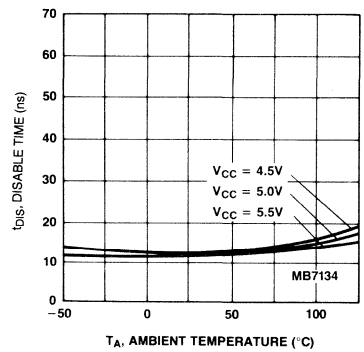
t_{AA} Access Time vs. Ambient Temperature



t_{DIS} Disable Time vs. Ambient Temperature

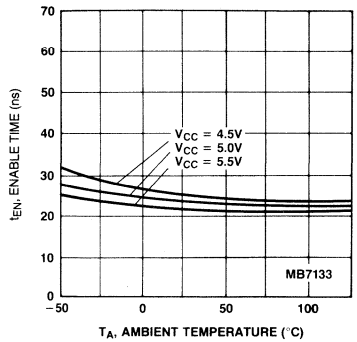


t_{DIS} Disable Time vs. Ambient Temperature

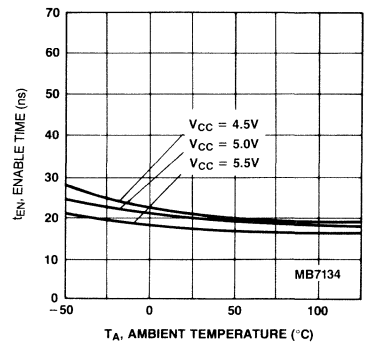


Typical Characteristics Curves
(Continued)

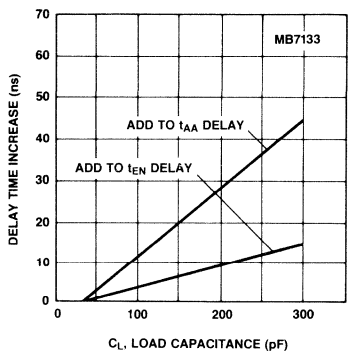
t_{EN} Enable Time vs. Ambient Temperature



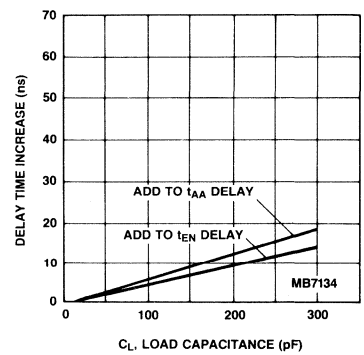
t_{EN} Enable Time vs. Ambient Temperature



Delay Time Increase vs. C_L Load Capacitance

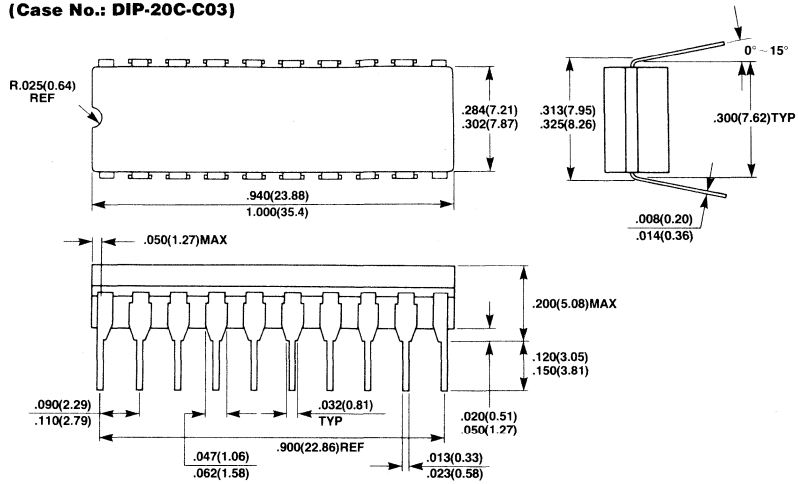


Delay Time Increase vs. C_L Load Capacitance

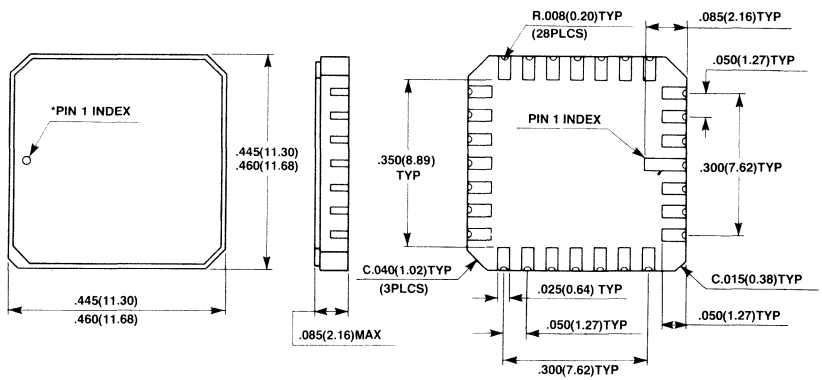


Package Dimensions
Dimensions in inches
(millimeter)

20-Lead Ceramic (CERDIP) Dual In-Line Package
(Case No.: DIP-20C-C03)

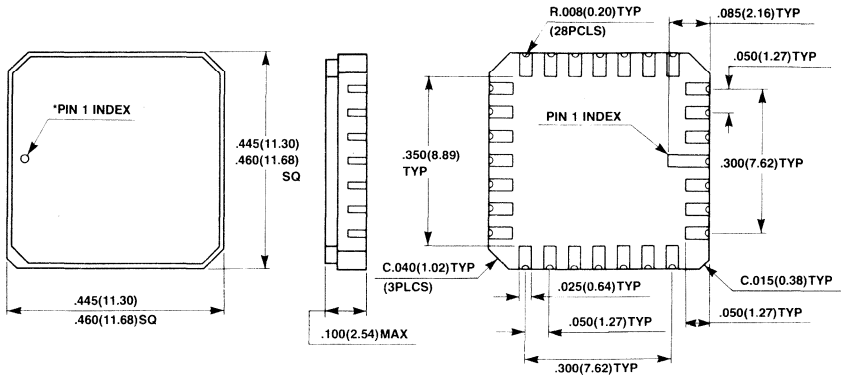


28-Pad Ceramic (Metal Seal) Leadless Chip Carrier
(Case No.: LCC-28C-A01)



Package Dimensions
(Continued)
Dimensions in inches
(millimeter)

28-Pad Ceramic (Metal Seal) LeadlessChip Carrier
(Case No.: LCC-28C-A02)



FUJITSU

MB7137E/H, MB7138E/H/Y, MB7137E-SK/H-SK, MB7138E-SK/H-SK/Y-SK

Programmable Schottky 16,384-Bit Read Only Memory

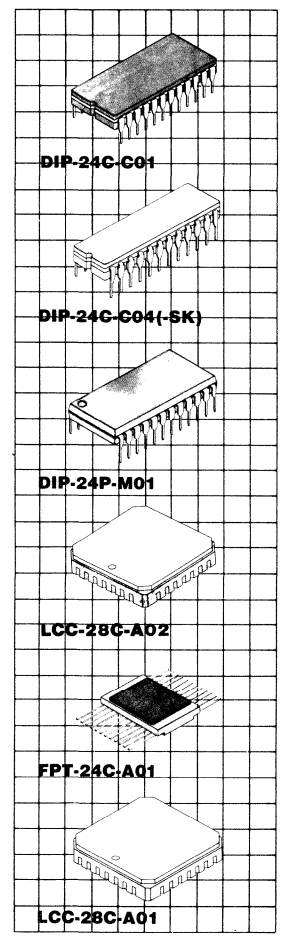
Description

The Fujitsu MB7137 and MB7138 are high speed Schottky TTL electrically field programmable read only memories organized as 2048 words by 8-bits. With uncommitted collector outputs provided on the MB7137 and three-state outputs on the MB7138, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP (Diffused Eutectic Aluminum Process) according to simple programming procedures.

The sophisticated passive isolation termed IOP (Isolation by Oxide and Polysilicon) with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.

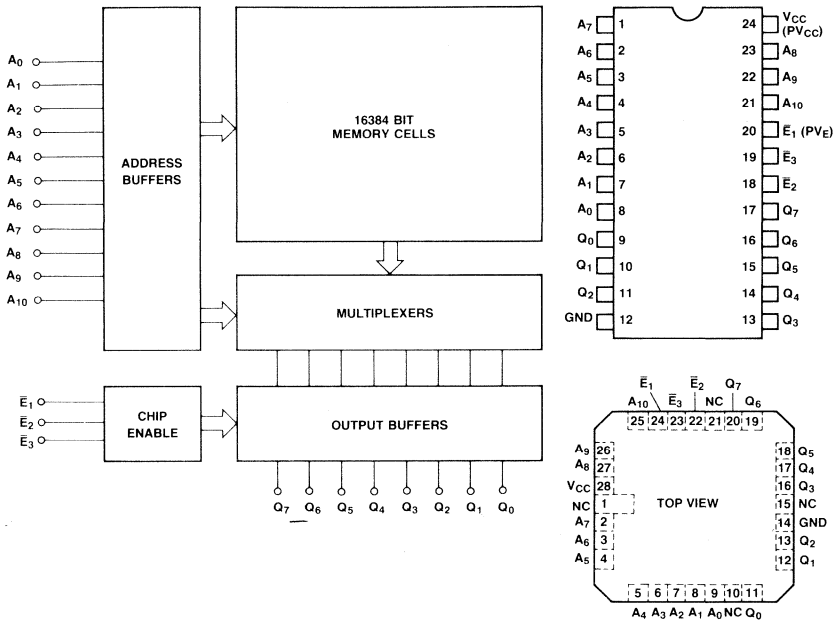


Features

- **Single +5V supply voltage**
- **2048 words x 8-bits organization, fully decoded**
- **Proven high programmability and reliability**
- **Programming by DEAP (Diffused Eutectic Aluminum Process)**
- **Simplified, low power programming**
- **Low current PNP inputs**
- **AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques**
- **Fast access time, 35 ns typ**
  Y: 35 ns max. (MB7138)
  H: 45 ns max.
  E: 55 ns max.
- **TTL compatible inputs and outputs**
- **Open collector outputs (MB7137)**
- **3 state outputs (MB7138)**
- **Three chip enable leads for simplified memory expansion**
- **300/600 mil 24-pin DIP package**
- **JEDEC approved pin out**
- **24-lead flatpack**
- **28-pad LCC**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB7137/7138 Block Diagram and Pin Assignments



Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Power supply voltage	V_{CC}	−0.5 to +7.0	V
Power supply voltage (during programming)	V_{CC}	−0.5 to +7.5	V
Input voltage	V_{IN}	−1.5 to 5.5	V
Input voltage (during programming)	V_{PRG}	22.5	V
Output voltage (during programming)	V_{PRG}	−0.5 to +22.5	V
Input current	I_{IN}	−20	mA
Input current (during programming)	I_{PRG}	+270	mA
Output Current	I_{OUT}	+100	mA
Output Current (during programming)	I_{PRG}	+150	mA
Storage temperature	t_{STG}	−65 to +150	°C
Output voltage	V_{OUT}	−0.5 to V_{CC}	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Guaranteed Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Input low voltage	V_{IL}	0		0.8	V
Input high voltage	V_{IH}	2.0		5.5	V
Ambient temperature	T_A	0		75	°C

Capacitance

(f = 1 MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			10	pF
Output capacitance	C_O			15	pF

DC Characteristics

(Full guaranteed operating conditions unless otherwise noted.)

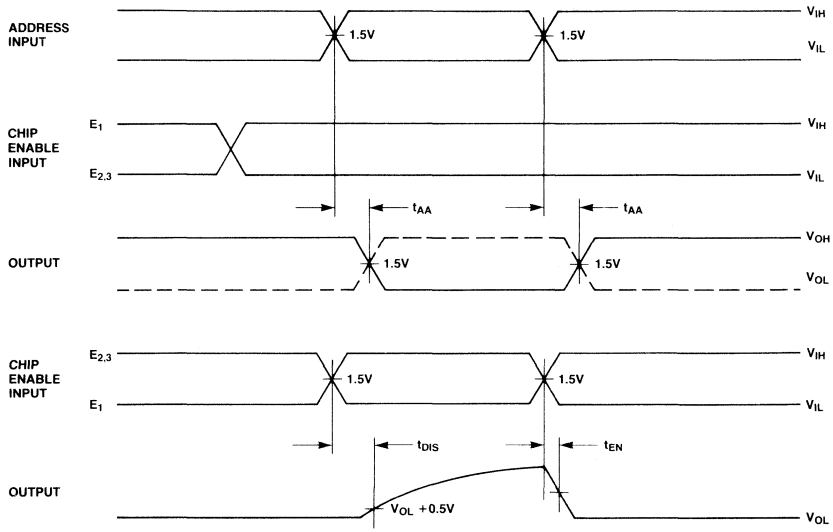
Parameter		Symbol	Min	Typ	Max	Unit
Input leakage current (V_{IH} = 5.5V)		I_{R1}			40	μA
Input load current (V_{IL} = 0.45V)		I_F			−250	μA
Output low voltage (I_{OL} = 10 mA)		V_{OL}			0.45	V
Output low voltage (I_{OL} = 16 mA)		V_{OL}			0.50	V
Output leakage current (V_O = 2.4V, chip disabled)	MB7137	I_{OLK}			40	μA
Output leakage current (V_O = 2.4V, chip disabled)	MB7138	I_{OIH}			40	μA
Output leakage current (V_O = 0.5V, chip disabled)	MB7138	I_{OIL}			−40	μA
Input clamp voltage (I_{IN} = −18 mA)		V_{IC}			−1.2	V
Power supply current (V_{IN} = OPEN or GND)		I_{CC}		130	180	mA
Output high voltage (I_O = −2.4 mA)	MB7138	V_{OH} *1	2.4			V
Output short circuit current (V_O = GND)	MB7138	I_{OS} *1	−15		−60	mA

AC Characteristics

(Full guaranteed operating conditions unless otherwise noted.)

		MB7137/7138E/-SK		MB7137/7138H/-SK		MB7138Y/-SK		
Parameter	Symbol	Typ	Max	Typ	Max	Typ	Max	Unit
Access time (via address input)	t_{AA}	35	55	35	45	28	35	ns
Output disable time	t_{DIS}		40		40		30	ns
Output enable time	t_{EN}		40		40		30	ns

Operation Timing Diagram

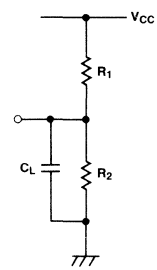


NOTE: OUTPUT DISABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO REACH A HIGH RESISTANCE STATE WHEN THE CHIP ENABLE IS DISABLED. OUTPUT ENABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO BECOME ACTIVE WHEN THE CHIP ENABLE IS ENABLED. THE HIGH RESISTANCE STATE IS DEFINED AS A POINT ON THE OUTPUT WAVEFORM EQUAL TO A ΔV OF 0.5V FROM THE ACTIVE OUTPUT LEVEL.

AC Test Conditions

Input Conditions

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5 ns from 1V to 2V
Frequency ..... 1 MHz



TRUTH TABLE

	MB7137/MB7138		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30 pF
t_{DIS}	300Ω	600Ω	30 pF
t_{EN}	300Ω	600Ω	30 pF

Input/Output Circuit Information

Input

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

Open-Collector Output

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB7138 (3-state) compared to OmA for the MB7137 (open-collector)

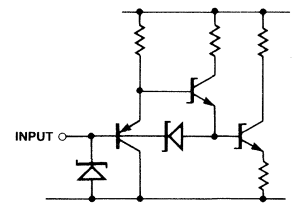
Three-State Output

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

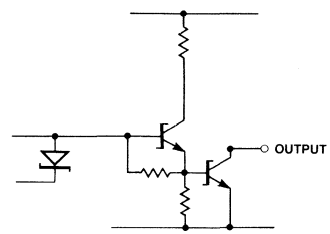
In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

In the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor provided in the output circuit is effective to decrease a load for the Chip Enable circuit.

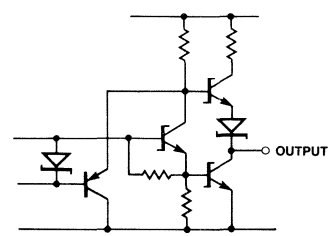
MB7137/7138 Input



MB7137 Output

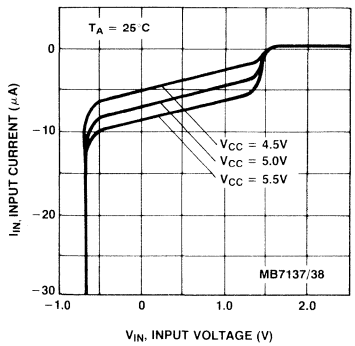


MB7138 Output

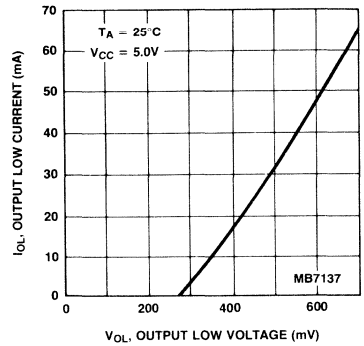


Typical Characteristics Curves

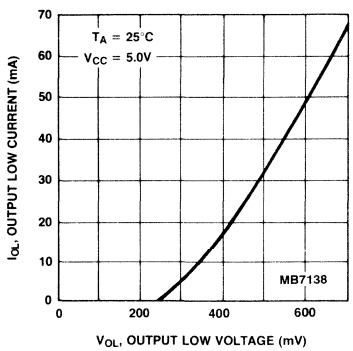
I_{IN} Input Current vs V_{IN} Input Voltage



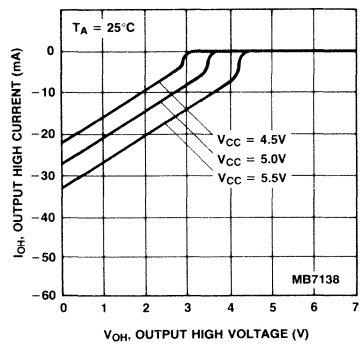
I_{OL} Output Low Current vs V_{OL} Output Low Voltage



I_{OL} Output Low Current vs V_{OL} Output Low Voltage

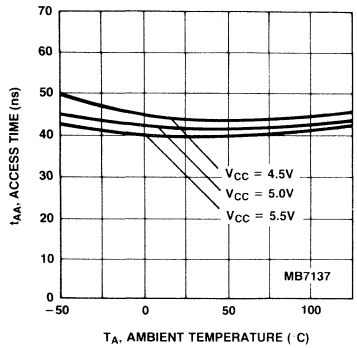


I_{OH} Output High Current vs V_{OH} Output High Voltage

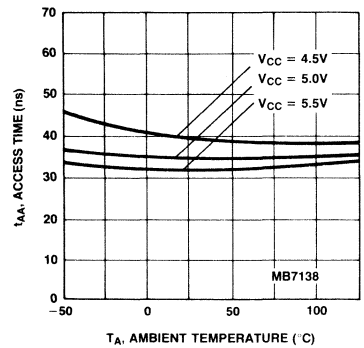


Typical Characteristics Curves
(Continued)

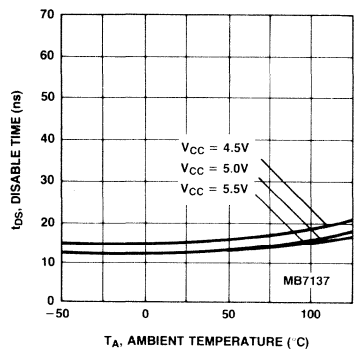
t_{AA} Access Time vs Ambient Temperature



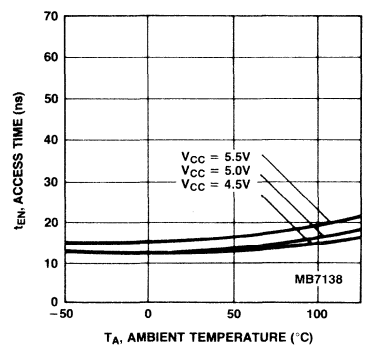
t_{AA} Access Time vs Ambient Temperature



t_{DS} Disable Time vs Ambient Temperature

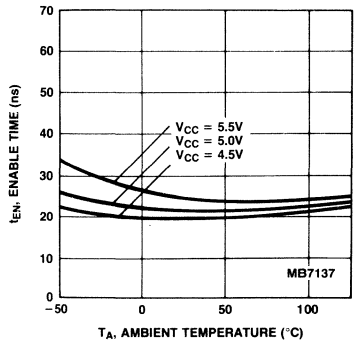


t_{DIS} Disable Time vs Ambient Temperature

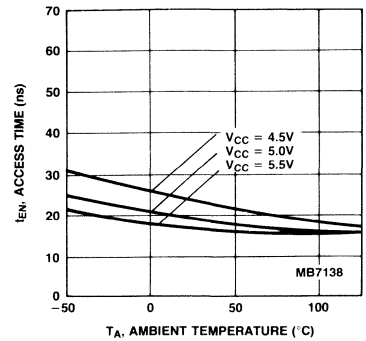


Typical Characteristics Curves
(Continued)

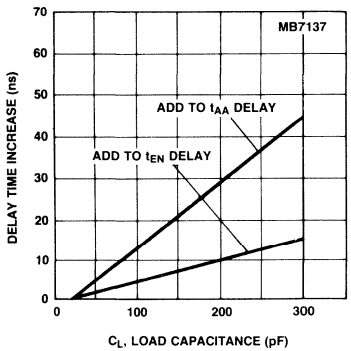
t_{EN} Enable Time vs Ambient Temperature



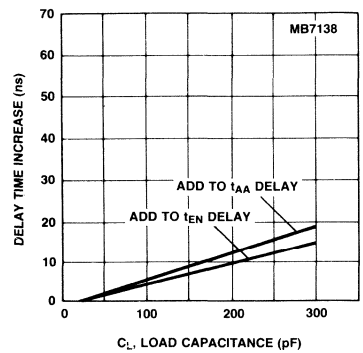
t_{EN} Access Time vs Ambient Temperature



Delay Time Increase vs C_L Load Capacitance

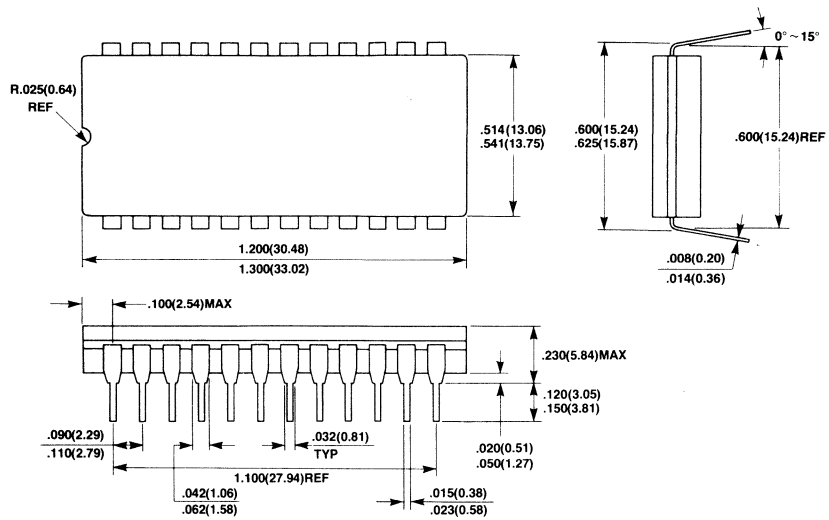


Delay Time Increase vs C_L Load Capacitance

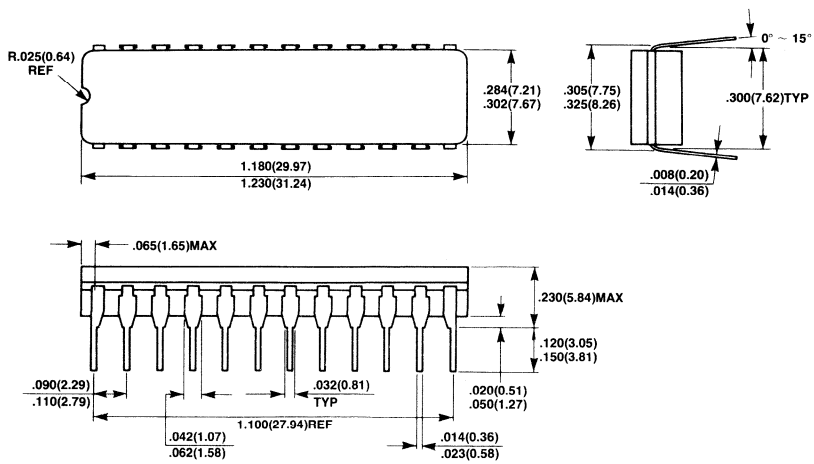


Package Dimensions
Dimensions in inches
(millimeter)

24-Lead Ceramic (CERDIP) Dual In-Line Package
(Case No.: DIP-24C-C01)

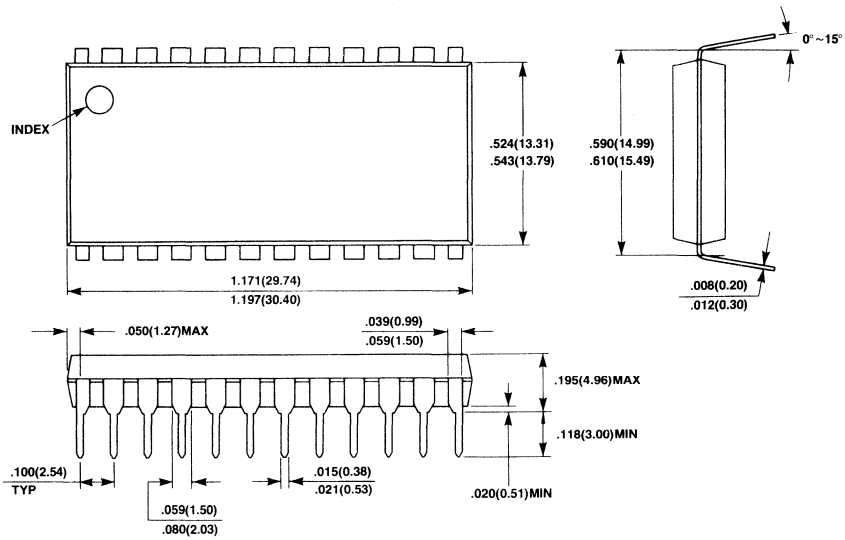


24-Lead Ceramic (CERDIP) Dual In-Line Package (-SK)
(Case No.: DIP-24C-C04)

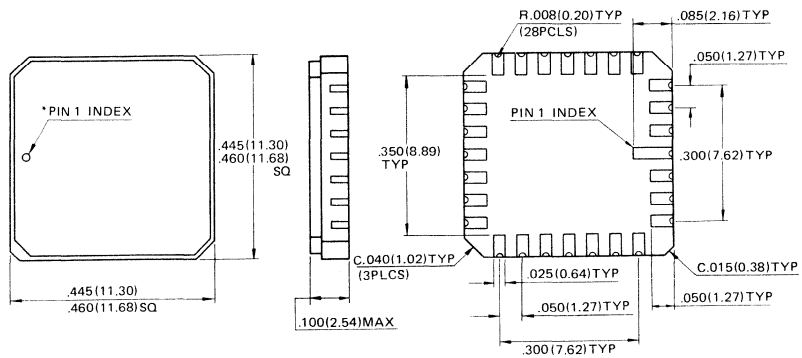


Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

24-Lead Plastic Dual In-Line Package
(Case No.: DIP-24P-M01)



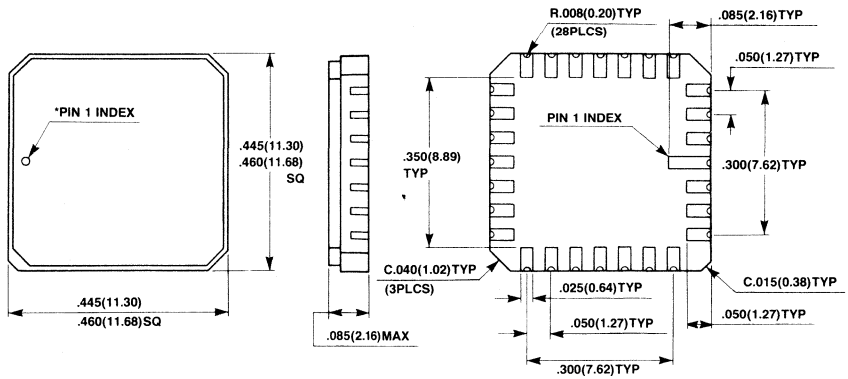
28-Pad Ceramic (Metal Seal) Leadless Chip Carrier
(Case No.: LCC-28C-A02)



*Shape of Pin 1 index : Subject to change without notice

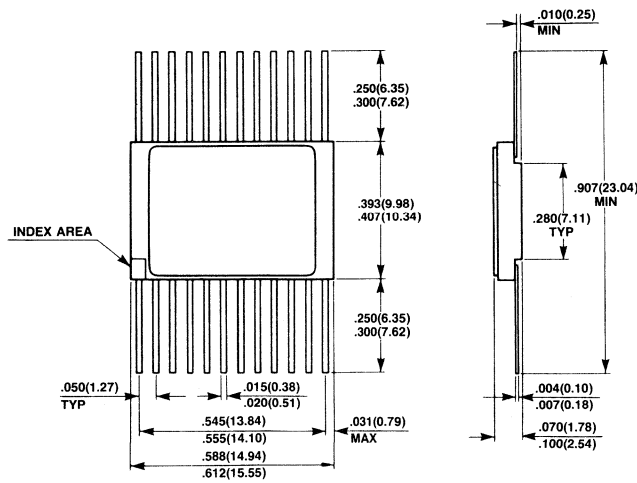
Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

28-Pad Ceramic (Metal Seal) Leadless Chip Carrier (Case No.: LCC-28C-A01)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

24C-Lead Ceramic (Metal Seal) Flat Package (Case No.: FPT-24C-A01)



FUJITSU

MB7138E-W
High Speed Schottky TTL 16,384-Bit PROM

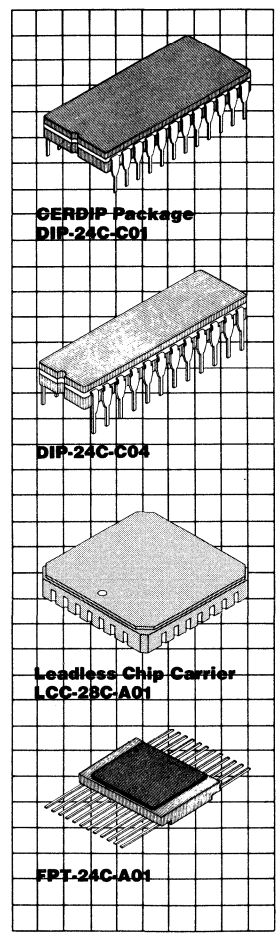
Description

The Fujitsu MB7138E-W is a high speed Schottky TTL electrically field programmable read only memory. With three-state outputs on the MB7138E-W, memory expansion is simple.

The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP™ (Diffused Eutectic Aluminum Process) during a simple programming procedure.

The sophisticated passive isolation termed IOP (Isolation by Oxide and Polysilicon) with thin epitaxial layer and Schottky TTL process enables small chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC, and programming tests prior to shipment. This results in extremely high programmability.

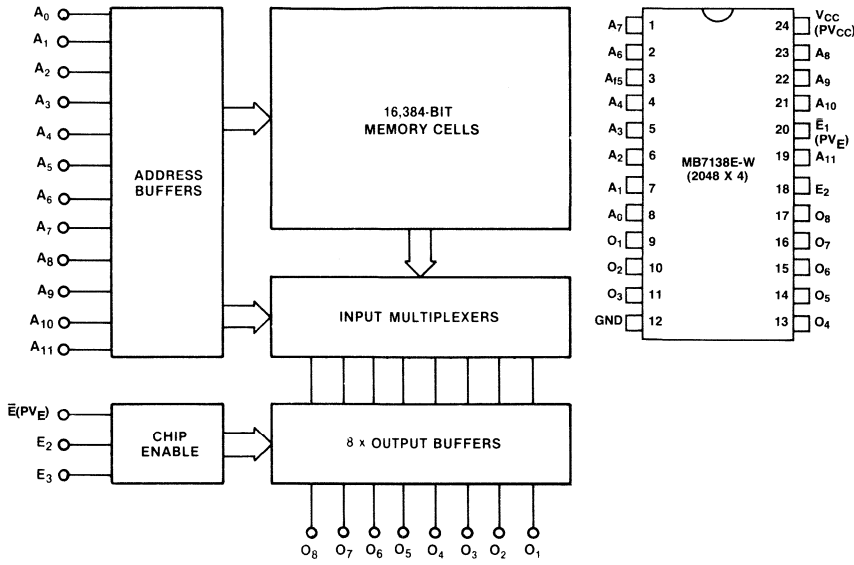


Features

- **Extended temperature range: −55° to +125°C**
- **Organization: 2,048 words by 8-bits**
- **Fast access time: 55 ns max. 35 ns typ.**
- **TTL compatible input/output**
- **AC characteristics are guaranteed over full operation voltage and temperature ranges via unique testing techniques**
- **Proven high programmability and reliability of DEAP™ (Diffused Eutectic Aluminum Process)**
- **Simplified, low power programming**
- **Low current PNP inputs**
- **MB7138E-W: three-state outputs**
- **Three-chip enable leads for easy memory expansion**
- **Standard 24-pin DIP package**
- **Also available in 28-pad LCC, 24-pin narrow dip, and 24-pin flatpack**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

MB7138E-W Block Diagram and Pin Assignment



Absolute Maximum Ratings
(See note)

Rating	Symbol	Value	Unit
Power supply voltage	V_{CC}	−0.5 to +7.0	V
Power supply voltage (during programming)	V_{CC}	−0.5 to +7.5	V
Input voltage	V_{IN}	−1.5 to +5.5	V
Input voltage (during programming)	V_{IPRG}	22.5	V
Output voltage (during programming)	V_{OPRG}	−0.5 to +22.5	V
Input current	I_{In}	−20	mA
Input current (during programming)	I_{IPRG}	+270	mA
Output current	I_{OUT}	+100	mA
Output current (during programming)	I_{OPRG}	+150	mA
Storage temperature	T_{STG}	−65 to +150	°C
Output voltage	V_{OUT}	−0.5 to $+V_{CC}$	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.50	5.0	5.50	V
Input low voltage	V_{IL}	0.0		0.8	V
Input high voltage	V_{IH}	2.0		V_{CC}	V
Ambient temperature	T_A	−55		+125	°C

Capacitance
(f = 1 MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			10	pF
Output capacitance	C_O			15	pF

DC Characteristics
(Full guaranteed operating ranges unless otherwise noted.)

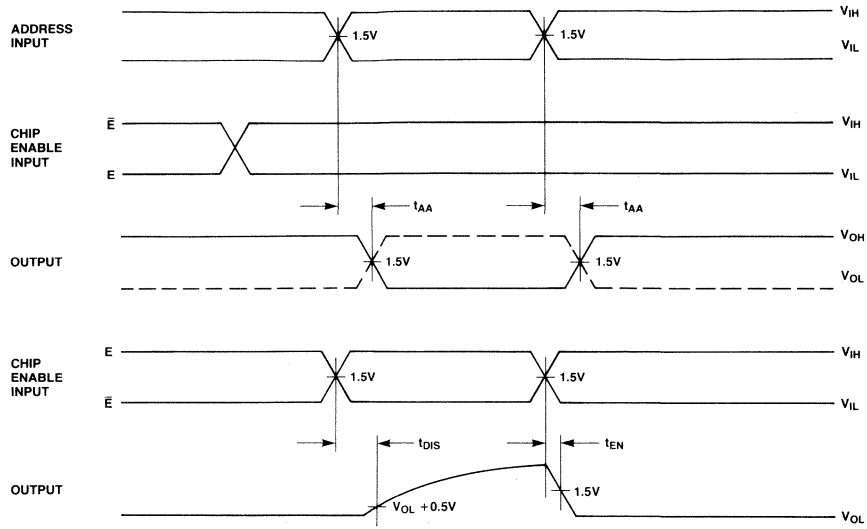
Parameter	Symbol	Min	Typ	Max	Unit
Input leakage current (V_{IH} = 5.5V)	I_R			40	μA
Input load current (V_{IL} = 0.45V)	I_F			−250	μA
Output low voltage (I_{OL} = 16 mA)	V_{OL}			0.50	V
Output leakage current (V_O = 2.4V, chip disable)	I_{OIH}			40	μA
Output leakage current (V_{OL} = 0.45V, chip disabled)	I_{OIL}			−40	μA
Input clamp voltage (I_{IN} = −18 mA)	V_{IC}			−1.2	V
Power supply current (V_{IN} = OPEN or GND)	I_{CC}		130	180	mA
Output high voltage (I_O = −2.4 mA)	V_{OH} *1	2.4			V
Output short circuit current (V_O = GND)	I_{OS} *1	−15		−60	mA

Note: *1 Denotes guaranteed characteristics of output high-level (ON) state when the chip is enabled and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

AC Characteristics
(Full guaranteed operating ranges unless otherwise noted.)

Parameter	Symbol	Typ	Max	Unit
Address access time	t_{AA}	35	55	ns
Output disable time	t_{DIS}		40	ns
Output enable time	t_{EN}		40	ns

Operation Timing Diagram



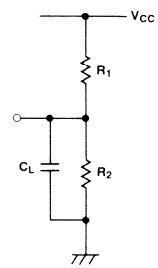
NOTE: OUTPUT DISABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO REACH A HIGH RESISTANCE STATE WHEN THE CHIP ENABLE IS DISABLED. OUTPUT ENABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO BECOME ACTIVE WHEN THE CHIP ENABLE IS ENABLED. THE HIGH RESISTANCE STATE IS DEFINED AS A POINT ON THE OUTPUT WAVEFORM EQUAL TO ΔV OF 0.5V FROM THE ACTIVE OUTPUT LEVEL.

AC Test Conditions

Input Conditions

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5 ns from 1V to 2V
Frequency ..... 1 MHz

R_1	R_2	C_L
300Ω	600Ω	30 pF



Input/Output Circuit Information

Input

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of the input circuit improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

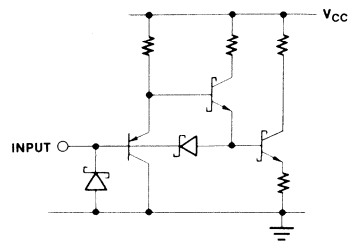
Three-state Output

A "three-state" output is a logic element which has three distinct output states of LOW, HIGH and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

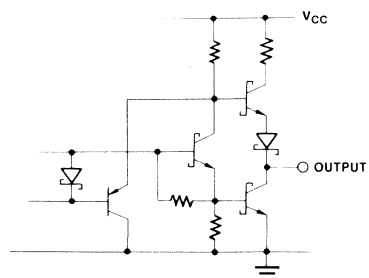
In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor is provided in the output circuit to decrease the load on the Chip Enable circuit.

MB7138E-W Input Circuit

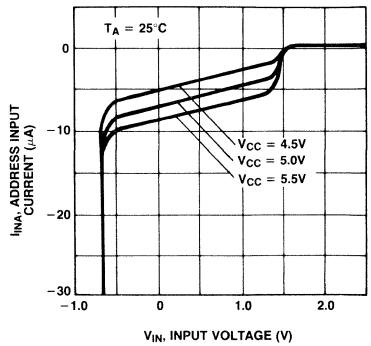


MB7138E-W Output Circuit

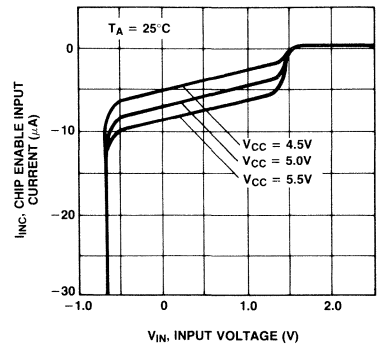


Typical Characteristics Curves

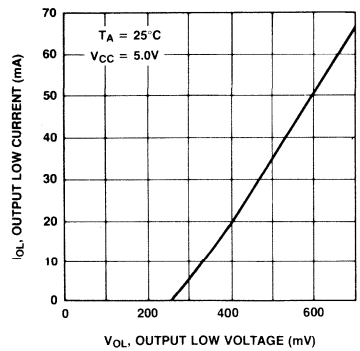
I_{INA} Input Current vs. V_{IN} Input Voltage



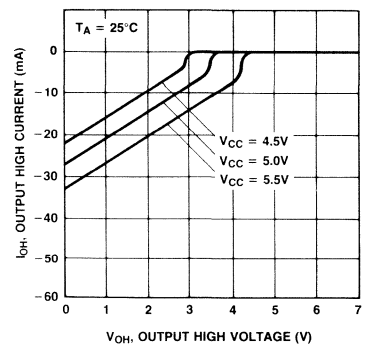
I_{INC} Input Current vs. V_{IN} Input Voltage



I_{OL} Output Low Current vs. V_{OL} Output Low Voltage

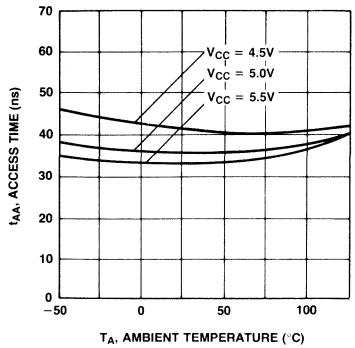


I_{OH} Output High Current vs. V_{OH} Output High Voltage

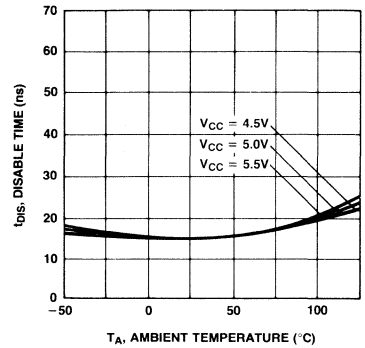


Typical Characteristics Curves
(Continued)

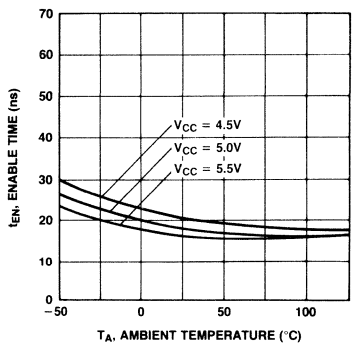
t_{AA} Access Time vs. Ambient Temperature



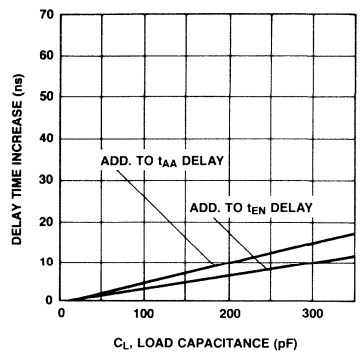
t_{DIS} Disable Time vs. Ambient Temperature



t_{EN} Enable Time vs. Ambient Temperature

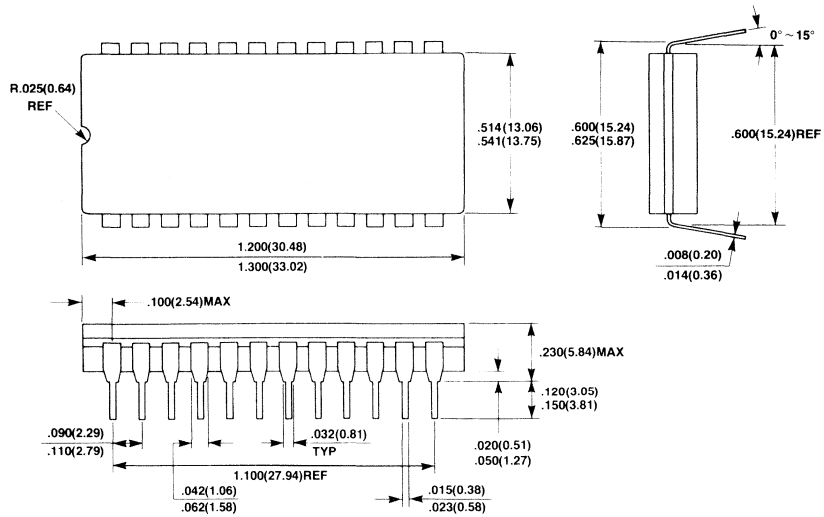


Delay Time Increase vs. C_L Load Capacitance

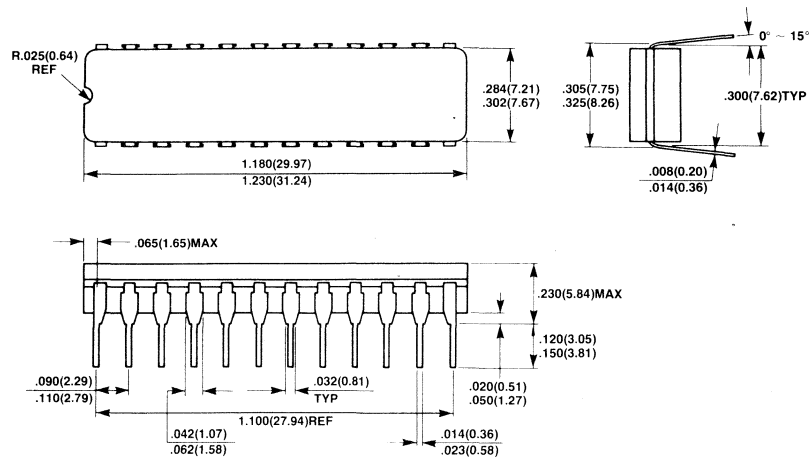


Package Dimensions
Dimensions in inches
(millimeters)

24-Lead Ceramic (CERDIP) Dual In-Line Package
(Case No.: DIP-24C-C01)

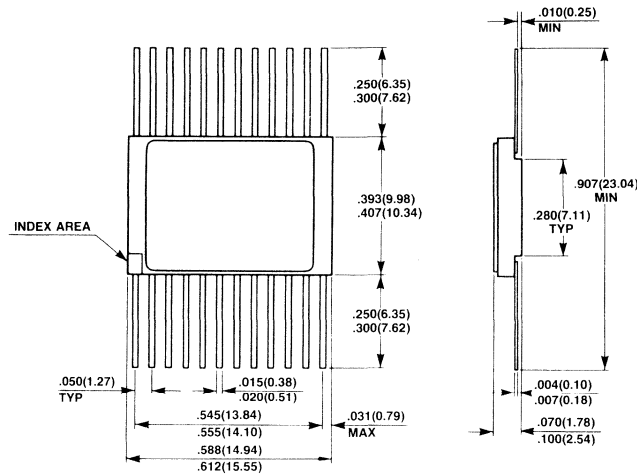


24-Lead Ceramic (CERDIP) Dual In-Line Package
(Case No.: DIP-24C-C04)

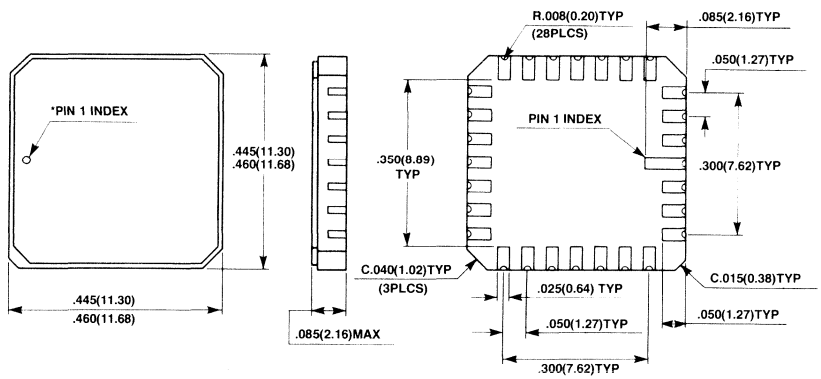


Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

24-Lead Ceramic (Metal Seal) Flat Package
(Case No.: FPT-24C-A01)



28-Pad Ceramic (Metal Seal) Leadless Chip Carrier
(Case No.: LCC-28C-A01)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

FUJITSU

MB7141E/H, MB7142E/H

Programmable Schottky 32,768-Bit Read Only Memory (4,096 Words x 8-Bits)

Description

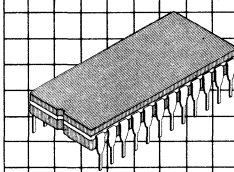
The Fujitsu MB7141 (open collector) and MB7142 (three-state) are high-speed, Schottky TTL electrically field programmable read-only memories organized as 4,096 words by 8-bits. With uncommitted collector outputs provided on the MB7141 and three-state outputs on the MB7142, memory expansion is simple.

Fujitsu PROMS utilize a unique Shallow V-Groove (SVG) passive isolation process which, combined with a very thin epitaxial layer and the Schottky TTL process, provides small die sizes and very fast access times.

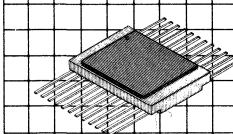
The memory is fabricated with all cells low, the "zero" value for positive logic. Logical "one" for a cell is achieved by programming. Individual cells are programmed to a logical "one" using the highly reliable Diffused Eutectic Aluminum Process (DEAP).

High programming yields are insured through the use of special test cells to verify programmability on each device prior to shipment.

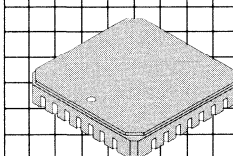
Two guaranteed maximum access time options are available: the 7141 or 7142 "E" versions guarantee 65 ns maximum access time; the 7141 or 7142 "H" versions guarantee 55 ns maximum access time.



Ceramic Package
DIP-24C-C01



Ceramic Package
FPT-24C-A01



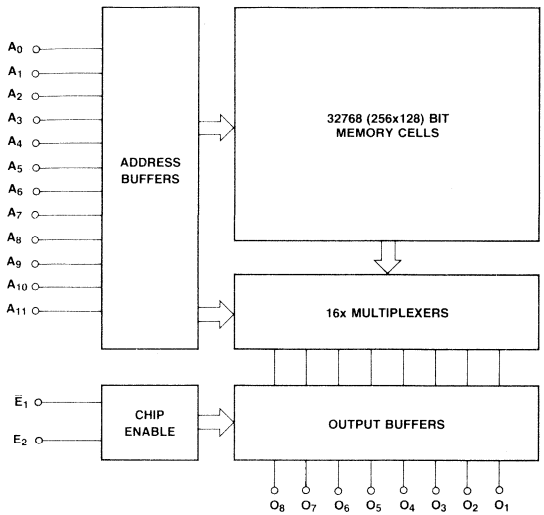
LCC-28C-A01

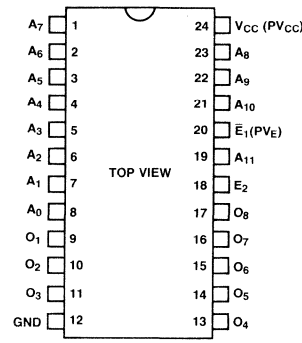
Features

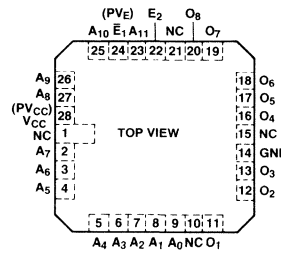
- **Single +5V power supply requirement**
- **4096 words x 8-bits; fully decoded**
- **High levels of programmability and reliability proven in use**
- **Unique, reliable DEAP programming process**
- **Low power, simplified programming techniques**
- **Low current PNP inputs**
- **AC characteristics guaranteed over the full operating range**
- **Fast. 45 ns typical access time with two guaranteed options:**
  7141/7142 E: 65 ns max.
  7141/7142 H: 55 ns max.
- **TTL compatible inputs and outputs; open collector (MB7141) or three-state (MB7142)**
- **Two Chip Enable input**
- **JEDEC standard pinout.**
- **24-pin flat, 28-LCC or 24-pin DIP packages**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB7141/7142 Block Diagram and Pin Assignment







Pad Configuration

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Power supply voltage	V_{CC}	−0.5 to +7.0	V
Power supply voltage (during programming)	V_{CC}	−0.5 to +7.5	V
Input voltage	V_{IN}	−1.5 to V_{CC}	V
Input voltage (during programming)	V_{PRG}	22.5	V
Output voltage (during programming)	V_{PRG}	−0.5 to +22.5	V
Input current	I_{IN}	−20	mA
Input current (during programming)	I_{PRG}	+270	mA
Output current	I_{OUT}	+100	mA
Output current (during programming)	I_{PRG}	+150	mA
Storage temperature	T_{STG}	−65 to +150	°C
Output voltage	V_{OUT}	−0.5 to V_{CC}	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Guaranteed Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Input low voltage	V_{IL}	0		0.8	V
Input high voltage	V_{IH}	2.0		V_{CC}	V
Ambient temperature	T_A	0		75	°C

Capacitance
(f = 1 MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			10	pF
Output capacitance	C_O			15	pF

DC Characteristics
(Full guaranteed operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Input leakage current (V_{IH} = 5.5V)		I_R			40A	μA
Input load current (V_{IL} = 0.45V)		I_F			−250	μA
Output low voltage (I_{OL} = 10 mA)		V_{OL}			0.45	V
Output low voltage (I_{OL} = 16 mA)		V_{OL}			0.50	V
Output leakage current (V_O = 2.4V, chip disabled)	MB7141	I_{OLK}			40	μA
Output leakage current (V_O = 2.4V, chip disabled)	MB7142	I_{OIH}			40	μA
Output leakage current (V_O = 0.45V, chip disabled)	MB7142	I_{OIL}			−40	μA
Input clamp voltage (I_{IN} = −18 mA)		V_{IC}			−1.2	V
Power supply current (V_{IN} = OPEN or GND)		I_{CC}		140	185	mA
Output high voltage*1 (I_O = −2.4 mA)	MB7142	V_{OH}	2.4			V
Output short circuit current*1 (V_O = GND)	MB7142	I_{OS}	−15		−60	mA

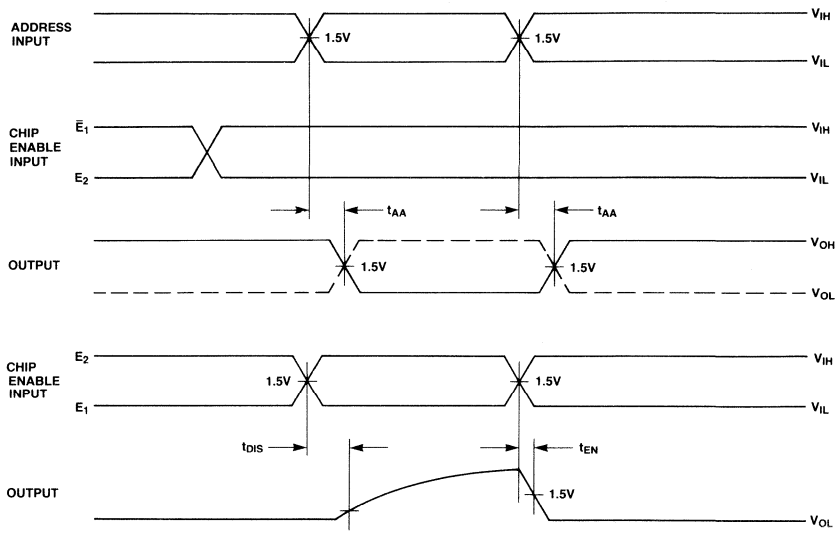
Note: *1 Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled (V_{IE} = 0.4V, V_{IE} = 2.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

AC Characteristics
(Full guaranteed operating conditions unless otherwise noted.)

Parameter	Symbol	E Typ	E Max	H Typ	H Max	Unit
Access time (via address input)	t_{AA}	45	65	45	55	ns
Output disable time	t_{DIS}		40		40	ns
Output enable time	t_{EN}		40		40	ns

AC Characteristics
(Continued)

Operation Timing Diagram

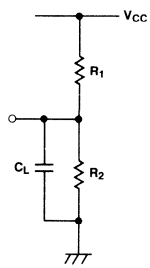


NOTE: OUTPUT DISABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO REACH A HIGH RESISTANCE STATE WHEN THE CHIP ENABLE IS TAKEN DISABLE. OUTPUT ENABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO BECOME ACTIVE WHEN THE CHIP ENABLE IS TAKEN ENABLE. THE HIGH RESISTANCE STATE IS DEFINED AS A POINT ON THE OUTPUT WAVEFORM EQUAL TO A ΔV OF 0.5V FROM THE ACTIVE OUTPUT LEVEL.

AC Test Conditions

Input Conditions

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5 ns from 1V to 2V
Frequency ..... 1 MHz



TRUTH TABLE

	MB7141/7142		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30 pF
t_{DIS}	300Ω	600Ω	30 pF
t_{EN}	300Ω	600Ω	30 pF

Input/Output Circuit Information

Input

Schottky TTL circuit technology is used in the input circuit to achieve high-speed operation. The PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. A protection diode for reliable operation protects against voltage transients.

Open-Collector Output

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30 mA for the MB7142 (three-state) compared to 0 mA for the MB7141 (open-collector).

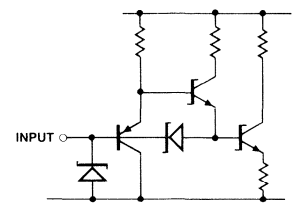
Three-State Output

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

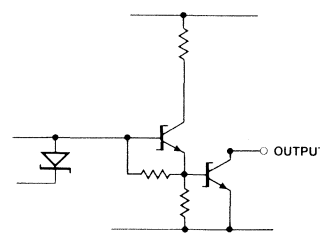
In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor provided in the output circuit decreases the load for the Chip Enable circuit.

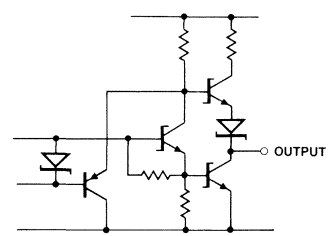
MB7141/7142 Input



MB7141 Output

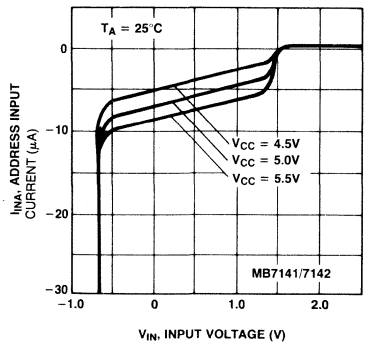


MB7142 Output

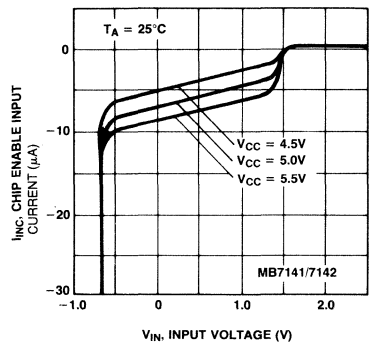


Typical Characteristics Curves

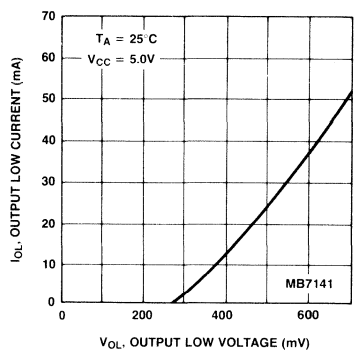
I_{INA} Input Current vs. V_{IN} Input Voltage



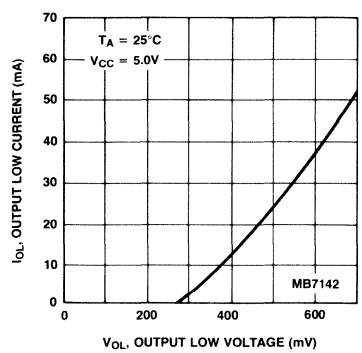
I_{INC} Input Current vs. V_{IN} Input Voltage



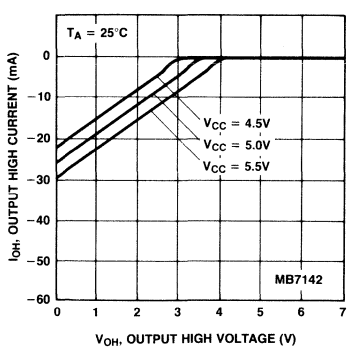
I_{OL} Output Low Current vs. V_{OL} Output Low Voltage



I_{OL} Output Low Current vs. V_{OL} Output Low Voltage

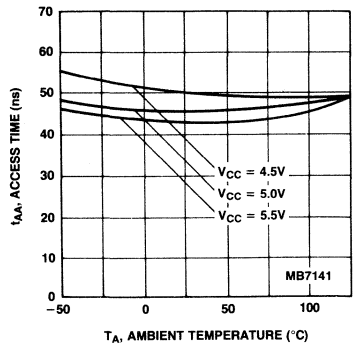


I_{OH} Output High Current vs. V_{OH} Output High Voltage

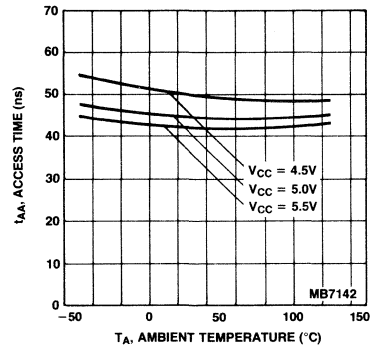


Typical Characteristics Curves
(Continued)

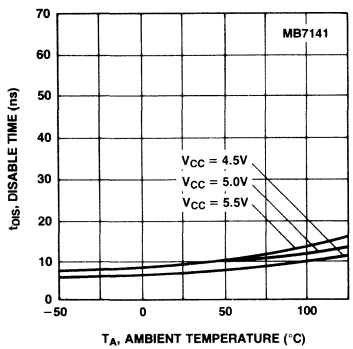
t_{AA} Access Time vs. Ambient Temperature



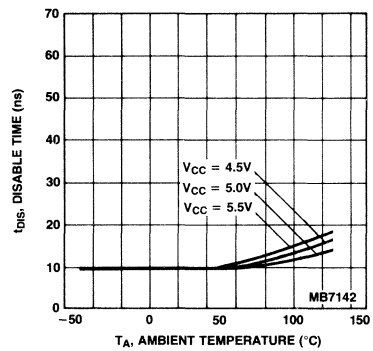
t_{AA}, Access Time vs. Ambient Temperature



t_{DIS} Disable Time vs. Ambient Temperature

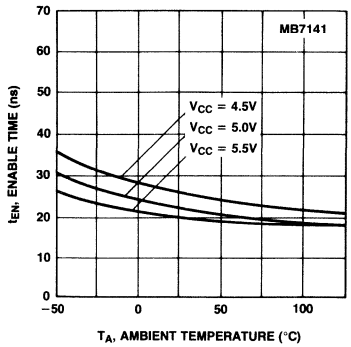


t_{DIS} Disable Time vs. Ambient Temperature

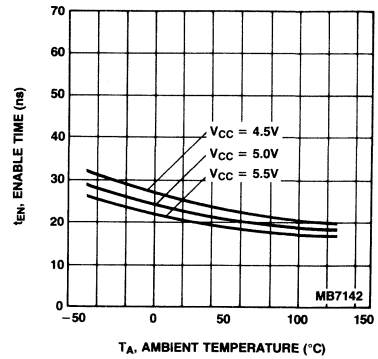


Typical Characteristics Curves
(Continued)

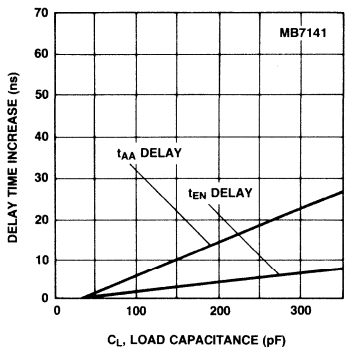
t_{EN} Enable Time vs. Ambient Temperature



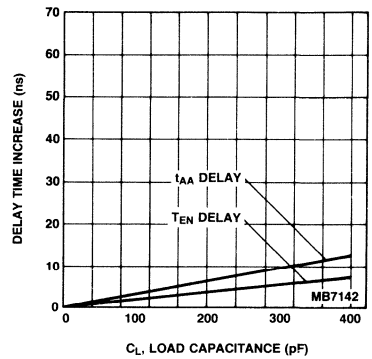
t_{EN} Enable Time vs. Ambient Temperature



Delay Time Increase vs. C_L Load Capacitance

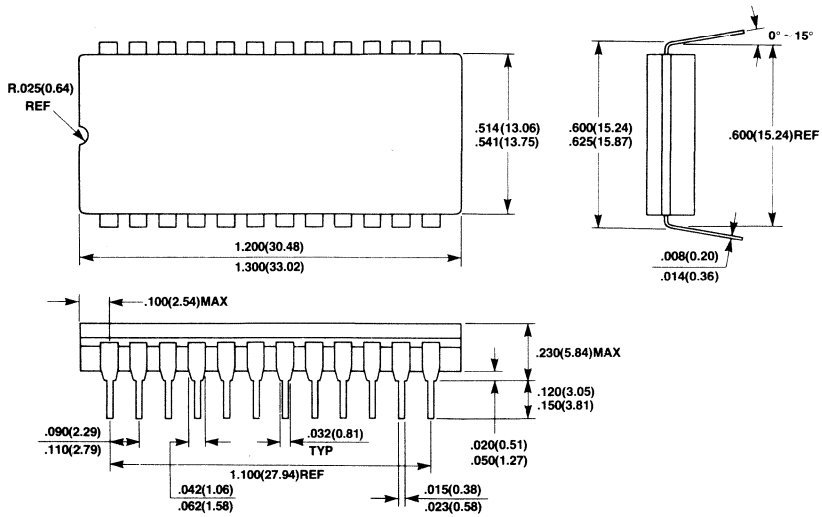


Delay Time Increase vs. C_L Load Capacitance

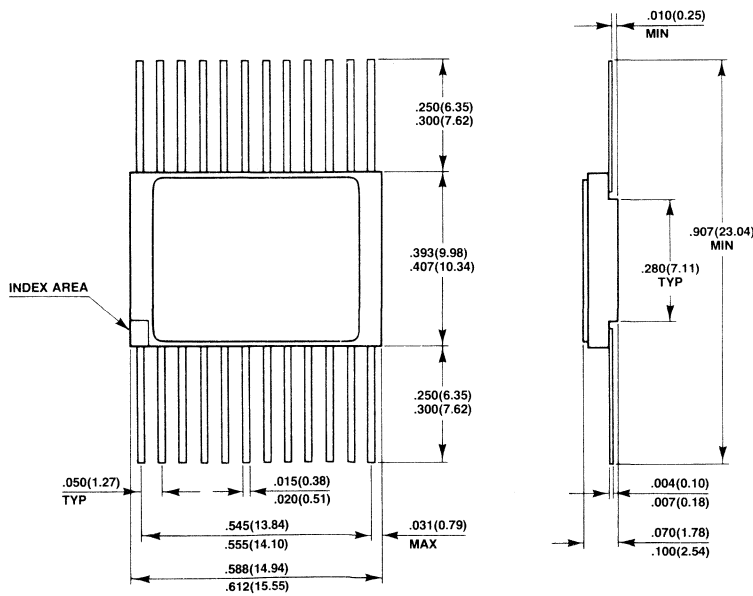


Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

24-Lead Ceramic (CERDIP) Dual In-Line Package
(Case No.: DIP-24C-C01)

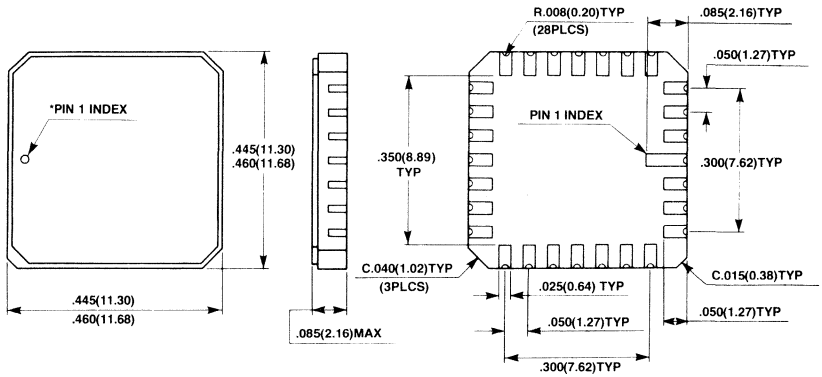


24-Lead Ceramic (Metal Seal) Flat Package
(Case No.: FPT-24C-A01)



Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

28-Pad Ceramic (Metal Seal) Leadless Chip Carrier
(Case No.: LCC-28C-A01)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

FUJITSU

■ MB7142E-W

High Speed Schottky TTL 32,768-Bit Prom

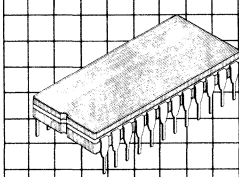
Description

The Fujitsu MB7142E-W is a high speed electrically field programmable read only memory. With three-state outputs on the MB7142E-W, memory expansion is simple.

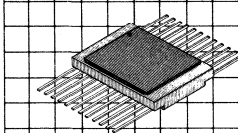
The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP™ (Diffused Eutectic Aluminum Process) during a simple programming procedure.

The sophisticated passive isolation termed IOP (Isolation by Oxide and Polysilicon) with thin epitaxial layer and Schottky TTL process enables small chip size and fast access time.

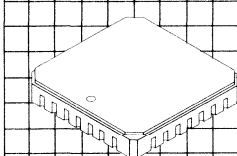
The extra test cells and unique testing methods provide enhanced correlation between programmed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.



Cerdip Package
DIP-24C-C01



FPT-24C-A01



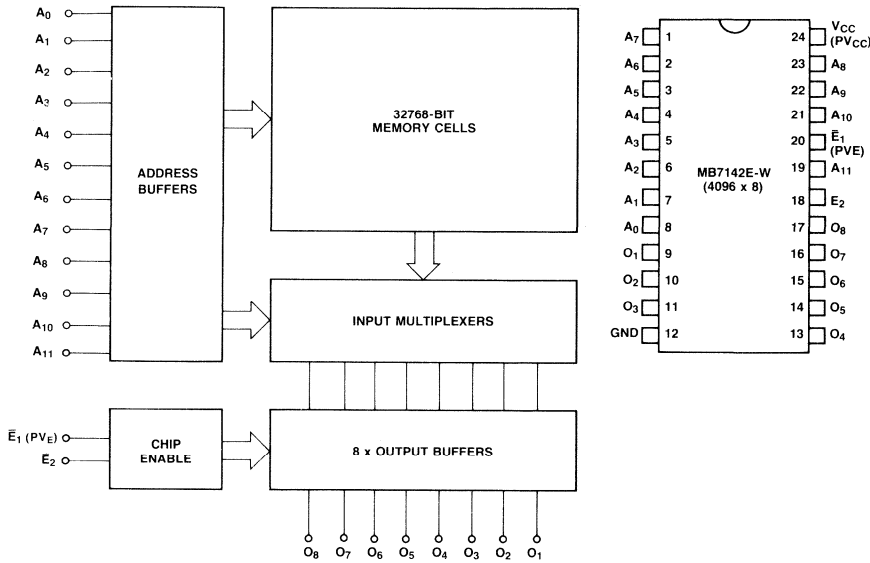
Leadless Chip Carrier
LCC-28C-A01

Features

- **Extended Temperature Range: −55° to +125°C**
- **Organization: 4096 words by 8-bits, fully decoded**
- **TTL compatible input/output**
- **Fast access time: 65 ns Max. 45 ns Typ.**
- **Single +5V supply voltage**
- **Simplified, low power programming**
- **Proven high programmability and reliability of DEAP™ (Diffused Eutectic Aluminum Process)**
- **Low current PNP inputs**
- **MB7142E-W: Three-state outputs**
- **Two chip enable inputs for easy memory expansion**
- **Standard 24-pin DIP package**
- **Also available in 28-pad LCC**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB7142E-W Block Diagram and Pin Assignment



Absolute Maximum Ratings

(See Note)

Rating	Symbol	Value	Unit
Power supply voltage	V_{CC}	−0.5 to +7.0	V
Power supply voltage (during programming)	V_{CC}	−0.5 to +7.5	V
Input voltage	V_{IN}	−1.5 to +5.5	V
Input voltage (during programming)	V_{IPRG}	22.5	V
Output voltage (during programming)	V_{OPRG}	−0.5 to +22.5	V
Input current	I_{IN}	−20	mA
Input current (during programming)	I_{IPRG}	+270	mA
Output current	I_{OUT}	+100	mA
Output current (during programming)	I_{OPRG}	+150	mA
Storage temperature	T_{stg}	−65 to +150	°C
Output voltage	V_{OUT}	−0.5 to $+V_{CC}$	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low voltage	V_{IL}	0.0		0.8	V
Input high voltage	V_{IH}	2.0		V_{CC}	V
Ambient temperature	T_A	−55		+125	°C

Capacitance
(f = 1 MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			10	pF
Output capacitance	C_O			15	pF

DC Characteristics
(Full guaranteed ranges unless otherwise noted.)

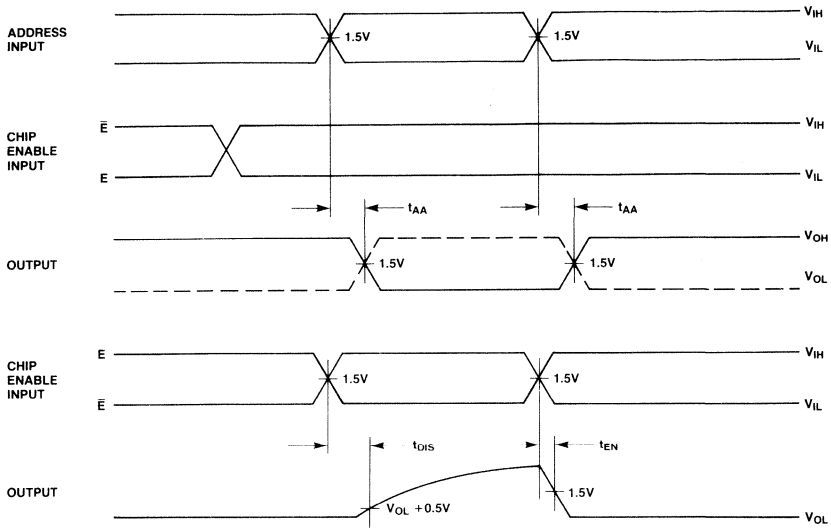
Parameter	Symbol	Min	Typ	Max	Unit
Input leakage current (V_{IH} = 5.5V)	I_R			40	μA
Input load current (V_{IL} = 0.45V)	I_F			−250	μA
Output low voltage (I_{OL} = 16 mA)	V_{OL}			0.50	V
Output leakage current (V_O = 2.4V, chip disable)	I_{OIH}			40	μA
Output leakage current (V_{OL} = 0.45V chip disabled)	I_{OIL}			−40	μA
Input clamp voltage (I_{IN} = −18 mA)	V_{IC}			−1.2	V
Power supply current (V_{IN} = OPEN or GND)	I_{CC}		140	185	mA
Output high voltage (I_O = −2.4 mA)	V_{OH} *1	2.4			V
Output short circuit current (V_O = GND)	I_{OS} *1	−15		−60	mA

Note: *1 Denotes guaranteed characteristics of output high-level (ON) state when the chip is enabled and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

AC Characteristics
(Full guaranteed operating ranges unless otherwise noted.)

Parameter	Symbol	Typ	Max	Unit
Address access time	t_{AA}	45	65	ns
Output disable time	t_{DIS}		40	ns
Output enable time	t_{EN}		40	ns

Operation Timing Diagram



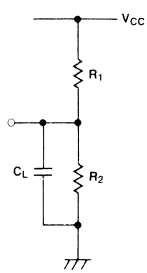
NOTE: OUTPUT DISABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO REACH A HIGH RESISTANCE STATE WHEN THE CHIP ENABLE IS DISABLED. OUTPUT ENABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO BECOME ACTIVE WHEN THE CHIP ENABLE IS ENABLED. THE HIGH RESISTANCE STATE IS DEFINED AS A POINT ON THE OUTPUT WAVEFORM EQUAL TO A ΔV OF 0.5V FROM THE ACTIVE OUTPUT LEVEL.

AC Test Conditions

INPUT CONDITIONS

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5 ns from 1V to 2V
Frequency ..... 1 MHZ

R_1	R_2	C_L
300Ω	600Ω	30 pF



Input/Output Circuit Information

Input

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor in the first stage of the input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

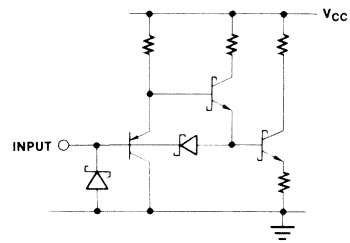
Three-State Output

A "three-state" output is a logic element which has three distinct output states of LOW, HIGH and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level.) Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

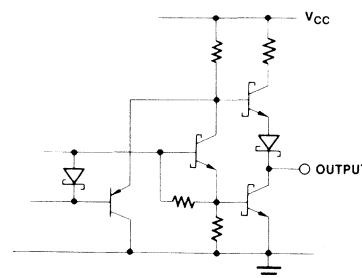
In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor is provided in the output circuit to decrease the load on the Chip Select circuit.

MB7142E-W Input Circuit

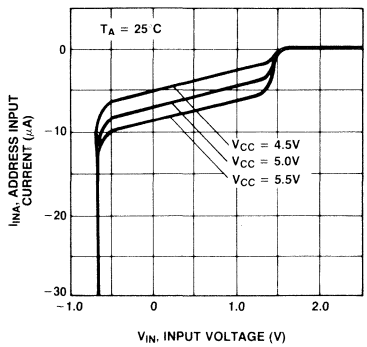


MB7142E-W Output Circuit

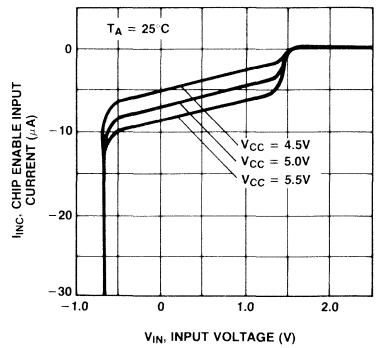


Typical Characteristics Curves

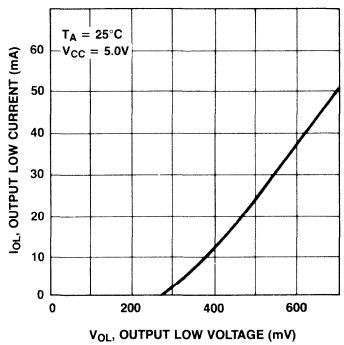
I_{INA} Input Current vs. V_{IN} Input Voltage



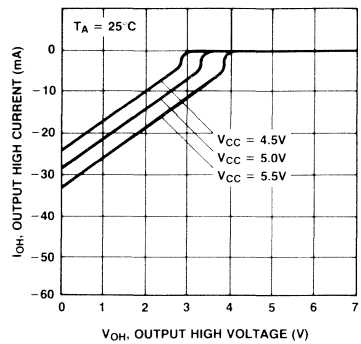
I_{INC} Input Current vs. V_{IN} Input Voltage



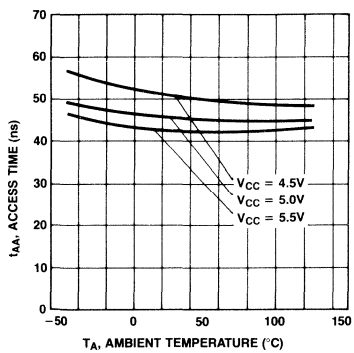
I_{OL} Output Low Current vs. V_{OL} Output Low Voltage



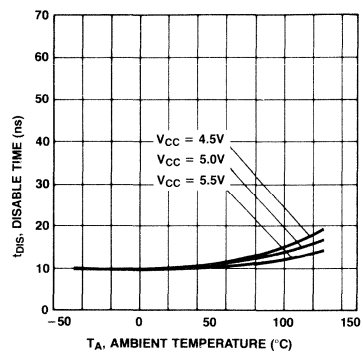
I_{OH} Output High Current vs. V_{OH} Output High Voltage



t_{AA} Access Time vs. Ambient Temperature

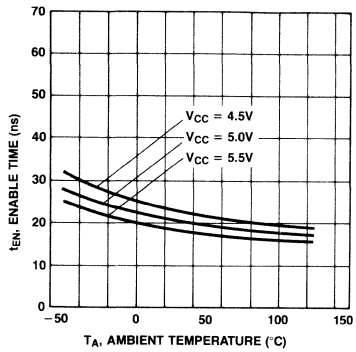


t_{DIS} Disable Time vs. Ambient Temperature

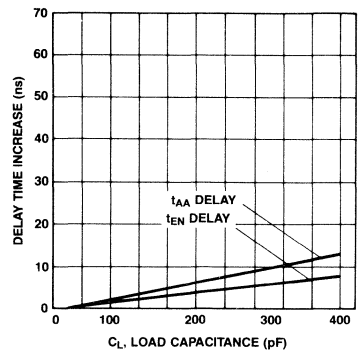


Typical Characteristics Curves
(Continued)

t_{EN} Enable Time vs. Ambient Temperature

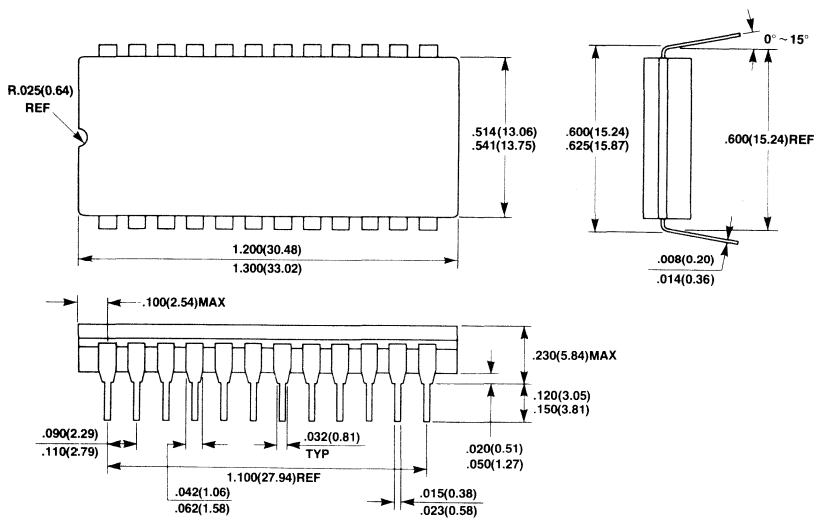


Delay Time Increase vs. C_L Load Capacitance



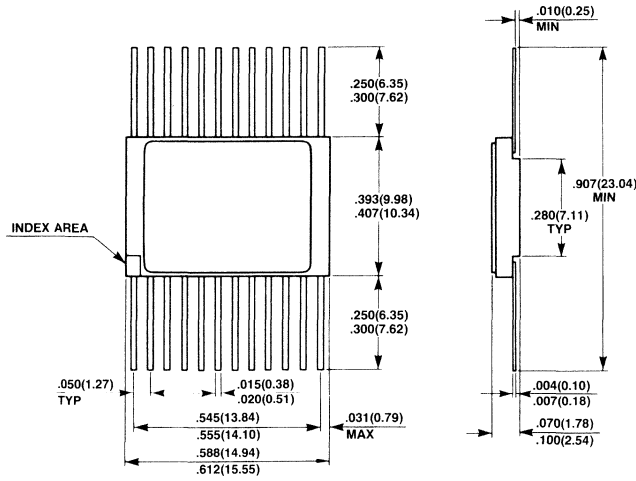
Package Dimensions
Dimensions in Inches
(millimeters)

24-Lead Ceramic (CERDIP) Dual In-Line Package (Case No.: DIP-24C-C01)



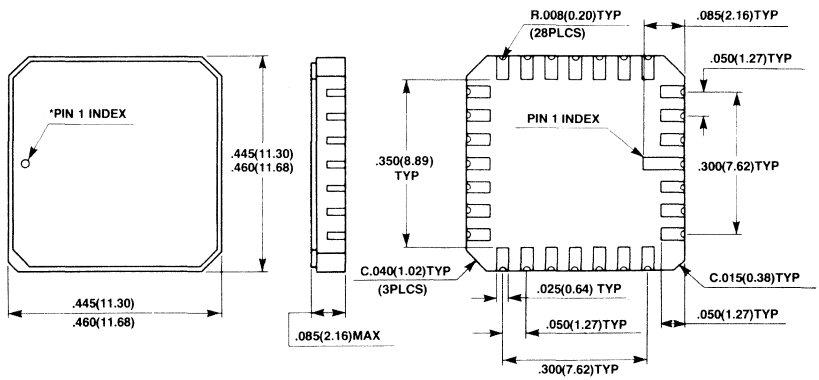
Package Dimensions
(continued)
Dimensions in inches
(millimeters)

24-Lead Ceramic (Metal Seal) Flat Package (Case No.: FPT-24C-A01)



Dimensions in inches (millimeters)

28-Pad Ceramic (Metal Seal) Leadless Chip Carrier (Case No.: LCC-28C-A01)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

MB7143E/H, MB7144E/H/Y

Programmable Schottky 65,536-Bit Read Only Memory (8,192 Words x 8-Bits)

Description

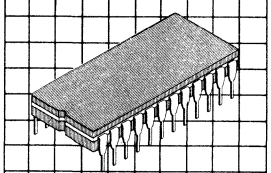
The Fujitsu MB7143 (open collector) and MB7144 (three-state) are high-speed Schottky TTL electrically field programmable read-only memories organized as 8,192 words by 8-bits. With uncommitted collector outputs provided on the MB7143 and three-state outputs on the MB7144, memory expansion is simple.

Fujitsu PROMS utilize a unique Shallow V-Groove (SVG) passive isolation process which, combined with a very thin epitaxial layer and the Schottky TTL process, provides small die sizes and very fast access times.

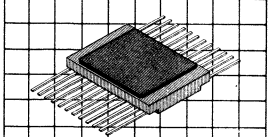
The memory is fabricated with all cells low, the "zero" value for positive logic. Logical "one" for a cell is achieved by programming. Individual cells are programmed to a logical "one" using the highly reliable Diffused Eutectic Aluminum Process (DEAP).

High programming yields are insured through the use of special test cells to verify programmability on each device prior to shipment.

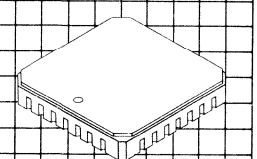
Three guaranteed maximum access time options are available: the 7143 or 7144 "E" versions guarantee 65 ns maximum access time; the 7143 or 7144 "H" versions guarantee 55 ns maximum access time. The 7144Y guarantees 45 ns maximum access time.



Ceramic Package
DIP-24C-C01



Ceramic Package
FPT-24C-A02



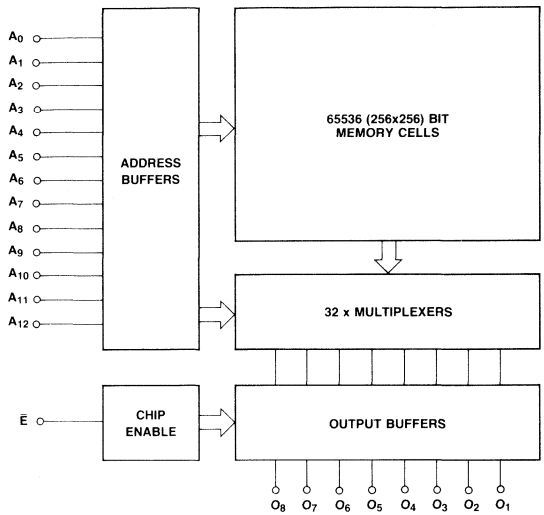
LCC-28C-A01

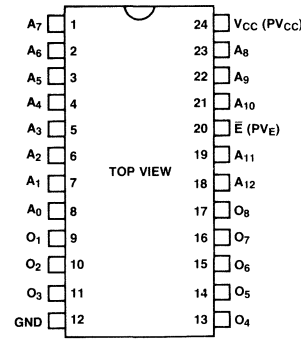
Features

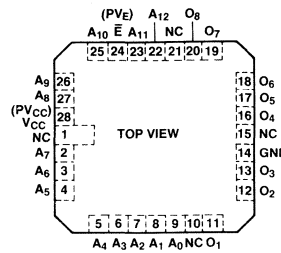
- **Single +5V supply voltage**
- **8192 words x 8-bits; fully decoded**
- **High levels of programmability and reliability proven in use**
- **Unique, reliable DEAP programming process**
- **Low power, simplified programming techniques**
- **Low current PNP inputs**
- **AC characteristics guaranteed over the full operating range**
- **Fast. 40 ns typical access time with three guaranteed options:**
  7143/7144 E: 65 ns max.
  7143/7144 H: 55 ns max.
  7144 Y: 45 ns max.
- **TTL compatible inputs and outputs; open collector (MB7143) or three-state (MB7144)**
- **Single Chip Enable input**
- **JEDEC standard pinout; 24-pin flat, 28-LCC or 24-pin DIP packages**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB7143/7144 Block Diagram and Pin Assignments







Pad Configuration

Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Power supply voltage	V_{CC}	−0.5 to +7.0	V
Power supply voltage (during programming)	V_{CC}	−0.5 to +7.5	V
Input voltage	V_{IN}	−1.5 to 5.5	V
Input voltage (during programming)	V_{PRG}	22.5	V
Output voltage (during programming)	V_{PRG}	−0.5 to +22.5	V
Input current	I_{IN}	−20	mA
Input current (during programming)	I_{PRG}	+270	mA
Output current	I_{OUT}	+100	mA
Output current (during programming)	I_{PRG}	+150	mA
Storage temperature	T_{STG}	−65 to +150	°C
Output voltage	V_{OUT}	−0.5 to V_{CC}	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Guaranteed Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.0	5.25	V
Input low voltage	V_{IL}	0		0.8	V
Input high voltage	V_{IH}	2.0		5.5	V
Ambient temperature	T_A	0		75	°C

Capacitance
(f = 1 MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			10	pF
Output capacitance	C_O			15	pF

DC Characteristics
(Full guaranteed operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Input leakage current (V_{IH} = 5.5V)		I_R			40	μA
Input load current (V_{IL} = 0.45V)		I_F			−250	μA
Output low voltage (I_{OL} = 10 mA)		V_{OL}			0.45	V
Output low voltage (I_{OL} = 16 mA)		V_{OL}			0.50	V
Output leakage current (V_O = 2.4V, chip disabled)	MB7143	I_{OLK}			40	μA
Output leakage current (V_O = 2.4V, chip disabled)	MB7144	I_{OIH}			40	μA
Output leakage current (V_O = 0.45V, chip disabled)	MB7144	I_{OIL}			−40	μA
Input clamp voltage (I_{IN} = −18 mA)		V_{IC}			−1.2	V
Power supply current (V_{IN} = OPEN or GND)		I_{CC}		160	190	mA
Output high voltage*1 (I_O = −2.4 mA)	MB7144	V_{OH}	2.4			V
Output short circuit current*1 (V_O = GND)	MB7144	I_{OS}	−15		−60	mA

Note: *1 Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled ($V_{I\overline{E}}$ = 2.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

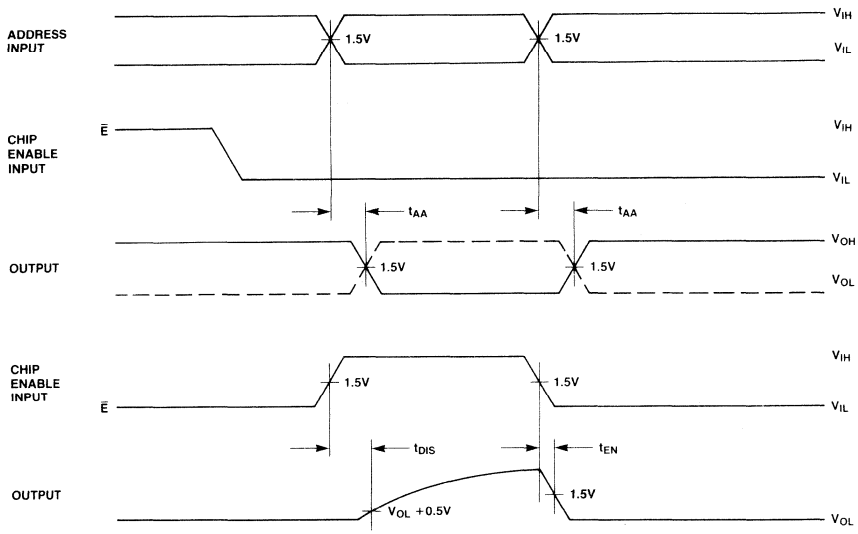
AC Characteristics
(Recommended operating conditions unless otherwise noted.)

		E		H		MB7144Y		
Parameter	**Symbol**	**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Unit**
Access time (via address input)	t_{AA}	40	65	40	55	40	45	ns
Output disable time	t_{DIS}		40		40		40	ns
Output enable time	t_{EN}		40		40		40	ns

AC Characteristics

(Continued)
(Recommended operating conditions unless otherwise noted.)

Operation Timing Diagram



NOTE: OUTPUT DISABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO REACH A HIGH RESISTANCE STATE WHEN THE CHIP ENABLE IS TAKEN HIGH. OUTPUT ENABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO BECOME ACTIVE WHEN THE CHIP ENABLE IS TAKEN LOW. THE HIGH RESISTANCE STATE IS DEFINED AS A POINT ON THE OUTPUT WAVEFORM EQUAL TO A ΔV OF 0.5V FROM THE ACTIVE OUTPUT LEVEL.

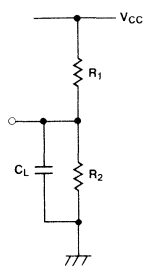
AC Test Conditions

Input Conditions

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5 ns from 1V to 2V
Frequency ..... 1 MHz

TRUTH TABLE

	MB7143/7144		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30 pF
t_{DIS}	300Ω	600Ω	30 pF
t_{EN}	300Ω	600Ω	30 pF



Input/Output Circuit Information

Input

In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. The PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

Open-Collector Output

The open-collector output is often utilized in high speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30 mA for the MB7144 (three-state) compared to 0 mA for the MB7143 (open-collector).

Three-State Output

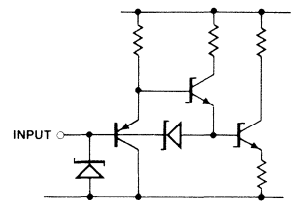
A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result.

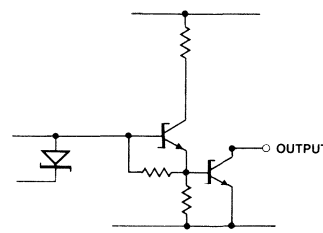
Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. A PNP transistor provided in the output circuit decreases the load for the Chip Enable circuit.

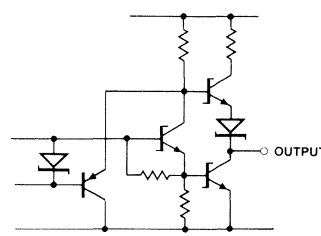
MB7143/7144 Input



MB7143 Output

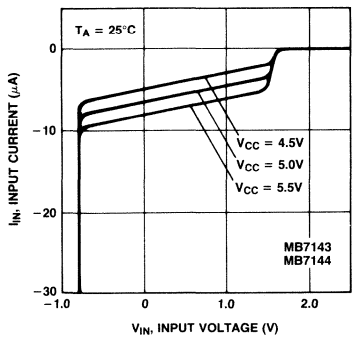


MB7144 Output

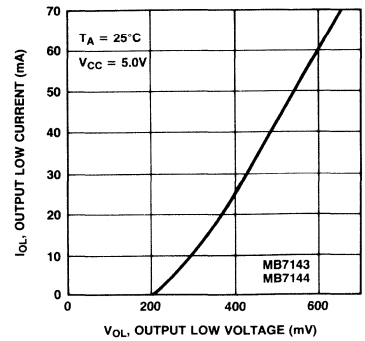


Typical Characteristics Curves

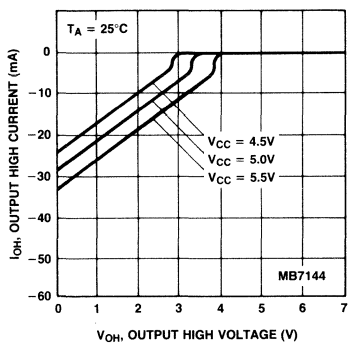
I_{IN} Input Current vs. V_{IN} Input Voltage



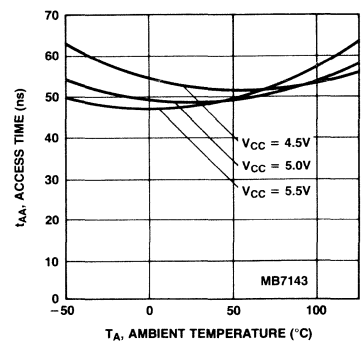
I_{OL} Output Low Current vs. V_{OL} Output Low Voltage



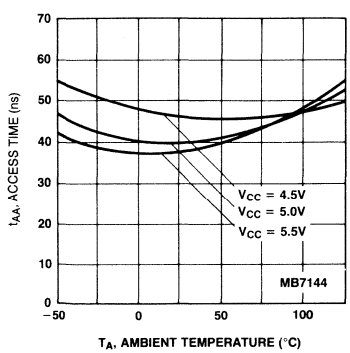
I_{OH} Output High Current vs. V_{OH} Output High Voltage



t_{AA} Access Time vs. Ambient Temperature

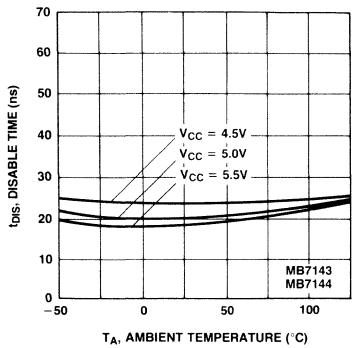


t_{AA} Access Time vs. Ambient Temperature

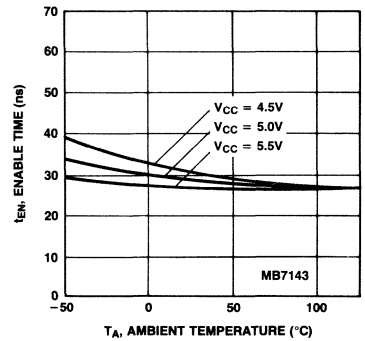


Typical Characteristics Curves
(Continued)

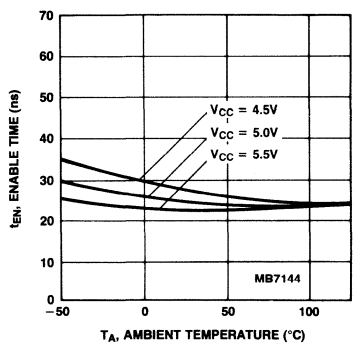
t_{DIS} Disable Time vs. Ambient Temperature



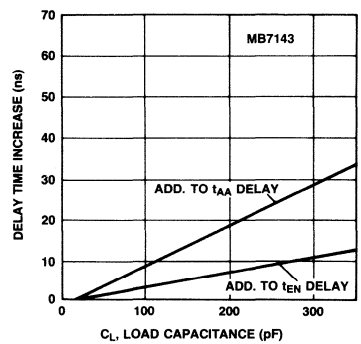
t_{EN} Enable Time vs. Ambient Temperature



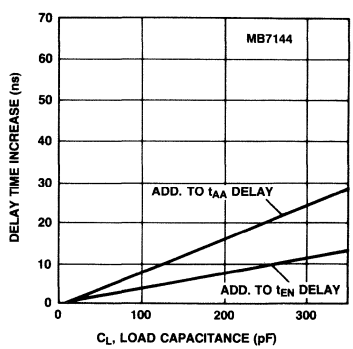
t_{EN} Enable Time vs. Ambient Temperature



Delay Time Increase vs. C_L Load Capacitance



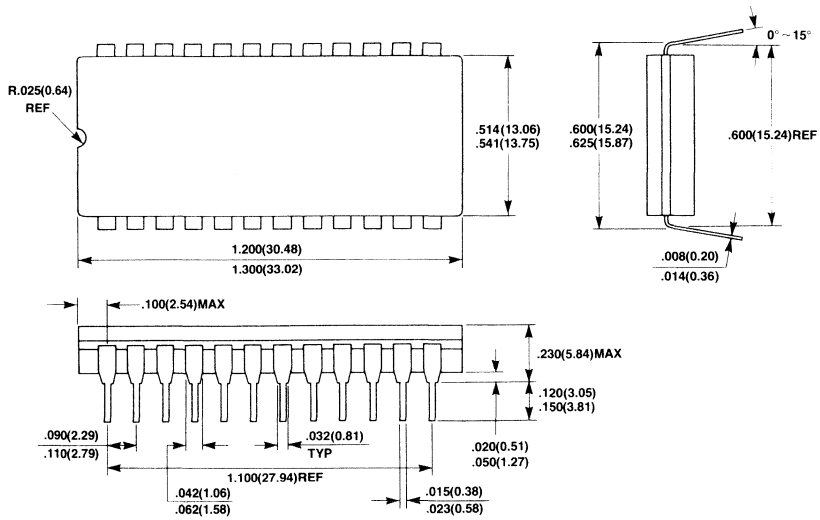
Delay Time Increase vs. C_L Load Capacitance



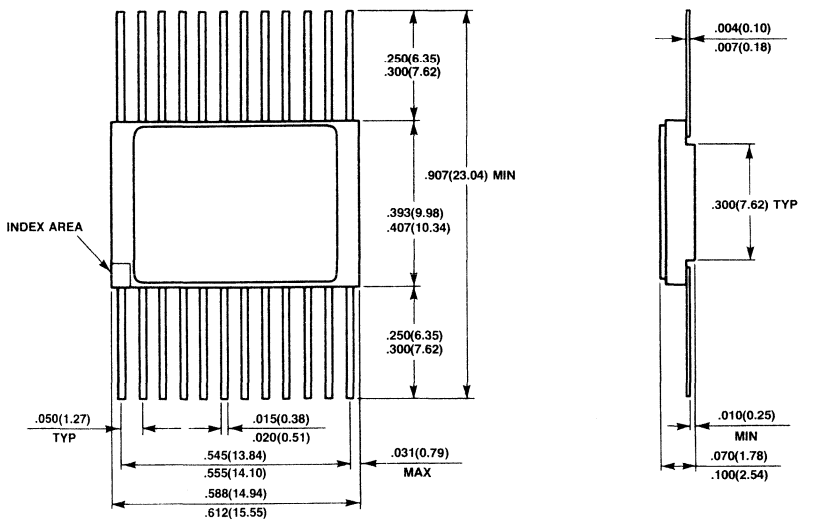
Package Dimensions

Dimensions in inches
(millimeters)

24-Lead Ceramic (CERDIP) Dual In-Line Package (Case No.: DIP-24C-C01)

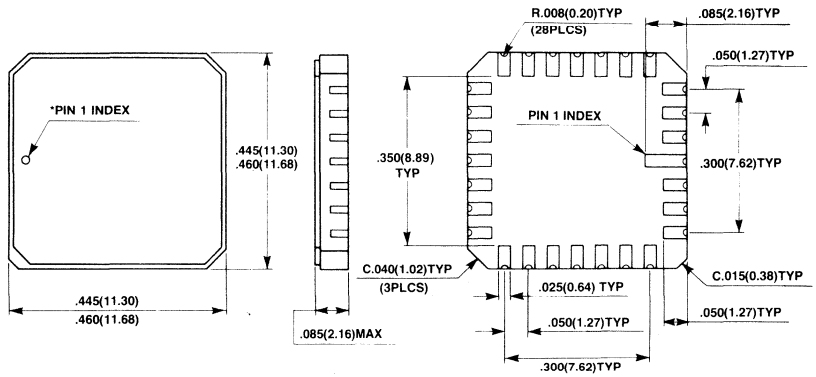


24-Lead Ceramic (Metal Seal) Flat Package (Case No.: FPT-24C-A02)



Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

28-Pad Ceramic (Metal Seal) Leadless Chip Carrier
(Case No.: LCC-28C-A02)



*SHAPE OF PIN 1 INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

Advanced Information

Availability Q2 '86

Bipolar PROM

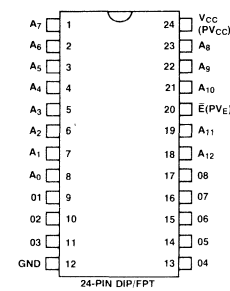
FUJITSU

■ MB7144Y

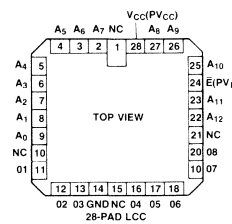
High Speed 65536-Bit
Schottky TTL PROM

Features

- **Organization:**
  8192 × 8-bits
- **Process:**
  Schottky TTL
- **Program:**
  Diffused Eutectic Aluminum Process (DEAP)
- **Output:**
  Three-State
- **Power Supply:**
  +5V ±5%
- **Power Dissipation:**
  998 mW max.
- **Address Access Time:**
  45 ns max.
- **Package:**
  24-pin DIP/FPT
  28-pad LCC



24-PIN DIP/FPT



28-PAD LCC

FUJITSU

MB7144E-W

Programmable Schottky 65,536-Bit Read Only Memory

Description

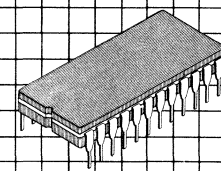
The Fujitsu MB7144E-W is a wide temperature range version of the 7144E field programmable read-only memory. Like the 7144E, it is organized as 8192 words by 8-bits.

The 7144E-W operates from 125 degrees C to −55 degrees C.

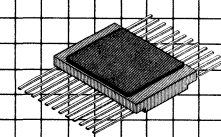
Fujitsu PROMS utilize a unique Shallow V-Groove (SVG) passive isolation process which, combined with a very thin epitaxial layer and the Schottky TTL process, provides small die sizes and very fast access times.

The memory is fabricated with all cells low, the "zero" value for positive logic. Logical "one" for a cell is achieved by programming. Individual cells are programmed to a logical "one" using the highly reliable Diffused Eutectic Aluminum Process (DEAP).

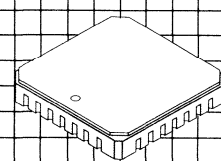
High programming yields are insured through the use of special test cells to verify programmability on each device prior to shipment.



Ceramic Package DIP-24C-C01



Ceramic Package FPT-24C-A02



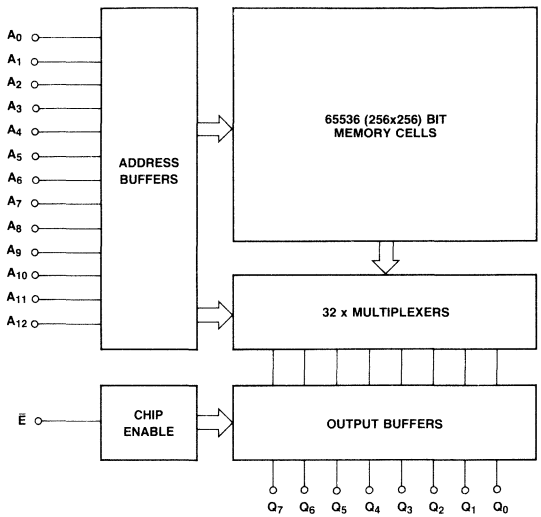
LCC-28C-A01

Features

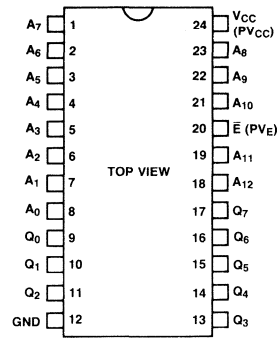
- **125°C to −55°C operating temperature range**
- **8192 words x 8-bits; fully decoded**
- **High levels of programmability and reliability proven in use**
- **Unique, reliable DEAP programming process**
- **Low power, simplified programming techniques**
- **Low current PNP inputs**
- **AC characteristics guaranteed over the full operating range**
- **Fast. 40 ns typical; 65 ns maximum access time**
- **TTL compatible inputs and outputs; open collector or three-state**
- **Single Chip Enable input**
- **JEDEC standard pinout; 24-pin flat, 28-LCC or 24-pin DIP packages**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

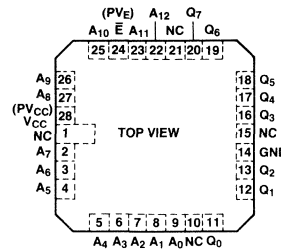
MB7144 Block Diagram and Pin Assignments



Pin Configuration for DIP/Flatpack



Pad Configuration



Absolute Maximum Ratings
(See Note)

Rating	Symbol	Value	Unit
Power supply voltage	V_{CC}	−0.5 to +7.0	V
Power supply voltage (during programming)	V_{CC}	−0.5 to +7.5	V
Input voltage	V_{IN}	−1.5 to 5.5	V
Input voltage (during programming)	V_{PRG}	22.5	V
Output voltage (during programming)	V_{PRG}	−0.5 to +22.5	V
Input current	I_{IN}	−20	mA
Input current (during programming)	I_{PRG}	+270	mA
Output current	I_{OUT}	+100	mA
Output current (during programming)	I_{PRG}	+150	mA
Storage temperature	T_{STG}	−65 to +150	°C
Output voltage	V_{OUT}	−0.5 to V_{CC}	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet.

Guaranteed Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input low voltage	V_{IL}	0		0.8	V
Input high voltage	V_{IH}	2.0		5.5	V
Ambient temperature	T_A	−55		125	°C

Capacitance
(f = 1 MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25°C)

Parameter	Symbol	Min	Typ	Max	Unit
Input capacitance	C_I			10	pF
Output capacitance	C_O			15	pF

DC Characteristics
(Full guaranteed operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Input leakage current (V_{IH} = 5.5V)	I_R			40	μA
Input load current (V_{IL} = 0.45V)	I_F			−250	μA
Output low voltage (I_{OL} = 16 mA)	V_{OL}			0.50	V
Output leakage current (V_O = 2.4V, chip disabled)	I_{OIH}			40	μA
Output leakage current (V_O = 0.45V, chip disabled)	I_{OIL}			−40	μA
Input clamp voltage (I_{IN} = −18 mA)	V_{IC}			−1.2	V
Power supply current (V_{IN} = OPEN or GND)	I_{CC}		160	190	mA
Output high voltage*1 (I_O = −2.4 mA)	V_{OH}	2.4			V
Output short circuit current*1 (V_O = GND)	I_{OS}*	−15		−60	mA

Note: *1 Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled (V_{ICE} = 0.4V, V_{ICE} = 2.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

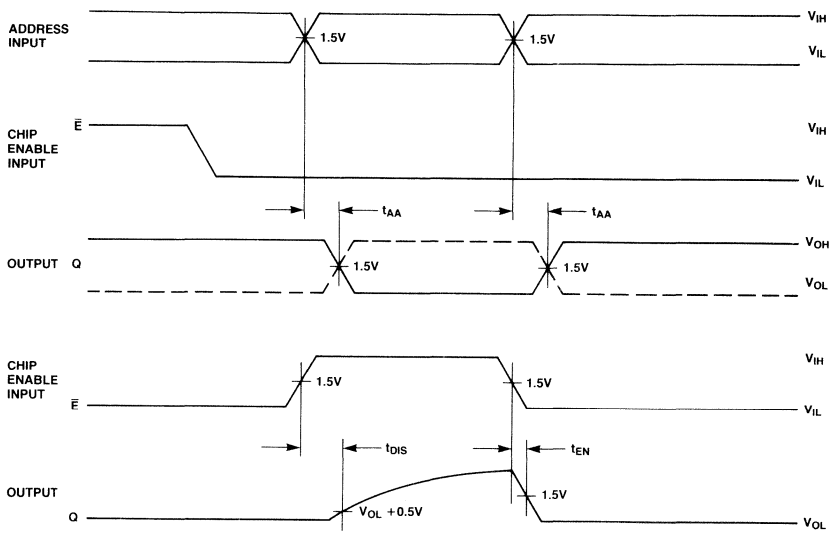
AC Characteristics
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB7144E-W Typ	MB7144E-W Max	Unit
Access time (via address input)	t_{AA}	40	65	ns
Output disable time	t_{DIS}	25	40	ns
Output enable time	t_{EN}	25	40	ns

AC Characteristics

(Continued)
(Recommended operating conditions unless otherwise noted.)

Operation Timing Diagram



NOTE: OUTPUT DISABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO REACH A HIGH RESISTANCE STATE WHEN THE CHIP ENABLE IS TAKEN HIGH. OUTPUT ENABLE TIME IS THE TIME TAKEN FOR THE OUTPUT TO BECOME ACTIVE WHEN THE CHIP ENABLE IS TAKEN LOW. THE HIGH RESISTANCE STATE IS DEFINED AS A POINT ON THE OUTPUT WAVEFORM EQUAL TO A ΔV OF 0.5V FROM THE ACTIVE OUTPUT LEVEL.

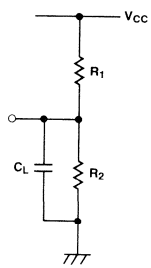
AC Test Conditions

Input Conditions

Amplitude ..... 0V to 3V
Rise and Fall Time ..... 5 ns from 1V to 2V
Frequency ..... 1 MHz

TRUTH TABLE

	MB7144-W		
	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30 pF
t_{DIS}	300Ω	600Ω	30 pF
t_{EN}	300Ω	600Ω	30 pF



Input/Output Circuit Information

Input

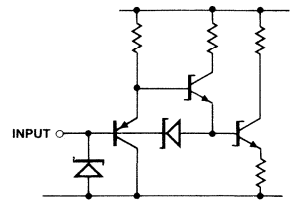
In the input circuit, Schottky TTL circuit technology is used to achieve high-speed operation. The PNP transistor in the first stage of input circuit remarkably improves input high/low current characteristics. Also, the input circuit includes a protection diode for reliable operation.

Three-State Output

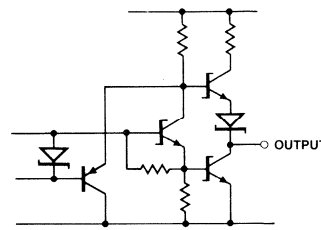
A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

MB7144 Input



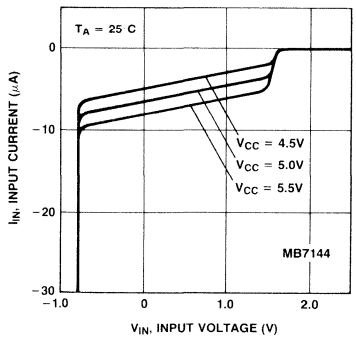
MB7144 Output



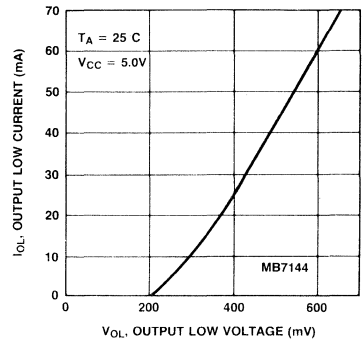
Also in the output circuit, Schottky TTL circuit technology is used to achieve high-speed operation. Also, a PNP transistor provided in the output circuit decreases the load for the Chip Enable circuit.

Typical Characteristics Curves

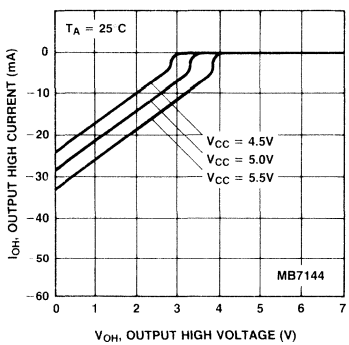
I_{IN} Input Current vs. V_{IN} Input Voltage



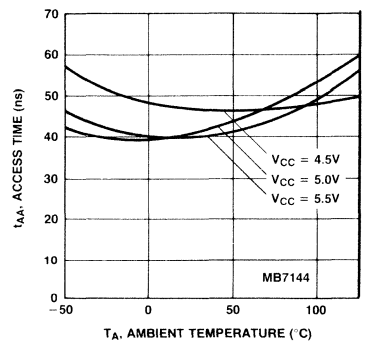
I_{OL} Output Low Current vs. V_{OL} Output Low Voltage



I_{OH} Output High Current vs. V_{OH} Output High Voltage

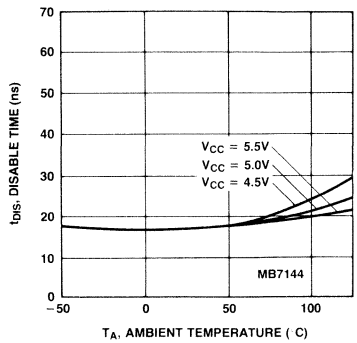


t_{AA} Access Time vs. Ambient Temperature

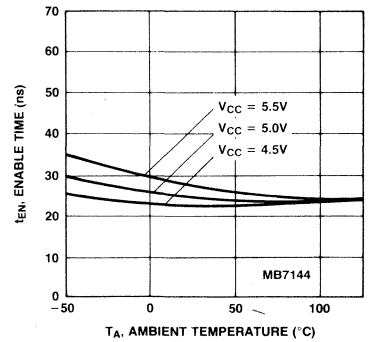


Typical Characteristics Curves
(Continued)

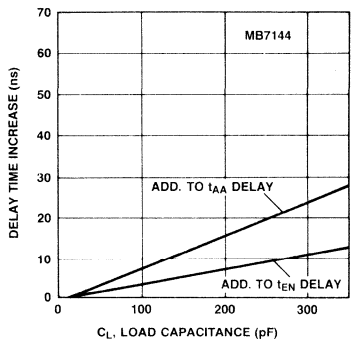
t_{DIS} Disable Time vs. Ambient Temperature



t_{EN} Enable Time vs. Ambient Temperature



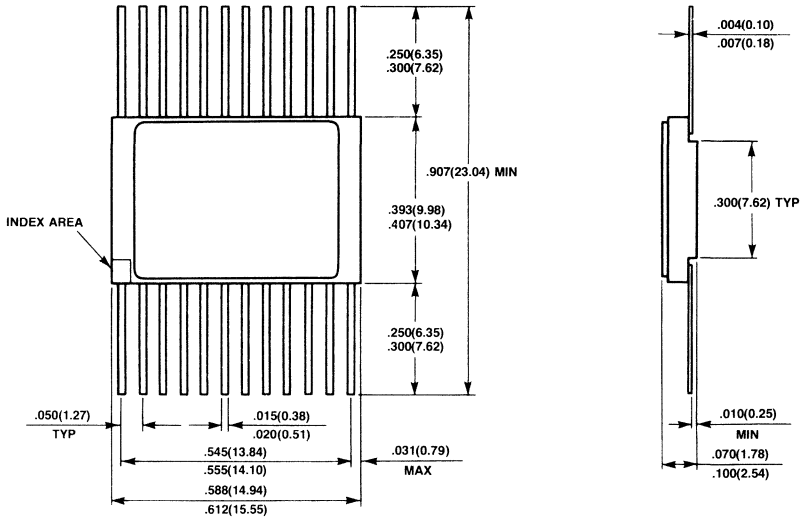
Delay Time Increase vs. C_L Load Capacitance



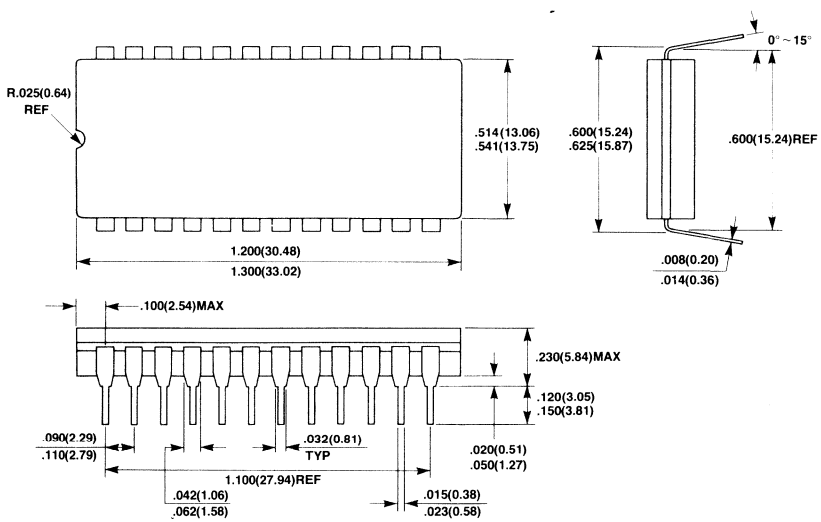
Package Dimensions

Dimensions in inches
(millimeters)

24-Lead Ceramic (Metal Seal) Flat Package (Case No.: FPT-24C-A02)

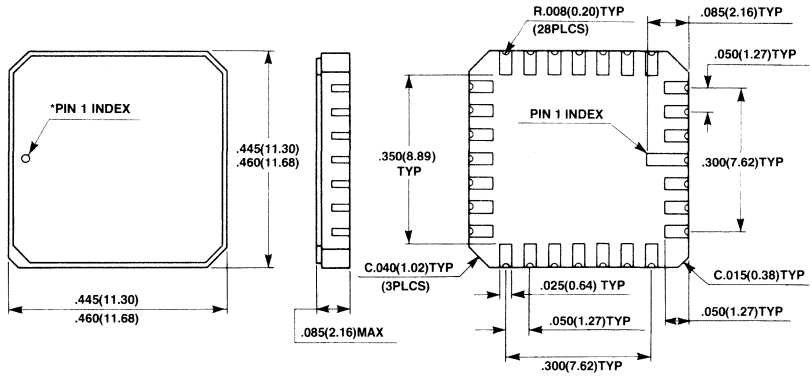


24-Lead Ceramic (CERDIP) Dual In-Line Package (Case No.: DIP-24C-C01)



Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

28-Pad Ceramic (Metal Seal) Leadless Chip Carrier
(Case No.: LCC-28C-A01)



*SHAPE OF PIN INDEX: SUBJECT TO CHANGE WITHOUT NOTICE

MB7151E/H, MB7152E/H/Y
Schottky TTL 16,384-Bit Bipolar Programmable Read-Only Memory

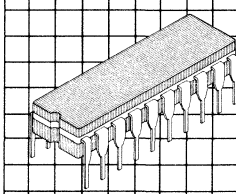
Description

The Fujitsu MB7151 and MB7152 are high speed Schottky TTL electrically field programmable read only memories organized as 4096 words by 4-bits. With uncommitted collector outputs provided on the MB7151 and three-state outputs on the MB7152, memory expansion is simple.

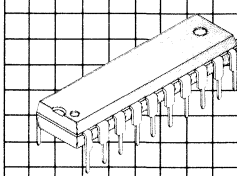
The memory is fabricated with all logic "zeros" (positive logic). Logic level "ones" can be programmed by the highly reliable DEAP™ (Diffused Eutectic Aluminum Process) according to simple programming procedures.

The sophisticated passive isolation termed IOP (Isolation by Oxide and Polysilicon) with thin epitaxial layer and Schottky TTL process permits minimal chip size and fast access time.

The extra test cells and unique testing methods provide enhanced correlation between programmed and unprogrammed circuits in order to perform AC, DC and programming test prior to shipment. This results in extremely high programmability.



Cerdip Package
DIP-20C-C03

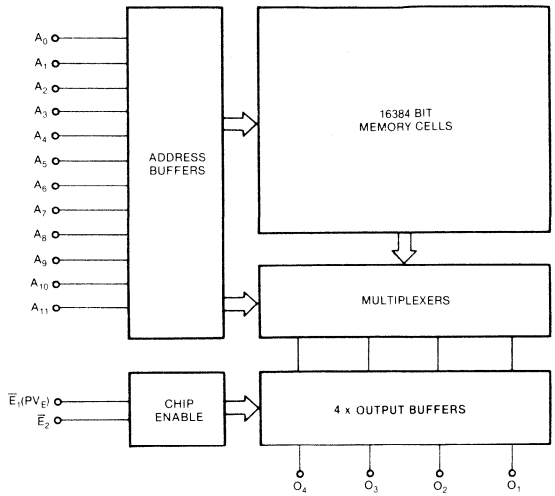


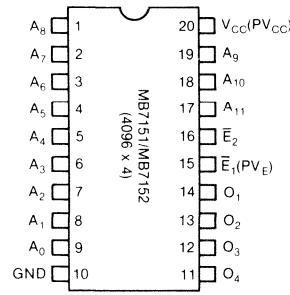
Plastic Package
DIP-20P-M01

Features

- Single +5V supply voltage
- Organized as 4096 words by 4-bits, fully decoded
- Proven higher programmability and reliability
- Programming by DEAP™ (Diffused Eutectic Aluminum Process)
- Simplified and lower power programming
- Low current PNP inputs
- AC characteristics guaranteed over full operating voltage and temperature range via unique testing techniques
- Fast access time, 35nsec typ.
  - E—55nsec max.
  - H—45nsec max.
  - Y—35nsec max.
- TTL compatible inputs and outputs
- Open collector outputs, MB7151
- Three-state outputs, MB7152
- Two chip enables for simplified memory expansion
- 300mil 20-pin DIP package

Block Diagram and Pin Assignment





Absolute Maximum Ratings
(See Note)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	−0.5 to +7.0	V
Power Supply Voltage (during programming)		V_{CC}	−0.5 to +7.5	V
Input Voltage		V_{IN}	−1.5 to +5.5	V
Input Voltage (during programming)		V_{PRG}	22.5	V
Output Voltage (during programming)		V_{PRG}	−0.5 to +22.5	V
Input Current		I_{IN}	−20	mA
Input Current (during programming)		I_{PRG}	+270	mA
Output Current		I_{OUT}	+100	mA
Output Current (during programming)		I_{PRG}	+150	mA
Storage Temperature	Ceramic: Plastic:	T_{stg}	−65 to +150 −40 to +125	°C
Output Voltage		V_{OUT}	−0.5 to V_{CC}	V

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Capacitance
(f = 1MHz, V_{CC} = +5V, V_{IN} = +2V, T_A = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I			10	pF
Output Capacitance	C_O			15	pF

Guaranteed Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	0		0.8	V
Input High Voltage	V_{IH}	2.0		V_{CC}	V
Ambient Temperature	T_A	0		75	°C

DC Characteristics

(Full guaranteed operating conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 5.5 V)		I_R			40	μA
Input Load Current (V_{IL} = 0.45 V)		I_F			−250	μA
Output Low Voltage (I_{OL} = 10 mA)		V_{OL}			0.45	V
Output Low Voltage (I_{OL} = 16 mA)		V_{OL}			0.50	V
Output Leakage Current (V_O = 2.4V, Chip disabled)	MB7151	I_{OLK}			40	μA
Output Leakage Current (V_O = 2.4V, Chip disabled)	MB7152	I_{OIH}			40	μA
Output Leakage Current (V_O = 0.45V, chip disabled)	MB7152	I_{OIL}			−40	μA
Input Clamp Voltage (I_{IN} = − 18 mA)		V_{IC}			−1.2	V
Power Supply Current (V_{IN} = OPEN or GND)		I_{CC}		120	170	mA
Output High Voltage (I_O = − 2.4 mA)	MB7152	V_{OH}*	2.4			V
Output Short Circuit Current (V_O = GND)	MB7152	I_{OS}*	−15		−60	mA

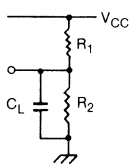
***Note:** Denotes guaranteed characteristics of the output high-level (ON) state when the chip is enabled (V_{ICE} = 0.4V) and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

AC Characteristics

(Full guaranteed operating conditions unless otherwise noted.)

Parameter	Symbol	E Typ	E Max	H Typ	H Max	MB7152Y Typ	MB7152Y Max	Unit
Access Time (via address input)	t_{AA}	35	55	35	45	28	35	ns
Output Disable Time	t_{DIS}		40		40		30	ns
Output Enable Time	t_{EN}		40		40		30	ns

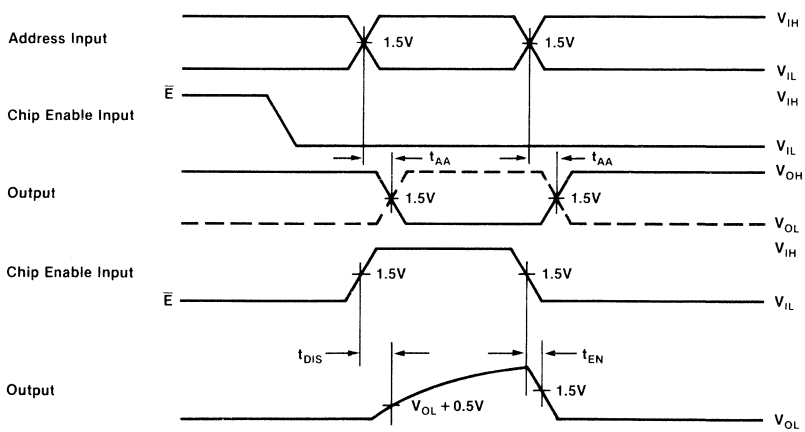
AC Test Conditions



Input Conditions
Amplitude: 0V to 3V
Rise and Fall Time: 5ns from 1V to 2V
Frequency: 1MHz

	MB7151/MB7152 R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30pF
t_{DIS}	300Ω	600Ω	30pF
t_{EN}	300Ω	600Ω	30pF

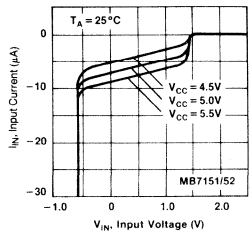
Operation Timing Diagram



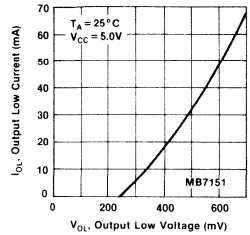
Note: Output disable time is the time taken for the output to reach a high resistance state when the chip enable is taken high (disabled). Output enable time is the time taken for the output to become active when all of chip enables are taken low (enabled). The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

Typical Characteristics Curves

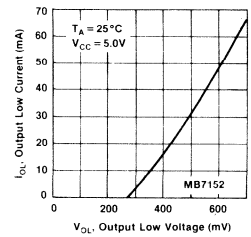
I_{IN} Input Current vs. V_{IN} Input Voltage



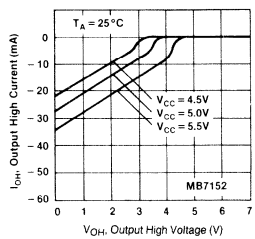
I_{OL} Output Low Current vs. V_{OL} Output Low Voltage



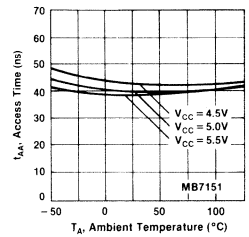
I_{OL} Output Low Current vs. V_{OL} Output Low Voltage



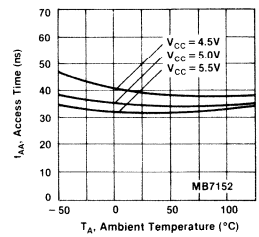
I_{OH} Output High Current vs. V_{OH} Output High Voltage



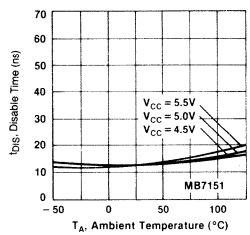
t_{AA} Access Time vs. Ambient Temperature



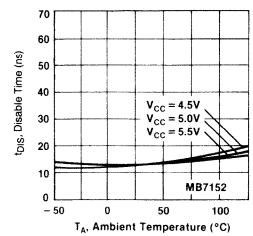
t_{AA} Access Time vs. Ambient Temperature



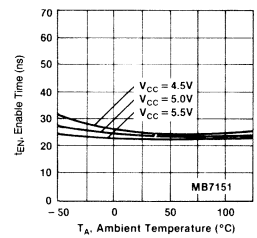
t_{DIS} Disable Time vs. Ambient Temperature



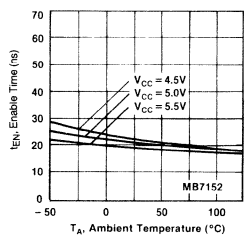
t_{DIS} Disable Time vs. Ambient Temperature



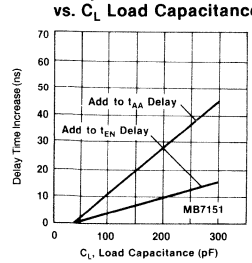
t_{EN} Enable Time vs. Ambient Temperature



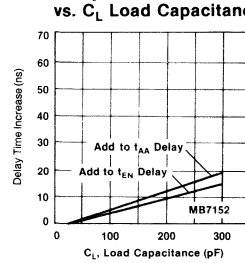
t_{EN} Access Time vs. Ambient Temperature



Delay Time Increase vs. C_L Load Capacitance



Delay Time Increase vs. C_L Load Capacitance



Input/Output Circuit Information

Input Circuit

Schottky TTL circuit technology is used in the input circuit to achieve high-speed operation. A PNP transistor in the first stage of input circuit improves input high/low current characteristics remarkably. The input circuit also includes a protection diode for reliable operation.

Open Collector Output

The open—collector output is often utilized in high-speed applications where power dissipation must be minimized. When the device is switched, there is no current sourced from the supply rail. Consequently, the current spike normally associated with TTL totem-pole outputs is eliminated. In high-frequency applications, this minimizes noise problems (false triggering) as well as power drain. For example, the transient current (low impedance high-level to low impedance low-level) is typically 30mA for the MB7152 (three-state) compared to 0mA for the MB7151 (open-collector).

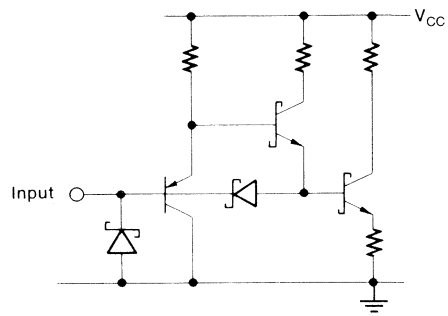
Three-State Output

A "three-state" output is a logic element which has three distinct output states of ZERO, ONE and OFF (wherein OFF represents a high-impedance condition which can neither sink nor source current at a definable logic level). Effectively, then, the device has all the desirable features of a totem-pole TTL output (e.g., greater noise immunity, good rise time, line driving capacity), plus the ability to connect to bus-organized systems.

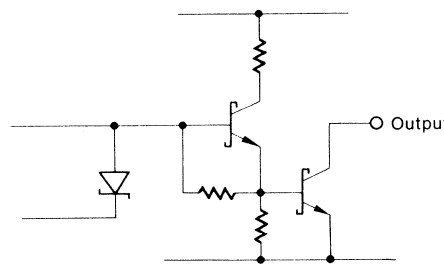
In the case where two devices are on at the same time, the possibility exists that they may be in opposite low impedance states simultaneously; thus, the short circuit current from one enabled device may flow through the other enabled device. While physical damage under these conditions is unlikely, system noise problems could result. Therefore, the system designer should consider these factors to ensure that this condition does not exist.

Schottky TTL circuit technology is also used in the output circuit to achieve high-speed operation. A PNP transistor is also provided in the output circuit and is effective in decreasing a load for the chip enable circuit.

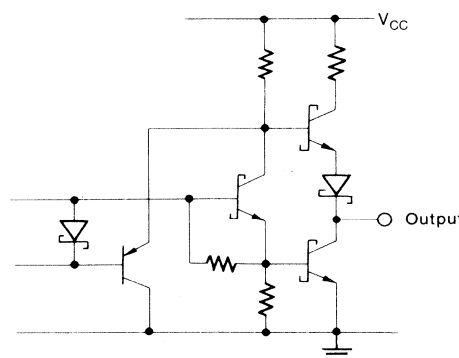
Common Input Circuit



Common Open Collector Output Circuit

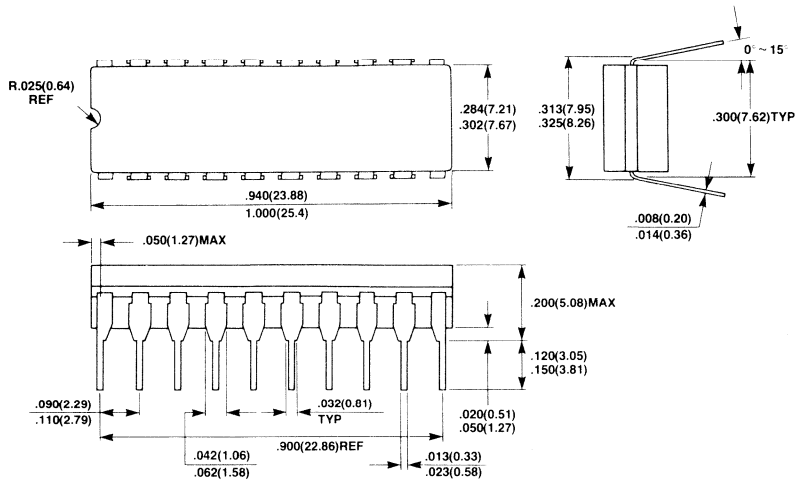


Common Three-State Output Circuit



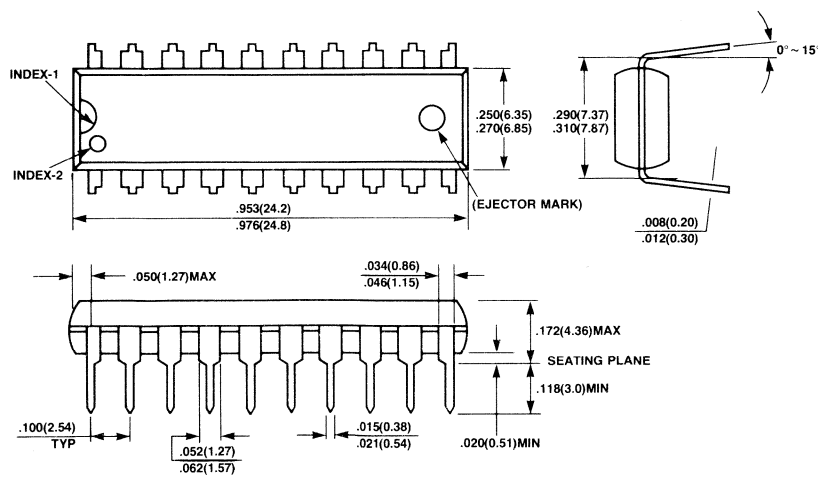
Package Dimensions
Dimensions in inches
(millimeters)

20-Pin Cerdip Dual In-Line Package
DIP-20C-C03



Package Dimensions
(Continued)
Dimensions in inches
(millimeters)

20-Pin Plastic Dual In-Line Package
DIP-20P-M01



Advanced Information

Availability Q4 '86

Bipolar PROM

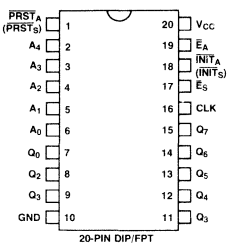
FUJITSU

■ MB7212RA-20/-25, MB7212RS-20/-25

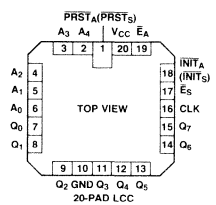
Schottky 256-Bit
Registered Output PROM

Features

- **Organization:**
  32 × 8-bits
- **Process:**
  Schottky TTL
- **Program:**
  Diffused Eutectic Aluminum Process (DEAP)
- **Output:**
  Three-State Output
  Output register can be initialized asynchronously (MB7212RA) or synchronously (MB7212RS)
- **Clock Access Time:**
  20 ns max. (MB7212RA/RS-20)
  25 ns max. (MB7212RA/RS-25)
- **Power Supply:**
  +5V ±5%
- **Power Dissipation:**
  788 mW max.
- **Package:**
  20-pin DIP/FPT
  20-pad LCC



20-PIN DIP/FPT



20-PAD LCC

MB7226RA-20, MB7226RA-25, MB7226RS-20, MB7226RS-25

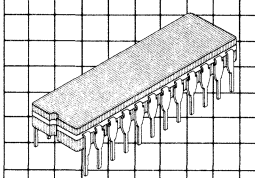
Schottky 4,096-Bit Registered Output PROM

Description

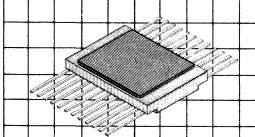
The Fujitsu MB7226 is a 4 K-bit bipolar programmable read-only memory circuit, with registered output (output data is latched in a register). The output register can be initialized to all 0s or all 1s, either synchronously (MB7226RS) or asynchronously (MB7226RA). Three-state outputs can also be enabled either synchronously or asynchronously, in either model. DEAP memory cells are used to provide fast and reliable programming.

Features

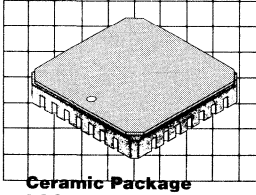
- **512 word x 8 bit PROM data organization**
- **Fast clock access time: 20 ns (MB7226RA/RS-20) 25 ns (MB7226RA/RS-25)**
- **Output register for data reads**
- **Register can be initialized to all 0s or 1s.**
- **Register can be initialized synchronously (MB7226RS) or asynchronously (MB7226RA).**
- **Single-supply +5V operation**
- **TTL-compatible I/O**
- **Fast Schottky bipolar circuitry**
- **Low current inputs**
- **Three-state outputs**
- **Outputs can be enabled either synchronously or asynchronously.**
- **DEAP (diffused eutectic aluminum process) memory cells are reliable and easily programmed.**
- **Test cells allow extensive testing of AC, DC, and programming characteristics before shipment.**



Ceramic Package DIP-24C-C04



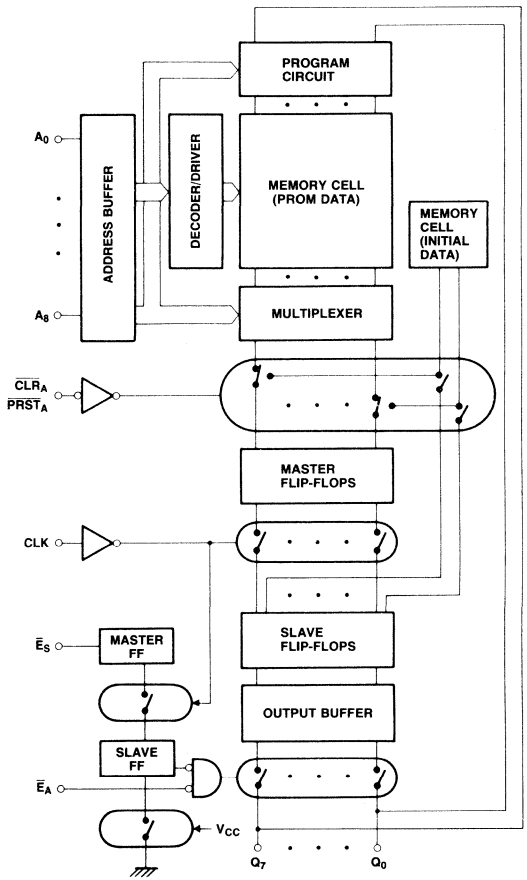
Ceramic Package FPT-24C-A01

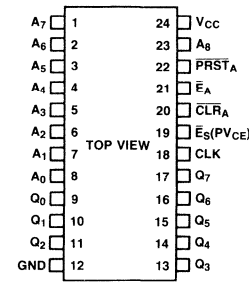


Ceramic Package LCC-28C-A01

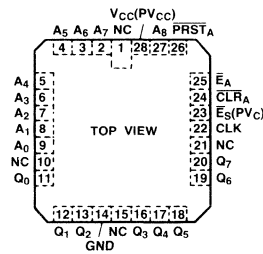
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB7226RA Block Diagram and Pin Assignments





MB7226RA Pinout

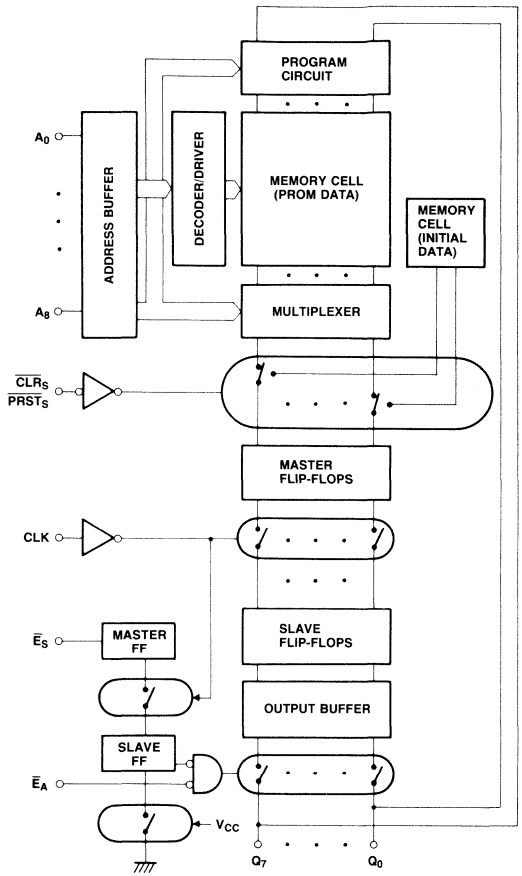


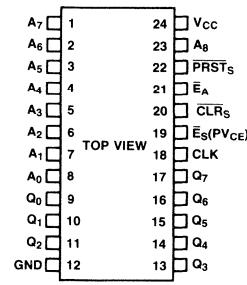
MB7226RA LCC Pinout

Input					Output	Operating mode	Remarks
$\overline{PRST}_A$	$\overline{CLR}_A$	CLK	$\overline{E}_A$	$\overline{E}_S$			
L	L	X	L	L	H	*1	
L	H	X	L	L	INITIAL DATA (H)	INITIALIZE	PROGRAMMED
H	L	X	L	L	INITIAL DATA (L)	INITIALIZE	PROGRAMMED
H	H	↑	L	L	PROM DATA	LOAD REGISTER	
X	X	↑	X	H	Z	CHIP DISABLE	
X	X	X	H	X	Z	CHIP DISABLE	

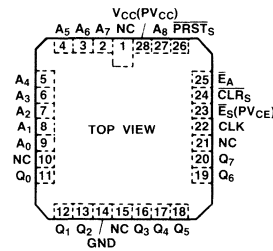
*1 When the $\overline{PRST}_A$ and $\overline{CLR}_A$ inputs are brought high at the same time, the output cannot be determined either H or L.

MB7226RS Block Diagram and Pin Assignments





MB7226RS Pinout



MB7226RS LCC Pinout

Input					Output	Operating mode	Remarks
$\overline{PRST_S}$	$\overline{CLR_S}$	CLK	$\overline{E_A}$	$\overline{E_S}$			
L	L	↑	L	L	—	—	
L	H	↑	L	L	INITIAL DATA (H)	INITIALIZE	PROGRAMMED
H	L	↑	L	L	INITIAL DATA (L)	INITIALIZE	PROGRAMMED
H	H	↑	L	L	PROM DATA	LOAD REGISTER	
X	X	↑	X	H	Z	CHIP DISABLE	
X	X	X	H	X	Z	CHIP DISABLE	

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power-supply voltage	V_{CC}	−0.5 to +7.0	V
Input voltage	V_{IN}	−1.5 to +5.5	V
Input current	I_{IN}	−20	mA
Output current	I_{OUT}	+100	mA
Power-supply voltage (during programming)	V_{CCP}	−0.5 to +7.5	V
Input voltage (during programming)	V_{IPRG}	+22.5	V
Input current (during programming)	I_{IPRG}	+270	mA
Output voltage (during programming)	V_{OPRG}	−0.5 to +22.5	V
Output current (during programming)	I_{OPRG}	+150	mA
Storage temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Read Operations

Overview

During PROM reads, data is shifted through a register, made of master-slave flip-flops, before appearing at the outputs. When a new address is applied to the address inputs (A_0 through A_8), new data appears in the master register. At the next clock pulse this data is transferred to the slave register. The slave register data appears at the three-state outputs when both chip-enable inputs are low. (Outputs are automatically disabled during power-up, when the inputs are in an indeterminate state.) For synchronous operation, the $\overline{E}_A$ input is kept low. Bringing the $\overline{E}_S$ input low will then enable the outputs at the next clock pulse, while bringing $\overline{E}_S$ high will disable them at the next clock pulse. For asynchronous operation, the $\overline{E}_S$ input is kept low. Bringing $\overline{E}_A$ low will then immediately enable the outputs, while bringing it high will immediately disable them.

If the $\overline{CLR}$ or $\overline{PRST}$ input is brought low the register latch is loaded with all 0s ($\overline{CLR}$) or all 1s ($\overline{PRST}$), rather than with PROM data. In the MB7226RS the master register is loaded immediately, and the contents are transferred to the slave register at the next clock pulse. In the MB7226RA both the master and slave registers are loaded immediately.

Timing Considerations

a) PROM Data Read

After an address change, address setup time $t_S(A)$ must elapse before the master register contains valid new PROM data. The clock must then rise, within address hold time $t_H(A)$, to shift the data to the slave register. The data will appear at the outputs within clock access time $t_A(CLK)$ after the rising edge of the clock, if the outputs had been previously enabled.

If the outputs were disabled when the data was shifted, and are subsequently enabled by bringing $\overline{E}_A$ low, asynchronous chip enable time $t_{EN}(\overline{E}_A)$ must elapse before the data appears at the outputs.

If $\overline{E}_S$ is brought low to enable the outputs, clock enable time $t_{EN}(CLK)$ must elapse after the rising edge of the next clock. During this time the data from the master register is shifted to the slave register and appears at the outputs.

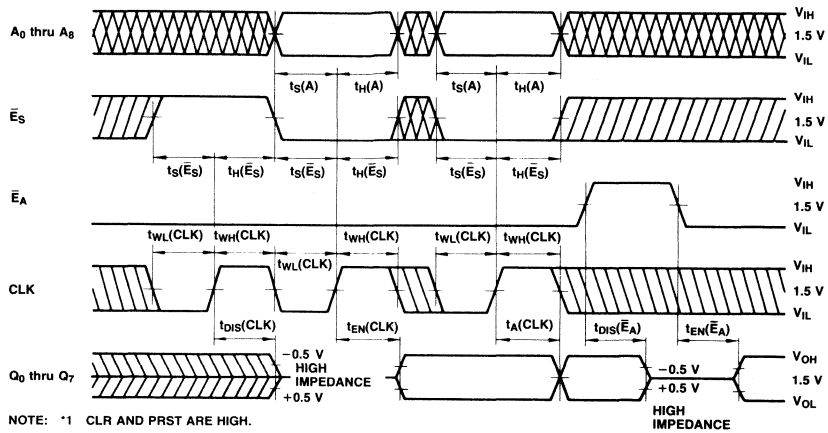
In the MB7226RA, when the registers have been initialized by $\overline{CLR}$ or $\overline{PRST}$, and the initialize input is then brought high to select PROM data, asynchronous initialize recovery time $t_R(\overline{CLR}_A)$ or $t_R(\overline{PRST}_A)$ must elapse before the clock signal is applied.

b) Initial Data Read

In the MB7226RA after the $\overline{CLR}$ or $\overline{PRST}$ input is brought low, asynchronous initialize access time $t_A(\overline{CLR}_A)$ or $t_A(\overline{PRST}_A)$ must elapse before the initial data appears at the outputs.

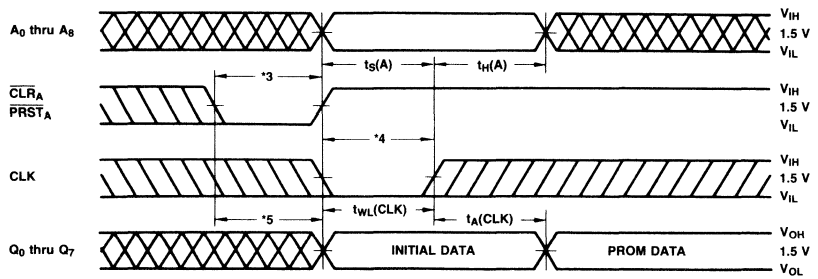
In the MB7226RS, after the $\overline{CLR}$ or $\overline{PRST}$ input is brought low, synchronous initialize access time $t_A(\overline{CLR}_S)$ or $t_A(\overline{PRST}_S)$ must elapse before valid initial data appears in the master register. It is then shifted and output in the same manner as PROM data.

Prom Data Read Timing*1



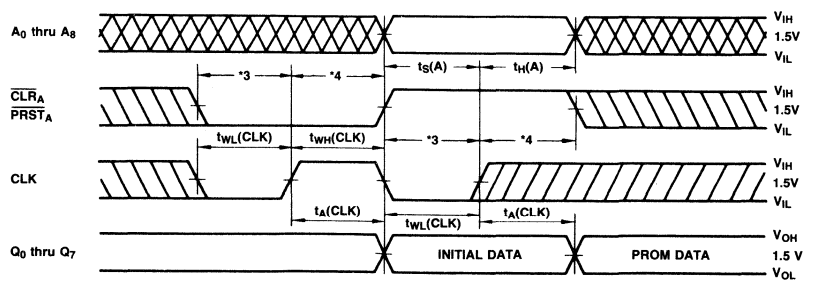
NOTE: *1 CLR AND PRST ARE HIGH.

Asynchronous Initial Data Read Timing (MB7226RA)*1



NOTES: *1 E_A, E_S INPUTS ARE LOW.
*2 DON'T CARE.
*3 t_{WL} (CLR_A), t_{WL}($PRST_A$)
*4 t_R(CLR_A), t_R($PRST_A$)
*5 t_A(CLR_A), t_A($PRST_A$)

Synchronous Initial Data Read Timing (MB7226RS)*1



NOTES: *1 E_A, E_S INPUTS ARE LOW.
*2 DON'T CARE.
*3 t_S(CLR_S), t_S($PRST_S$)
*4 t_H(CLR_S), t_H($PRST_S$)

Data Read Specifications
(Guaranteed Operating Conditions)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Power-supply voltage	V_{CC}	4.75	5.0	5.25	V	T_A = 0°C to 75°C
Input low voltage	V_{IL}	0	—	0.8	V	
Input high voltage	V_{IH}	2.0	—	5.5	V	

AC Characteristics

Parameter	Symbol	Typ	MB7226RA/RS-20 Min	MB7226RA/RS-20 Max	MB7226RA/RS-25 Min	MB7226RA/RS-25 Max	Unit	Remarks
Address setup time	$t_S(A)$	20	30		35		ns	
Address hold time	$t_H(A)$	−5	0		0		ns	
Clock access time	$t_A(CLK)$	16		20		25	ns	
Clock pulse width	$t_{WH}(CLK)$ / $t_{WL}(CLK)$	10	20		20		ns	
Synchronous enable setup time	$t_S(E_S)$	5	10		15		ns	
Synchronous enable hold time	$t_H(E_S)$	0	5		5		ns	
Asynchronous initialize access time	$t_A(\overline{CLR}_A)$ / $t_A(\overline{PRST}_A)$	17		25		25	ns	MB7226RA
Asynchronous initialize recovery time	$t_R(\overline{CLR}_A)$ / $t_R(\overline{PRST}_A)$	8	20		20		ns	MB7226RA
Asynchronous initialize pulse width	$t_{WL}(\overline{CLR}_A)$ / $t_{WL}(\overline{PRST}_A)$	12	20		20		ns	MB7226RA
Synchronous initialize setup time	$t_S(\overline{CLR}_S)$ / $t_S(\overline{PRST}_S)$	TBD	TBD		TBD		ns	MB7226RS
Synchronous initialize hold time	$t_H(\overline{CLR}_S)$ / $t_H(\overline{PRST}_S)$	TBD	TBD		TBD		ns	MB7226RS
Clock enable time	$t_{EN}(\overline{CLK})$	18		25		30	ns	
Asynchronous enable time	$t_{EN}(\overline{E}_A)$	15		25		30	ns	
Clock disable time*2	$t_{DIS}(CLK)$	18		25		30	ns	
Asynchronous disable time*2	$t_{DIS}(\overline{E}_A)$	11		25		30	ns	

Notes: *1 At T_A = 25°C and V_{CC} = 5.0V.
*2 Measured at a point on the output waveform 0.5V from the active output level.

DC Characteristics

(Under Guaranteed Operating Conditions)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input current	I_{IH}	V_{IH} = 5.5V	—	—	40	μA
	I_{IL}	V_{IL} = 0.45V	—	—	−250	μA
Input clamp voltage	V_{IC}	I_I = −18 mA	—	—	−1.2	V
Output low voltage	V_{OL}	I_{OL} = 10 mA	—	—	0.45	V
		I_{OL} = 16 mA	—	—	0.5	μA
Output leakage current (Chip disabled)	I_{OIL}	V_O = 0.45V	—	—	−40	μA
	I_{OIH}	V_O = 2.4V	—	—	40	μA
Output high voltage*1	V_{OH}	I_{OH} = −2.4 mA	2.4	—	—	V
Output short-circuit current*1	I_{OS}	V_O = 0V	−15	—	−60	mA
Power supply current	I_{CC}	V_I = Open or 0V	—	120	170	mA
Power dissipation	P_D	V_I = Open or 0V	—	600	893	mW

Note: *1 Denotes guaranteed characteristics of the output high-level state when the chip is enabled and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

Terminal Capacitance

(T_A = 25°C, V_{CC} = +5.0V, VIN = +2.0V, f = 1 MHz)

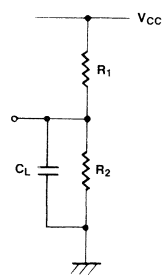
Parameter	Symbol	Typ	Max	Unit
Input terminal capacitance	C_{IN}	—	10	pF
Output terminal capacitance	C_{OUT}	—	15	pF

AC Test Conditions

INPUT CONDITIONS

Amplitude:	0V to 3V
Rise and Fall Time:	5 ns from 1V to 2V
Frequency:	1MHz

LOAD CONDITION



R_1 ... 300Ω
R_2 ... 600Ω
C_L ... 50pF

Fabrication Technology

Input/Output Circuits

The inputs use Schottky TTL circuitry to achieve a fast response time. A PNP transistor is used in the first stage to minimize switching current. Protection diodes are also included.

The three-state outputs (high, low; and high-impedance states) combine the advantages of totem-pole outputs (high noise immunity, fast rise time, ample line-driving capacity) and direct connection to bus-oriented systems. Schottky TTL circuitry is used for fast operation. A PNP transistor in the output circuit minimizes the load on the chip enable circuitry.

Memory Cells

The memory cells in the MB7226 are of the junction-shorting type, using DEAP (Diffused Eutectic Aluminum Process) technology. They are initially all in the 0 (low voltage) state. In this state, the cell's programmable element, a PN diode, blocks current flow. During programming, the diode's junction is shorted, allowing it to conduct current, and permanently changing the cell's state to 1 (high).

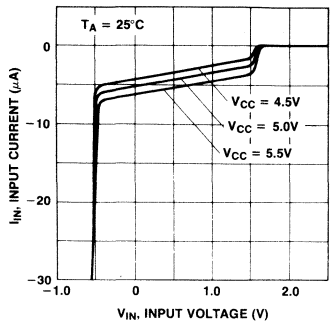
By applying reverse current pulses to the diode's cathode, the temperature at the junction is raised. When the temperature reaches the point where the silicon and aluminum form a eutectic, the eutectic diffuses from the surface of the metal-silicon contact region to the anode of the PN diode, and shorts the junction. The power dissipation at the junction immediately drops to less than one fifth, thus lowering the temperature. This drop in temperature stops further diffusion of the eutectic, and protects the PNP transistor from destruction.

In the memory cell array, the word line islands are divided by IOP (Isolation by Oxide and Polysilicon) passive isolation. Memory cells in the same island are divided by SVG (Shallow V-Groove) passive isolation. The vertically structured memory cells permit a high packing density.

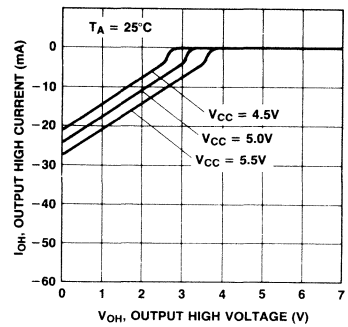
Typical Characteristics Curves

DC Characteristics

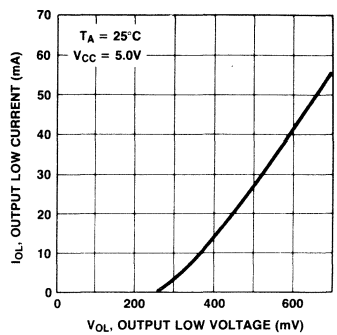
I_{IN} Input Current vs. V_{IN} Input Voltage



I_{OH} Output High Current vs. V_{OH} Output High Voltage

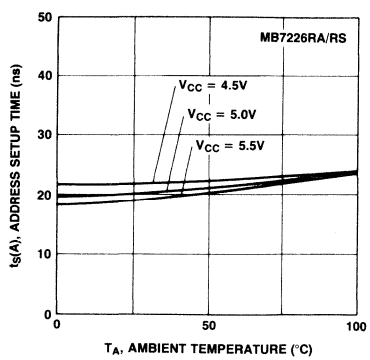


I_{OL} Output Low Current vs. V_{OL} Output Low Voltage

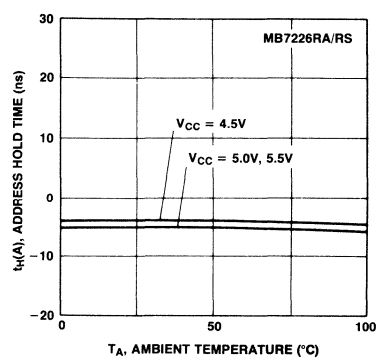


AC Characteristic

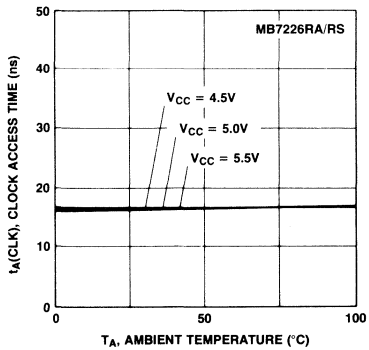
$t_S(A)$ Address Setup Time vs. Ambient Temperature



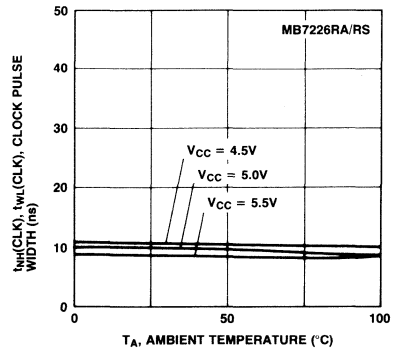
$t_H(A)$ Address Hold Time vs. Ambient Temperature



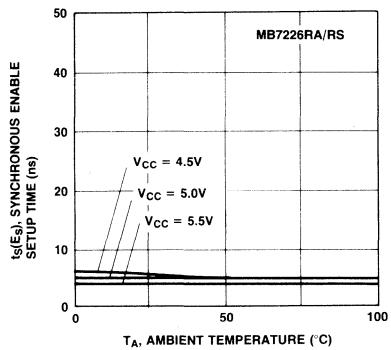
t_A(CLK) Clock Access Time vs. Ambient Temperature



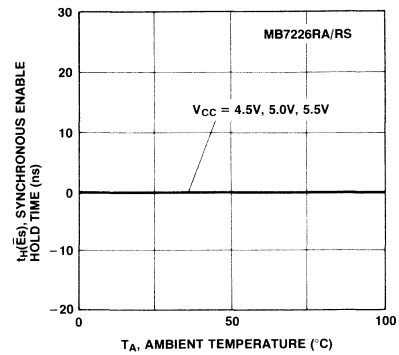
t_{WH}(CLK) and t_{WL}(CLK) Clock Pulse Width vs. Ambient Temperature



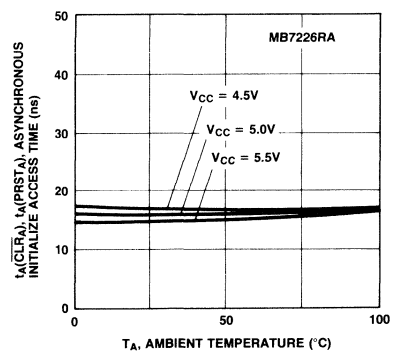
t_S(E_S) Synchronous Enable Setup Time vs. Ambient Temperature



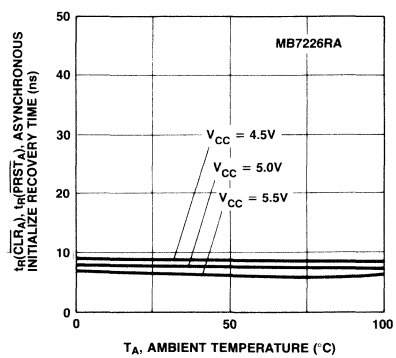
t_H($\overline{E_S}$) Synchronous Enable Hold Time vs. Ambient Temperature



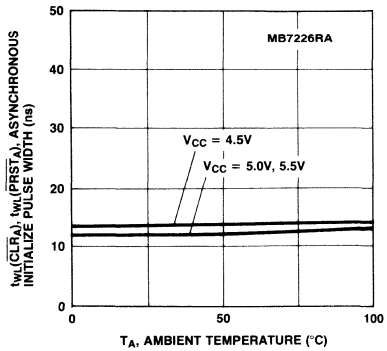
t_A($\overline{CLR_A}$) and t_A($\overline{PRST_A}$) Asynchronous Initialize Access Time vs. Ambient Temperature



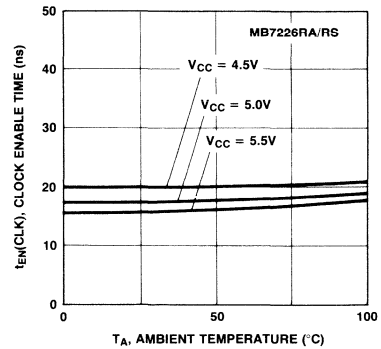
t_R($\overline{CLR_A}$) and t_R($\overline{PRST_A}$) Asynchronous Initialize Recovery Time vs. Ambient Temperature



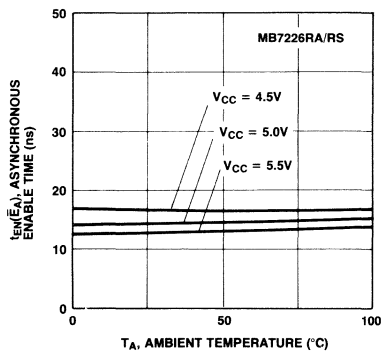
$t_{WL}(\overline{CLR}_A)$ and $t_{WL}(\overline{PRST}_A)$ Asynchronous Initialize Pulse Width vs. Ambient Temperature



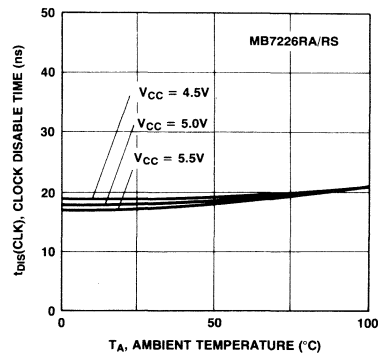
$t_{EN}(CLK)$ Clock Enable Time vs. Ambient Temperature



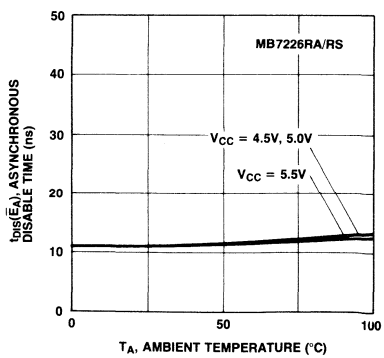
$t_{EN}(\overline{E}_A)$ Asynchronous Enable Time vs. Ambient Temperature



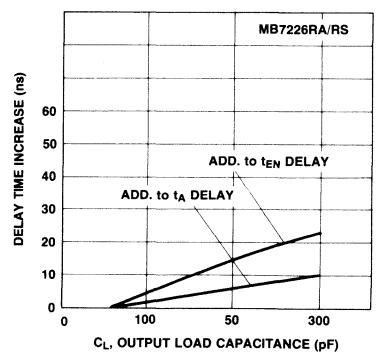
$t_{DIS}(CLK)$ Clock Disable Time vs. Ambient Temperature



$t_{DIS}(\overline{E}_A)$ Asynchronous Disable Time vs. Ambient Temperature

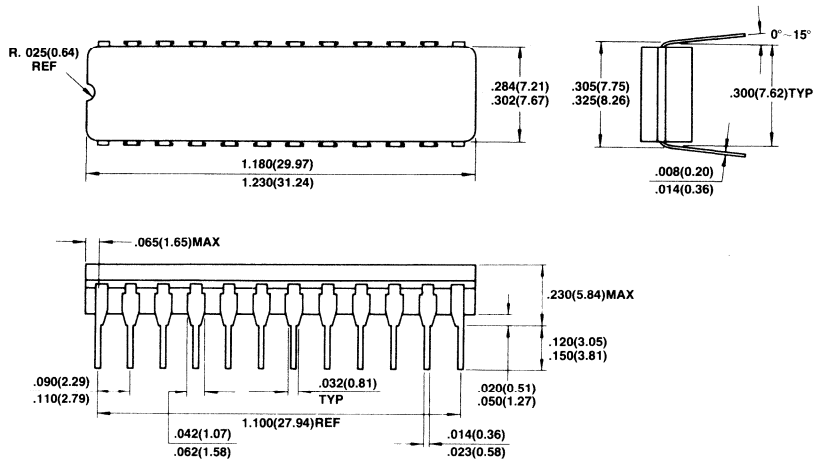


Delay Time Increase vs. Load Capacitance

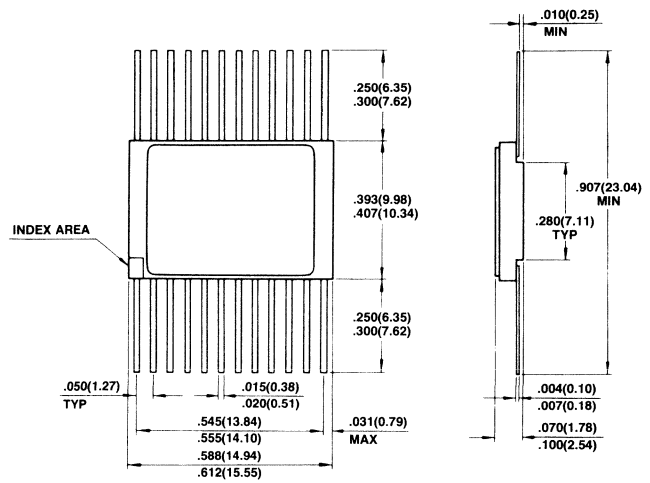


Package Dimensions
Dimensions in inches
(millimeters)

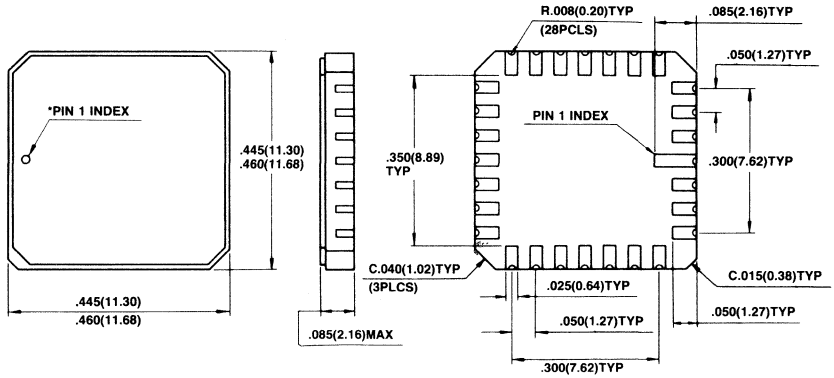
24-Lead Ceramic (CERDIP) Dual In-Line Package
(Case No.: DIP-24C-C04)



24-Lead Ceramic (Metal Seal) Flat Package
(Case No.: FPT-24C-A01)



28-Pad Ceramic (Metal Seal) Leadless Chip Carrier
(Case No.: LCC-28C-A01)



*Shape of Pin 1 index: Subject to change without notice

MB7232RA-20, MB7232RA-25, MB7232RS-20, MB7232RS-25

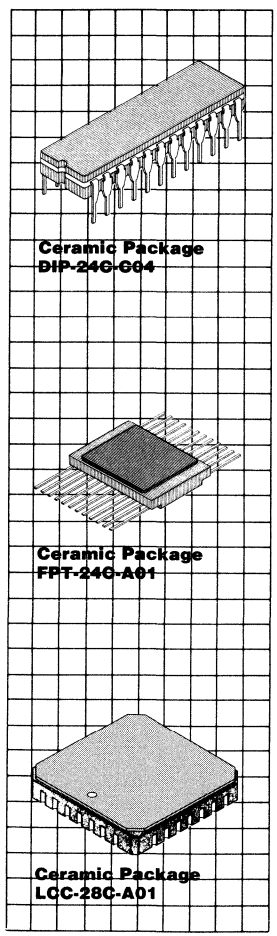
Schottky 8,192-Bit Registered Output PROM

Description

The Fujitsu MB7232 is an 8 K-bit bipolar programmable read-only memory circuit, with registered output (output data is latched in a register). The output register can be initialized to a programmable value, either synchronously (MB7232RS) or asynchronously (MB7232RA). Three-state outputs can also be enabled either synchronously or asynchronously, in either model. DEAP memory cells are used to provide fast and reliable programming.

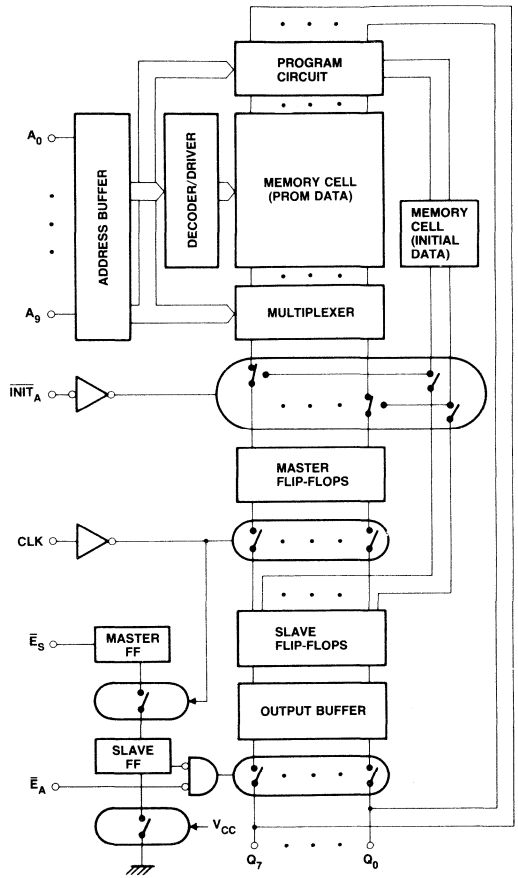
Features

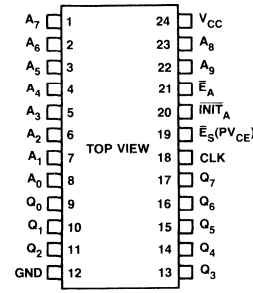
- **1024 word x 8 bit PROM data organization**
- **Fast clock access time: 20 ns (MB7232RA/RS-20) 25 ns (MB7232RA/RS-25)**
- **Output register can be preset to a field-programmable value**
- **Register can be preset synchronously (MB7232RS) or asynchronously (MB7232RA)**
- **Single +5V operation**
- **TTL-compatible I/O**
- **Low current inputs**
- **Three-state outputs**
- **Outputs can be enabled either synchronously or asynchronously**
- **Outputs are kept disabled on power-up**
- **DEAP (diffused eutectic aluminum process) memory cells are reliable and easily programmed**
- **Test cells allow extensive testing of AC, DC, and programming characteristics before shipment**



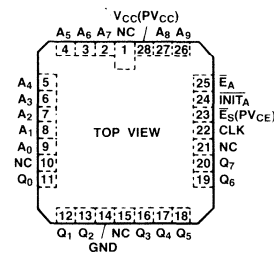
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB7232RA Block Diagram and Pin Assignments





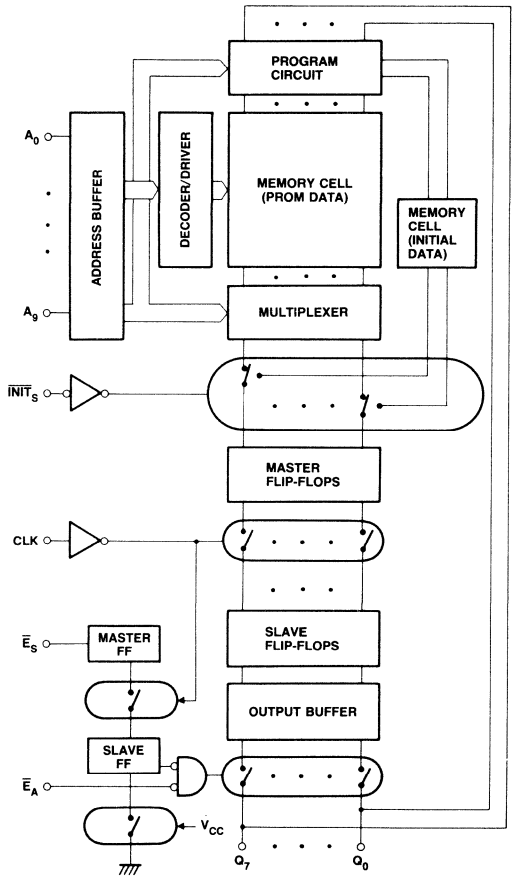
MB7232RA Pinout

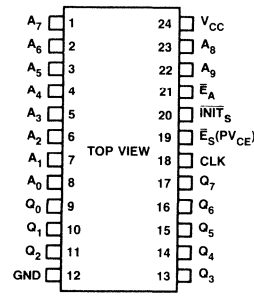


MB7232RA LCC Pinout

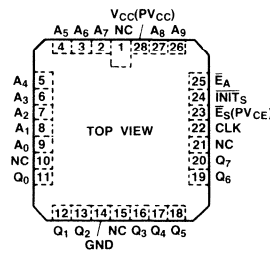
Input				Output	Operating mode	Remarks
$\overline{INIT}_A$	CLK	$\overline{E}_A$	$\overline{E}_S$			
L	X	L	L	INITIAL DATA	INITIALIZE	PRO-GRAMMABLE
H	↑	L	L	PROM DATA	LOAD REGISTER	
X	↑	X	H	Z	CHIP DISABLE	
X	X	H	X	Z	CHIP DISABLE	

MB7232RS Block Diagram and Pin Assignments





MB7232RS Pinout



MB7232RS LCC Pinout

Input				Output	Operating mode	Remarks
$\overline{INIT}_S$	CLK	$\overline{E}_A$	$\overline{E}_S$			
L	↑	L	L	INITIAL DATA	INITIALIZE	PRO-GRAMMABLE
H	↑	L	L	PROM DATA	LOAD REGISTER	
X	↑	X	H	Z	CHIP DISABLE	
X	X	H	X	Z	CHIP DISABLE	

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power-supply voltage	V_{CC}	−0.5 to +7.0	V
Input voltage	V_{IN}	−1.5 to +5.5	V
Input current	I_{IN}	−20	mA
Output current	I_{OUT}	+100	mA
Power-supply voltage (during programming)	V_{CCP}	−0.5 to +7.5	V
Input voltage (during programming)	V_{IPRG}	+22.5	V
Input current (during programming)	I_{IPRG}	+270	mA
Output voltage (during programming)	V_{OPRG}	−0.5 to +22.5	V
Output current (during programming)	I_{OPRG}	+150	mA
Storage temperature	T_{STG}	−65 to +150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Read Operations

Overview

During PROM reads, data is shifted through a register latch, made of master-slave flip-flops, before appearing at the outputs. When a new address is applied to the address inputs (A_0 through A_9), new data appears in the master register. At the next clock pulse this data is transferred to the slave register.

Both of the chip enable inputs must be low in order for the data in the slave register to appear at the outputs (Q_0 through Q_7). If the $\overline{E}_S$ input is already low, bringing the asynchronous chip enable ($\overline{E}_A$) low immediately enables the outputs. With $\overline{E}_A$ low, bringing the synchronous chip enable ($\overline{E}_S$) low enables the outputs at the next clock pulse. Likewise, when the outputs are enabled, bringing either input high will cause them to be disabled, in other words put into a high-impedance state. When $\overline{E}_A$ is brought high, the outputs are immediately disabled, whereas when $\overline{E}_S$ is brought high, they are disabled after the next clock pulse.

If the $\overline{INIT}$ input is brought low the register latch is loaded with a field-programmable initial value, rather than with PROM data. In the MB7232RS the master register is loaded immediately, and the contents are transferred to the slave register at the next clock pulse. In the MB7232RA both the master and slave registers are loaded immediately.

Timing Considerations

a) PRM Data Read

After an address change, address setup time $t_S(A)$ must elapse before the master register contains valid new PROM data. The clock must then rise, within address hold time $t_H(A)$, to shift the data to the slave register. The data will appear at the outputs within clock access time $t_A(CLK)$ after the rising edge of the clock, if the outputs had been previously enabled.

If the outputs were disabled when the data was shifted, and are subsequently enabled by bringing $\overline{E}_A$ low, asynchronous chip enable time $t_{EN}(\overline{E}_A)$ must elapse before the data appears at the outputs.

If $\overline{E}_S$ is brought low to enable the outputs, clock enable time $t_{EN}(CLK)$ must elapse after the rising edge of the next clock. During this time the data from the master register is shifted to the slave register and appears at the outputs.

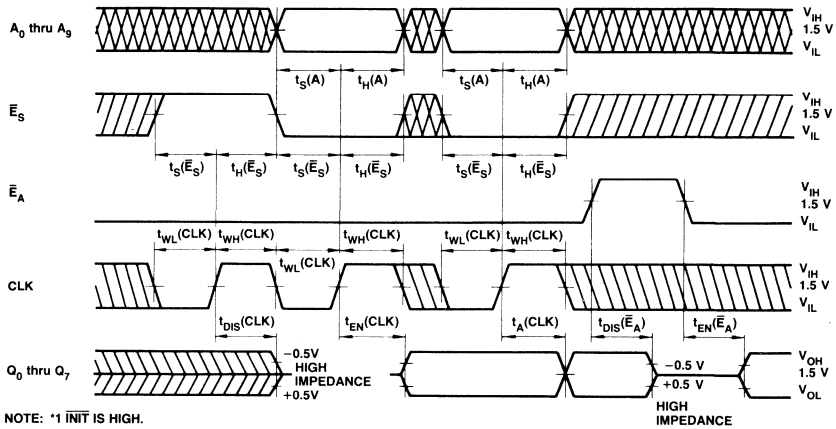
In the MB7232RA, when the registers have been initialized by $\overline{INIT}$, and $\overline{INIT}$ is then brought high to select PROM data, asynchronous initialize recovery time $t_R(\overline{INIT}_A)$ must elapse before the clock rises to shift the new data.

b) Initial Data Read

In the MB7232RA, after the $\overline{INIT}$ input is brought low, asynchronous initialize access time $t_A(\overline{INIT}_A)$ must elapse before the initial data appears at the outputs.

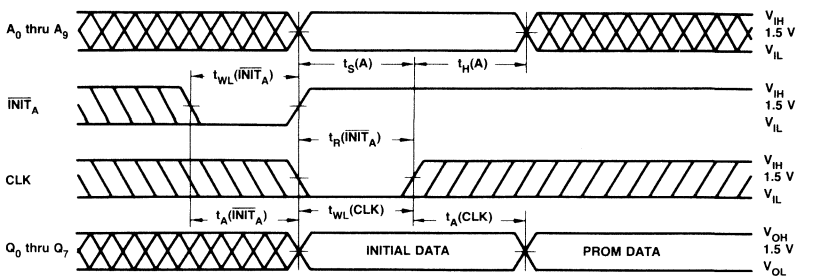
In the MB7232RS, after the $\overline{INIT}$ input is brought low, synchronous initialize access time $t_A(\overline{INIT}_S)$ must elapse before valid initial data appears in the master register. It is then shifted and output in the same manner as PROM data.

PROM Data Read Timing[*1]



NOTE: *1 $\overline{INIT}$ IS HIGH.

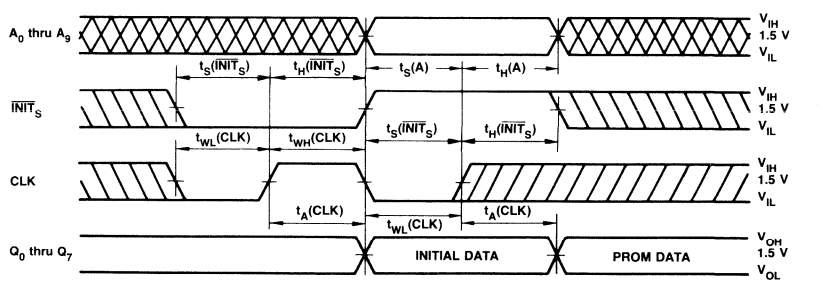
Asynchronous Initial Data Read Timing (MB7232RA)[*1]



NOTES: *1 $\overline{E}_A$, $\overline{E}_S$ INPUT ARE LOW.

*2 ▨ DON'T CARE.

Synchronous Initial Data Read Timing (MB7232RS)[*1]



NOTES: *1 $\overline{E}_A$, $\overline{E}_S$ INPUT ARE LOW.

*2 ▨ DON'T CARE.

Data Read Specifications
(Under Guaranteed Operating Conditions)

Parameter	Symbol	Min	Typ	Max	Unit	Operating Temperature
Power-supply voltage	V_{CC}	4.75	5.0	5.25	V	T_A = 0°C to 75°C
Input low voltage	V_{IL}	0	—	0.8	V	
Input high voltage	V_{IH}	2.0	—	5.5	V	

AC Characteristics

Parameter	Symbol	Typ	MB7232RA/RS-20 Min	MB7232RA/RS-20 Max	MB7232RA/RS-25 Min	MB7232RA/RS-25 Max	Unit	Remarks
Address setup time	$t_S(A)$	20	30		35		ns	
Address hold time	$t_H(A)$	−5	0		0		ns	
Clock access time	$t_A(CLK)$	15		20		25	ns	
Clock pulse width	$t_{WH}(CLK)$ / $t_{WL}(CLK)$	10	20		20		ns	
Synchronous enable setup time	$t_S(\overline{E}_S)$	5	10		15		ns	
Synchronous enable hold time	$t_H(\overline{E}_S)$	0	5		5		ns	
Asynchronous initialize access time	$t_A(\overline{INIT}_A)$	20		30		30	ns	MB7232RA
Asynchronous initialize recovery time	$t_R(\overline{INIT}_A)$	11	20		20		ns	MB7232RA
Asynchronous initialize pulse width	$t_{WL}(\overline{INIT}_A)$	13	20		20		ns	MB7232RA
Synchronous initialize setup time	$t_S(\overline{INIT}_S)$	TBD	TBD		TBD		ns	MB7232RS
Synchronous initialize hold time	$t_H(\overline{INIT}_S)$	TBD	TBD		TBD		ns	MB7232RS
Clock enable time	$t_{EN}(CLK)$	18		25		30	ns	
Asynchronous enable time	$t_{EN}(\overline{E}_A)$	15		25		30	ns	
Clock disable time*2	$t_{DIS}(CLK)$	18		25		30	ns	
Asynchronous disable time*2	$t_{DIS}(\overline{E}_A)$	11		25		30	ns	

Notes: *1 At T_A = 25°C and V_{CC} = 5.0V.
*2 Measured at a point on the output waveform 0.5V from the active output level.

DC Characteristics

(Under Guaranteed Operating Conditions)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input current	I_{IH}	V_{IH} = 5.5V	—	—	40	μA
	I_{IL}	V_{IL} = 0.45V	—	—	−250	μA
Input clamp voltage	V_{IC}	I_I = −18 mA	—	—	−1.2	V
Output low voltage	V_{OL}	I_{OL} = 10 mA	—	—	0.45	V
		I_{OL} = 16 mA	—	—	0.5	μA
Output leakage current (Chip disabled)	I_{OIL}	V_O = 0.45V	—	—	−40	μA
	I_{OIH}	V_O = 2.4V	—	—	40	μA
Output high voltage*1	V_{OH}	I_{OH} = −2.4 mA	2.4	—	—	V
Output short-circuit current*1	I_{OS}	V_O = 0V	−15	—	−60	mA
Power supply current	I_{CC}	V_I = Open or 0V	—	140	185	mA
Power dissipation	P_D	V_I = Open or 0V	—	700	972	mW

Note: *1 Denotes guaranteed characteristics of the output high-level state when the chip is enabled and the programmed bit is addressed. These characteristics cannot be tested prior to programming, but are guaranteed by factory testing.

Terminal Capacitance

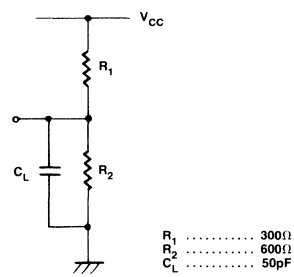
(T_A = 25°C, V_{CC} = +5.0V, VIN = +2.0V, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input terminal capacitance	C_{IN}	—	10	pF
Output terminal capacitance	C_{OUT}	—	15	pF

AC Test Conditions

INPUT CONDITIONS
Amplitude: 0V to 3V
Rise and Fall Time: 5 ns from 1V to 2V
Frequency: 1 MHz

LOAD CONDITION



Fabrication Technology

Input/Output Circuits

The inputs use Schottky TTL circuitry to achieve a fast response time. A PNP transistor is used in the first stage to minimize switching current. Protection diodes are also included.

The three-state outputs (high, low, and high-impedance states) combine the advantages of totem-pole outputs (high noise immunity, fast rise time, ample line-driving capacity) and direct connection to bus-oriented system. Schottky TTL circuitry is used for fast operation. A PNP transistor in the output circuit minimizes the load on the chip enable circuitry.

Memory Cells

The memory cells in the MB7232 are of the junction-shorting type, using DEAP (Diffused Eutectic Aluminum Process) technology. They are initially all in the 0 (low voltage) state. In this state, the cell's programmable element, a PN diode, blocks current flow. During programming, the diode's junction is shorted, allowing it to conduct current, and permanently changing the cell's state to 1 (high).

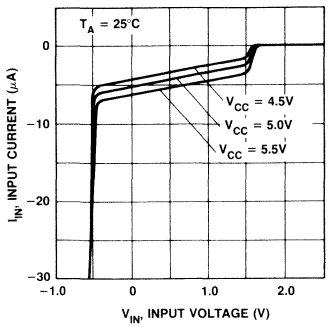
By applying reverse current pulses to the diode's cathode, the temperature at the junction is raised. When the temperature reaches the point where the silicon and aluminum form a eutectic, the eutectic diffuses from the surface of the metal-silicon contact region to the anode of the PN diode, and shorts the junction. The power dissipation at the junction immediately drops to less than one fifth, thus lowering the temperature. This drop in temperature stops further diffusion of the eutectic, and protects the PNP transistor from destruction.

In the memory cell array, the word line islands are divided by IOP (Isolation by Oxide and Polysilicon) passive isolation. Memory cells in the same island are divided by SVG (Shallow V-Groove) passive isolation. The vertically structured memory cells permit a high packing density.

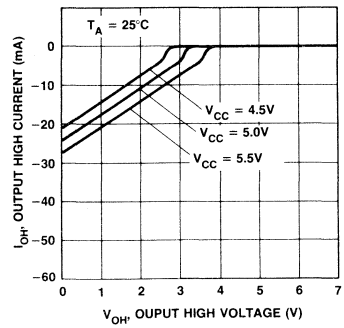
Typical Characteristics Curves

DC Characteristics

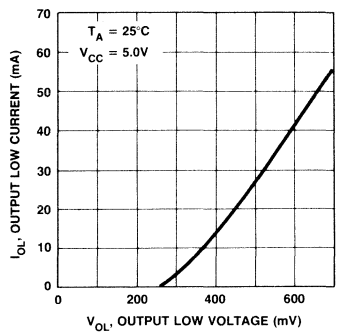
I_{IN} Input Current vs. V_{IN} Input Voltage



I_{OH} Output High Current vs. V_{OH} Output High Voltage

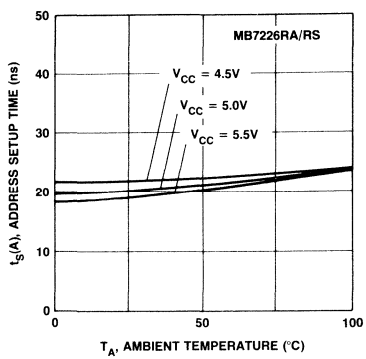


I_{OL} Output Low Current vs. V_{OL} Output Low Voltage

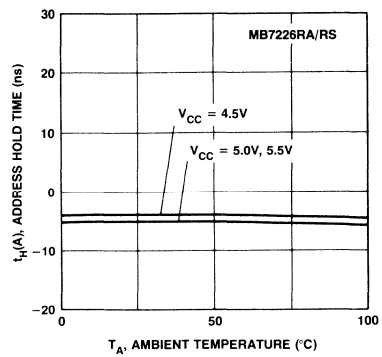


AC Characteristic

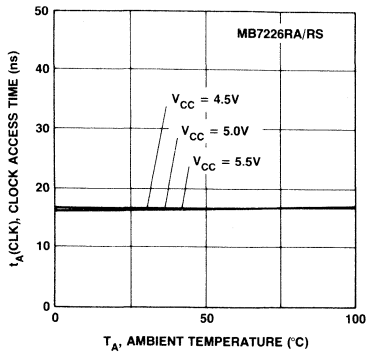
t_S(A) Address Setup Time vs. Ambient Temperature



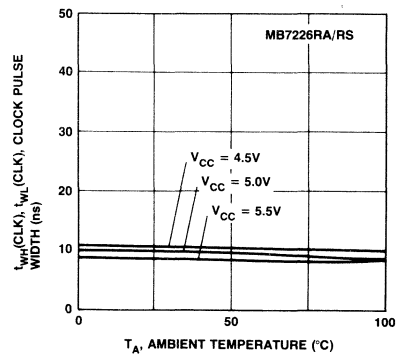
t_H(A) Address Hold Time vs. Ambient Temperature



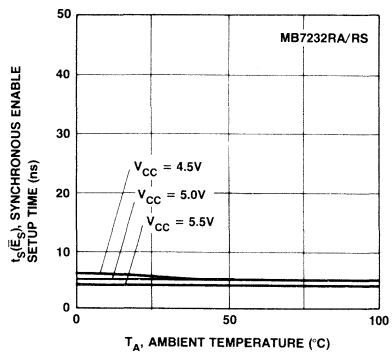
t_A(CLK) Clock Access Time vs. Ambient Temperature



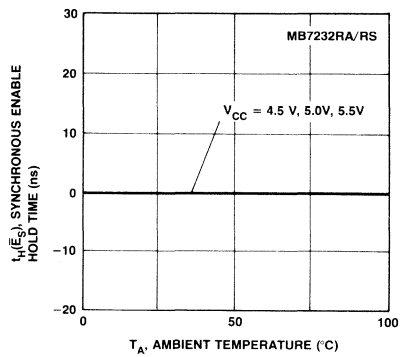
t_{WH}(CLK) and t_{WL}(CLK) Clock Pulse Width vs. Ambient Temperature



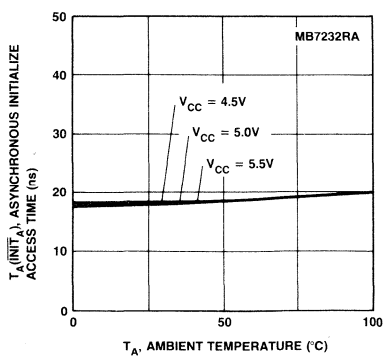
$t_S(\overline{E}_S)$ Synchronous Enable Setup Time vs. Ambient Temperature



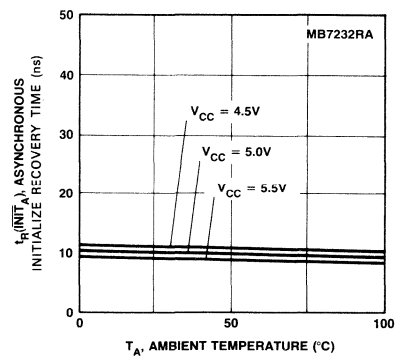
$t_H(\overline{E}_S)$ Synchronous Enable Hold Time vs. Ambient Temperature



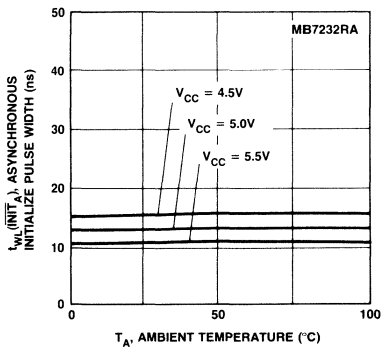
$t_A(\overline{INIT}_A)$ Asynchronous Initialize Access Time vs. Ambient Temperature



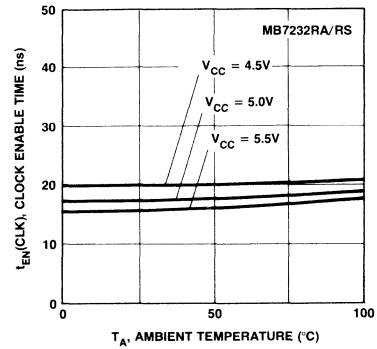
$t_R(\overline{INIT}_A)$ Asynchronous Initialize Recovery Time vs. Ambient Temperature



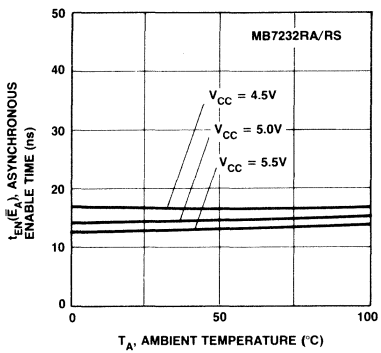
$t_{WL}(\overline{INIT}_A)$ Asynchronous Initialize Pulse Width vs. Ambient Temperature



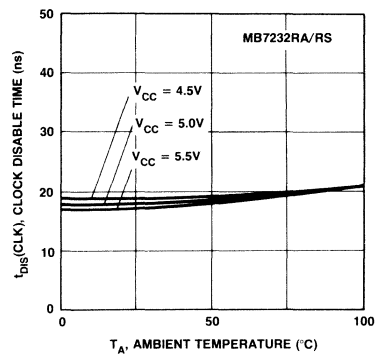
t_{EN}(CLK) Clock Enable Time vs. Ambient Temperature



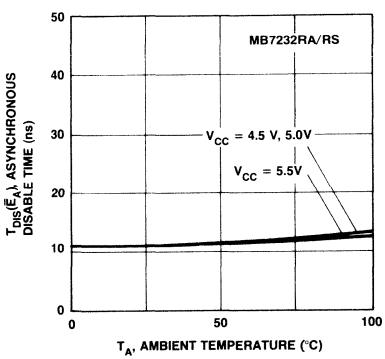
$t_{EN}(\overline{E}_A)$ Asynchronous Enable Time vs. Ambient Temperature



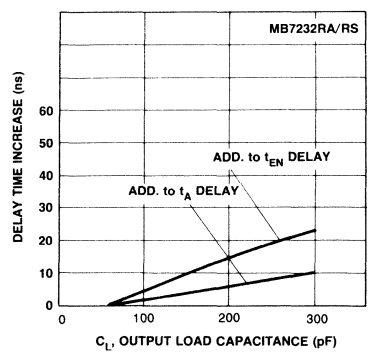
t_{DIS}(CLK) Clock Disable Time vs. Ambient Temperature



$t_{DIS}(\overline{E}_A)$ Asynchronous Disable Time vs. Ambient Temperature

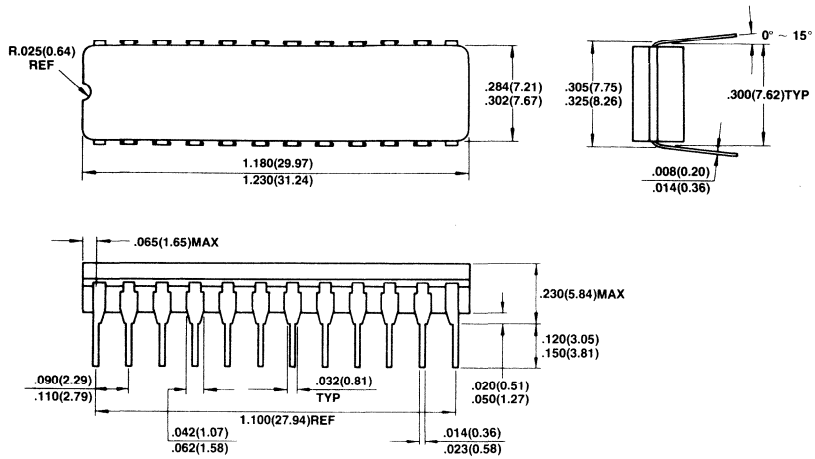


Delay Time Increase vs. Load Capacitance

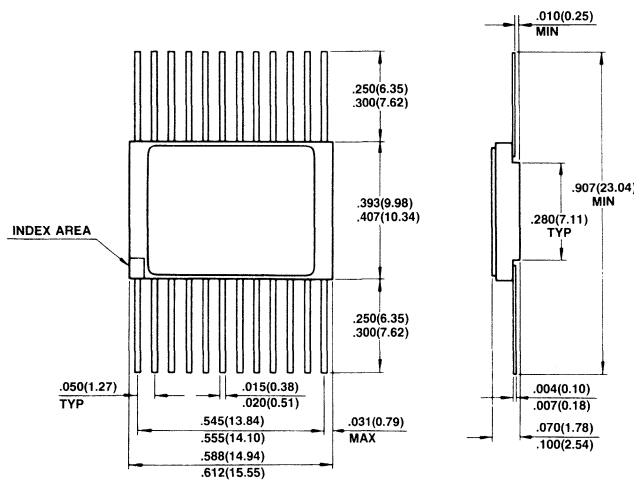


Package Dimensions
Dimensions in inches
(millimeters)

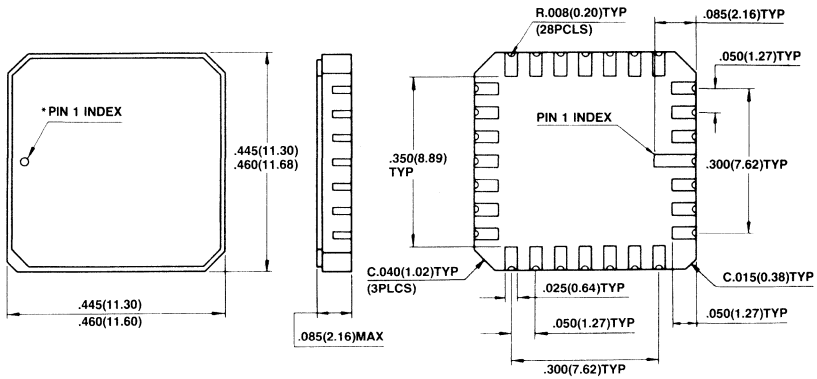
24-Lead Ceramic (CERDIP) Dual In-Line Package
(Case No.: DIP-24C-C04)



24-Lead Ceramic (Metal Seal) Flat Package
(Case No.: FPT-24C-A01)



28-Pad Ceramic (Metal Seal) Leadless Chip Carrier (Case No.: LCC-28C-A01)



*Shape of Pin 1 index : Subject to change without notice

Advanced Information

Availability Q4 '86

Bipolar PROM

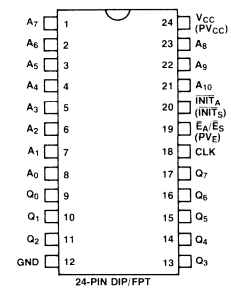
FUJITSU

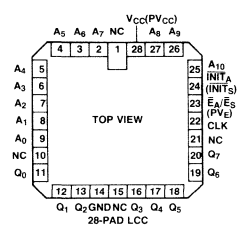
■ MB7238RA-20/-25,MB7238RS-20/-25

Schottky 16K-Bit
Registered Output PROM

Features

- **Organization:**
  2048 × 8-bits
- **Process:**
  Schottky TTL
- **Program:**
  Diffused Eutectic Aluminum Process (DEAP)
- **Output:**
  Three-State Output
  Output register can be initialized asynchronously (MB7238RA) or synchronously (MB7238RS)
- **Clock Access Time:**
  20 ns max. (MB7238RA/RS-20)
  25 ns max. (MB7238RA/RS-25)
- **Power Supply:**
  +5V ±5%
- **Power Dissipation:**
  945 mW max.
- **Package:**
  24-pin DIP/FPT and 28-pad LCC





Advanced Information

Availability Q4 '86

Bipolar PROM

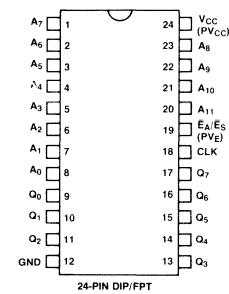
FUJITSU

■ MB7242RS-20/-25

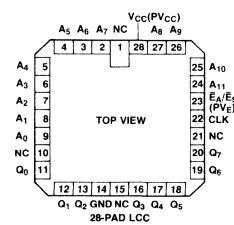
Schottky 32K-Bit
Registered Output PROM

Features

- **Organization:**
  4096 × 8-bits
- **Process:**
  Schottky TTL
- **Program:**
  Diffused Eutectic Aluminum Process (DEAP)
- **Output:**
  Three-State Output
  Output register can be initialized synchronously
- **Clock Access Time:**
  20 ns max. (MB7242RS-20)
  25 ns max. (MB7242RS-25)
- **Power Supply:**
  +5V ±5%
- **Power Dissipation:**
  971 mW max.
- **Package:**
  24-pin DIP/FPT and 28-pad LCC



24-PIN DIP/FPT



28-PAD LCC

Application and Technical Notes

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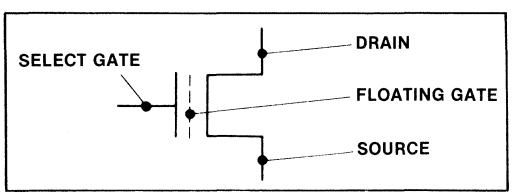
Fujitsu EPROMS
Programming, Erasing, and Data Retention

INTRODUCTION

Most microprocessor based systems have long and fluctuating development cycles. This includes both hardware and software modifications. Software must be stored in a nonvolatile device to insure that the micro-code will not change during a system power down period. Therefore, a nonvolatile device with easily alterable characteristics is the most efficient media for storage in this application. Fujitsu's EPROM devices can provide the microprocessor user with just such a dependable device. Simple programming procedures, quick and easy erasure procedures, and access times fast enough to interface with today's popular microprocessors make Fujitsu's EPROMs ideal for microprocessor applications. This application note will examine the programming, erasure, and data retention characteristics of Fujitsu's EPROMs.

FIGURE 1

FAMOS STACKED GATE N-CHANNEL EPROM MEMORY CELL

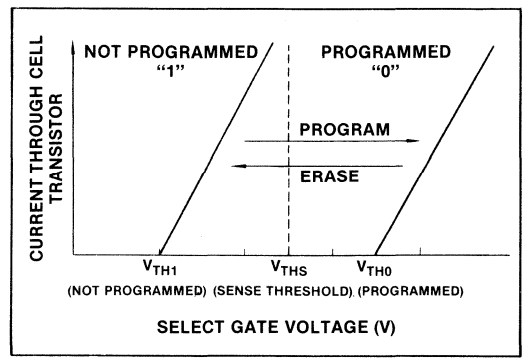


PROGRAMMING

The reliability proven FAMOS stacked gate EPROM cell (figure 1) is used in all of Fujitsu's EPROMs. The cell consists of the conventional n-channel MOS transistor drain and source along with a specialized stacked double gate construction. The top gate, also known as the select gate, is connected to the row decoder which activates that particular cell when it is accessed. The bottom gate, also known as the storage gate, is where the charge is stored when the cell has been programmed. This cell is programmed by the injection of high energy electrons onto this storage gate.

FIGURE 2

MEMORY CELL THRESHOLD SHIFT



This injection is accomplished by raising the voltage on the select gate and drain to attract the high energy electrons from the substrate through the thin gate oxide region into the storage gate. Since this storage gate is electrically isolated (completely surrounded by silicon dioxide, SiO_2) these electrons are trapped. The presence of an electrical charge causes the threshold of the cell to shift upward (see figure 2). This shift will not allow the transistor to turn on when accessed. When the cell is programmed, it is said to be programmed to output a logic "0" when it is accessed. The status of the cell (programmed or unprogrammed) can be determined by testing the cell at its sense threshold voltage. This voltage is indicated by the dotted line in figure 2. The threshold voltage of a MOS transistor is one the most important and basic parameters in MOS device structures. If there is any ion surface charge contamination during fabrication, the threshold of the cell will tend to drift. If the contamination content becomes excessive, the threshold might drift undesirably after extended periods of operation. Figure 3 indicates that the Fujitsu EPROM fabrication techniques have minimized these contamination effects.

FIGURE 3

EPROM THRESHOLD DRIFT

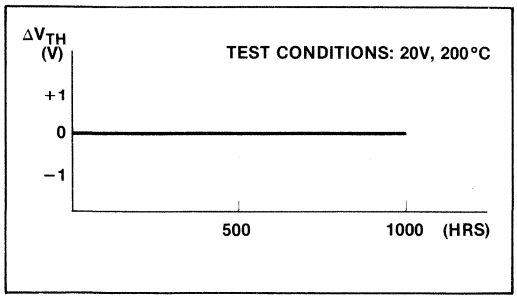


Table 1 points out the status of the control pins for each particular device that is to be programmed. Due to the continual increase in density, the increase in physical chip size, and a corresponding increase in pin count, these changes in programming procedures and voltages were unavoidable. These changes have however given the programmer a more definitive programming procedure. The memory array should be entirely erased before programming to avoid any partial programming. A valuable standard procedure for the user would be to include an initial erasure period before programming the device. For detailed timing specifications on the programming of each device, consult each device's respective data sheet. Consult Fujitsu Technical Brief TB-002 for a detailed 32k bit EPROM programming hardware list for a few of the most popular commercially available prom programmers.

UV ERASING

As stated in the previous section, the entire array must be erased before being reprogrammed. Electrons in the conduction and valence energy bands of the programmed storage gate will absorb photons from various light sources. These electrons eventually become excited enough to photo-emit from the storage gate into the surrounding oxide. They are then swept away into the substrate or select gate depending on the orientation of the internal electric fields. Although electrons from both energy bands can absorb these photons, emission out of the conduction band requires the absorbed photons to have 3.2 eV of energy compared to 4.3 eV for the valence band. However, the rate of photo-emission for the valence band electrons is much higher than that of the conduction band electrons. This is due to the availability of many more valence band electrons in the programmed gate.

A dosage of 15 watt-seconds per square centimeter (W-sec/cm^2) is required to entirely erase an EPROM array. The most commonly used source of these high energy photons is the mercury vapor ultraviolet lamp. Placed one inch away from the array, this source emits ultraviolet light with a wavelength of 2537 angstroms (Å), equivalent to 4.9 eV with a level of radiation intense enough (12000 uW/cm^2) to erase the entire array in approximately 15 to 20 minutes.

Light sources with wavelengths less than 4000 angstroms will eventually erase an EPROM array. The time required to do so is dependent upon the intensity of the source. Fluorescent light and sunlight (even after atmospheric filtering) have wavelengths short enough to eventually erase an array.

TABLE 1

CONTROL PIN STATUS WHILE PROGRAMMING

Device	V_{PP}	V_{PP} Location	$\overline{OE}$	$\overline{OE}$ Location	$\overline{CE}$	$\overline{CE}$ Location	$\overline{PGM}$	$\overline{PGM}$ Location
MBM2716	25V	Pin 21	V_{IH}	Pin 20	Pulsed to V_{IH}	Pin 18	—	—
MBM2732	25V	Pin 20	—	Note 1	Pulsed to V_{IL}	Pin 18	—	—
MBM2732A	21V	Pin 20	—	Note 1	Pulsed to V_{IL}	Pin 18	—	—
MBM2764 MBM27C64	21V	Pin 1	V_{IH}	Pin 22	V_{IL}	Pin 20	Pulsed to V_{IL} (Note 2)	Pin 27
MBM27128 MBM27C128	21V	Pin 1	V_{IH}	Pin 22	V_{IL}	Pin 20	Pulsed to V_{IL} (Note 2)	Pin 27

Note 1: V_{PP} and $\overline{OE}$ are multiplexed on the same pin.

Note 2: The MBM27C64 $\overline{PGM}$ pulse width can be reduced to 25 msec minimum versus 45 msec for all other devices. This is an approximate 44% savings in programming time.

Note 3: The Fujitsu Quick-pro algorithm can be used to program the 64K and 128K families of EPROMs.

Their minimum wavelengths of ~3000 angstroms, corresponding to 4.1 eV, are strong enough to cause photoemission of electrons out of the conduction band. As discussed earlier, photoemission of conduction band electrons is at a much lower rate than the valence band electrons. Therefore, this would require extended exposure times to these sources, approximately three orders of magnitude longer than exposure to the above mentioned mercury vapor light source. However, care must be taken to insure that arrays are not subjected to prolonged periods of exposure to such common sources. An opaque label may be placed on the window of the device to block out the undersired wavelengths. Periodic intensity measurements should be performed on the UV source to insure that it is continually emitting the proper intensity of UV light.

DATA RETENTION

Data retention is one characteristic that needs to be addressed when determining the quality of EPROMs. Since ultra-violet light is present in most every form of light, data retention is affected during normal use as well as when purposely erasing the cells as in the previous **UV ERASING** section. In addition to accidental array erasures affecting the data retention characteristics, numerous physics phenomena and manufacturing defects can affect the data retention. This section will discuss the use of the Arrhenius relationship, the various failure mechanisms, and three methods for calculating the failure rates of UV erasable EPROMs.

FAILURE MECHANISMS

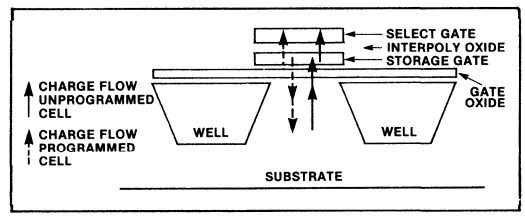
Failure mechanisms cause the charge on the storage gate to vary. The cell cross section in figure 4 is a graphic illustration of the FAMOS n-channel stacked gate cell used in all of Fujitsu's EPROMs. Since each cell is in one of two states, programmed or unprogrammed, these mechanisms will affect the stored charge in various ways. Therefore, the programmed and unprogrammed states need to be discussed separately.

When the cell has been programmed, this charge will flow either through the interpoly oxide onto the select gate or through the thin gate oxide into the substrate. Charge flow in either direction will cause a reduction in trapped charge, which in turn will reduce the threshold voltage of the cell.

Failure mechanisms also cause memory degradation when the cell has been erased or unprogrammed. Charge flow, however, will tend to flow in one direction toward the select gate, located in the upper most region of the cell in figure 4. Seen as though the storage gate is in the relative center of the gate region, the charge will be flowing into the storage gate on one side and out of the storage gate on the other side, as noted in figure 4. When the electric fields are oriented to cause flow into the storage gate from the substrate, the gate will experience an increase in charge. These fields will also cause the electrons to leave the gate through the interpoly oxide onto the select gate. This will cause the storage gate to experience a decrease in electrical charge.

FIGURE 4

CELL STRUCTURE AND CHARGE FLOW



When the storage gate experiences a net gain in charge, the flow through the gate oxide is said to have been the predominant flow. This will cause a rise in the threshold voltage of the cell. As this threshold becomes higher, it begins to approach the seperation threshold between the programmed and unprogrammed states shown by the dotted line in figure 2.

Failure mechanisms are device dependent due to the properties of the particular memory cell. The most common failure mechanisms that relate to UV erasable EPROMs, their activation energies and descriptions are listed in table 2. These mechanisms are described in the following sections.

TABLE 2

FAILURE MECHANISMS

Activation Energy	Failure Result	Failure Mechanism
0.3eV	Infant Random Bit Loss	Silicon Defects
0.6eV	Random Bit Charge Loss or Gain	Oxide Defects
0.75 to 0.80eV	Random Bit Charge Loss	Thermo-Chemical Reaction
1.2eV	Edge Bit Charge Loss	Ionic Contamination
1.4eV	Multiple Bit Charge Loss	Wear Out From Intrinsic Charge Loss

OXIDE DEFECTS

The oxide defect mechanism, which is associated with a 0.6 eV activation energy, seems to effect a single bit at random in either a positive or negative threshold shift. This failure is most often related to manufacturing defects; and it usually occurs during the early period of the device's life span. However, this failure is seldom seen with Fujitsu's expertise in manufacturing techniques.

SILICON DEFECTS

This failure mechanism is associated with a 0.3 eV activation energy. It manifests itself in a manner similar to that of the oxide defect previously mentioned; but it is characterized by only a negative threshold shift (charge loss). The trapped charge on the storage gate can emit through these silicon defects and scatter into other regions of the cell.

THERMO-CHEMICAL REACTIONS

When no environmental or mechanical stresses exist, the majority of failures in EPROMs can be attributed to thermo-chemical reactions. These reactions, associated with a 0.75 to 0.80 eV activation energy, become activated primarily during high temperature storage or data retention bakes. This failure mechanism is also characterized by a charge loss, resulting from thermo-emission of electrons to and from the storage gate.

IONIC CONTAMINATION

The ionic contamination effect, associated with a 1.0 to 1.4 eV activation energy, appears to start on an edge bit. It then disperses throughout the array effecting more and more bits. The ionic impurities, which have penetrated beneath the layers of protective glass, diffuse along the storage gate connections spreading the effect. These impurities compensate (pair-up) for the electrons in the gates which yields a net loss in charge and a corresponding drop in threshold voltage.

INTRINSIC WEAR-OUT

Intrinisic wear-out is associated with activation energies of 1.4 eV and greater. As previously discussed in the **PROGRAMMING** section, programming is accomplished by the injection of hot-energy electrons through the gate oxide and into the storage gate. A small percentage of these electrons may obtain enough energy to enter the gate oxide, but not enough to proceed through it. Therefore, these lower energy electrons are trapped in this gate oxide region. Since ultra-violet erasure techniques are relatively ineffective at removing these electrons from the oxide, repeated programming cycles will cause a sizeable collection of electrons. This will result in a permanent threshold shift of the cell. This threshold shift may reduce the device's operating margin eventually leading to device wear-out.

The actual failure rate would be determined by summing up the contributions from all failure mechanisms. Studies have shown that quality EPROMs from Fujitsu and other manufacturers can conservatively evaluated using only thermo-chemical reactions (0.80 ev) as failure mechanism contributions.

FAILURE RATES (F.R.)

F.R. AT A SINGLE TEMPERATURE

In order to compare device quality, failure rates, herein referred to as F.R., from competetive devices can be used. Using a set of actual test results, a calculation for the failure rate at a single temperature can be determined by using equation 1.

$$\text{F.R.} = \frac{\text{FAILURES}}{\text{\# OF DEVICES x HOURS TESTED}} \quad \text{(equ. 1)}$$

INTRODUCTION OF A STATISTICAL CONCEPT

The introduction of a statistical approach to this failure rate will yield a much higher level of confidence in obtaining a failure rate value. Using the concept that these failures are randomly distributed throughout the time frame, the "Chi-square" (x^2) distribution analysis becomes applicable. Using the same set of actual test results with the Chi-square formula in equation 2, the adjusted failure rate can be determined as the Mean Time Between Failure (MTBF) for a single temperature.

$$\text{MTBF} = \frac{1}{\text{FAILURE RATE}} = \frac{2 \times T}{x^2} \quad \text{(equ. 2)}$$

where "T" is equal to the number of device hours and "x^2" can be extracted from the x^2 distribution table found in table 3.

TABLE 3 **CHI-SQUARE DISTRIBUTION**

d.o.f. \ Confidence Level	0.10	0.20	0.30	0.40	0.50	0.60	0.70	0.80	0.90	0.95	0.975	0.99
1	0.0158	0.0642	0.148	0.275	0.455	0.708	1.07	1.64	2.71	3.84	5.02	6.63
2	0.211	0.446	0.713	1.02	1.39	1.83	2.41	3.22	4.61	5.99	7.38	9.21
3	0.584	1.00	1.42	1.87	2.37	2.95	3.67	4.64	6.25	7.81	9.35	11.3
4	1.06	1.65	2.19	2.75	3.36	4.04	4.88	5.99	7.78	9.49	11.1	13.3
5	1.61	2.34	3.00	3.66	4.35	5.13	6.06	7.29	9.24	11.1	12.8	15.1
6	2.20	3.07	3.83	4.57	5.35	6.21	7.23	8.56	10.6	12.6	14.4	16.8
7	2.83	3.82	4.67	5.49	6.35	7.28	8.38	9.80	12.0	14.1	16.0	18.5
8	3.49	4.59	5.53	6.42	7.34	8.35	9.52	11.0	13.4	15.5	17.5	20.1
9	4.17	5.38	6.39	7.36	8.34	9.41	10.7	12.2	14.7	16.9	19.0	21.7
10	4.87	6.18	7.27	8.30	9.34	10.5	11.8	13.4	16.0	18.3	20.5	23.2
11	5.58	6.99	8.15	9.24	10.3	11.5	12.9	14.6	17.3	19.7	21.9	24.7
12	6.30	7.81	9.03	10.2	11.3	12.6	14.0	15.8	18.5	21.0	23.3	26.2
13	7.04	8.63	9.93	11.1	12.3	13.6	15.1	17.0	19.8	22.4	24.7	27.7
14	7.79	9.47	10.8	12.1	13.3	14.7	16.2	18.2	21.1	23.7	26.1	29.1
15	8.55	10.3	11.7	13.0	14.3	15.7	17.3	19.3	22.3	25.0	27.5	30.6
16	9.31	11.2	12.6	14.0	15.3	16.8	18.4	20.5	23.5	26.3	28.8	32.0
17	10.1	12.0	13.5	14.9	16.3	17.8	19.5	21.6	24.8	27.6	30.2	33.4
18	10.9	12.9	14.4	15.9	17.3	18.9	20.6	22.8	26.0	28.9	31.5	34.8
19	11.7	13.7	15.4	16.9	18.3	19.9	21.7	23.9	27.2	30.1	32.9	36.2
20	12.4	14.6	16.3	17.8	19.3	21.0	22.8	25.0	28.4	31.4	34.2	37.6
21	13.2	15.4	17.2	18.8	20.3	22.0	23.9	26.2	29.6	32.7	35.5	38.9
22	14.0	16.3	18.1	19.7	21.3	23.0	24.9	27.3	30.8	33.9	36.8	40.3
23	14.8	17.2	19.0	20.7	22.3	24.1	26.0	28.4	32.0	35.2	38.1	41.6
24	15.7	18.1	19.9	21.7	23.3	25.1	27.1	29.6	33.2	36.4	39.4	43.0
25	16.5	18.9	20.9	22.6	24.3	26.1	28.2	30.7	34.4	37.7	40.6	44.3
26	17.3	19.8	21.8	23.6	25.3	27.2	29.2	31.8	35.6	38.9	41.9	45.6
27	18.1	20.7	22.7	24.5	26.3	28.2	30.3	32.9	36.7	40.1	43.2	47.0
28	18.9	21.6	23.6	25.5	27.3	29.2	31.4	34.0	37.9	41.3	44.5	48.3
29	19.8	22.5	24.6	26.5	28.3	30.3	32.5	35.1	39.1	42.6	45.7	49.6
30	20.6	23.4	25.5	27.4	29.3	31.3	33.5	36.3	40.3	43.8	47.0	50.9
31	21.4	24.3	26.4	28.4	30.3	32.3	34.6	37.4	41.4	45.0	48.2	52.2
32	22.3	25.1	27.4	29.4	31.3	33.4	35.7	38.5	42.6	46.2	49.5	53.5
33	23.1	26.0	28.3	30.3	32.3	34.4	36.7	39.6	43.7	47.4	50.7	54.8
34	24.0	26.9	29.2	31.3	33.3	35.4	37.8	40.7	44.9	48.6	52.0	56.1
35	24.8	27.8	30.2	32.3	34.3	36.5	38.9	41.8	46.1	49.8	53.2	57.3
36	25.6	28.7	31.1	33.3	35.3	37.5	39.9	42.9	47.2	51.0	54.4	58.6
37	26.5	29.6	32.1	34.2	36.3	38.5	41.0	44.0	48.4	52.2	55.7	59.9
38	27.3	30.5	33.0	35.2	37.3	39.6	42.0	45.1	49.5	53.4	56.9	61.2
39	28.2	31.4	33.9	36.2	38.3	40.6	43.1	46.2	50.7	54.6	58.1	62.4
40	29.1	32.3	34.9	37.1	39.3	41.6	44.2	47.3	51.8	55.8	59.3	63.7
41	29.9	33.3	35.8	38.1	40.3	42.7	45.2	48.4	52.9	56.9	60.6	65.0
42	30.8	34.2	36.8	39.1	41.3	43.7	46.3	49.5	54.1	58.1	61.8	66.2
43	31.6	35.1	37.7	40.0	42.3	44.7	47.3	50.5	55.2	59.3	63.0	67.5
44	32.5	36.0	38.6	41.0	43.3	45.7	48.4	51.6	56.4	60.5	64.2	68.7
45	33.4	36.9	39.6	42.0	44.3	46.8	49.5	52.7	57.5	61.7	65.4	70.0
46	34.2	37.8	40.5	43.0	45.3	47.8	50.5	53.8	58.6	62.8	66.6	71.2
47	35.1	38.7	41.5	43.9	46.3	48.8	51.6	54.9	59.8	64.0	67.8	72.4
48	35.9	39.6	42.4	44.9	47.3	49.8	52.6	56.0	60.9	65.2	69.0	73.7
49	36.8	40.5	43.4	45.9	48.3	50.9	53.7	57.1	62.0	66.3	70.2	74.9
50	37.7	41.4	44.3	46.9	49.3	51.9	54.7	58.2	63.2	67.5	71.4	76.2

Before extracting the x^2 value from the table, the level of confidence and number of degrees of freedom need to be determined. The formula for degrees of freedom (df) is shown in equation 3 where "f" is equal to the number of failures in the test results.

$$df = 2f + 2 \qquad \text{(equ. 3)}$$

Confidence levels of 60 and 90% are commonly used by the semiconductor industry. The 60% level is normally used with EPROMs.

CONVERTING AMBIENT TEMPERATURES TO JUNCTION TEMPERATURES

The junction temperature, as seen in equation 4, is a function of the outside ambient temperature (T_A), maximum power dissipation of the part (P—the product of maximum V_{CC} and maximum I_{CC}), and the thermal impedance of the package from outside the package to the junction regions (Θ_{JA}).

$$T_J = T_A + (\Theta_{JA} \times P) \qquad \text{(equ. 4)}$$

The thermal impedance, Θ_{JA}, is package (type and size) dependent and approximately 56°C per watt maximum for the 24 pin cerdip package and 51°C per watt maximum for the 28 pin cerdip package. Thus for specific ambient temperatures, the junction temperature can be determined. Note that the temperatures used in this evaluation must be junction temperatures.

F.R. AT ALL TEMPERATURES USING ACCELERATION FACTORS

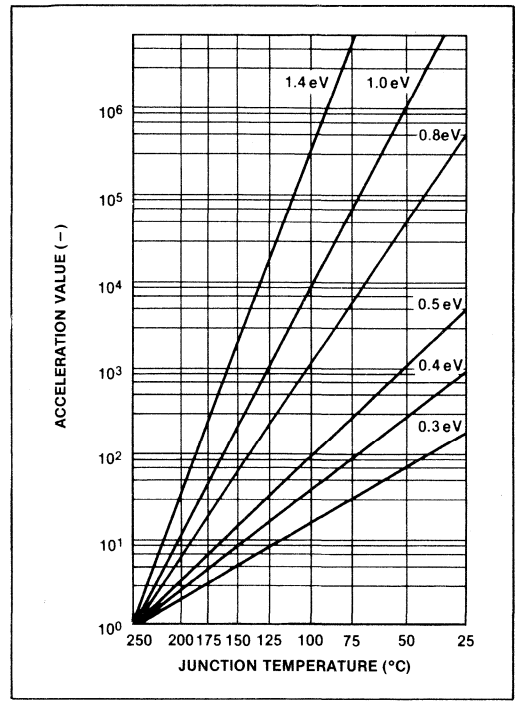
Since extended life testing can become long in duration and tediously repetitive, accelerated testing becomes the most viable approach to failure rate evaluation. Failure rates can be determined by subjecting the EPROMs to elevated temperatures for comparably shorter periods of time. One can estimate the failure rate at any temperature by obtaining the failure rate at the elevated test temperature (using one of the two previous methods) and using the Arhennius plot in figure 5 to determine the acceleration factor $F[f(T_1, T_2)] = F.R.(T_1) / F.R.(T_2)$.

One can estimate the failure rate for any other temperature (T_2) by using equation 5. Dividing the failure rate at temperature T_1 by the acceleration factor $F[f(T_1, T_2)]$, the failure rate at temperature T_2 is obtained.

$$F[f(T_1, T_2)] \times F.R.(T_2) = F.R.(T_1) \qquad \text{(equ. 5)}$$

FIGURE 5

ARHENNIUS PLOT



F.R. CALCULATION EXAMPLE

After obtaining test results from a controlled test set-up, the previously discussed methods can be used to determine the failure rate. The following hypothetical test results will be used for an example:

> 3600 NMOS EPROMs devices were tested at an ambient temperature of 70°C for 1000 hours. The tests performed indicated that 2 of the devices failed some portion of the tests.

Using equation 1 with these test results will yield a failure rate of

$$F.R.(T_1) = \frac{2 \text{ failures}}{3600 \text{ device hours}} = .055\% \text{ per 1000 hours}$$

An alternate approach would be to use the Chi-square statistical approach. Using equation 3, the number of degrees of freedom would be equal to

$$df = 2(2) + 4 = 6$$

For a 60% confidence level, the X^2 value would be equal to 6.2 (extracted from table 3). Using equation 2, the test results would then yield a failure rate of

$$MTBF = \frac{2 \times 3.6 \times 10^6 \text{ device hours}}{6.2} = 1.16 \text{ per 1000 hours}$$

$$F.R.(T_1) = \frac{1}{MTBF} = .086\% \times 10^6 \text{ hours}$$

A typical 32K EPROM in a 24-pin Cerdip package has the following characteristics:

$$\text{Max } V_{PP} = 5.5 \text{ volts; Max } I_{CC} = 150 \text{ mA;}$$
$$\Theta_{JA} = 56\,°C/W$$

Assuming an ambient temperature T_A of 70 °C, equation 4 yields a junction temperature T_J of

$$T_J = 70\,°C + (825 \text{ mW})(56\,°C/W) = 70\,°C + 46.2\,°C = 116\,°C$$

Using this value for T_J, E_A = 0.80eV and the plot in figure 6, the failure rate for a device whose junction temperature is kept at 116 °C is shown to be over 12 times ($8 \times 10^4/6.5 \times 10^3 = F[f(T_1, T_2)]$) that of a device whose junction temperature is kept at 70 °C. One must note that to keep the junction temperature at 70 °C, the outside ambient temperature must be kept at approximately room temperature, 24 °C.

Using equation 5, and the results from the Chi-square method, the failure rate at junction temperature T_2 (70 °C) would then be

$$F.R.(T_2) = F.R.(T_1)/12 = .086\% \text{ per 1000 hours}/12 = .007\% \text{ per 1000 hours}$$

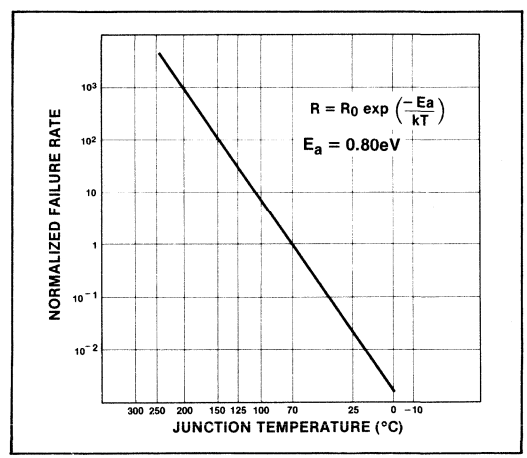
FUJITSU'S CHARACTERISTICS

Fujitsu entire line of EPROMs have a MTBF value of 1.28×10^8 hours, which corresponds to a failure rate of .00078% per 1000 hours. This failure rate was determined at T_A = 75 °C, for a confidence level of 60%, and for an activation energy of 0.75 eV (thermo-chemical reactions).

Figure 6 shows an Arhennius plot of failure rate versus junction temperature for an activation energy of 0.80 eV with a normalized failure rate at a junction temperature of 70 °C.

FIGURE 6

FAILURE RATE vs. JUNCTION TEMPERATURE



FUJITSU'S OUTPUT REGISTERED PROMS

In the world of microprocessor and microcontroller design, the more common so-called "logic primatives", often hamper the speed and efficiency of these machines. The ability to combine one or more necessary devices onto a single I.C. enhances the performance of the resultant circuitry. In the case of Programmable Read Only Memories (PROMs), the requirements of pipelined instruction sets call for a more flexible and cost/space efficient method of providing the microcode instruction as required by the processor.

A PROM is a permanent memory that can be given its data "in the field", that is to say, it can be programmed at any time after it has been manufactured. This unique characteristic makes PROMs ideal for instruction storage for computers, processors, and other automated equipment. They make modification easy. All one has to do in order to change some parameters is to replace the PROM with another one which incorporates the changes desired. One of the major characteristics of standard PROMs is that the data will remain on the output (in the read mode) only as long as the address remains unchanged. In other words, if the input address changes, or goes away, the data on the PROM output will change as well. Under most circumstances, this is not a drawback. But in some applications, it is necessary to hold data on the outputs of the PROMs while a new address is being loaded in. In the past, it has been necessary to use outboard registers with their uncertain timing characteristics to accomplish this task. In order to accomodate this mode of operation, Fujitsu Microelectronics has just introduced a family of PROMs which have the registers and all control inputs on the same chip. These are called Registered Proms or R-PROMs.

The Fujitsu Registered PROMs are being offered in two initial configuarations: a 4K device organized as 512 words by 8-bits, and an 8K device organized as a 1024 words by 8-bits. Each of these devices is, in turn, offered in either synchronous or asynchronous form.

R-PROMs are especially advantageous to designers of pipelined microprogrammable systems because the register which contains the instruction, during execution, is now located on the PROM chip itself. This feature offers significant advantages over conventional design methods for this type of architecture. Improvements are seen in the areas of power consumption, cycle times and board space. A further advantage to the R-PROM is in its ability to allow for the upgrade of current systems to pipeline status without resorting to complicated PC board changes.

THE FUJITSU REGISTERED PROMs

There are four Fujitsu registered PROMs in this current plan:

MB7226RA - 512 x 8 organization, asynchronous
MB7226RS - 512 x 8 organization, synchronous
MB7232RA - 1024 x 8 organization, asynchronous
MB7232RS - 1024 x 8 organization, synchronous

THREE STATE OUTPUTS

All Fujitsu R-PROMs have outputs which are of the three state configuration and are compatable with the low-power Schottky three-state bus standard. The three states are; 1 (on), 0 (off) and the "Tri-Stated" or high impedence mode. This configuration effectively provides the device with all of the desirable features of a totem pole TTL output. These include greater noise immunity, high source current for good line driving capability, and fast, symetrical rise and fall times.

EDGE TRIGGERED REGISTERS

The outputs of the PROM sections of the R-PROMs are loaded into the on-board 8 bit register on the rising edge of the clock. It should be noted here that a 'register' contains master-slave flipflops and is different from a 'latch' which contains gated or R-S flipflops.

SYNCHRONOUS AND ASYNCHRONOUS ENABLES

Optionally, the user may choose either synchronous or asynchronous enables. The Fujitsu R-PROMs may be distinguished as synchronous or asynchronous by the suffix (A) for asynchronous or (S) for synchronous on the part number. The synchronous enable option is to be chosen when multiple R-PROMs are bused together for increased word length (such as in 16- or 32-bit systems). When this option is chosen (see figure one), the enables become the most significant address bits and must be registered along with the rest of the data word. In other words, when the clock goes high, the address is free to change. This of course requires that the enable information be stored at some location on the R-PROM.

In cases where the enable is not used, or when the PROM outputs are to be gated onto a system bus, the synchronous enable becomes a disadvantage. In cases such as these it is advantageous for the designer to choose the asynchronous enable option, which allows direct control of the enable function (figure two).

Figure 1 Synchronous Enable

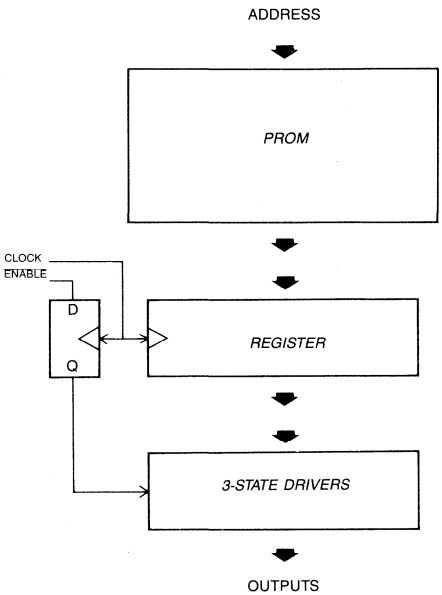
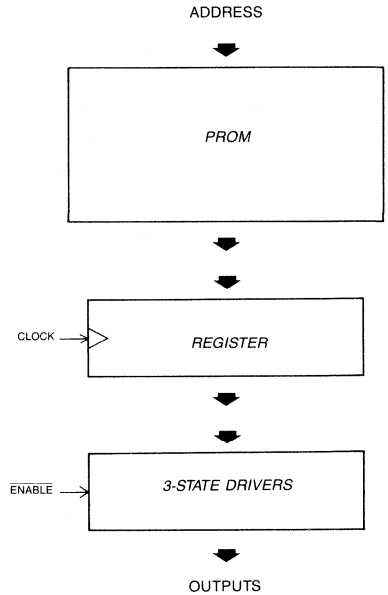


Figure 2 Asynchronous Enable



INITIAL DATA READOUT

Either of the following two types of initial data can be selected:

(1) All lows (mask programmed on the MB7226RA/S)
(2) All highs (mask programmed on the MB7226RA/S)

These options can be selected by the /INITs on the MB7232RS and the /INITa on the MB7232RA. On the MB7226RA, the initial data option can be selected using the /CLRa and the /PRSTa pins and the /CLRs and /PRSTs pins are used for this purpose on the MB7226RS.

The method used to read the initial data is the same as for PROM data readout.

THE MEMORY CELL

The Fujitsu family of Registered PROMs are junction - shorting types. This means that ones are programmed instead of zeros. A memory cell in these devices consists of a programmable element, which includes a PN diode and a vertically connected PNP transistor. The normal current blocking state of the reverse diode can be biased in the programming mode to conduct current.

During programming, reverse current pulses are applied to the cathode of the PN diode increasing the temperature at the junction. When the temperature reaches a high enough point, the silicon and aluminum form a eutectic bond (start to alloy) which diffuses from the surface of the metal-silicon contact region to the anode of the PN diode, thus shorting the junction. As soon as the junction becomes shorted, the power dissipation at the junction drops rapidly along with the eutectic keeping it from diffusing further, and protects the PNP transistor from destruction. This programming method is called the Diffused Eutectic Aluminum Process or DEAP, and is the basis for all current Fujitsu PROM technology.

Each word line island in the memory cell area is divided from its neighbors by passive isolation called Isolation by Oxide and Polysilicon or IOP. Each memory on the word line island is in turn separated by a passive isolation process called shallow V-groove or SVG. The vertical structure of the junction shorting cell makes a high packing density possible.

PROGRAMMING PROCEDURE

Fujitsu registered PROMs are manufactured with the contents of all memory cells low which results in a "positive logical zero". To make the contents of a particular cell high (in other words, a one) the blocked state of the reverse PN junction must be changed to the conducting state. This happens when the R-PROMs are programmed.

A logical one can be permanently programmed into a selected bit location. The bit to be programmed is selected using the address inputs to turn on transistors Q1 and Q2 (see figure three). By applying the PVCE pulse voltage, the chip is disabled and transistor Q3 is held off. When the train of programming pulses is applied to the appropriate output, it passes through the memory cell into transistor Q1. This programming current changes the state of the junction so that it will conduct. The pulse train stops as soon as the output voltage indicates that the state of the selected bit has reached a logical one (1). Two additional programming pulses are applied to ensure that the element has been programmed properly.

Each memory cell has to be programmed individually because the internal decoding circuit can sink the programming current of only one bit at a time.

PROGRAMMING INITIAL DATA

On the MB7232RA and the MB7232RS (1024 x 8) Fujitsu Registered PROMs, the initial data can be programmed by the user. The memory cells which comprise the initial data portion of the R-PROM are fabricated as logical zeros at the factory in addition to the rest of the PROM memory cells. Ones can be programmed by selecting the initial data cells through applying a logical zero signal to the initialize-input pin (/INIT) and applying programming current pulses to the output terminals (Q0 through Q7) as directed in on the initial data programming chart shown in figure four.

Figure 3 Programming Circuit of Fujitsu R-PROMs

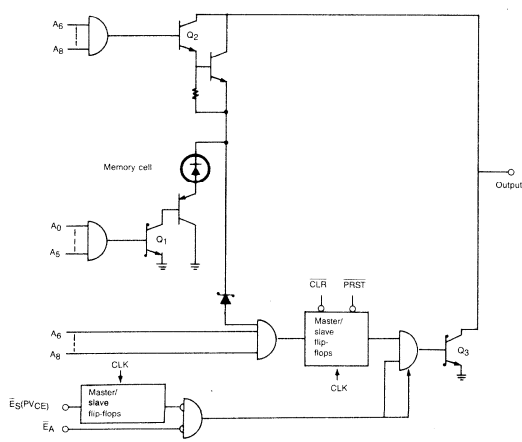


Figure 4 Programming Chart for R-PROMs

Input					Output	Operating mode	Remarks
$\overline{PRST}_A$ $\overline{PRST}_S$	$\overline{CLR}_A$ $\overline{CLR}_S$	CLK	$\overline{E}_A$	$\overline{E}_S$			
H	H	†	×	PV_{CE}	Z	PROGRAM	PROM DATA
H	H	†	L	L	L/H	VERIFY	

Notes
H: High level
L: Low level
X: Don't care
PV_{CE}: 20 V
Z: High impedance
†: Rising edge

*1: If an H level is changed at the same time $\overline{PRST}_A/\overline{CLR}_A$ is input, the output cannot be determined (either H or L).

PIPELINED MICROPROGRAMMABLE SYSTEMS

Microprogrammed processors and controllers are generally either pipelined or non-pipelined. The difference between these two types of systems is that in the non-pipelined system the "instruction fetch" command is not given until the processor is ready to accept it and in a pipelined system, the instruction fetch for the next instruction is given while the previous instruction is being executed. Therefore, the pipelined approach is much faster than non-pipelined because the microcycle of the pipelined system is defined by the length of either the fetch or execution time and not by the sum of both as in a non-pipelined arrangement. This improvement in speed can be as great as 2:1 depending on the microprocessor used, the location of the registers used to hold the next instruction, and the length of the fetch and execution cycles. The fastest time, of course, is when fetch and execution times are equal. Any gain in cycle time is lost, however, when a branch circuit requires the look-ahead fetch to be discarded. A typical pipelined microprogrammed system is shown in figure five.

BENEFITS OF REGISTERED PROMS IN PIPELINED SYSTEMS

As can be seen, the R-PROM is ideal for use in pipelined microprogrammable systems. The major advantages are:

* Faster Cycle Times
* Lower Parts Count For Simplified Board Layout
* Lower Power Consumption

STATE MACHINES AND OTHER STRUCTURED LOGIC CIRCUITS

Fujitsu R-PROMs can be used as basic logic circuits which, when used in conjunction with other basic logic building blocks can define a number of structured logic architectures.

One of the most basic logic circuits possible with the R-PROM is a state machine. As shown in figure six, such a sequencer is formed by feeding the outputs of the register back into the address inputs. The resultant state machine will then sequence from one state to the next as defined by the present state as it appears on the register outputs, and the address inputs which contain both the present state information as well as the inputs from outside.

Powerful microprogrammer sequencers can be constructed using the R-PROM as a state machine in conjunction with other memory elements and logic elements.

The example applications contained in this note demonstrate that Fujitsu Registered PROMs offer the logic designer a new tool in the field of computer and processor architecture.

Figure 5 Typical Pipelined Microprogrammable System

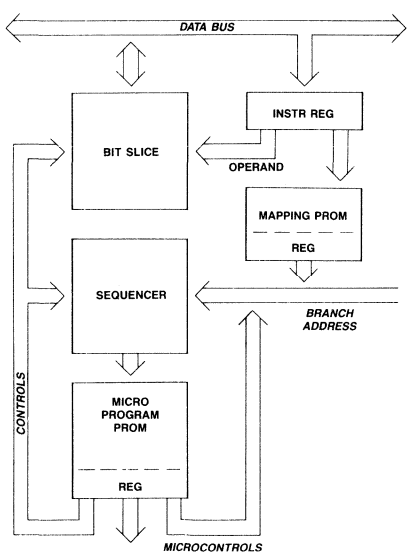
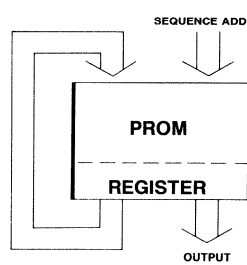


Figure 6 State Machine Using R-PROM



ADDRESSING CONSIDERATIONS WHEN TESTING THE MB81256/7

To properly test a random access memory a detailed description of the internal topology and address decoding of the device is required in order to run complex disturb patterns and to optimize testing procedures. This applications note supplies sufficient addressing information to properly test the MB81256 (page mode) and MB81257 (nibble mode).

ADDRESS SCRAMBLING

It is often necessary to access a particular memory cell location when testing the MB81256/7. However, the internal addresses corresponding to the actual physical memory cell locations are different from the addresses applied to the external address pins of the device. The address scrambler converts the logical or external address to the internal or physical address corresponding to the physical memory location (Fig 1). To determine the actual internal address, a transformation must be made in accordance with the following logic diagram and equations as shown in fig 2 and fig 3. This address, when converted to decimal, can then be physically located on the die using the internal bit topology diagram (Fig 4).

Figure 1. Address Scrambling

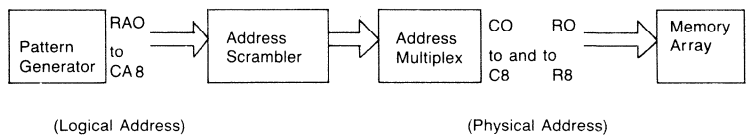


Figure 2.

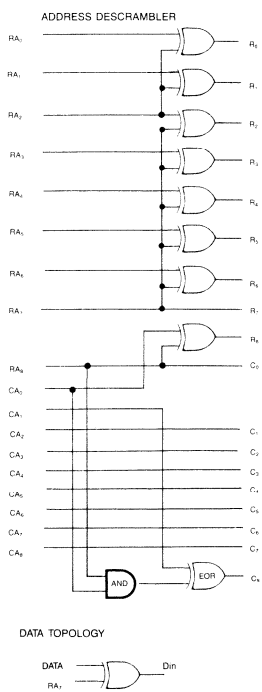


Figure 3. Address Scramble Equations

R0 = RA0 EOR RA2
R1 = RA1 EOR RA2
R2 = RA2 EOR RA7
R3 = RA3 EOR RA7
R4 = RA4 EOR RA7
R5 = RA5 EOR RA7
R6 = RA6 EOR RA7
R7 = RA7
R8 = RA8 EOR CA0

C0 = RA8
C1 = CA2
C2 = CA3
C3 = CA4
C4 = CA5
C5 = CA6
C6 = CA7
C7 = CA8
C8 = (RA8 and CA0)
EOR CA1

RN and CA: Internal physical address
RAN and CAN: Pattern generator address (external logical address)
EOR: Exclusive OR Gate

Example of address scrambling,

Logical address (by pattern generator);

RA0	RA1	RA2	RA3	RA4	RA5	RA6	RA7	RA8	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8
0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	0

Address Scrambler

Physical Address (to the memory array)

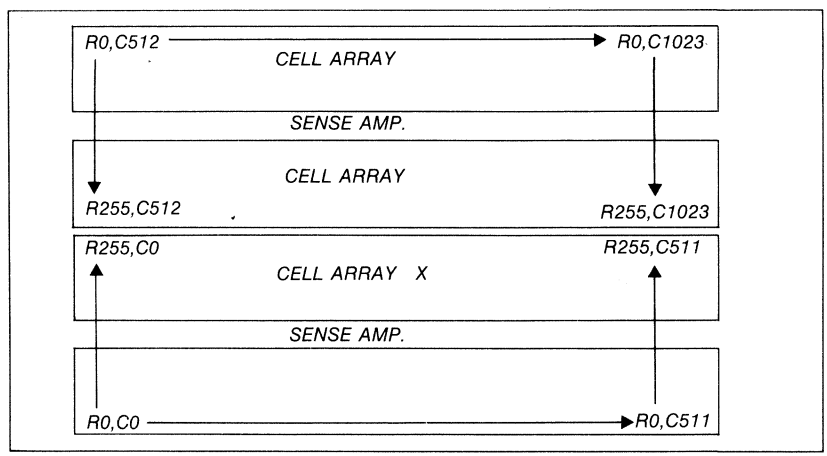
R0	R1	R2	R3	R4	R5	R6	R7	R8	C0	C1	C2	C3	C4	C5	C6	C7	C8
0	1	1	0	1	0	1	1	0	0	0	1	0	1	0	1	0	1

C0	C2	C3	C4	C5	C6	C7	C8	C9	C1

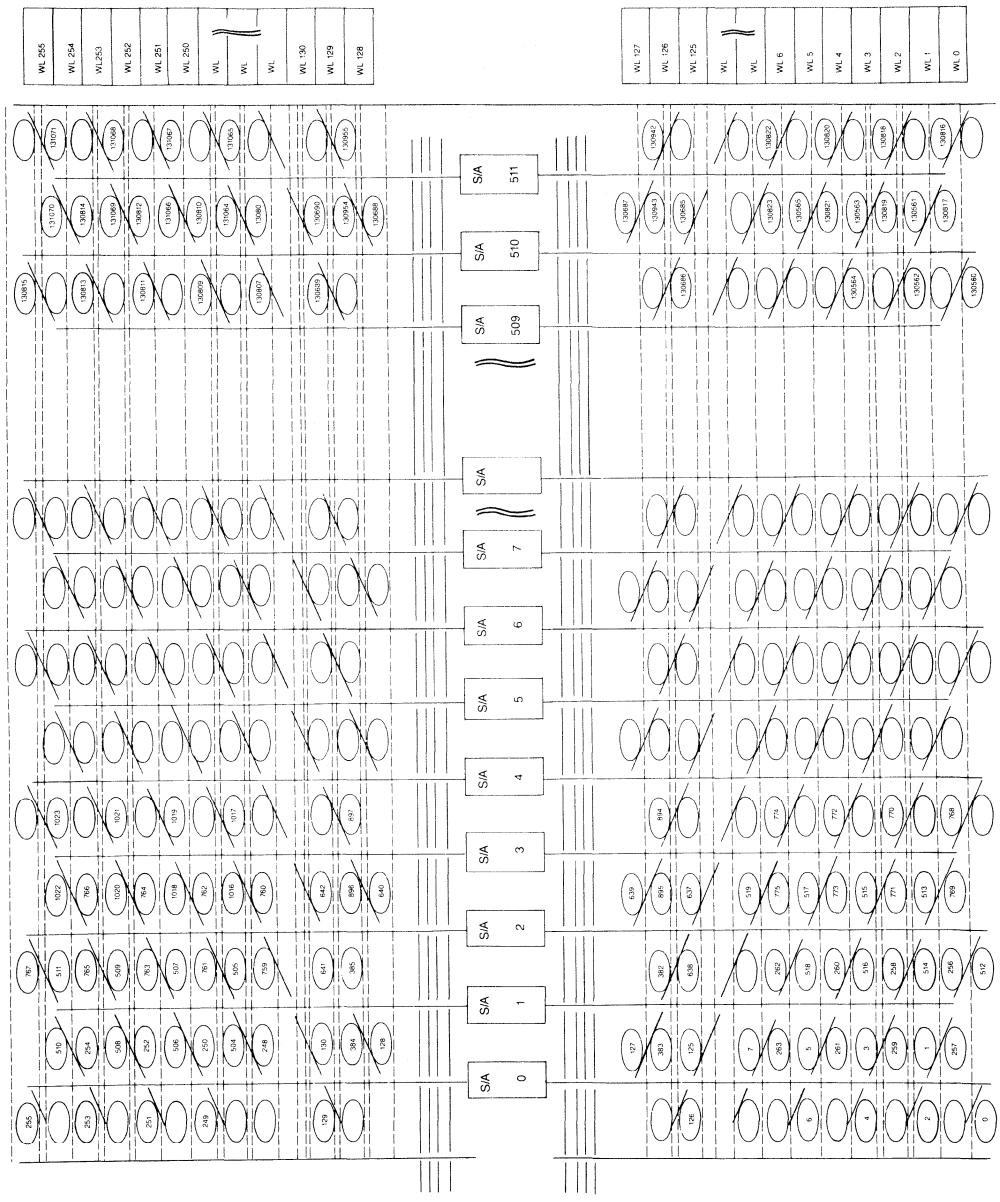
R:214 (Decimal) *C:338 (Decimal)*

This address (R:214 and C:338) is location "X" in the internal bit topology shown in Fig. 4.

Figure 4. Internal Bit Topology



MB81256/MB81257 Bit Map (Lower 128k)



Addressing Considerations When Testing the MB8264 and MB8265

To properly test a random access memory requires a detailed description of the internal topology and address decoding of the device in order to properly run complex disturb patterns and to optimize testing procedures. This note will supply this information for the MB8264 and MB8265, 64K-bit dynamic RAMs.

Since the design of this product is quite complex, four separate considerations must be made when determining bit topology:

ADDRESS TOPOLOGY

The address pins were labeled on the MB8264 and MB8265 data sheets for marketing convenience and do not correspond to the actual internal address designations. To determine the actual internal address, a transformation must be made in accordance with Figure 1.

Any further references in this paper refer to actual internal MB8264 and MB8265 addresses, not data sheet labeling.

DECODING TOPOLOGY

Optimizing row and column decoder layouts resulted in a scrambling of the addressing sequence. This scrambling must be taken into consideration if bits are to be addressed in a topological sequential manner. A logic diagram is supplied in Figure 2 to decode this scrambling. Figure 2 gives the resulting descrambled addresses in terms of row (Rn) and column (Cn) addresses. By multiplexing the row and column addresses, Rn is produced from An at $\overline{RAS}$ time and Cn is produced during $\overline{CAS}$ time. For comparison, a bit map is supplied in Figure 3 showing the addressing scheme before descrambling.

DATA POLARITY

Since balanced sense amplifiers are used, positioned between rows 63_{10} and 64_{10}, and 191_{10} and 192_{10} of the matrix, this requires that the data on one side of the sense amplifiers be stored at an inverted polarity from the other side. This inversion is automatically done by internal circuitry so it is transparent to the user. If it is necessary to write all bits to the same internal state, the data transformation in Figure 4 must be observed. To understand topologically which quadrants store same polarity data and which store inverted polarity data, refer to Figure 6.

BIT TOPOLOGY

Optimum design strategies resulted in the actual bit topology as presented in Figure 5. Note that the cells of the MB8264 and MB8265 are laid out in pairs, one on each side of the column, or bit line. This topology layout as well as the address decoding must be taken into consideration, especially when running disturb patterns designed to check for bit to bit shorts, leakage, or crosstalk.

To understand the actual physical arrangement of the MB8264 and MB8265, Figure 6 is presented to relate the array orientation to the input pad orientation on the actual chip.

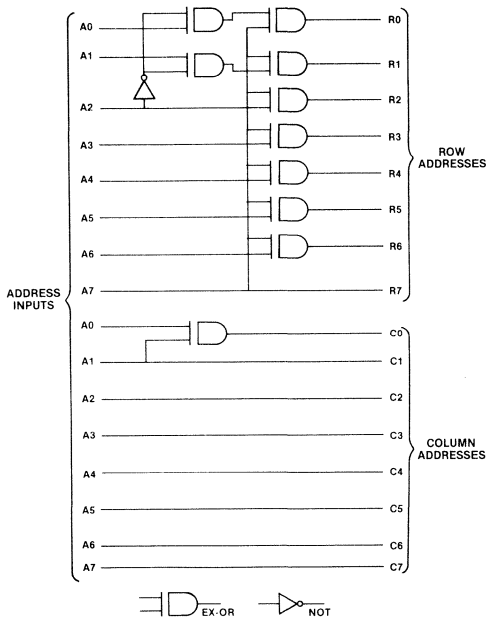
FIGURE 1

TRANSFORMATION FROM DATA SHEET ADDRESS NOTATION TO ACTUAL MB8264/MB8265 INTERNAL ADDRESSES

PIN NUMBER	DATA SHEET LABEL	ACTUAL INTERNAL ADDRESS
13	A_6	A_0
12	A_3	A_1
11	A_4	A_2
5	A_0	A_3
6	A_2	A_4
7	A_1	A_5
10	A_5	A_6
9	A_7	A_7

FIGURE 2

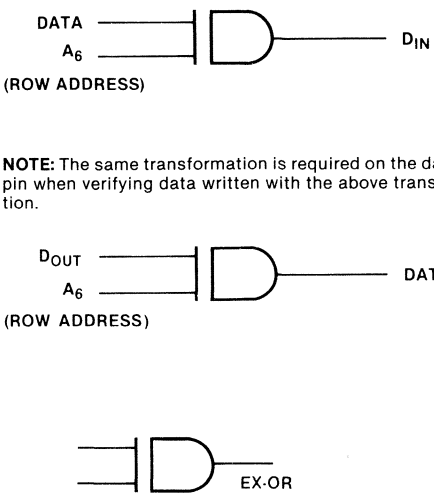
EXTERNAL ADDRESSING TRANSFORMATION REQUIRED TO DESCRAMBLE INTERNAL ADDRESSING SEQUENCE



NOTE: The above logic symbols are used solely to represent "exclusive or" and "not" functions, and are not a suggested implementation of logic.

FIGURE 4

EXTERNAL DATA TRANSFORMATION TO DECODE THE INTERNAL DATA INVERSION OF THE MB8264/MB8265



NOTE: The same transformation is required on the data out pin when verifying data written with the above transformation.

NOTE: The above logic symbol logic symbol is used solely to represent the "exclusive or" function and is not a suggested implementation of logic.

FIGURE 3

MB8264 and MB8265 BIT MAP SHOWING INTERNAL ADDRESS SCRAMBLING

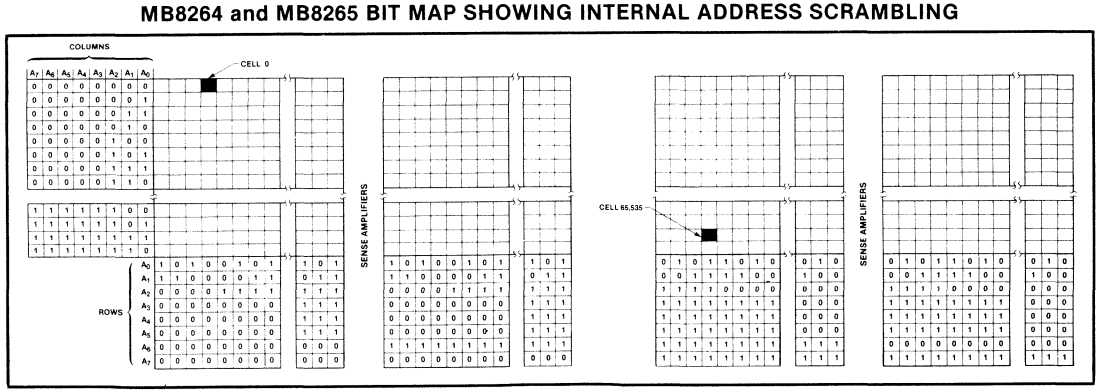


FIGURE 5

INTERNAL BIT TOPOLOGY OF THE MB8264 and MB8265

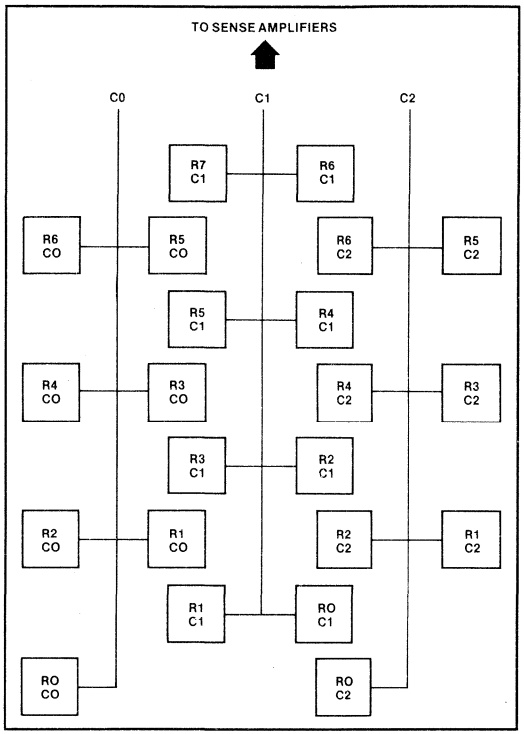
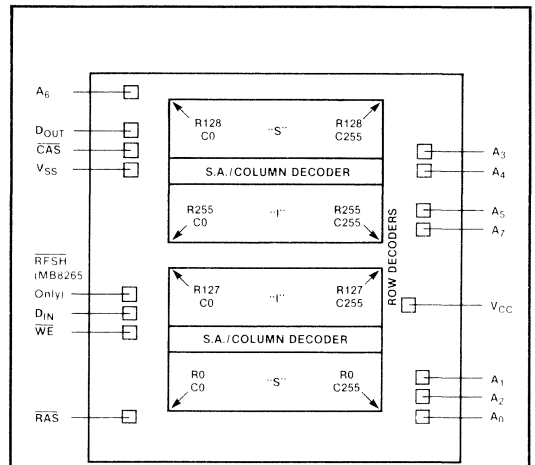


FIGURE 6

CHIP ARCHITECTURE OF THE MB8264 and MB8265



NOTE: "S" — Same polarity as D_{IN}
"I" — Inverted polarity from D_{IN}

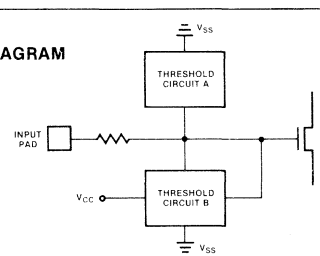
NOTE: Address labeling reflects data sheet notation, not actual internal addressing. Corners are labeled above in transformed column and row notation.

Leakage and Continuity Test Considerations Using Fujitsu's Single Supply DRAMs

INPUT PROTECTION CIRCUIT

When electrostatic discharge (ESD) is induced on the pin of an integrated circuit, voltages in the KV range can occur. This can cause gate breakdown of an unprotected MOS structure. If this breakdown occurs, the gate of the input transistor may be shorted and a heavy current will flow through the pin. Therefore, precautions against electrostatic breakdown of the gate are important. All the inputs of Fujitsu's single supply DRAMs have an ingenious Input Protection Circuit (IPC) (see Figure 1) that isolates the internal chip circuitry from damage caused by normal handling procedures. In order to provide adequate protection for the device, the IPC provides two separate low impedance paths to V_{SS} for static charge to traverse. The threshold circuit A is activated if a voltage of 12V or greater is detected between the pin and V_{SS}. This provides a path to V_{SS} for the charge to travel. When no power is applied, a transistor contained within circuit B provides the second low impedance path to V_{SS}. At normal bias, this shunt transistor is clamped off by V_{CC}. Normal operating parameters are not affected by the IPC in any way.

FIGURE 1
IPC BLOCK DIAGRAM



INPUT LEAKAGE MEASUREMENTS

As described above, Fujitsu implements an input protection circuit to guard against electrostatic breakdown of the input transistor on the input pin and protect the interior from surge voltages. However, the way the IPC was designed necessitates that power be applied during leakage and continuity tests. Once a static bias is attained, leakage measurements can be taken by the usual methods. First, all input pins not under test should be tied to 0V. The supply voltage, V_{CC}, should be set to 5.5V for a worst case test. The input leakage current can be measured by impressing a voltage (V_{IN}) between 0V and 5.5V. Normal leakage currents will be between −10 and +10 microamps. If a larger leakage current is detected, the device has a leakage problem.

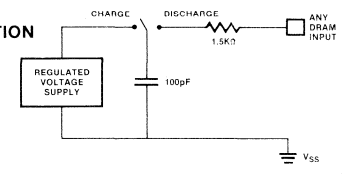
CONTINUITY MEASUREMENTS

Previous generations of integrated circuits used continuity measurement techniques that involved forward biasing an equivalent diode structure that usually existed between the input and the substrate. However, to accurately test Fujitsu's single supply DRAMs it is required that the device be actively biased to insure proper operation of the IPC. The proper test conditions recommended are as follows: $V_{CC} = 5.5V$, $\overline{RAS} = \overline{CAS} = 0V$ (except when $\overline{RAS}/\overline{CAS}$ pins are under test), all other pins are left open. The test is conducted by forcing a 1μA current through the pin and measuring the voltage impressed across the pin. If the voltage across the pin is less than 7V, continuity on that pin can be guaranteed. If a voltage of greater than 7V is detected, the pin has a continuity problem.

TESTING THE IPC FOR ELECTROSTATIC PROTECTION

Testing for ESD protection is accomplished by charging a capacitor of 100pF to a specified voltage, then discharging it through a 1.5K ohm load into an input (see figure 2). This test method is consistent with the ESD protection test procedure described in MIL STD 883B Method 3015.1. The voltage impressed on the input pin should not exceed 600V or else the reliability of the device may be affected.

FIGURE 2
INPUT PROTECTION TEST CIRCUIT



INPUT CAPACITANCE

The input capacitance of the various inputs of Fujitsu's 64K DRAMs have been measured and the results are summarized in table 1.

TABLE 1
TYPICAL INPUT CAPACITANCE OF MB8264/65

Input	Typical Value	Spec. Value
A0	3.5pF	5pF
A1 ~ A7	2.5pF	5pF
D_{IN}	2.6pF	5pF
$\overline{RAS}$	3.7pF	8pF
$\overline{CAS}$	4.5pF	8pF
$\overline{WE}$	3.8pF	8pF

Test conditions: $V_{CC} = 5V$, $V_{SS} = 0V$, Pins not under test should be set to 2.0V. Instrument: Bontoon meter @ 1Mhz.

DATA OUTPUT CIRCUIT

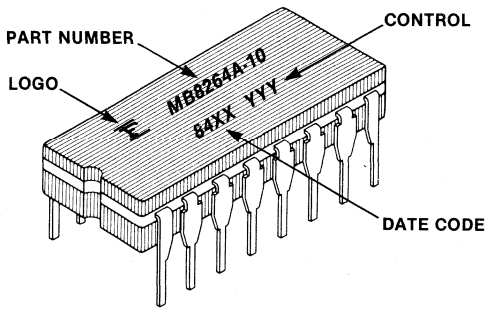
When making leakage mearurements on the data output pin it is necessary to insure that both of the output transistors are off. This is done simply by insuring that V_{CC} is in the normal operating range and that the level of $\overline{CAS}$ is above 2.4V (V_{IH}).

Ordering Information

Product Marking Specifications 12-2
Ordering Code 12-2

Ordering Information

Product Marking



Ordering Code

MB 8264-15 Z

- Z — PACKAGE
  - C-CERAMIC
  - P-PLASTIC
  - Z-CERDIP
- 15 — PERFORMANCE VARIATIONS (WHEN USED)
  - E, H OR DASH NUMBERS DENOTE ACCESS TIME VARIATIONS
  - L-DENOTES LOW POWER
- 8264 — DEVICE TYPE
- MB — MANUFACTURER DESIGNATOR
  - MB-DEVICE TYPE IS FUJITSU INTERNAL NUMBER
  - MBM-DEVICE TYPE IS INDUSTRY STANDARD MEMORY NUMBER